ANALOG DESIGN IN DEEP SUBMICRON CMOS PROCESSES FOR LHC

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Abstract

The feasibility of analog integrated circuits for LHC experiments in deep submicron CMOS technologies has been investigated. This paper discusses general design issues and presents a systematic study of fundamental analog characteristics of commercial deep submicron CMOS processes.

1. INTRODUCTION

Present state-of-the-art CMOS technologies integrate MOS transistors with a minimum gate length of 0.18 μm-0.25 μm and operate with a maximum power supply of 2.5 V. The thin gate oxide used in these technologies has a high tolerance to total dose effects. Therefore, circuits designed in these technologies using dedicated layout techniques (enclosed layout transistors and guard-rings) show a total dose resistance complying LHC specifications [1].

Some of the integrated circuits for LHC have moreover strict requirement on integration and low power consumption, especially in the inner parts of the detectors. A deep submicron technology is therefore a very suitable choice for digital ASIC design, whereas its use for analog and mixed-mode circuits must be investigated more carefully.

Commercial submicron technologies are in fact mainly intended for large volume digital applications. The data available from the manufacturers concerning properties like noise and matching may be not completely satisfactory from the analog designer's point of view. The power supply allowed by a typical 0.25 μm technology (2.5 V) is almost at the edge of the use of standard analog design techniques. This is of particular concern, for instance, for circuits like switched capacitors analog memories, which are extensively used in high energy physics applications.

A submicron technology offers however attractive features also to the analog designer. The many layers of interconnects can be used to improve the quality of analog signals, especially in mixed-mode designs. Due to the squeezed design rules, also density can improve, though not in the same proportion as for digital circuits.

The aim of this work is to investigate the analog performances of commercial 0.25 μm CMOS technologies.

In section 2 we discuss the main design aspects which have to be considered in using a deep submicron technology for analog and mixed-mode design. Section 3 describes the test structures we have designed to investigate the analog performances of the technologies and in section 4 measurements performed on such structures are presented.

2. DESIGN ISSUES

2.1 Noise

The input-referred spectral density of the channel thermal noise can be expressed as [2]

$$V_n^2 = 4kT(1+\delta)\gamma\frac{1}{g_m} \qquad (1).$$

In the above equation k is the Boltzmann constant and T is the absolute temperature.

For an ideal device, $\gamma = 2/3\cdot\Gamma$ in strong inversion and $\gamma = 1/2\cdot\Gamma$ in weak inversion. Γ is the so called excess noise factor and indicates how much the measured noise exceeds the theoretical value calculated using the long channel MOS equations. Values of Γ reported in the literature for non submicron technologies range from 1 to 1.5 [3].

The correction term $(1 + \delta)$ is introduced to take into account the effect of fixed bulk charge on g_m [2,4].

The transconductance g_m in strong inversion is defined by the well known equation

$$g_m = \sqrt{2K(W/L)I_{DS}} \qquad (2).$$

Due to the thin gate oxide, the parameter $K=\mu C_{ox}$ improves in submicron technologies, as can be seen from table 1.

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Table 1: Technological parameter for different CMOS technologies (NMOS).

L_{min} (μm)	t_{ox} (nm)	K (μA/V^2)
1.2	24	68
0.8	14	90
0.5	10	134
0.25	5	280

For instance, a transistor with W=20 μm, L=2 μm, and I_{DS}=100 μA will have a g_m of about 370 μS if implemented in a 1.2 μm technology and of 780 μS if produced using a 0.25 μm technology.

In a deep submicron process, however, the possibility of scaling the L of the transistors is not as useful as it could be argued form eq. (3). In fact, for short channel devices, the increase in transconductance predicted by (3) is limited by velocity saturation effects [4]. Additional effects like hot carriers and weak avalanche phenomena may also worsen the noise performances, increasing Γ significantly above 1 [4].

The increase in K has anyway an interesting effect, because it increases also the current limit between weak and strong inversion. This current is defined as [5]

$$I_{lim} = 2nK(W/L)U_T^2 \tag{4}$$

where n is the slope factor and U_T is the thermal voltage.

This limit for a fixed aspect ratio is a linear function of K. In other words deep submicron makes weak inversion operation easier. This is an attractive feature for low noise and low power amplifiers, since the weak inversion operation maximises the transconductance to current ratio and minimises the input referred noise for a given power budget.

The other source of noise which has to be considered is the flicker noise. The flicker noise spectral density can be expressed as [3]

$$V_n^2 = \frac{K_a}{C_{ox}^2 WL}\frac{1}{f^{\alpha}} \tag{5}.$$

Due to the increase in C_{ox} the flicker noise for a given transistor area is expected to reduce if the device is implemented in a submicron technology [6].

2.2 Matching

The matching between nominally identical components plays an important role in basic analog building blocks like differential amplifiers, comparators and current mirrors.

The threshold voltage mismatch of MOS transistors is characterised by measuring the difference between the thresholds of many couples of nominally identical devices. The standard deviation of the difference distribution is usually used as a measure of mismatch and is described by the following equation

$$\sigma_{Vth} = \frac{A_{Vth}}{\sqrt{WL}} \tag{6}.$$

The term A_{Vth} is a constant for a given technology and is given by

$$A_{Vth} = B \cdot t_{ox} \tag{7}$$

where t_{ox} is the oxide thickness and B can be assumed to be 1 mV·μm/nm for many different processes [7].

Data available in literature clearly indicate that A_{Vth} reduces with the oxide thickness [8,9]. A submicron technology has therefore better threshold matching performances for a given transistor area.

The standard deviation in case of the current gain factors β=K(W/L) is expressed as

$$\sigma_{\Delta\beta/\beta} = \frac{A_{\beta}}{\sqrt{WL}} \tag{8}.$$

Values of A_β found in literature are 1-3 %μm [10].

However, in high energy physics applications enclosed devices are often required to guarantee an adequate radiation resistance. Results about matching properties of enclosed transistor are described in section 4.

2.3 Power supply limitations

A 0.25 μm CMOS technology typically operates with power supply of 2.5 V. Transistor threshold voltages are in the order of 450-550 mV. The maximum signal swing is hence reduced compared to a 5 V technology, and can consequently affect the dynamic range.

The most serious drawback of the required low voltage operation may occur in switched capacitor circuits. The elementary sampling cell of fig. 1 is used as an example.

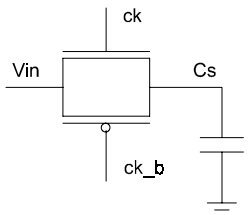

Fig. 1: CMOS transmission gate.

Let's suppose that the switch is closed (ck = Vdd, ck_b = 0). In principle, in these conditions, the switch should provide a low impedance path and any voltage between 0 and Vdd could be sampled on capacitor Cs.

However, it can be shown that if Vdd is smaller than the sum of the threshold voltages of the two transistors, a region exists in which neither device conducts. Therefore, when the switch is closed a low impedance path for each value of Vin between 0 and Vdd is not guaranteed anymore. This, of course, affects very seriously the dynamic range of conventional switched capacitor circuits.

In evaluating the minimum power supply required by the circuit of fig. 1 to work properly care must be paid to the bulk effect, which can rise the threshold voltages up to 1 Volt [6].

The minimum voltage is therefore about 2 V, which is not very far from the maximum operating voltage of a quarter micron technology (2.5 V).

On the other hand, in switching circuits power consumption benefits a lot from the reduced supply. A capacitive ladder of a charge redistribution A/D converter operating at 2.5 V will dissipate only 25% of the power required by a converter operating at 5 V (provided, of course, that capacitor size and operating frequency remain the same) [5].

2.4 Digital noise coupling

The front end chip used in high energy physics applications are mixed mode circuits in which sensitive analog parts (low noise preamplifiers) are implemented on the same chip together with digital functions. In some cases, the amount of digital logic required can be very high.

In submicron technologies the devices are usually built in a relatively thin (few microns) high resistivity layer which is epitaxially grown on a highly conductive bulk. This bulk provides a medium by which the switching noise of the digital part can easily propagate to the analog circuitry.

The best way to overcome this problem is to physically glue the backside of the chip to a ground plane. This solution is not always practical, because the backside is often passivated and a thinning-metallization procedure would be required.

Actually, it is worth saying that this problem is not peculiar to deep submicron technologies only. A large fraction of the mixed mode technologies currently available are derived from former pure digital processes and use the low doped epitaxial layer grown on a highly conductive wafer.

Deep submicron technologies offer however a high number (5 to 7) of metal layers for the interconnections. These layers can be used to avoid any sharing of power and grounding paths between digital and analog circuits.

3 TEST STRUCTURES

To study the problems discussed above a number of test structures were designed in 0.25 μm CMOS technology, namely:

- transistor pairs for matching measurements;
- wide transistors for noise measurements;
- transimpedance amplifiers;
- an analog memory and a switched capacitor successive approximation A/D converter.

The noise structures and the transimpedance amplifiers were implemented in two different technologies, whereas the other structures were designed only for one technology.

Up to now it has been possible to measure wide transistors (in both technologies, hereafter referred to as tech_a and tech_b), matching structures and the amplifier implemented in tech_a.

The results of these tests are discussed in the following section.

4. TEST RESULTS

4.1 Noise measurements

The noise measurements have been carried out for all devices in the three different regions of operation. The appropriate bias current for each device has been selected through a measurement of the g_m/I_d characteristic.

A typical g_m/I_d curve is shown in figure 2.

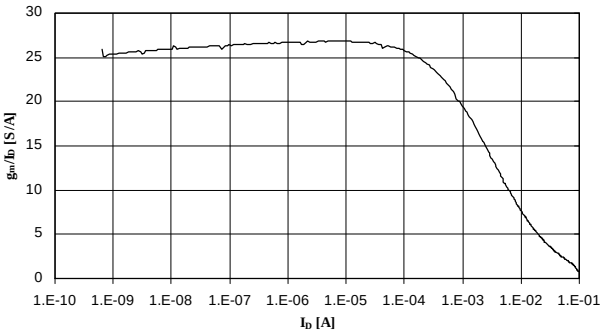

Figure 2: Typical g_m/I_d curve.

For our measurements, we have chosen the following currents:

- 30 μA for weak inversion
- 500 μA for moderate inversion
- 20 mA for strong inversion

In figure 3 and 4 typical noise spectra for NMOS and PMOS transistors are shown for both technologies. These spectra were obtained biasing the transistors in the moderate inversion region, with a current of 500 μA and applying a drain-source voltage of 800 mV.

From the measurements we have estimated the excess noise factor Γ and the flicker noise coefficient K_a. The excess noise factors are reported in table 2.

We point out that for the moderate inversion region we have reported γ, since in this region the value of the inversion layer thermal noise coefficient (which is 2/3 in strong inversion and 1/2 in weak inversion) is not exactly known.

In weak and moderate inversion the excess noise factor is comparable to what is found in literature for non submicron technologies [2,3].

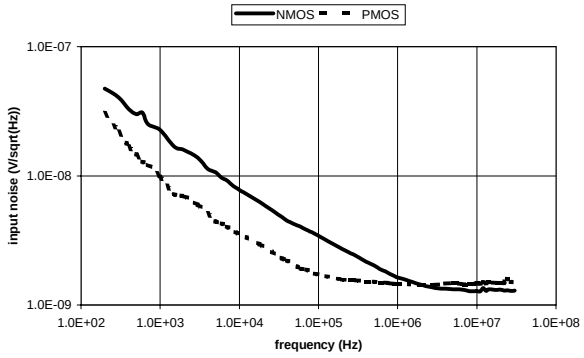

Figure 3: Example of noise spectra for devices of tech_a (Ibias=500 μA: moderate inversion) W/L=1000/0.35.

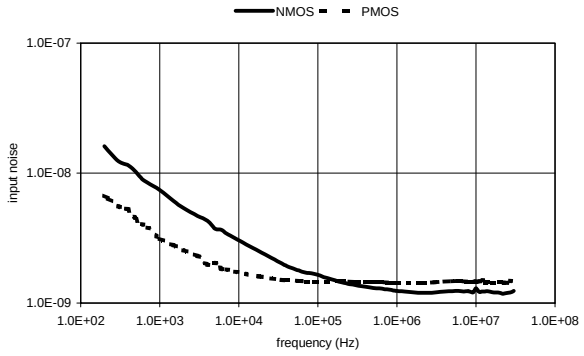

Figure 4: Example of noise spectra for devices of tech_b (Ibias=500 μA: moderate inversion) W/L=2000/0.78.

Table 2: Excess white noise factors.

	tech_a	**tech_b**
W.I.	$\Gamma = 1.1$	$\Gamma = 1.1$
M.I.	$\gamma = 0.85$	$\gamma = 0.65$
S.I.	$4 < \Gamma < 5.5$	$2 < \Gamma < 3.4$

The higher values of Γ we have found in strong inversion are consistent with other results previously reported for submicron technologies [4].

However, it is worth pointing out that a typical input transistor of a low noise front-end amplifier (W/L from 200/1 to 2000/1 and bias current from 50 μA to 500 μA) would rather operate in weak or moderate inversion.

The highest value of the flicker noise coefficient K_a we have measured for PMOS transistors is $6 \cdot 10^{-28}$ C^2/m^2. For NMOS transistors the maximum value is $3 \cdot 10^{-27}$ C^2/m^2.
A value which is used in noise calculations for NMOS transistors in conventional technologies is $6 \cdot 10^{-27}$ C^2/m^2 [3], which is in the same order of magnitude.

4.2 Matching measurements

In this work we have investigated in particular the matching behaviour of enclosed devices.
We have measured about 100 chips. Each chip contains 5 enclosed NMOS differential pairs with different gate area. For each device we have extracted the threshold voltage, the β and the standard deviations of the difference distribution have been calculated.

We have observed that enclosed devices follow equation (6) and (8) for small gate areas, whereas they exibit a "saturation" behaviour for gate area above 50 μm^2.

We have therefore modified equations (6) and (8) as following

$$\sigma_{Vth} = \sqrt{\left(\frac{A_{Vth}}{\sqrt{WL}}\right)^2 + \sigma_{Vth0}^{\ 2}} \qquad (10)$$

and

$$\sigma_{\Delta\beta/\beta} = \sqrt{\left(\frac{A_{\beta}}{\sqrt{WL}}\right)^2 + \sigma_{\beta 0}^{\ 2}} \qquad (11).$$

The value found for A_{Vth} is 5.4 mV/μm which is consistent with eq. (7) since t_{ox} is about 5.5 nm in this technology. The value of σ_{Vth0} is 0.95 mV. For A_β we found a value of 1.5% μm, with σ_{β_0}=0.33%.

Due to these "saturation effects", enclosed layout transistors tend to have worse matching performances. The values at which the saturation occurs are however still compatible with the needs of precise analog design.

4.3 Transimpedance amplifier results

The transimpedance amplifier uses the scheme detailed in [11,12] in which a current controlled g_m stage in used as feedback around a single stage cascode amplifier. The input device of the preamplifier is a NMOS with W/L=500/0.35; an oxide capacitance per unit area of 6.9 fF/μm^2 and a g_m of 7 mS for the input transistor have been used in the noise calculations. The transimpedance gain has been adjusted to 300 kΩ. In the test set-up, the capacitance seen by the input of the preamplifier was calculated to be 5 pF.

The output measured with a digital oscilloscope in these conditions is reported in fig. 5.

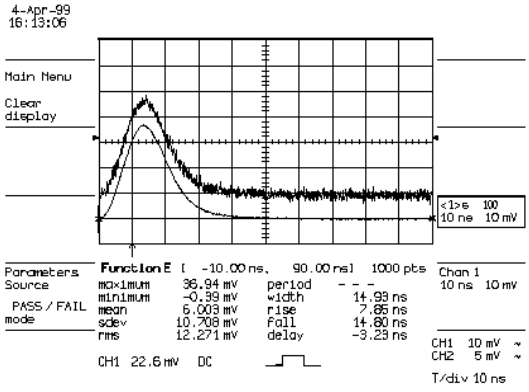

Figure 5: Preamplifier pulse response (input charge: 4 fC).

The output swing for 4 fC input signal is 37.5 mV, with a peaking time of 13 ns. The output noise was

measured with a true r.m.s voltmeter and was found to be about 0.7 mV r.m.s, which corresponds to an input referred noise of 434 electrons. The noise slope was 81 electrons/pF. This value agrees with the one calculated for a second order system (72 electrons/pF) using the formulae proposed in [3].

5 CONCLUSIONS

In this work basic issues related to the use of deep submicron technologies for analog integrated circuits design have been investigated and dedicated test structures have been designed.

Particular care has been paid to the study of the noise performances of the technologies and of the matching properties of enclosed layout devices, which are needed in most applications in order to achieve the required radiation resistance.

The results on the matching of enclosed transistors show that the dispersion of the threshold voltage saturates at a value of 0.95 mV for transistor area above 50 μm^2. This, however, is not a serious drawback for most analog applications.

The noise excess factors found in weak and moderate inversion are close to the minimum theoretical values. Higher excess noise factor have been measured in strong inversion. This region of operation should be avoided in input transistors of low noise amplifiers.

A transimpedance amplifier has been completely characterised. For a power consumption of 1 mW, the amplifier gain is 9.4 mV/fC and the input referred noise for an input capacitance of 5 pF is 434 electrons r.m.s. The noise slope (80 electrons/pF) is consistent with the theoretical calculations (g_m of the input transistor 7 mS) for a second order system, given the short peaking time (13 ns).

Test performed up to now show the compatibility of the measured devices with the requirements of low noise and precise analog designs. Some penalty can be paid if enclosed layout transistors are used in structures whose performances heavily rely on matching.

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