WAFER SCREENING OF THE FRONT−END ASICS FOR ATLAS SCT

Carlos Lacasta, Instituto de Física Corpuscular, Valencia, Spain (e−mail: Lacasta@ific.uv.es)
Jan Kaplon, CERN, Geneva, Switzerland (e−mail: Jan.Kaplon@cern.ch)

Abstract

The continuous increase in volume of silicon trackers in the coming experiments poses a number of new issues to unravel. Among them, the high number of detector readout modules to be built in a relatively quick time will require the use of preselected ASICs. In the particular case of the ATLAS SCT, where about 6 million channels have to be read out with little chance for replacement of the electronics, that becomes a considerable challenge. Specific architecture features of the front−end chips will call for very specific and dedicated electronic testers to provide a full and efficient characterization. This paper describes the system built for the preselection and characterization of the ABCD front−end chip to be used in the readout of the ATLAS SCT microstrip silicon sensors. The system has been used successfully during the last year to tag the 6000 ABCD chips that have been built up to now and has been upgraded to cope with the new features of the last version of the chip.

1. THE ABCD CHIP.

The Atlas Binary Chip DMILL (ABCD [3]) design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker [1]. The Radiation Hard DMILL technology [2], in which the ABCD chip is fabricated, offers the unique possibility of combining a bipolar front−end amplifier/comparator with the CMOS logic in a single chip.

A major issue in the binary architecture implemented in the ABCD chip is the matching between the channels. Two versions of the chip, presenting different solutions of this problem, are currently under development. The ABCD2T version has a gain of 80 mV/fC and a 4−bit DAC for the threshold correction implemented in each channel, together with a common threshold, controlled by a 8−bit DAC, for all the channels, allowing to tune the matching between them. The second version, the ABCD2NT chip, with only the common threshold for its 128 channels, has twice higher gain before the comparator and a layout optimized for better matching.

The block diagram of the chip is shown in Fig. 1. The preamplifier−shaper circuit provides signals with a peaking time of 25 ns, sufficient to keep the time walk of the discriminator in the range of 12 ns and a double peak resolution of 50 ns. This circuit is followed by a comparator whose threshold is applied channel by channel as explained above. The binary data from the discriminator are latched in the input register in either level or edge sensing mode −with a time resolution of 25 ns− and clocked into a 132−cell deep pipeline. For each trigger, the data are transferred from the pipeline to the second level buffer, 128 bits wide and 24 locations deep, that serves as a derandomizing buffer which removes the fluctuations from the L1 trigger distribution. It will store three bits of data per channel, corresponding to the three beam crossings centered on the L1 trigger time, and are set if the input was above threshold during the corresponding crossings. The data compression logic will take these data and suppress the empty channels making the chip output only the hits which match the pattern programmed in the configuration register. The readout logic will be responsible for the capture and release of the token and outputting data from the chip. The readout circuit always waits until the token arrives and on its arrival it outputs the data of the chip. If the chip is in the middle of the chain, sends a token to the next chip. If the chip is configured in send−id mode, it will output the contents of the configuration register instead of the data from the channels.

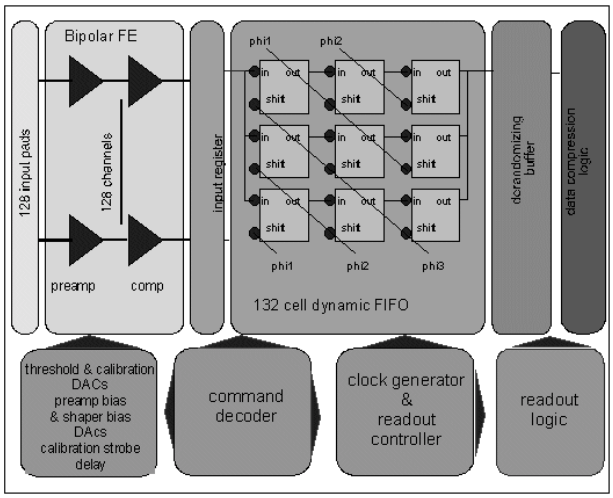

Fig. 1. Block diagram of the ABCD chip.

In addition to the basic functional blocks described above, the ABCD comprises a calibration circuitry for internal generation of calibration pulses whose amplitude is set by a 8−bit DAC and their delay relative to the clock phase is controlled by a delay buffer of 6−bit resolution.

2. THE SETUP

The setup, as sketched in Fig. 2, is based on a Karl SUSS PA200−II probe station with a fully motorized chuck stage whose movement is controlled through the

GPIB interface. The functions implemented in the ABCD chip for internal testability, like internal calibration circuitry or pulsing input register function, allowed to build a simple and robust system where all the communication to the chip is done via digital serial interface. Since the goal is to test the chip with a high frequency clock −up to 50 Mhz−, all signals delivered to and received from the chip had to be buffered on the PCB close to the needles. To this end, a custom designed probe card (PCB) has been made with standard technology and 64 needles with the standard pitch of 200 μm

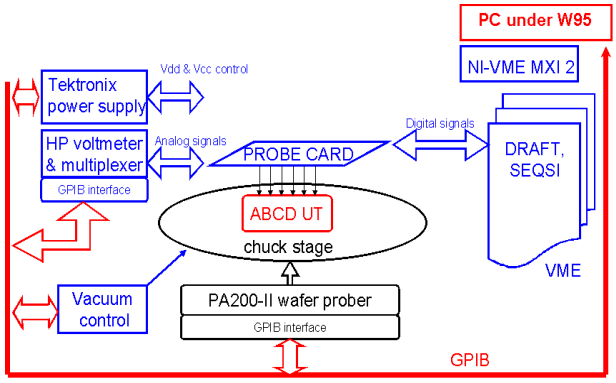

Fig. 2. Schematic diagram of the wafer test system.

The chip control and data acquisition is based on two VME modules: a sequencer (SEQSI [4]) which provides the clock and control signals to the chip, and a data receiver and decoder (DRAFT [5]).

For measurements of the characteristics of the digital−to−analogue converters on the chip, a HP voltmeter with an analogue multiplexer is used, and it is connected to the system through the GPIB bus. The same device is used to control the vacuum to fix the wafer onto the prober chuck. A Tektronics power supply is used to provide the chip with the digital and analogue bias and also to measure the power consumption of those lines.

All the system is controlled by a dedicated program written in C++ and running in a PC under Windows 95. The program controls the VME and the GPIB buses. It programs the sequencer to set the phase between the clock and the command line of the chip, builds the commands to carry out the tests and reads out the DRAFT. On the GPIB side, it controls all the movements of the wafer prober, sets up the voltmeters and power supplies and reads from them all the data. Probe movements are programmed very cautiously and all the system stops whenever any disagreement is found between programmed and monitored coordinates or the vacuum fails. Concerning the tests, it allows to independently select and configure any of them to be done and also takes care of the data acquisition and storage using standard packages to compress the data in order to save as much space as possible. In total, the system takes between 300 and 200 seconds to perform the complete set of tests in a chip, depending on whether the chip is a trim dac version or not.

On a second stage, the data collected by the acquisition program is analyzed using a separate software in order to effectively classify the chips. It also produces a sort of data summary file and provides the information needed to feed a chip database to help in the control of chip quality and distribution.

3. TEST PROCEDURE.

The ABCD chips will be assembled on the hybrids as unpacked devices and, in consequence, the chip preselection and characterization process has to be carried out at the level of wafer screening. The characterization process needs to be complete, accurate and as fast as possible since about 50000 chips need to be preselected. Inasmuch as the ABCD chip follows the binary architecture, a considerable amount of measurements are needed to obtain any information on the analogue performance of the front−end. Also a complete set of digital tests proving the readout protocol, different modes of operation and functionality of the whole logic, together with the characterization of the on−chip digital to analogue converters (DAC), need to be designed and carried out.

3.1. Digital tests.

A number of tests are made to check all the digital functionalities of the chip. The main characteristics to peruse are related to chip control, inter−chip communication and data compression. Additionally, some functionalities like channel masking and redundancy mechanisms should be proven. All the tests make an extensive use of some of the testing tools provided by the chip, like pulsing the input register or generating output patterns through the mask register. To evaluate the performance of the chip in the different tests, four different patterns with a length of 128 bits are usually injected:

- a sequence of 128 ones,
- a sequence of 010101...01,
- a sequence of 101010...10 and
- a sequence with 30% of the channels set to one randomly.

In order to evaluate the performance of the chip under the different tests, a fixed number of events were triggered for each of the patterns and the resulting efficiency studied.

Another key issue concerning the performance of the digital part is to determine the maximum speed of the selected chips. Since the maximum frequency clock attainable in the setup −50 Mhz− is lower than the maximum speed of the ABCD chip for nominal bias conditions[1], the chip performance degradation was

[1]Results from IMS tester performed on diced chips show functionality up to 70 Mhz.

simulated by lowering the power supply. For that reason, all the tests were repeated for two different clock frequencies −nominal 40 MHz and 50 Mhz− and for several values of the digital power supply (Vdd): from 3.3 V up to 4.2 V. The minimum Vdd for which a chip still shows full efficiency at 50 MHz was used to classify them according to their speed performance and in the yield calculation. This is shown in Fig. 3. The histogram has as X−Y coordinates the cells in the wafer and on the Z axis how far from the nominal Vdd −4 V− the chip still shows full functionality at 50 MHz.

The next paragraphs describe the digital tests performed:

- *Configuration register input/output*:
  This is one of the most determinant tests because it proves that the chip can be configured. The configuration register is written with random values, keeping the chip always as master and end chip. The values are then compared with the data returned by the chip in the send identification mode. Since addressing is not meant to be test here, the *universal* address is used.
- *Addressing:*
  The ABCD is supposed to be mounted in a module populated with 12 chips. In order to configure each of the ABCDs independently an addressing mechanism has been implemented which is tested here. The chip is given a random address and it is configured using that address. The value is compared with the one returned in the chip data.
  An extra test is done at this level: The L1 counter is followed and its value stored. It should start at 0 and increase in steps of 1.
- *Input Register:*
  To check the functionality of the mask register, the four patterns are loaded in the mask register and the input register is pulsed. Pulsing the input register *sets to one* the 128 channels. At the output, only the channels allowed in the mask register should be at one.
- *Input Lines:*
  The functionality of both input lines for the chip clock and commands is tested by injecting the four patterns through the mask register and sending the clock and the commands through both lines. The output is contrasted with the patterns.
- *Fake slave:*
  The chip is set as master and middle chip. In the first part of the test the token transmission through both lines is checked. In a second stage, a sequence simulating the data of a slave chip is injected through both input lines of the chip and contrasted with its output. The chip is also provided with a pattern programed in the mask register in order to check that it merges properly its data with that of the slave.
- *Slave:*
  The chip is set as slave and end chip. The four patterns are injected through the mask register and the token sent, after each trigger, through both input lines. The chip output is also searched on those lines.

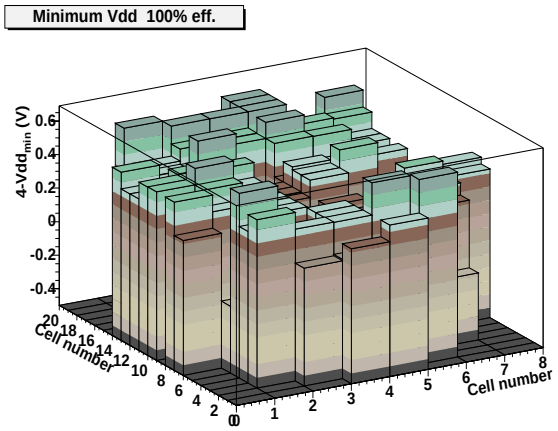

Fig. 3. Wafer map of the maximum distance in volts down the nominal Vdd −4 V− at which the chips, operated at 50 Mhz, still show full digital functionality. The X−Y plane represents the cells in the wafer.

3.2 Power Consumption.

The setup measures the power consumption both of the digital part and the analogue part. To simulate the nominal requirements for the ATLAS SCT occupancy and L1 trigger rate, the measurement was done applying a 100 kHz trigger with an occupancy of 3% of the channels selected randomly. Fig. 5 shows the average values obtained for all the chips passing the digital tests in one of the wafers. Although the distributions are quite narrow, still some chips are far away from the peak. Those chips, with such a high power consumption, are rejected during the selection process due to possible weaknesses of some parts of the digital logic.

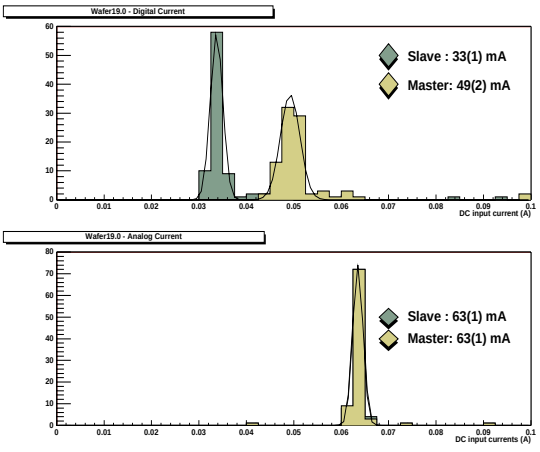

Fig. 4. Current measured for the digital (upper plot) and analog (lower plot) voltages of the chip.

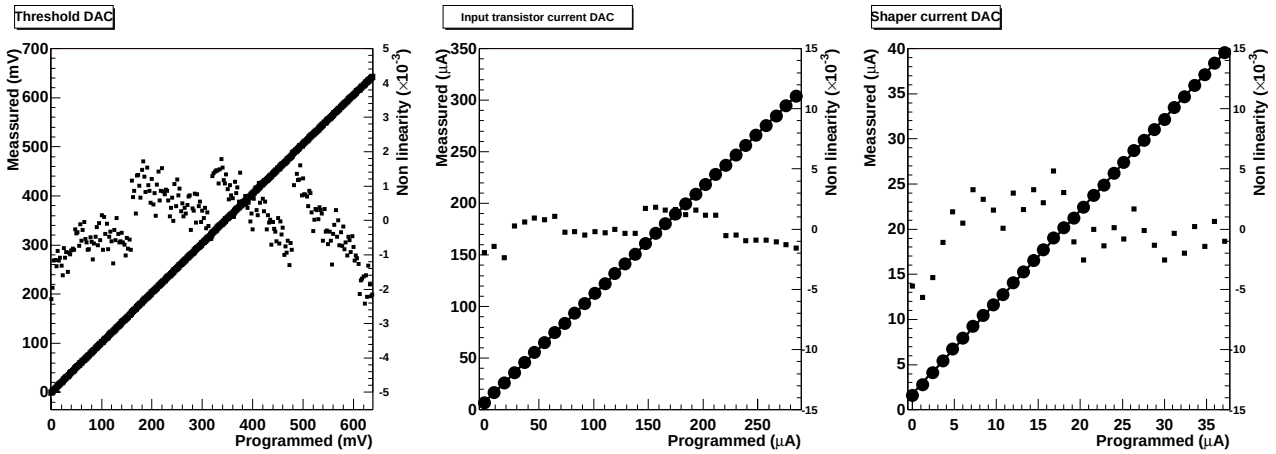

Fig. 5. Linearity of the threshold and bias DACs. The round bullets show how the DC levels change while increasing the values of the DAC registers. The linear fit performed to the data is also shown. The small squared bullets show the deviation from linearity relative to the range of the DAC. Its scale is shown on the right axis.

3.3 Digital to Analogue Converters.

The ABCD has 3 main DACs whose performance have to be carefully tested:

- Threshold DAC (8 bits),
- input transistor current DAC (5 bit) and
- shaper current DAC (5 bit)

The chip incorporates one additional 8 bit DAC for the calibration pulse height which is not directly tested and its failure will translate in a deficient analogue performance. The trim dac version of the chip incorporates an additional DAC per channel to individually trim the value of the threshold. The test performed on this DAC are described in 3.4.1.

In order to prove the behavior of the three DACs, a full scan on the DAC bits is done and the DC levels provided by the chip in its test pads are read with the HP voltmeter. This will allow to measure their linearity, as shown in Fig. 5, where the relative deviation from linearity with respect to the DAC range is also depicted.

3.4 Analogue performance.

The goal of these tests is to determine the basic analogue parameters of the front−end: gain, noise and discriminator offset spread. To this end, a threshold scan for three different input charges is done for each channel in every chip, as described in [6]. The input transistor current and the shaper bias are set to the nominal values and the chip is driven by a 40 Mhz clock. Three s−curves per channel are fitted to a complementary error function. From the 50% points the gain curve is built and fitted to a straight line. The gain and the offset are taken as the slope and the offset, respectively, of the linear fit. The electronic noise information is also obtained, for each pulse, from the s−curve fit.

Fig. 6 shows the distributions of the gain and noise of all the no trim dac chips in a wafer.

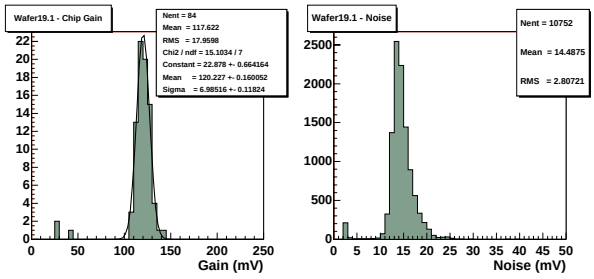

Fig. 6. Average chip gain and noise of all the chips in a wafer.

3.4.1 Trim DAC test.

For the trim dac version of the chip a full scan of the dac bits is done for all the channels and for a fixed calibration pulse. Applying the same analysis described for the gain and offset measurements an overall characteristic of the trim DAC is obtained.

4. YIELD CALCULATION.

To calculate the yield, a selection criteria has been defined based on the results on the digital and analogue tests, together with the power consumption measurement and the DAC studies. Results from the analogue tests are correlated with the digital tests done at different clock frequencies and Vdd. At any of those points a chip will be considered as non−functional whenever a single failure is found in any digital test, the power consumption both in the analogue and the digital parts exceeds 20% the mean value from the wafer, the DAC non linearity is out of range or it has one or more dead channels. A channel is said to be dead when it does not respond to the calibration pulse −or its efficiency is smaller than 95%−, its gain is 20% lower than the mean value of the wafer or the noise is higher than 1500 e^- ENC.

Concerning the DAC linearity, although there is no strong constrain from the specifications, a selection criteria has been defined so that chips will be rejected whenever the spread of the non linearity distribution exceeds 1% in the threshold DAC and 10% in the bias DACs.

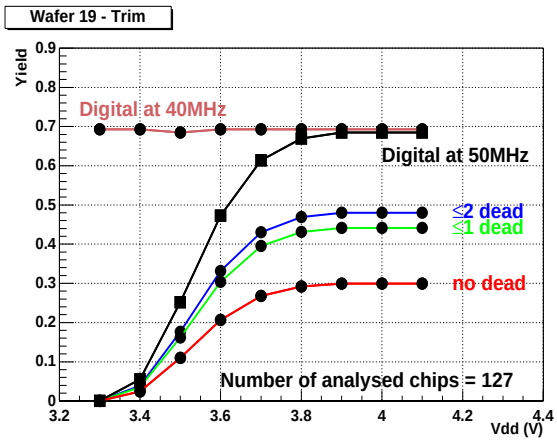

Fig. 7. The lines labeled as Digital show the yield of the digital part of the chip obtained under different test conditions. The line labeled as no dead, shows the final yield after applying the criteria of the analogue tests, power consumption and DAC linearity. Also the yield values obtained when relaxing the requirement on the number of dead channels allowed in the chip are shown.

Fig. 7 shows the digital yield for different digital biases and clock frequencies. The final value of the yield after applying the restrictions on the analogue performance, power consumption and DACs tests is also shown. Typical values of about 30% have been obtained from the wafers of the last process if no dead channels is allowed in any of the chips.

As for the analogue performance, a quality factor is defined as the ratio between the gain and the matching, defined as the spread of the 50% points. This factor is not directly used in the yield calculation although it is widely used during the selection of the chips. The distribution of the quality factor is shown in Fig. 8 for both versions of the chip. For the trim dac version, the quality factor is computed without trimming the channels. On diced chips, and after trimming, a quality factor of 20 has also been obtained.

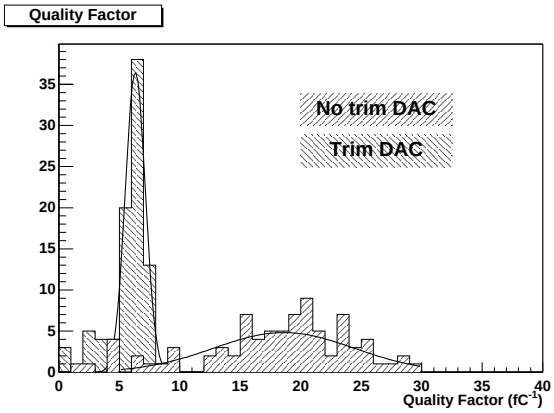

Fig. 8. Quality factor distribution for all the chips in a wafer.

5. CONCLUDING REMARKS

A system has been built which is able to test all the functionalities of the ABCD chip on the wafer. It has proven to perform fast and accurately, providing all the information needed to tag the chips and build a general database for control and distribution of the chips. The system has been successfully used to test all the ABCD wafers supplied up to now and has been upgraded to cope with the new features of the last versions of the chip.

REFERENCES

[1] ATLAS TDR 5, Inner Detector Technical Design Report, Vol. II, CERN/LHCC/97−17, 30 April 1997.

[2] RD29 Status Report "DMILL, A Mixed Analog−Digital Radiation hard Technology for High Energy Physics Electronics", CERN/LHCC/97−15, 11 Mar. 1997.

[3] ABCD Chip Specification. Version 2.0, Dec. 12, 1998.

[4] SEQSI (RAL PC2935), M. Morrisey.

[5] DRAFT (RAL PC3080), M. Morrissey.

[6] Test on ABCD Chips. ATL−INDET−98−217.