Progress in development of the ASDBLR ASIC for the ATLAS TRT

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Abstract

The ATLAS TRT straw tracker will consist of more than 420K straw tubes filled with a Xenon based fast *gas located in a magnetic field of 2T. Some tubes will operate at rates up to 15 MHz. Stringent signal processing goals include: the ability to detect energetic Transition Radiation photons as well as the earliest clusters from ionizing tracks without baseline shifts have been determined using both simulation tools and measurement standards set by hand tuned discrete component prototypes. High channel count and restrictions on cable plant led to the development of custom ASICS to house the detector mounted front end electronics and digitized readout. The ASDBLR is a custom analog bipolar ASIC that provides the full signal processing chain from straw input to the output logic pulse.*

A. *Introduction*

The straw-tube Transition Radiation Tracker (TRT) in the ATLAS detector at LHC [1] is being designed to operate at extremely high radiation levels. Some elements of the 425,000 straw tube detector are expected to operate at rates approaching 20MHz. Each straw has a cathode diameter of 4mm, anode wire diameter of 30μm and will be filled with a gas mixture of 70%Xe+20%CF_4+10%$C0_2$ and operated at a gain of $\approx 2 \times 10^4$. Xenon gas improves the efficiency for stopping TR photons, but lengthens the *ion tail* of the current pulse significantly compared to more conventional Argon based mixtures. In order to achieve the required 150μm track resolution, at high rates, the baseline will need to be stable so that the avalanche signal from the first primary electrons can be accurately detected. Ionizing tracks will deposit an average of $2KeV$ resulting in a charge of approximately 20fC at the input to the amplifier during the 7.5ns peaking time. Due to the circular cathode geometry and the relatively low velocity of the primary ions there is significant variation in the signal shape and total charge. For high efficiency it is necessary to operate at thresholds of 2fC or $200eV$ equivalent energy loss. Signals of 20-50 times threshold will occur frequently making it important that the signal at the input to the comparator be adjusted to reliably return to baseline as soon as possible after the last of the drift electrons from a track have arrived at the wire. Radiation and breakdown issues place relatively strict requirements on the gas gain, making it necessary to employ low noise design techniques. Finally, the large number of *detector mounted* electronics channels make it important to keep the power dissipation as low as feasible.

B. *ASDBLR ASIC BLOCKS*

The eight channel ASDBLR wire chamber ASIC, currently in its third generation, has been developed to meet the tracking and particle identification objectives of the ATLAS TRT using inherently radiation tolerant analog bipolar processes.

A block diagram of the first version of the circuit is shown in Figure 1. A more detailed description of each

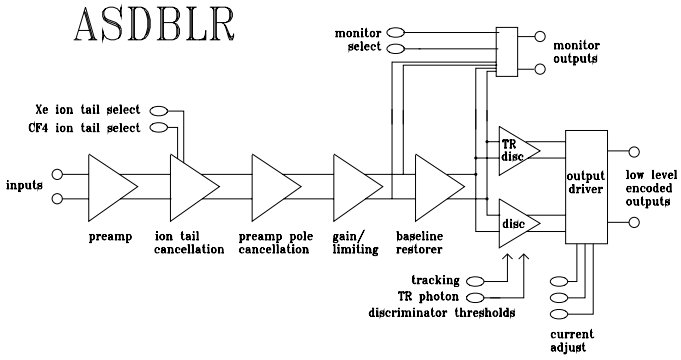


Figure 1: Blocks of the ASDBLR Circuit

block may be found in reference [2]. Good common mode rejection, both on and off chip is achieved by providing package leads to both 150MHz preamplifiers on each channel. All remaining stages are fully differential. The shaper provides ion tail cancellation for either Xenon or Argon based gas selected by an externally controlled logic level. Ion tail cancellation is designed to operate linearly over a 600fC range with a soft saturation characteristic so that lingering ion current from large depositions does not severely inhibit double pulse resolution. Ion tail cancellation is followed by a multi-pole shaping block to provide noise filtering without compromising double pulse resolution. The signal at the output of the shaper is limited to about 120fC of equivalent input charge, the largest allowable threshold setting. A baseline restorer BLR is included to eliminate effects of pileup, reduce sensitivity to mismatch in the ion tail compensation and decouple the DC offsets in the preamplifier and shaper from the comparator section.

A low and high level comparator on each channel allows the ASIC to trigger on the earliest arriving clusters from tracks for optimal position resolution and to detect energetic TR photons with high efficiency. The peaking time of the signal into the low level or tracking comparator is 7.5ns, chosen to optimize tradeoffs between signal to noise and tracking resolution. The high level, TR photon discriminator, has a longer, 10ns, peaking time to allow the prompt and reflected signal from the

unterminated straw to be integrated. This reduces the amplitude dependence on the position of the charge deposition along the wire, increasing the threshold dead band between ionized track depositions and TR photons. The output of the two comparators is summed as a differential current that forms a ternary output level of 0, 200 or 400 μA. A more detailed described of each block may be found in reference [2].

C. Measurements

Measurement of the first version of the ASDBLR pointed to the need for an increased gain (40%) in the BLR and a reduced shaping time. This was due to the realized gain of the straw and fabricated amplifier, combined with a minimum signal size requirement in the BLR for low signal attenuation. Taking advantage of

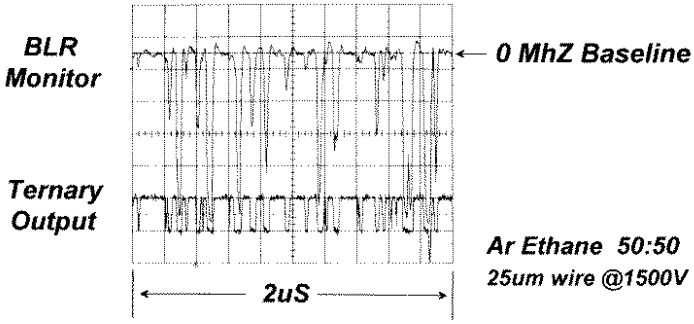


Figure 2: Measurements of the revised ASDBLR triggering at 10MHz induced by distributed Sr90 sources.

provisions made for metal layer revision, we were able to use wafers held at pre-metalization from the first run to fabricate parts with the revised design parameters. This revised design has been measured extensively and meets all basic design requirements.

High rate operation has been measured with Argon and Xenon based gas mixtures. Figure 2 shows a scope plot of the first high rate operation of the ASDBLR attached to a straw module. The upper trace in the scope plot shows the analog monitor of the BLR output and the lower trace shows the ternary comparator output from the same channel. The straw was irradiated by several Sr90 sources achieving an effective rate of 10MHz. No baseline shift was observed. The operation of the ternary output is demonstrated in the last time division where the a discriminator trigger of twice the standard amplitude signals detection of an input pulse above the low and the high threshold levels.

Test beam measurements (Summer 1998) were taken at the CERN H8 beam line using a silicon-strip detector telescope sandwiched around a straw module to measure track position. Radioactive sources were added to study rate dependence. Track resolution and efficiency were measured at rates up to 20MHz using both the ASDBLR and a carefully tuned, DC coupled, single channel of discrete electronics. A comparison of the measurements is

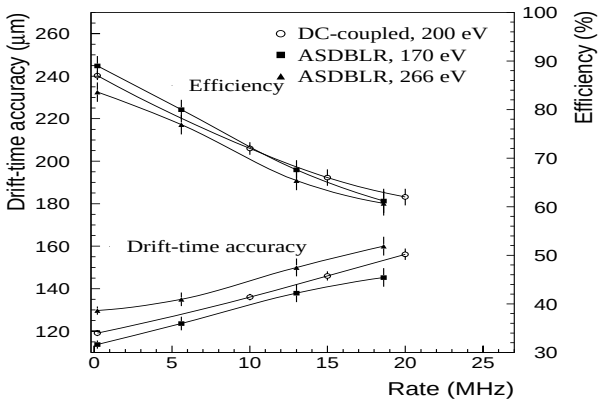


Figure 3: Test Beam measurements comparing the performance of the ASDBLR at two different gas gains and a hand tuned, DC coupled, single channel of discrete electronics. Note that the efficiency in the plot is defined as a hit withing 2σ of an associated track.

shown in Figure 3. With the gas gain set to its nominal value, the lowest operational threshold was $266eV$. At this value, the ASDBLR offered slightly poorer track resolution than the hand tuned electronics channel. Raising the gain by 50% improved the performance to better than that of the hand tuned channel suggesting that a higher internal gain before the BLR might help improve track resolution.

As the size and complexity of high energy physics detectors has grown there has been an increasing reliance on simulation tools to predict the detailed performance of high rate detectors. In Figure 4 the predictions of a montecarlo tool developed specifically for the TRT that includes the effects of the baseline restorer overshoot are compared with data measured in the test beam using the fabricated ASDBLR.

D. ASDBLR in Rad Hard BiCMOS

Significant overhead in the power and connections between the analog front end and the digital time measurement chip could be eliminated by the use of a *radiation hardened* BiCMOS process. We are evaluating the risks and benefits of using a relatively new SOI process, DMILL.

1) Prototype Version

In June 1997 we submitted a prototype six channel ASDBLR with three channels of Xenon and three channels of Argon tail compensation in this process.

A key part of this submission was the implementation of a new baseline restorer circuit. In this design, the shaper output is capacitively coupled to the BLR as before, but the simple diode shunt across the coupling capacitors is replaced by a four diode bridge. The impedance between the outputs is regulated by a differential pair that controls the current in the bridge. When the signal is of the desired polarity, the current is

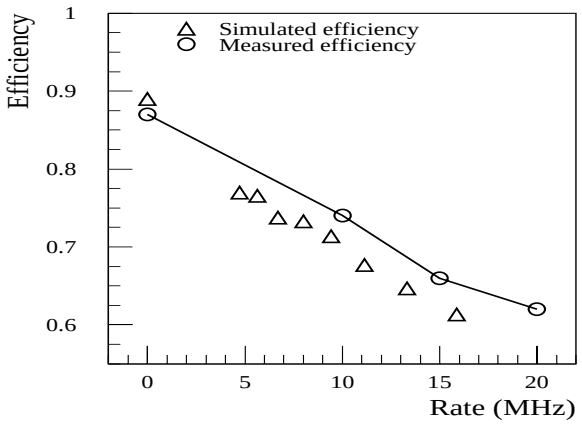


Figure 4: Triggering Efficiency for hits within 2σ of the reconstructed track (The raw hit efficiency at 0 MHz is 97%). Good agreement is shown between test beam data and a simulation tool that predicts tracking efficiency for straw tubes based on characteristics of the tube and shape of the ASIC signal at the on chip comparator input. This tool will be employed in Monte-Carlo predictions of detector performance.

reduced to near zero, increasing the impedance of the bridge to minimize the discharge of the BLR coupling capacitors. As the shaper output returns to baseline droop in the coupling capacitors causes the BLR output to overshoot. The current regulator shifts more current into the diode bridge which quickly equalizes the voltage of the coupling capacitor outputs. The shaper and BLR response of the new circuit to a 2fC (200eV) input signal is plotted in Figure 5. In Figure 6 the advantage of the bridge over

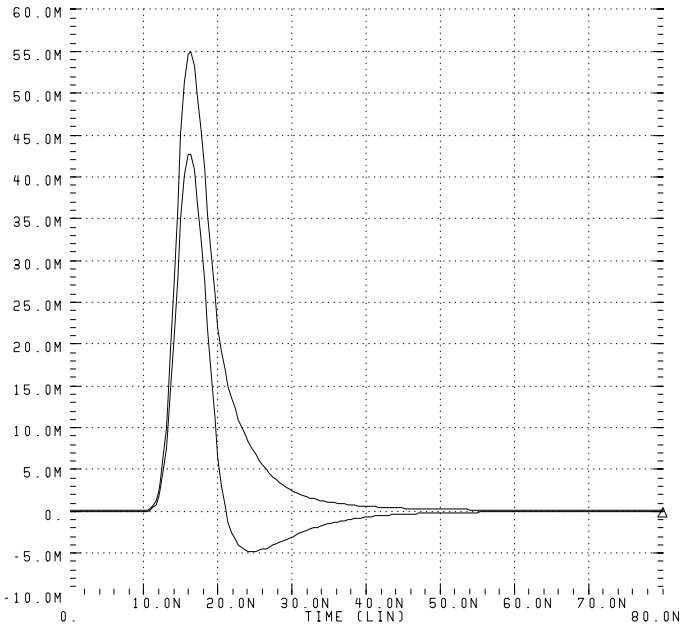
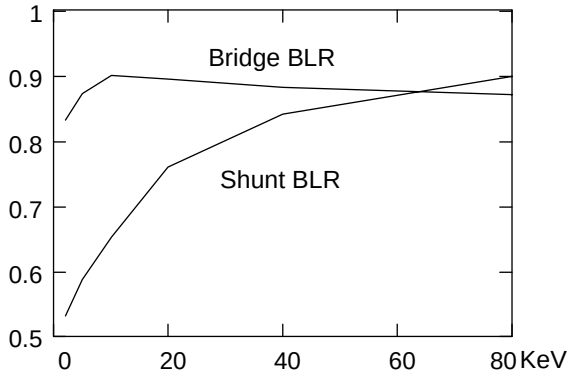


Figure 5: The above traces show the Shaper and BLR response as calculated by HSPICE for a 2fC ($200eV$ equivalent deposition) parameterized TRT pulse into an ASD with bridge type BLR.

the shunt BLR is demonstrated over a large part of the expected operational range. SPICE calculations of gain and maximum overshoot are plotted for each BLR type over a range of input charge from $200eV$ to $8KeV$. The bridge BLR gain is nearly uniform down to the $200eV$, threshold level, inputs. Fabricated parts demonstrated

BLR GAIN .VS. INPUT CHARGE



BLR OVERSHOOT RATIO .VS. INPUT CHARGE

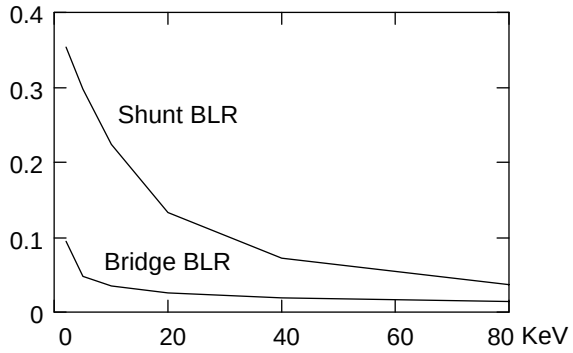


Figure 6: Comparison of overshoot and gain of the *bridge* and *shunt* type Baseline Restorer as a function of input charge.

high yield and good uniformity, but also indicated that the process was not yet mature. The resistors measured 25% higher than nominal and we observed a tendency for harmonic oscillation. Nonetheless, the fabricated ASIC provided useful measurements for all aspects of operation.

Figure 8 shows the shape of the TRT straw signal at the input to the ASDBLR in the upper trace and the processed signal after tail cancellation observed at the monitor output in the lower trace.

Although the preamp and shaping section circuit configuration is virtually identical to that of our previous design, we have observed high frequency harmonics in the DMILL prototype that are not present in either of two predecessor designs manufactured in an analog bipolar bulk silicon process. In these designs, the tail cancellation stage is differential, with each input connecting to one of the preamplifiers. Tail cancellation depends on a sharp differentiation of the input signal which is accomplished using a large capacitor at the emitters of a differential transistor pair. One side of this capacitor is exposed to the

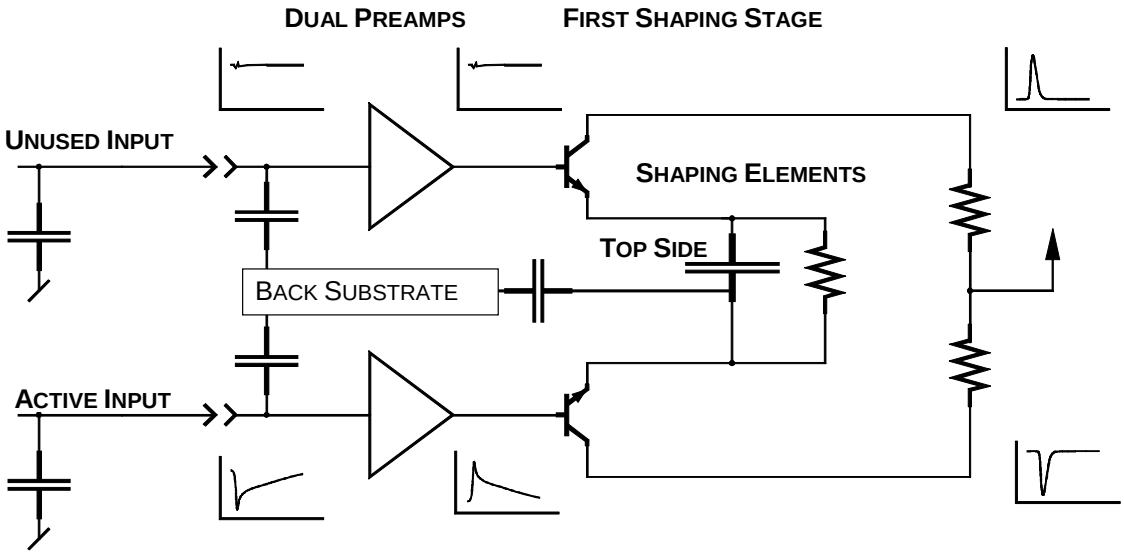


Figure 7: The figure above depicts the model used for SPICE calculations of the effects of charge coupled to the uncommitted substrate below the insulator layer for the ASDBLR preamplifier fabricated in the DMILL SOI process. An important element is the capacitor between the emitters of the differential pair. A pulse applied to the *unused* preamp input generates a signal on the top side of the capacitor and does not produce additional harmonics in the output. A pulse applied to the *active* input does.

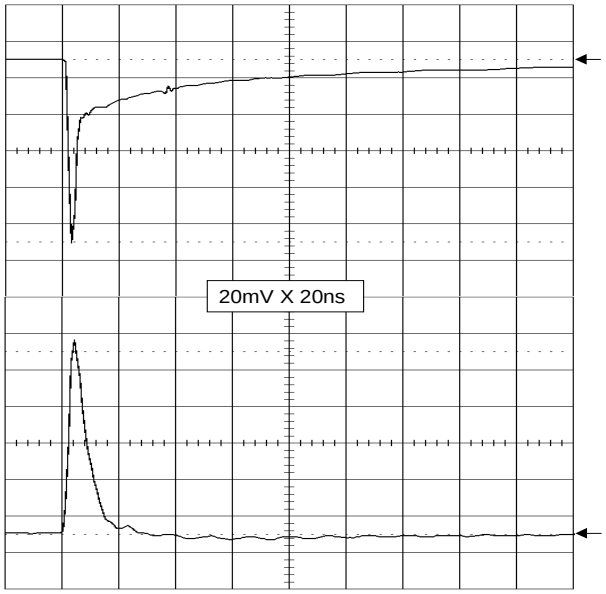


Figure 8: The upper trace is the recorded signal from a pulser designed to mimic the shape of point ionizations in a TRT straw filled with a Xenon based fast gas. As can be seen in the plot, there is still appreciable current flowing 180ns after the pulse. The response of the prototype DMILL ASDBLR after tail cancellation is shown in the lower trace. Considering the fact that the process resistors were 25% above their nominal value, the circuit for shortening the ion tail appears to be quite robust.

back substrate and carries the amplified signal from the *active* input. The other side faces away from the substrate and carries the amplified signal from the *unused* input. In the DMILL SOI process, the relatively low resistance back substrate can not be directly contacted through the 450nm insulator layer and is floating. We found that the harmonics observed in the prototype are consistent with capacitive coupling from the tail cancellation circuit to the inputs through the back substrate (see Figure 7). Pulser studies showed that when the hookup capacitance at the inputs is unbalanced, as will be the case when attaching to a TRT straw, harmonics are observed at the analog monitor output when a signal is applied to the *active* input, but not when an inverted polarity input is applied to the *unused* input.

The left plot in Figure 9 shows two measurements taken with a digital oscilloscope. In the upper trace, a positive pulse is injected into the *unused* input and in the lower trace a negative signal was injected into the *active* input. Similar behavior is demonstrated in the plot on the right side of Figure 9 using the simple SPICE model shown in Figure 7. The external capacitance at the inputs is unbalanced (5pF and 17pF) and a 100fF capacitance couples each input to the uncommitted substrate node. One plate of the tail cancellation capacitor couples to the back substrate with 300fF.

2) Engineering Version

We recently submitted an extensively revised and optimized version of the ASDBLR in the DMILL process that should meet or exceed the signal processing goals of the TRT readout. Each channel has approximately six hundred hand sized and placed components. SPICE based performance calculations were aided by the use of substantially more sophisticated models of the DMILL process revised to include the *predictable* parasitic

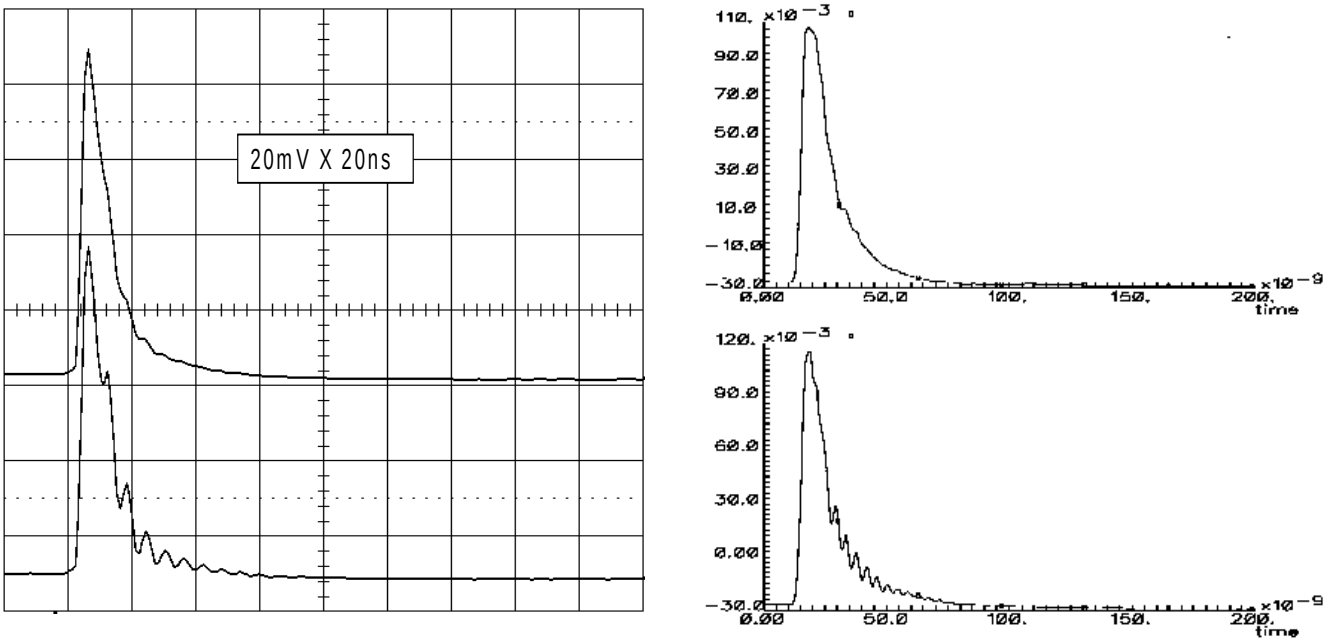


Figure 9: *Left Figure:* The signal at the shaper monitor point of the DMILL ASDBLR exhibits an input and load-dependent harmonic pickup. In the upper trace a positive pulse is injected into the *unused* input, in the lower trace a negative pulse (straw polarity) is injected into the *active* input.
Right Figure: The results of a SPICE calculation with 100fF feedback from a global substrate node to the inputs. The plots show the calculated response at the shaper output with a positive signal into the *unused* input in the top plot and a negative signal into the *active* input in the lower plot.
The capacitive load on the *unused* input is much lower than on the *active* input in all cases above.

capacitance to the back substrate. The calculated power dissipation is 36mW/channel and the RMS equivalent input noise is 2000e. Several changes to the prototype design were employed to reduce the susceptibility to pickup from the back substrate. These include: 1) the installation of a grounded guard ring around input devices, 2) connection of unused silicon on the top side of the insulator to a fixed potential 3) the addition of a low gain differential stage to symmetrize the preamp signal before tail cancellation, 4) splitting of the tail cancellation capacitor into two half size capicators cross coupled, 5) the use of two terminal pad structures that provide contact to a conductive buried layer just above the insulator to shield the signal on the pad from the substrate below the insulator. Important features of this submission are:

- Dual inputs with negative Input Protection using NPN transistors for fast response.
- Digitally selectable Xenon or Argon based ion tail cancellation.
- Digitally adjustable tuning of the ion tail cancellation to accomodate a change in gas mixture or wire diameter.
- Bridge type baseline restorer
- Two level discrimination: *Low level*- 7.5ns peaking time, 0-10fC range. *High Level*- 10ns peaking time, 15-120fC range.
- Programmable current ternary output 0 - 3mA steps (200uA design)
- Analog monitor of the input and output to the baseline restorer on channel 1 and 8.

This chip was designed for use with a partner chip, the DTMROC, which will decode the ASDBLR ternary output, register the time of leading and trailing edges of low level triggers as well as indicate the presence of a high level trigger (suggesting the presence of a TR photon).

I. References

[1] *ATLAS TDR 4* CERN/LHCC/97-16, ISBN92-9083-102-2, April, 1997.
[2] B. Bevensee, F.M. Newcomer et al. *An Amplifier Shaper Discriminator with Baseline Restoration* IEEE Transactions on Nuclear Science, 1996, V43 Pg. 1725.