PERFORMANCE OF THE ELECTRICAL MODULE PROTOTYPES FOR THE ATLAS SILICON TRACKER

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ABSTRACT

Electrical modules for the ATLAS Silicon Tracker (SCT) have been fabricated and tested. The modules consist of 6 ABCD front-end chips connected to silicon strip detectors, with the electronics hybrid and detector geometry as specified for the barrel and forward parts of the tracker. Tests were done with the second batch of the ABCD chip (ABCD2), connected to 6cm or 12cm long strip detectors. The functionality of the modules is demonstrated. The performance of modules depends on the signal gain in ABCD2 chips and on the grounding scheme. The design of the chip has been improved according to these observations. Recent results obtained with the new release of the chip (ABCD2T/NT) mounted on modules with 12cm strip detectors show the expected noise level of less than 1500 el., intrinsic stability and channel matching performance within 5%.

1. INTRODUCTION

The ABCD design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker. The DMILL[1] technology, in which ABCD is fabricated, is one of the possible choices for building the radiation hard front-end electronics. The functionality is fully compatible with another option developed for the SCT with two chips: CAFÉ-M, a front-end chip in MAXIM bipolar process, and ABC, a binary readout chip in rad-hard HONEYWELL CMOS process.

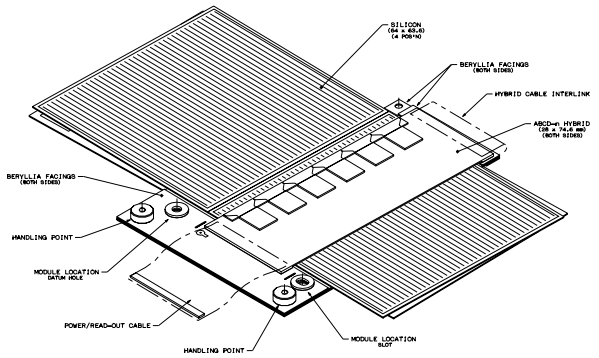
Initial results with single chips of the second run received last year (ABCD2) have been reported [1]. Modules have been built with 6 ABCD2 chips and the associated number of silicon strip detectors. Excessive mismatch of channel-to-channel threshold (already known at the chip level) and a large noise increase, observed only when all chips were mounted to the biased detectors, caused the analysis of the parasitic effects affecting the system stability and of the matching properties of some components. A new design (ABCD2T/NT) with protection against noise pick-up and the selection of new components from the technology has been done and chips were fabricated. The very recent results obtained with electrical module prototypes demonstrate the effectiveness of the new design.

2. CONSTRUCTION OF ELECTRICAL MODULES

The module prototypes are built according to the geometry of either the barrel part of the detector or the forward disks.

[1] TEMIC Semiconductors, La Chantrerie, F-44306 Nantes

A typical geometry for the barrel is shown on Figure 1.



The electrical module has three main components: the silicon strip detector is made of two daisy-chained 6cm long p-on-n silicon strip detectors. There are 768 strips at a pitch of 80um. The hybrid is the support component for the electronics and provides the connectivity between detector, electronics and cables. The readout chips (ABCD) are glued and bonded directly to the hybrid. A realization of the hybrid for double-sided modules is shown in Figure 2 [2].

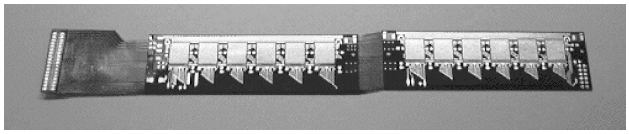
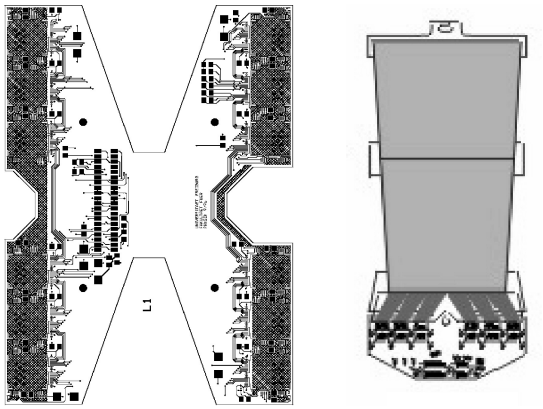


Figure 2: Kapton Hybrid for the barrel SCT detector (electrical prototype).

The geometry for the forward region uses an end-tap configuration and the hybrid has a "butterfly" shape. The typical layout for the forward hybrid and a preliminary drawing of the forward module are shown on Figure 3.



(a) (b)

Figure 3: Kapton hybrid (a) and module (b) for the forward SCT detector (electrical prototype).

3. ELECTRICAL MODULE WITH ABCD2

The detailed evaluation of ABCD2 chip demonstrated complete functionality, a channel gain of 120mv/fC, a channel noise of 760el before detector mounting, but an excessive spread of threshold setting from channel to channel [1]. The construction of complete modules with 6 daisy-chained ABCD2 chips bonded to detectors exhibited a large increase in noise with 12cm strips, although with 6cm strips the noise remained acceptable. This is demonstrated on Figure 4.

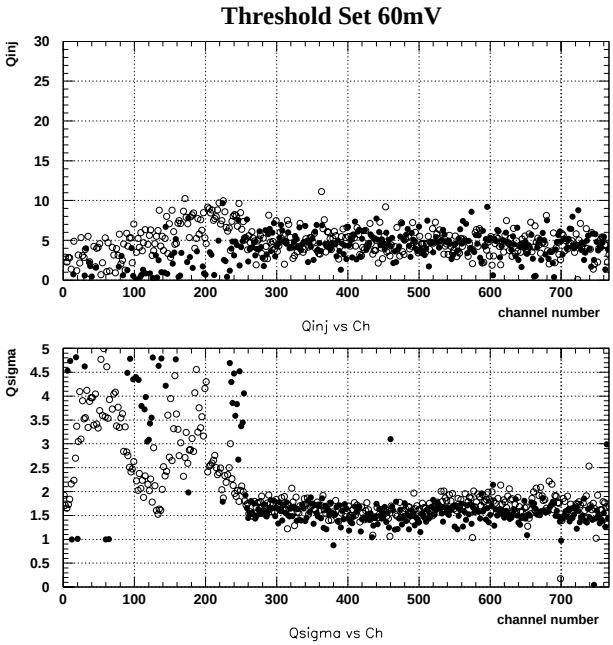


Figure 4: S-curve 50% point distribution (upper curve) and noise distribution (lower curve) for one module with 2 ABCD2 chips with 12cm strips and 4 with 6cm strips

The upper graph on Figure 4 is the plot of the injected signal amplitude per channel (arbitrary units are on the vertical scale) to get the channel output being statistically 50% of the time 0 or 1 (the so-called 50% S-curve point) when threshold for all channels was set to 60mV. The horizontal axis shows the channel number, ranging from 1 to 128 for the first ABCD2 chip, 129 to 256 for the second chip, up to 768 for the last channel of the last chip. The two first chips (channel range from 1 to 256) were mounted with channels alternatively bonded to 6cm and 12cm strips. The last four chips (channel range from 257 to 768) were always bonded to 6cm strips. The lower plot of figure 4 shows the large increase in noise as soon as there are channels connected to 12 cm strips, affecting even the channels interleaved with 6cm strips.

Another demonstration of the excess noise with 12cm detectors is shown on Figure 5: the S-curve is plotted for all 128 channels for each of the 6 chips on one module. When all 6 chips are bonded to 6cm strip detectors only, the shapes of the curves are correct (except for the last chip in this figure) (plain lines on Figure 5). When one of the chips is bonded to 12cm strips instead of 6cm, the S-curves for all the chips are degraded (dotted lines on Figure 5).

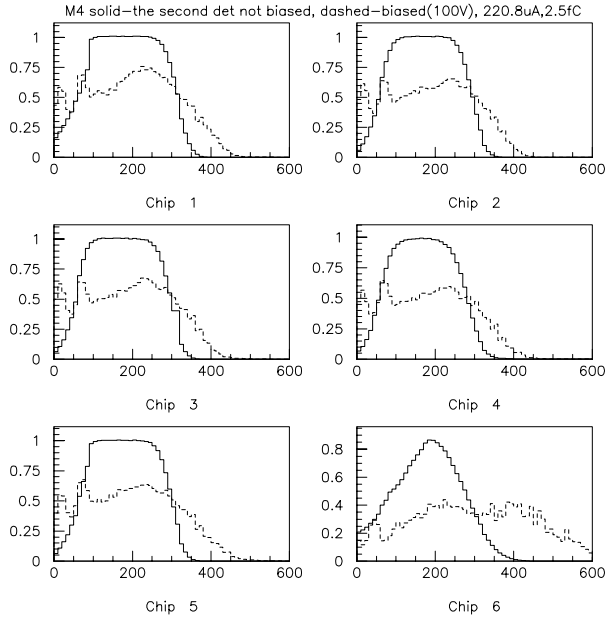


Figure 5: S-curve for each of the 6 chips on one module. Plain lines: all channels connected to 6cm strips. Dotted lines: one chip is bonded to 12cm strips (all others with 6cm).

It was possible to deduce from these measurements the following conclusions [2,3,4,5]:

- The excess noise was unavoidable on modules with more than a few tenths of channels connected to 12 cm strips at nominal operating conditions
- It could be removed by reducing the signal gain per channel (60mV/fC instead of 120mV/fC)

Different combinations in hybrid ground plane geometry and different grounding schemes used to connect the detector bias to the analog ground of the chip were tested but without gaining any substantial improvement.

4. ABCD2T/NT DESIGN

4.1. Excess Threshold Spread Correction

Both new technology choice and design change were made to reduce the threshold spread observed on ABCD2 chips. The new ABCD2NT version keeps a high gain (140mV/fC) in signal amplification, but large size analog components are used to improve the matching properties. Also new high value resistors were used (extrinsic base resistor), instead of low implant resistor.

The ABCD2T version is using a more drastic option to reduce offset mismatch: there is a 4 bit linear DAC (trim DAC) included in each channel to correct for individual mismatch of the threshold in the range of 150mV. The 128 trim DAC are loaded with a new instruction set developed for this version of the chip.

4.2. Excess Noise Protection

The main correction concerns the pad layout of the channel inputs. DMILL is an SOI technology with an oxide buried layer framed inside the silicon volume below the active parts of the components. The silicon volume below the oxide (backside) can be left floating (no connection to any potential) or be connected to a potential as ground. The buried oxide layer acts as adding capacitance coupling between the nodes of some components (mainly the collector of bipolar transistors, the bottom of capacitors, the metal of I/O pads) toward the backside. In the case of modules with ABCD2, a very strong effect is observed depending on the connection of the backside to the ground. No stable operating condition was found (even without detector) if the backside was left floating. Simulation of the front-end (128 channels) with models of the couplings to the backside, with a full strip detector electrical model could confirm this observation. A possibility of the technology is to add a conductive implant layer below the pad metal [6]. The cross-section is shown in Figure 6. The buried implant layer is connected to a dedicated “ground” pad with no connection to other components of the chip, in order to minimize the risk of coupling the input pads to other nodes.

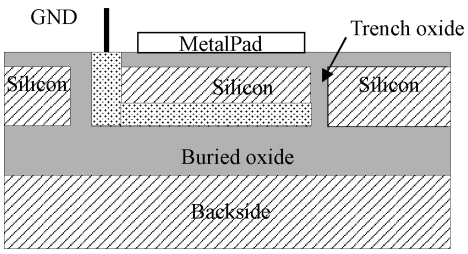


Figure 6 : Cross-section of a modified input pad with shielding between pad metal and backside.

Some other improvements were made in order to reduce the coupling and parasitic effects toward the backside and between components.

5. ELECTRICAL MODULE WITH ABCD2T/NT

Electrical module prototypes with ABCD2T (low gain, trim DAC version) and ABCD2NT (high gain, no trim DAC) with 12cm strip detectors were found operating without excess noise in the full range of possible biasing of amplifiers.

5.1. Module with ABCD2NT

Figure 7 and 8 show the gain and the noise measured on a module with 6 chips and strip detector. Chip number 3 (channel range 256 to 383) is mounted with 1/3 channels to 12cm strips, 1/3 to 6cm strips, and 1/3 are not connected to detector. All other chips are connected to 12cm strips.

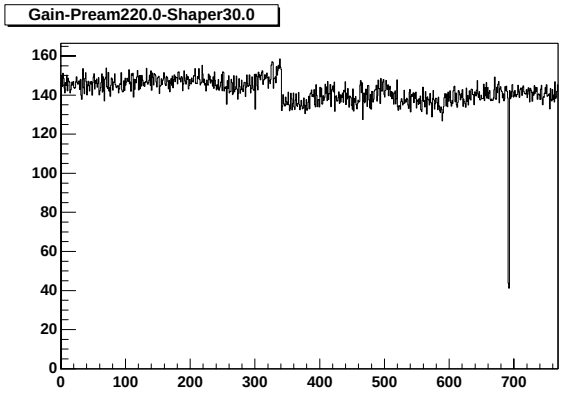


Figure 7: Gain distribution along one module (6 ABCD2NT chips). 1fC input charge. Chip number 3 (channels 256 to 384) is bonded with different strip lengths. Horizontal axis is channel number. Vertical axis is mV.

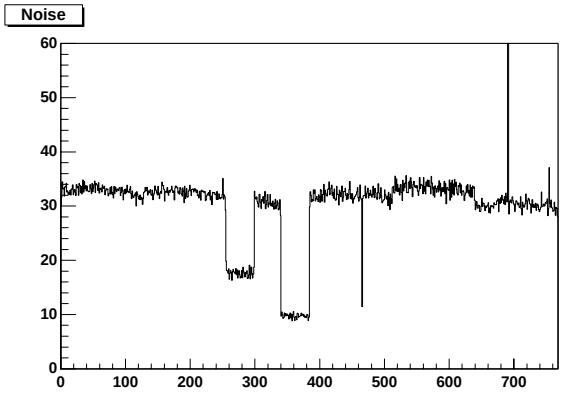


Figure 8: Noise distribution along one module (6 ABCD2NT chips). Chip number 3 (channels 256 to 384) is bonded with different strip lengths. Horizontal axis is channel number. Vertical axis is mV.

The noise amounts to 1400 (resp. 770, 430) electrons with 12cm strips (resp. 6cm and no detector bonded). The gain is as expected in the range of 140mV/fC.

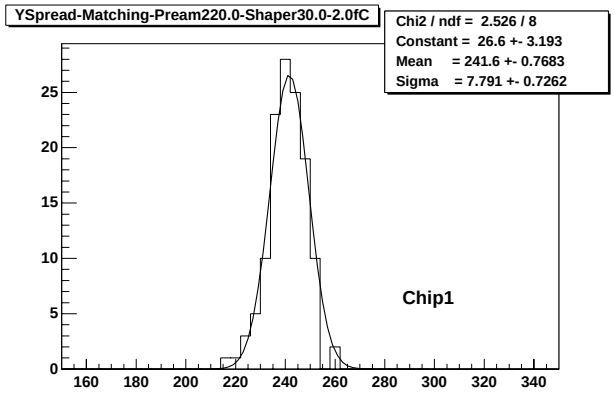


Figure 9: Histogram of the S-curve 50% points for the 128 channels of chip1 on module with ABCD2NT chips. Horizontal axis is in mV. Injected charge is 2fC.

Figure 9 represents the histogram of the S-curve 50% point along one module (the chip number 3 with different input loads has been removed from analysis). The spread of threshold is 7.8mV rms, which translates to 5.5% rms spread at 1fC threshold.

5.2. Module with ABCD2T

Figure 10 and 11 show the gain and the noise distribution measured on a module with 6 chips and strip detector. All chips are connected to 12cm strips. The noise amounts to 1375 electrons with the 12cm strips. The gain is in the range of 65mV/fC.

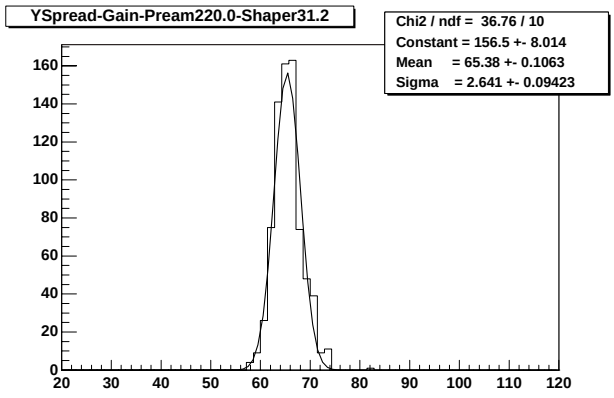


Figure 10: Gain distribution along one module (6 ABCD2T chips). 1fC input charge. Horizontal axis is mV. Vertical axis is mV

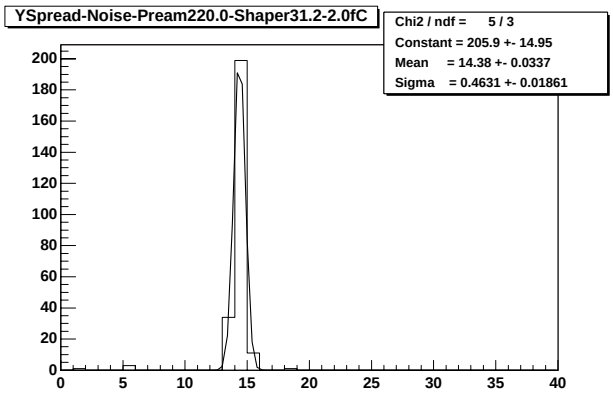


Figure 11: Noise distribution along one module (6 ABCD2T chips). Horizontal axis is mV. Vertical axis is mV.

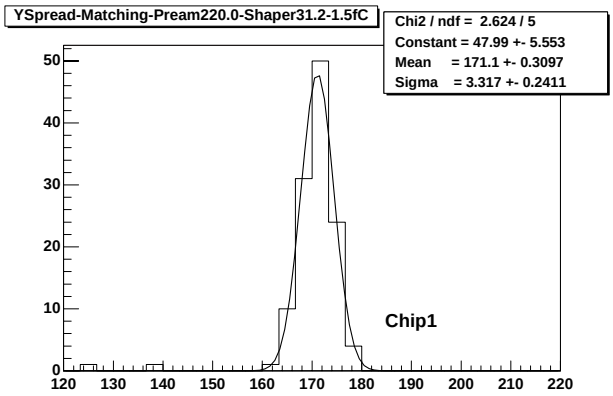


Figure 12: Histogram of the S-curve 50% points for the 128 channels of chip1 on module with ABCD2T chips, after trimming the threshold for each channel. Horizontal axis is in mV. Injected charge is 1.5fC.

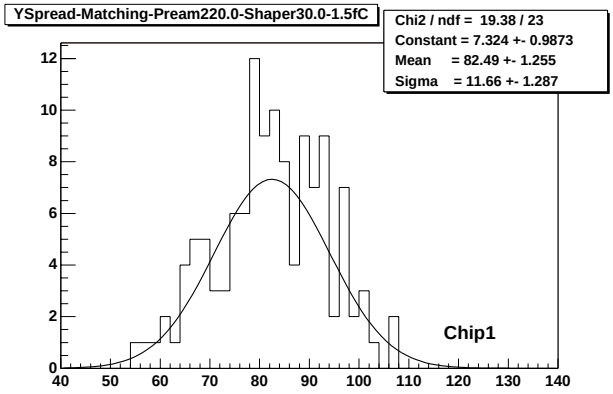


Figure 13: Histogram of the S-curve 50% points for the 128 channels of chip1 on module with ABCD2T chips, before trimming the threshold for each channel. Horizontal axis is in mV. Injected charge is 1.5fC.

Figure 12 represents the histogram of the S-curve 50% point along one module. The spread of threshold is 3.3mV rms, which translates to 5.1% rms spread at 1fC threshold. This value is obtained after the individual trimming of threshold for each channel. Before trimming the spread is 11.6mVrms (18.3% at 1fC threshold) as seen on figure 13.

6. CONCLUSIONS

We have built working electrical prototypes of the SCT modules designed for the barrel and forward parts of the detector. Results obtained with the last version of the ABCD readout chips (ABDC2T/NT) show a gain uniformity of less than 3%, noise level below 1500 electrons with 12cm silicon strip detectors, channel-to-channel uniformity of threshold of 5.5% at 1fC (ABCD2NT) or 5.1% at 1fC (ABCD2T, after trimming). Power consumption is 4V, 45mA for the digital part at 40MHz clock frequency, and 3.5V, 60mA for the analog part of the chip.

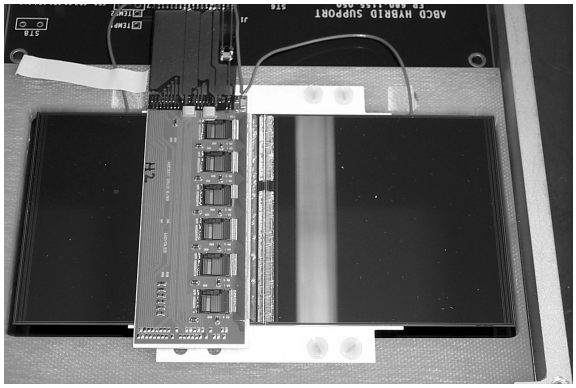


Figure 14: Picture of one module prototype with 6 ABCD2T chips for the SCT detector barrel.

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