Performance Studies of Pixel Readout Electronics in RICMOS IV-SOI and DMILL processes

W. Karpinski, K. Lübelsmeyer, G Pierschel, D. Quadflieg
I. Physikalisches Institut, RWTH Aachen, D-52056 Aachen, Germany

Abstract

The CMS Pixel Collaboration investigates two radiation hard processes, DMILL and RICMOS IV-SOI Honeywell, for the production of the front-end electronics. To evaluate the applicability of the two technologies for this project a readout chip for a 22x30 pixel detector array has been developed. Chips were fabricated first in DMILL process (PSI30) [1], and then we translated this architecture to RICMOS IV technology. For both implementations, detailed measurements are presented before and following irradiation up to 30 Mrad.

1. INTRODUCTION

Experiments at the forthcoming LHC will place stringent requirements on electronics used in the tracking of charged particles, especially for those components which will be installed close to the beamline. The devices will be exposed to irradiation levels around 50 Mrad and 10^{14} particles/cm^2 over their life time. Nevertheless, low noise operation is to be preserved, timing resolution must remain adequate and power consumption per channel has to be kept at a tolerable level. The technology used determines the quality of the whole readout system. To make the best choice and to prepare alternatives for mass production, the CMS Pixel Collaboration has been investigating two radiation hard processes: DMILL [2] and RICMOS IV [3].

We have previously tested the applicability of enhanced RICMOS IV (0,65 μm SOI CMOS) technology for pixel detector front-end electronics by measuring DC, AC and noise parameters of NMOS and PMOS transistors before and after irradiation with gammas from Co^{60} up to a total dose of 50 Mrad [4]. All devices remained functional after irradiation with no anomalous behaviour. The threshold voltage of the top channel shifted less than 140 mV for PMOS and 200 mV for NMOS transistors. The transconductance decreased only by 10% for PMOS and 20% for NMOS transistors. No radiation induced leakage current was observed over the entire duration of the tests. The devices exhibited low noise characteristics. After 30 Mrad the white serial noise increased by 10% for PMOS and 30% for NMOS.

2. READOUT CHIPS

2.1 Chip overview

The main purpose of the chips discussed here is to implement fully the analogue block and evaluate it with all the realistic difficulties of an electronic system, like power surges, crosstalk and device variations in larger pixel arrays. Therefore the analogue block has all functions implemented, but the readout block has a reduced circuit architecture and has been changed in subsequent versions of the chip. Each pixel cell contains a preamplifier, shaper, comparator, flag register and a shift register directing the readout. The gain of the preamplifier as well as the time constant of the shaper are controlled by feedback resistors. The shaper output is connected to a capacitor, which acts as an analogue store, and to the input of the comparator. A common threshold for all pixels can be set. For pixel to pixel variations a threshold trim mechanism is implemented using a 3-bit SRAM. One trim state is reserved to switch the comparator off. This pixel masking capability allows the removal of noisy pixels. In the data taking mode the same mechanism can be used to inject a calibration test charge into selected pixels. The readout is organized in double columns of pixels. The double column periphery is equipped with control logic that recognizes a hit in a pixel, provides a twelve-bit buffer for time stamping and organizes the data transfer from the pixels to the periphery.

All bias voltages and bias currents have to be set externally. This allows the control of parameter shifts before and after irradiation. In the final pixel chips biasing will be realized by an I2C programmable control register, DACs and current sources.

2.2 Physical Implementation

The architecture and the circuit schematics of both chip implementations are widely identical, but there are also some differences.

- The layout of the Honeywell chip has been changed to benefit from the advantages of the RICMOS IV process: higher transistor density and three metal layers for the interconnections.
- The DMILL chip consists of 660 pixels organized in 22 columns with 30 pixels per column. The RICMOS IV chip contains 704 pixels at 32 pixels a column.
- On a RICMOS IV chip a pixel covers an area of 125μm x 125μm. In the measured version of the DMILL chip (PSI34) the size of the pixels has been changed to 150μm x 150μm to accommodate the optimized size of the detector cell.
- The analogue output stage in this DMILL version

(PSI34) has been improved to provide higher gain. The comparison between the two chip layouts shows that to implement the same functions we consume up to a factor of two less area in RICMOS IV than in DMILL technology [4].

3. EXPERIMENTAL RESULTS

3.1 Test set-up

The chips were mounted and wire-bonded on a fine line PCB. The board was interconnected to a peripheral PCB carrying the additional components necessary for power supply, bias generation, input and output buffers. The analogue and digital outputs were unity gain buffered. The drive system was based on the Tektronix pattern generator DG2020 used to program the trim bits of each pixel cell and to set the calibration mechanism and for generate the repetitive readout sequences. A programmable pulse generator of the HP8110A series served to inject a test charge into the pixel cells. A LeCroy scope displayed and digitized the output data, and finally the programmable Racal-Dana 1992 counter recorded the detected hits. The whole system was controlled by a PC running LabView software.

3.2 Measuring conditions

The chips were characterized electrically using the analogue test input. A variable X-ray source enabled us to calibrate the test capacitance. This amounts to 1.73 fF and 1.68 fF for DMILL and RICMOS IV respectively. The DMILL and RICMOS IV chips were set up with the bias currents and voltages optimized for correct operation in each case. However the total power dissipation for both designs was kept the same and equal to 40 µW per pixel. The measurements were performed before and after irradiation with photons from a Co^{60} source. The following quantities were examined: shaper response, analogue output, noise, timewalk and threshold behaviour.

3.3 Measurements before irradiation

Fig. 1 shows shaper pulses of DMILL and RICMOS IV chips corresponding to an input charge of 10000 e^-.

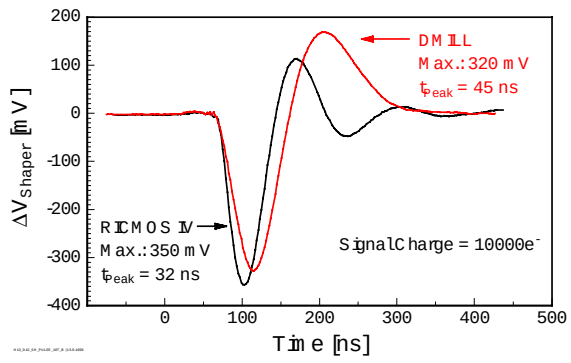

Fig. 1 Signal pulse at the shaper output

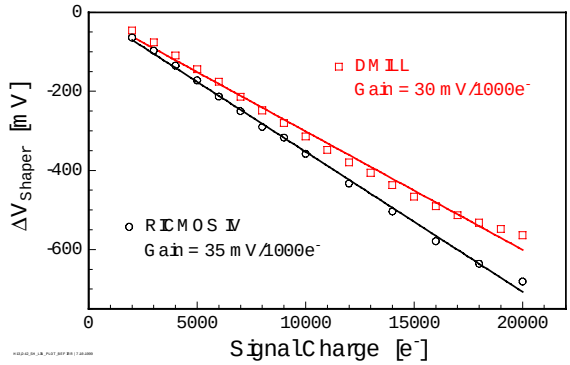

Fig. 2 Linearity measurement of the shaper pulse

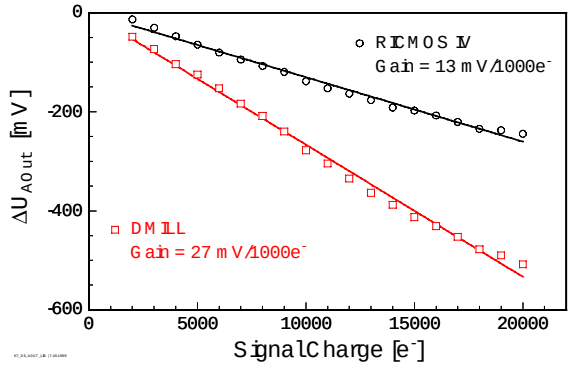

Fig. 3 Linearity measurement of the analogue output

Obviously the RICMOS IV type is faster and produces higher amplitudes. This can be explained by the fact that transistors in RICMOS IV technology have lower drain capacitance. Fig. 2 presents the gain of the preamplifier-shaper chain for both versions. In both cases we observe a good linearity in the range below 15000 e^-. In this region the gain amounts to 30 mV/1000 e^- and 35 mV/1000 e^- for DMILL and RICMOS IV, respectively. Above 15000 e^- the response becomes non-linear. Due to the planned charge sharing between adjacent pixels, we have adjusted the chips to have a large gain for relatively small pulseheights at the expense of some non-linearity for the relatively unlikely large pulses. Fig 3 illustrates the signal at the analogue output of the chip for the two implementations. Both curves show approximately the same characteristics as the corresponding shaper output (Fig. 2), but the gain of the DMILL circuitry is larger. This is due to the improved output stage in the measured version of DMILL chips (PSI34). This improvement is not yet implemented in the RICMOS IV chips.

The noise of the amplifier in each design is determined by a threshold scan as shown in Fig. 4. For this measurement the discriminator threshold is set to a fixed value (2200 e^-). Test charges with increasing amplitudes are then injected into a pixel. The fraction of hits detected by the discriminator is modulated by the noise of the amplifier. The slope of the curve is thus proportional to the noise. The rms width σ of the Gaussian noise distribution is given by the increase of signal charge needed to raise the detection efficiency from 50% to 84%.

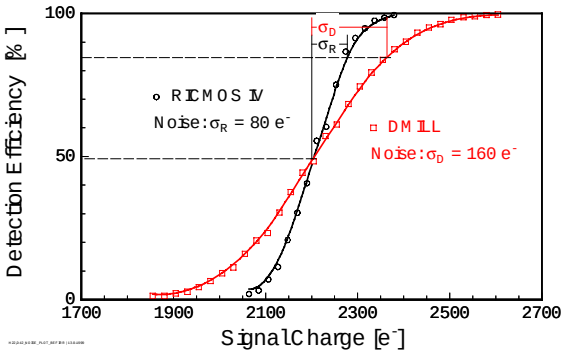

Fig. 4. Threshold scan indicating noise measurement.

Typical values are 160 e^- and 80 e^- for DMILL and RICMOS IV respectively.

Another parameter important to the operation of the pixel arrays at LHC is the timing performance of the complete system. Pixel hits must be correctly associated with the proper LHC bunch crossing. However, precise determination of the hit time is often limited by pulse-height-dependent delay effects (timewalk). This has been studied by measuring the timewalk as a function of the input charge. The threshold used for this study is 2500 electrons. The time is measured relative to the response time for very large signals (30000 e^-). It is clear that for charges close to the threshold, timewalk becomes very significant and the discriminator is not fast enough to meet LHC requirements. For RICMOS IV input charges of more than 420 e^- above threshold are needed to have a delay of less than 25 ns, whereas the DMILL version requires an input charge of more than 1190 e^- over threshold for a delay of less than 25 ns (Fig. 5).

We have measured the variations of the pixel thresholds before and after trimming. For this measurement the chip was run in its regular mode using the time stamp mechanism. The distribution of the thresholds in a complete chip before and after adjustment is shown in Figs. 6 and 7 for DMILL and RICMOS IV, respectively. There is no systematic dependence of the threshold on the position of the pixel within the chip. The plots illustrate that after trimming the width of the threshold distribution has significantly decreased to roughly 120 e^- in both cases. The minimal threshold which could be achieved amounts

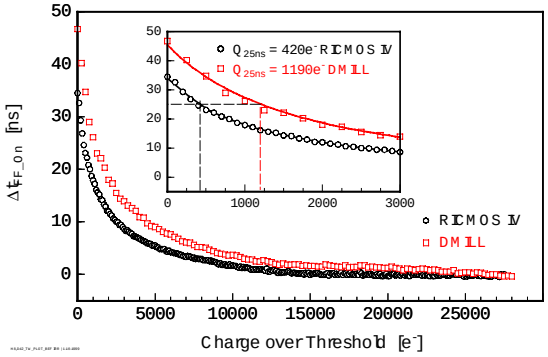

Fig. 5 Timewalk performance for a single pixel in DMILL and RICMOS IV implementation

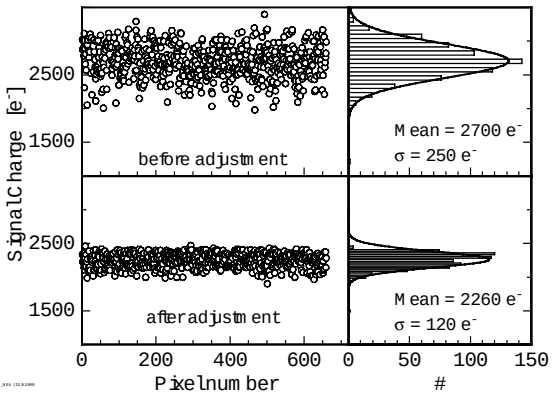

Fig. 6 Distribution of the pixel threshold for all 660 pixels in DMILL version of the readout chip

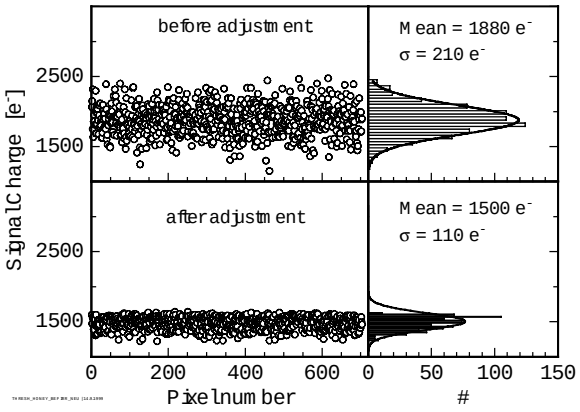

Fig. 7 Distribution of the pixel threshold for all 704 pixels in RICMOS IV version of the readout chip

to 2200 e^- and 1500 e^- for chips realized in DMILL and RICMOS IV technology respectively. This difference can be explained by the fact that the power distribution in the RICMOS IV implementation is better since we use two metal layers for power arrangement. Also the crosstalk between the analogue part and the digital part is reduced (due to the higher transistor density in RICMOS IV technology, the size of these two blocks is smaller and the distance between them can be made larger).

3.4 Measurements after irradiation

To investigate the radiation hardness of the chips a Co^{60} source was used. The chips were irradiated to 10 Mrad and 30 Mrad at a dose rate of 150 rad/s, measured with an accuracy of 10%. The chips were tested directly after irradiation and after annealing for one week at 100°C. In both cases the bias voltages were set to achieve as much as possible the same pulse shape as for the unirradiated case, and the settings for the bias currents were adjusted to give the same supply currents as prior to irradiation.

After the 10 Mrad irradiation chips were operational (except that for the DMILL chip the pixel masking feature was not functional any more). After 30 Mrad the RICMOS IV chip was operational, but the DMILL chip was not (its pixel analogue electronics and the readout part were operational, but its calibration mechanism and

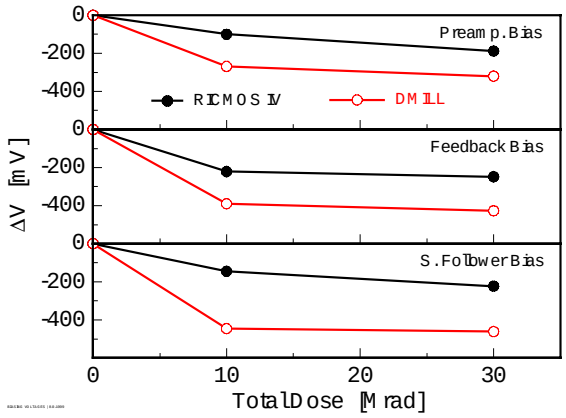

Fig. 8 Change of the bias voltages in DMILL and RICMOS IV chips as a function of irradiation dose

the programming mechanism were out of order). This made testing of the chip impossible. Since only a single chip was irradiated to 30 Mrad, conclusions should be drawn only after more samples have been irradiated and measured.

Fig. 8 illustrates for both the DMILL and RICMOS IV implementations the change of the bias voltages for the preamplifier stage, its feedback transistor and the source follower as a function of the total irradiation dose. It is seen that the shift of the bias voltages in DMILL (approx. 400 mV) is by a factor of two higher than in RICMOS IV (approx. 200 mV).

As shown in Figs. 9a and 9b for both technologies we observe no change of the shaper pulse. The noise measured as described before does not increase significantly (from 160 e^- before irradiation to 170 e^- after 10 Mrad for DMILL and from 80 e^- before irradiation to 90 e^- after 10 Mrad and to 100 e^- after 30 Mrad for RICMOS IV).

Figs. 10a and 10b illustrate the linearity of the analogue output for both versions of the chip before and after irradiation. We observe that the gain of the analogue output of the DMILL chip decreases slightly for large pulses after irradiation to 10 Mrad. The gain characteristic of the analogue output remains stable for the RICMOS IV chips even after irradiation up to 30 Mrad.

(a)

(b)

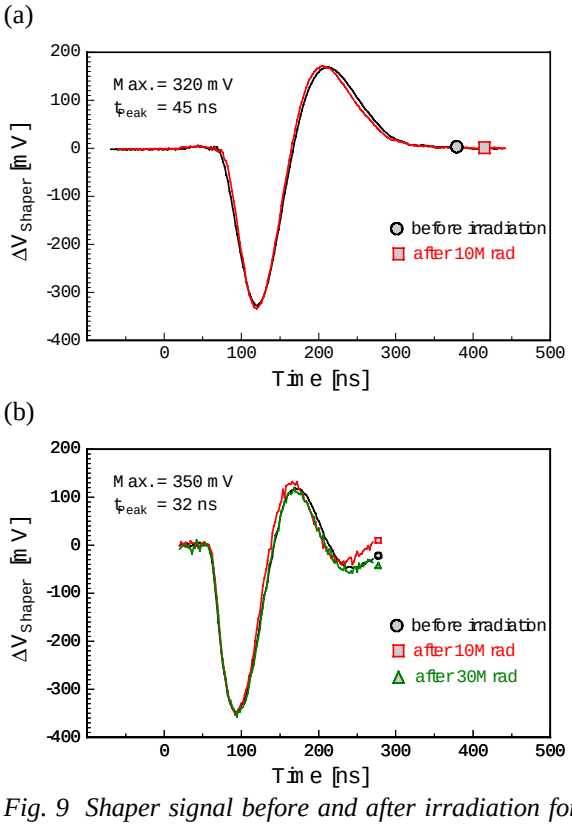

Fig. 9 Shaper signal before and after irradiation for a chip realized in a) DMILL, b) RICMOS IV

(a)

(b)

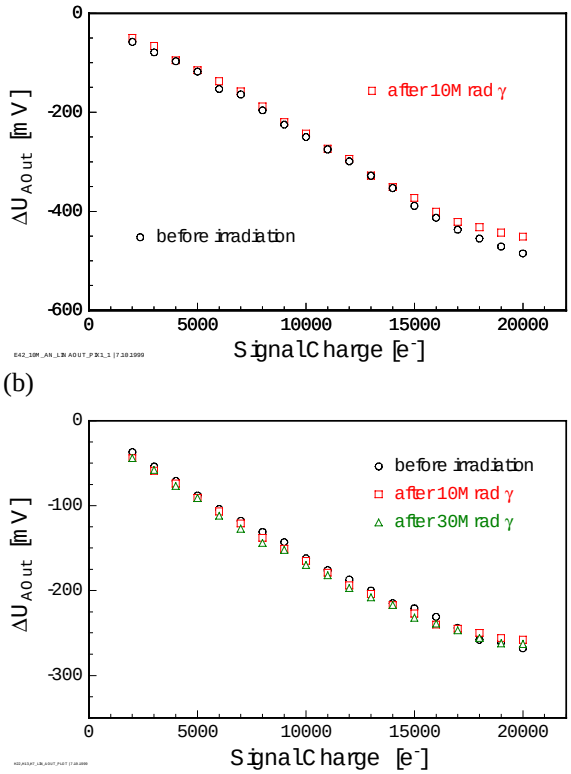

Fig. 10 Performance of the analogue output of a single pixel in a chip realized in a) DMILL technology, b) RICMOS IV technology

In Figs. 11a and 11b we plot the timewalk measurements performed on a single pixel. The Figures display no change of the timewalk for pixels in DMILL technology after 10 Mrad. The same measurements for pixels in the RICMOS IV chip show a that the charge over threshold corresponding to a timewalk of 25 ns has a small increase from 420 e^- before irradiation to 490 e^- after 30 Mrad.

The threshold scan for the complete chip after irradiation and annealing shows that in the DMILL case the average threshold and the threshold dispersion remain the same, but we observe a kind of “edge effect” for RICMOS IV technology. As illustrated in Fig. 12a irradiation alone does not cause a significant change of the threshold behaviour, if one neglects a slight shift of the distribution.

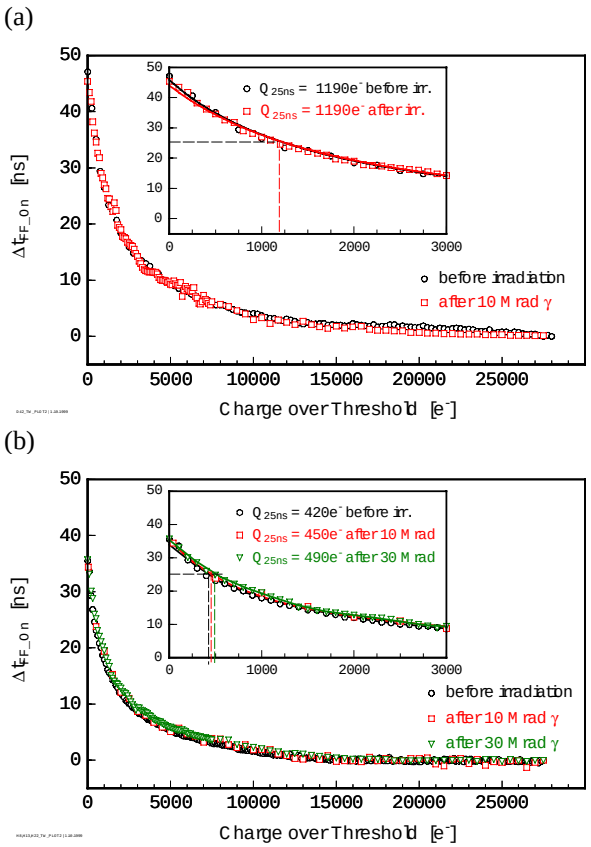

Fig. 11 Timewalk performance for a single pixel before and after irradiation to the specified irradiation doses for the chip in: a) DMILL technology, b) RICMOS IV technology

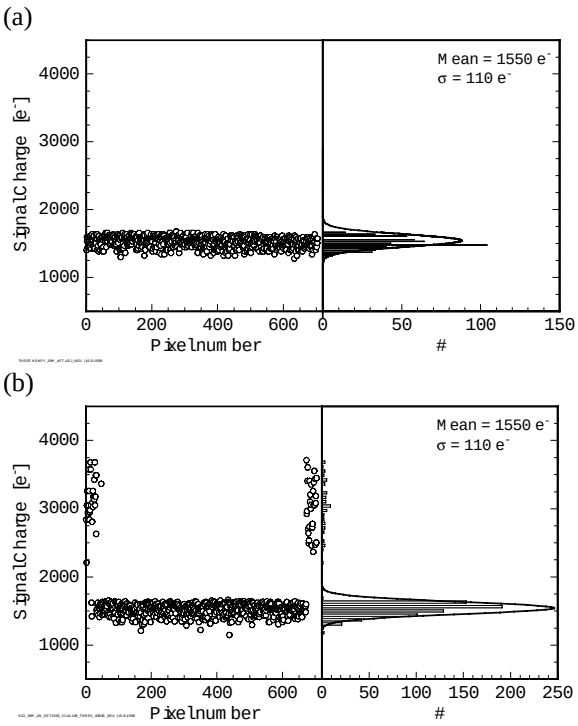

Fig. 12 Pixel threshold distribution for an irradiated chip realized in RICMOS IV a) before and b) after annealing at 100°C for one week.

However, as shown in Fig. 12b, after annealing pixels in the outer columns, #1 and #22 at the border of the chip, show a remarkably higher threshold: The threshold value is nearly twice as large as before. We do not see such problems for any other pixel within the pixel array. Such behaviour has not been observed for annealed chips not exposed to γ irradiation. Thus it seems that the combination of radiation and heat deteriorates the behaviour of those pixels sitting close to the chip border. We have not yet been able to determine the cause of the problem.

4. CONCLUSIONS

The prototype readout chip for the CMS pixel detector has been manufactured first in DMILL technology. This full mixed-mode circuit has then been successfully implemented in Honeywell RICMOS IV technology. The RICMOS IV run achieved a very good yield of 85%. We have made a comparative study of both designs. The measurements show that both prototypes are fully functional before as well as after irradiation to 10 Mrad. The results presented demonstrate that the RICMOS IV implementation has a better performance than the DMILL one in shaper response, noise, timewalk and threshold behaviour before as well as after irradiation. Following irradiation the shift of the bias voltages in the RICMOS IV version is smaller than for DMILL. Apart from "edge effects", which we have observed in the RICMOS IV implementation after irradiation and subsequent annealing, measurements established that the RICMOS IV circuit tolerated a total gamma dose of 30 Mrad, while maintaining full functionality with only minor degradation of parameters. The high transistor density and the availability of four metal layers in the RICMOS IV technology are very advantageous because of better power distribution and lower area consumption. Our experience shows that to implement the same functions one needs an active area smaller by a factor of two in the RICMOS IV technology than in the DMILL case.

5. REFERENCES

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