A pixel readout chip for tracking at ALICE and particle identification at LHCb

K. Wyllie [1], M. Burns[1], M. Campbell[1], E. Cantatore[1], V. Cencelli[2], R. Dinapoli[3], F. Formenti[1], T. Grassi[1], E. Heijne[1], P. Jarron[1], K. Kloukinas[1], P. Lamanna[3], M. Morel[1], V. O'Shea[4], V. Quiquempoix[1], D. San Segundo Bello[5], W. Snoeys[1]

[1] CERN, Geneva, Switzerland
[2] INFN Rome, Italy
[3] University and INFN Bari, Italy
[4] University of Glasgow, Glasgow, UK
[5] NIKHEF, Amsterdam, The Netherlands.

Abstract

The ALICE1 chip is a mixed-mode integrated circuit to read out silicon pixel detectors used for particle tracking in the ALICE Silicon Pixel Detector or particle identification in the LHCb Ring Imaging Cherenkov detector. The chip will be fabricated in a commercial 0.25µm technology and transistors are designed with a radiation-tolerant geometry. It consists of 256 × 32 pixel cells, each of 50µm × 400µm, and can be operated in one of two modes. In tracking mode, all cells are read out. In particle identification mode, 8 cells are grouped together, reducing the effective granularity to 32 × 32 cells of 400µm × 400µm. The cell architecture is described in detail, together with the two operational modes and issues of system integration.

1. INTRODUCTION

Pixel detectors will form an integral part of the detector systems of the Large Hadron Collider (LHC) at CERN. Using a hybrid structure of sensor and readout chip, they offer several advantages over other detector technologies in the severe environment of the LHC. The low noise and low power consumption per channel obtainable with such devices will allow the construction and operation of systems with high channel densities, low mass, and tolerance to radiation. The ALICE experiment [1] will use pixel detectors as part of its Inner Tracking System (ITS) [2]. Here, the pixel system will have to track particles in a high multiplicity environment close to the interaction point. The LHCb experiment [3] is investigating three different technologies for photon detectors in its Ring Imaging Cherenkov detector (RICH), one of which uses pixel sensors and readout chips to detect photoelectrons produced by Cherenkov photons. Although the requirements of the two detectors are quite different, an architecture for a pixel readout chip has been designed which, by means of a selectable mode of operation, can satisfy the needs of both systems. This paper describes the architecture of the chip, known as ALICE1, and its application in ALICE and LHCb.

2. PIXELS FOR TRACKING IN ALICE

2.1 Requirements

The silicon pixel detector in ALICE will form the two layers of the ITS closest to the interaction point. Thus a major requirement is that the mass of the system be minimised to reduce the chance of multiple scattering. Tracking precision is required in the r-ϕ direction with a resolution of 12µm. The nature of the heavy ion collisions will generate events of high multiplicity, and the system must be able to cope with a hit occupancy of 1%.

Any hits detected by the readout chip must be delayed until the arrival of the Level-1 trigger, which has a maximum latency of 10µs and a rate of a few kHz depending on the types of particles being collided in ALICE. The duration of the trigger signal is one clock period of the 10MHz system clock, so the delay of hits must be accurate to 100ns across this 10µs. The readout of the pixel chips is initiated by a Level-2 trigger, which has a maximum latency of 100µs and a rate of a few kHz.

To keep the deadtime under the specified 10%, the readout of an entire event from the pixel detector system must be completed within 400µs. The final requirement is that the system be tolerant to an ionising radiation dose of 500krad, integrated across 10 years of LHC operation.

2.2 Implementation

To minimise the mass of the detector, the silicon sensors will be thinned to 150µm. This implies that the most probable signal produced by a minimum ionising particle will be about 12,000 electrons. Hits detected by the front end will be time-stamped according to the system clock and then precisely delayed by means of digital circuitry. All events accepted by the Level-1 trigger will be buffered inside the chip, which allows a number of chips to be readout sequentially using the 10MHz clock within the required 400µs.

The detector system will be constructed from a number of components. The basic 'building block' is a *ladder*, which consists of 8 readout chips bump-bonded to a single silicon sensor. 4 ladders are aligned in *Z* to form a *stave*, and the entire system consists of 60 staves arranged in two barrels around the interaction point.

A readout unit is formed by a *half-stave* of 16 chips, read out sequentially in 400µs. A half-stave is shown schematically in Figure 1. The 120 half-staves of the system are read out in parallel.

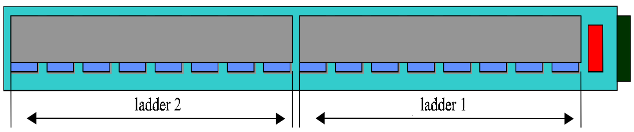

Figure 1: Schematic of an ALICE half-stave, showing the 16 front-end chips and 2 silicon sensors, readout electronics and connector. The length of a half-stave will be about 20cm and the width 17mm.

3. PIXELS FOR PARTICLE ID IN LHCb

The concept of encapsulating a pixel sensor and readout chip within a vacuum tube to form a hybrid photon detector (HPD) has been demonstrated with a number of prototypes [4],[5]. This has led to the development of larger area pixel HPDs in the framework of LHCb [3]. Figure 2 shows schematically the concept of the pixel HPD. Photons incident on an optical input window release a photo-electron from a photo-sensitive cathode layer deposited on the inner surface. These photo-electrons are accelerated within the vacuum by a high potential and electrostatically focussed onto an anode which in this case is the pixel sensor and chip. The data from the chip is transmitted out of the device by means of vacuum-tight feed-throughs.

3.1 Requirements

The demands on such a device are dictated by the sensitivity requirements and the need to maximise the data produced for physics analysis. The HPDs must be sensitive to single photoelectrons. They must also provide a very clean signal, since a high proportion of noise hits will deteriorate the pattern recognition. The requirements on spatial resolution can be met with a 2.5mm × 2.5mm channel size, but this also implies an occupancy of up to 8% in some regions of the RICH detector.

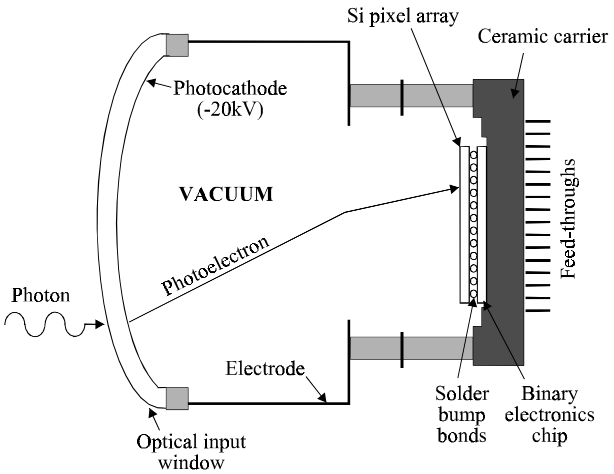

Figure 2: Schematic of a pixel HPD.

The LHCb Level-0 trigger will be applied to the front-end chips, and arrives at an average rate of 1MHz after a latency of 4µs. Since this is a mean rate, triggered events must be de-randomised to ensure a regular transfer of data from the detector. To keep the deadtime to below 1%, a triggered event must be completely read out from a chip in 900ns.

3.2 Implementation

The accelerating voltage applied to the HPDs will be 20kV, which generates a signal of around 5000 electrons in the pixel sensor. The encapsulation of the electronics within the vacuum envelope means that the chip and its packaging must be compatible with the all the steps in the manufacturing process of the HPD. Additionally, since the vacuum will present difficulties to the removal of heat, the chip must consume minimal power.

The electrostatic focussing de-magnifies an image on the input window by a factor of 5, so the 2.5mm × 2.5mm channel size maps to a 500µm × 500µm granularity on the pixel sensor.

Triggered events are de-randomised by buffering on the chip, and a 40MHz clock is then applied for the readout. A complete detector system for the RICH of LHCb would consist of 500 HPDs.

4. THE ALICE1 CHIP

The complementary requirements of these two detectors can be met by the architecture of the ALICE1 chip, described in this and the following sections.

4.1 Chip description

The chip will be fabricated in a commercial 0.25µm CMOS process. This offers two major advantages, namely a high component density and an intrinsic radiation tolerance due to the thin gate oxide of the transistors which will undergo only small changes in threshold voltage after irradiation [6],[7]. The radiation tolerance is further enhanced by the use of enclosed gates for the NMOS transistors to minimise drain-to-source leakage, and guard rings to prevent inter-component leakage and reduce the risk of electrically- or radiation-induced latch-up [8]. A test chip designed in the same technology and with the same transistor layout geometry remained fully functional with up to 30Mrad of X-ray irradiation [9]. All digital storage elements in the chip have been designed to be immune to single-event-upset, a phenomenon which can alter the configuration of a chip during operation. They use a special latch design which recovers its original state following an upset [10].

Both the analog and digital circuitry has been designed to operate with a 1.6V power supply, and the total static power consumption will be 400mW. The chip will contain around 9 million transistors.

Figure 3 shows a schematic floorplan of the chip. The sensitive area measures 12.8mm × 12.8mm, and is divided into 8192 pixel cells of 50µm × 400µm. These pixels are arranged in 256 rows and 32 columns. The remainder of the chip consists of peripheral control logic, biasing circuitry, a JTAG serial interface and the input/output blocks, which will be described in Section 6.

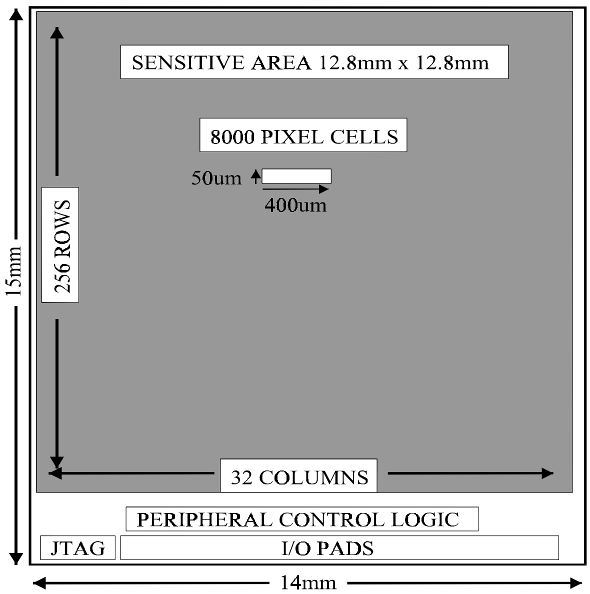

Figure 3: Schematic floorplan of the ALICE1 chip.

4.2 Pixel Cell

The pixel cell is divided into an analog and a digital part, as shown in the schematic of Figure 4.

The analog front-end consists of a pre-amplifier followed by a shaper stage with a peaking time of 25ns. Both of these blocks are differential, with one input carrying the detector signal and the other tied to a clean reference. This has been done to improve the common-mode rejection of the circuitry and to minimise the sensitivity to digital switching noise injected into the front-end through the substrate. A test input can be given to the pre-amplifier using a voltage step applied across a capacitor. The size of the step is controlled on the chip and is triggered by a logic pulse generated externally. This scheme avoids having to send an analog test pulse to the chip, which would be sensitive to any external noise in the system.

A discriminator compares the output of the shaper with a threshold fixed globally across the chip. In addition, each pixel contains three logic bits which can be used to finely adjust the thresholds on a pixel-to-pixel basis. The outputs of the discriminators in the pixel matrix provide a fast-OR signal which is foreseen for diagnostic purposes during testing and for self-triggering. The static consumption of the front-end of each cell is 50µW.

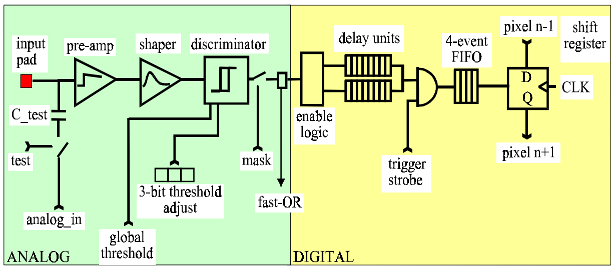

Figure 4: A schematic of the circuitry within one pixel cell

The discriminator output is fed into the digital part of the cell. The first stage consists of two digital delay units, whose purpose is to store a hit for the duration of the trigger latency. Each delay unit consists of an 8-bit latch which, on receipt of a hit from the discriminator, latches the bit-pattern present on an 8-bit bus. This pattern is the Gray-encoded contents of an up-down counter whose state changes synchronously with the clock and has an adjustable modulo *n*. Gray-coding was chosen to minimise the digital switching in each clock cycle, and thus reduce the risk of noise coupling into the analog circuitry. The time structure of the pattern is shown in Figure 5.

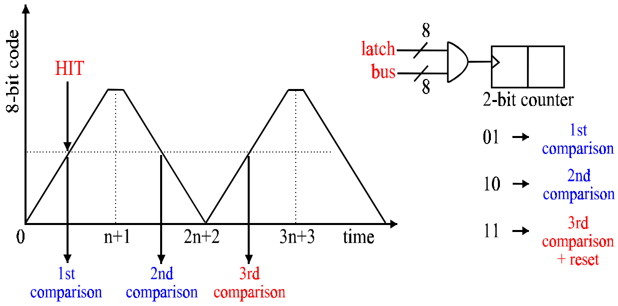

Figure 5: The time structure of the pattern used to timestamp hits in the delay units.

The contents of each latch are compared with the pattern on the bus and, on each positive comparison, a 2-bit counter is incremented. The third positive comparison occurs $2n$+2 clock ticks after the hit, and a logic one is then presented to the coincidence logic. This state also resets the delay unit. In this case, $2n+2$ clock ticks represent the trigger latency and this can be adjusted to meet the requirements of the experiment.

The result of the trigger coincidence is loaded into the next-available cell of a 4-event FIFO, which acts as the multi-event buffer and de-randomiser. This FIFO is read/write addressable by means of two 4-bit busses which again carry Gray-encoded patterns.The contents of the FIFO cells waiting to be read out are loaded into a flip-flop by the Level-2 trigger in ALICE and a NEXT-EVENT-READ signal in LHCb. The flip-flops of each column form a shift register, and the data is shifted out using the system clock.

Finally, there are five latches inside the cell whose contents switch on or off the test input to the front-end, mask or activate a pixel, and provide the three bits of threshold adjustment. These latches have been designed to be resistant to single-event upset.

Much attention has been paid to reducing the risk of noise injection via the substrate. In addition to the Gray-encoding of the busses and the differential front-end, the logic cells used in the pixels are current-starved, to minimise any bounce induced in the power supplies during switching.

5. OPERATIONAL MODES

With the addition of some extra logic, this architecture can be used for both applications. The mode of operation is selected by an external control signal.

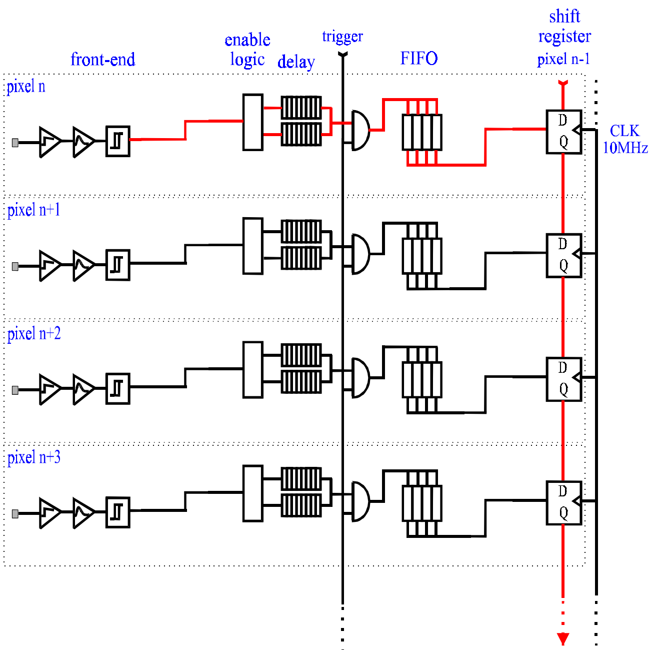

Figure 6: The configuration in ALICE mode.

5.1 ALICE mode

In this mode, each pixel cell acts as an individual channel and the full matrix of 256 × 32 cells is read out.

Using the two delay units, each cell has the capability of simultaneously storing two hits for the trigger latency.

The 32 columns are read out in parallel. Using the 10MHz clock, a complete event is read out from the chip in 25.6µs. Figure 6 shows the configuration of the pixel cells in ALICE mode.

5.2 LHCb mode

In LHCb mode, eight pixels in the vertical direction are configured as a 'super-pixel' of 400µm × 400µm, which is close to the LHCb requirements of 500µm × 500µm. The discriminator outputs of the super-pixel are OR-ed together and the sixteen delay units of these eight cells are configured as an array. Four of the 4-event FIFOs are connected together to form a 16-event FIFO, which can be written to by any of the sixteen delay units. This meets the required de-randomiser depth for LHCb. The FIFO output is loaded into the flip-flop of the top pixel in the group, which bypasses the other seven during readout. This scheme reduces the matrix to 32 × 32 cells and allows a complete event to be read out within 800ns using a 40MHz clock. Figure 7 shows the configuration of the pixel cells in LHCb mode.

The sixteen delay units are necessary for storing the large number of hits which will occur in the high occupancy regions of the RICH. Additionally, the use of the eight separate analog blocks reduces the effective occupancy seen by the front-end. If the occupancy

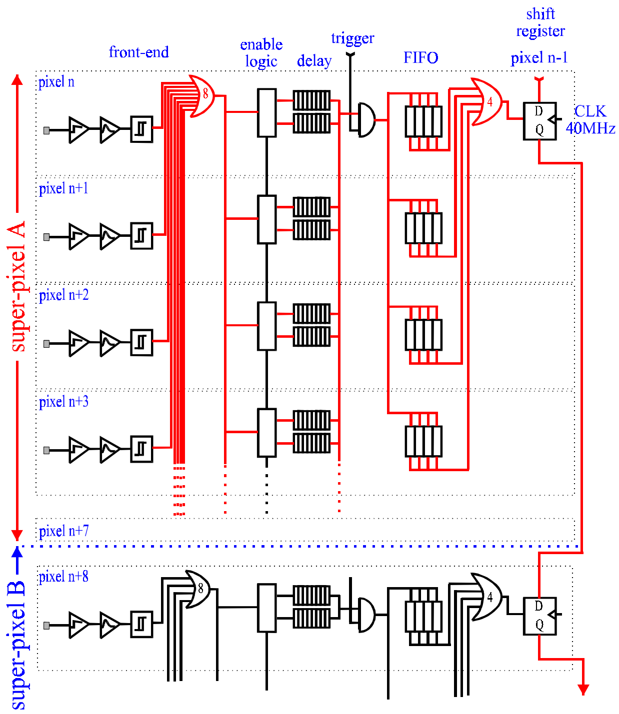

Figure 7: The configuration in LHCb mode.

remained high, then there would be a risk of pulse pile-up and a subsequent loss of hits. Thus, the segmentation of the front-end relaxes the requirements on the return-to-zero time of the pre-amplifier and shaper.

6. PERIPHERY, CONFIGURATION AND I/O INTERFACE

The peripheral logic of the chip contains the counters to address the delay units and the FIFOs. Additionally, there are a number of 8-bit digital-to-analog convertors to provide voltage and current references for the analog front-ends and the current-starved logic. Any memory on the periphery is again constructed from un-upsettable cells. At the top of the chip will be a number of test cells connected to analog output buffers which will allow the observation of the pre-amplifier and shaper outputs during chip testing.

The configuration of both the peripheral logic and the matrix of pixel cells is done by means of a serial interface following the IEEE JTAG standard [11]. This has a number of advantages. It allows both the write and read of the configuration settings in the chip, including the test, mask and threshold-adjust states of each pixel. It also allows the reading back of the analog levels generated by the digital-to-analog convertors via an additional output line. Connectivity tests of chips mounted on a stave can be done using the boundary-scan feature of JTAG. Additionally, the JTAG test feature has been adapted to detect bad chips in the serial chain and indicate their location.

The width of the ALICE stave restricts the number of lines available for signalling, and for this reason a single-ended standard has been adopted. Gunning Transceiver Logic (GTL) [12] will be used for all the digital signals to and from the chip. This has the advantage of a low signal swing (~800mV) which again reduces the risk of noise injection. Additionally, the output buffers on the chip have an adjustable slew-rate control which can be controlled to match the system requirements. These buffers are powered with a supply separate from that of the rest of the chip. Finally, multiple bonding pads have been provided for the supply lines to minimise the inductance of the connection and limit the supply bounce during switching.

7. CONCLUSIONS

The ALICE1 chip has been designed with an architecture which provides the functionality required by both the ALICE tracker and the LHCb RICH. The choice of a deep sub-micron technology has allowed the inclusion of a large amount of functionality within each pixel to meet the demands of both experiments.

Careful consideration has been given to a number of factors. Firstly, the risk of switching noise has been minimised by design features. Furthermore, the power consumed by the front-end has been kept to a minimum. Questions of testability have been addressed, and the chip contains features which are foreseen to ease its integration into a system. Finally, the circuitry has been designed to be tolerant to radiation, both total dose and single event effects.

The final stages of the chip layout are underway. Chip testing is planned to begin in 2000 and will be followed by first system tests.

8. ACKNOWLEDGMENTS

We would like to thank our colleagues from the ALICE ITS and LHCb RICH for their comments and help in the preparation of this paper.

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