Analog Readout for the ATLAS Semiconductor Tracker

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DISSERTATION

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Abstract

The context of the work, described in this document, is the development of electronic components for future high-energy physics experiments.

The first part deals with design and evaluation of an electronic device for reading and processing the signals, created by charged elementary particles in solid state detectors. This device has to work within an experimental environment, which imposes very rigorous requirements in terms of signal processing speed, noise performance, power dissipation, radiation hardness and size as well as in terms of system complexity. These constraints force its realization as a VLSI integrated circuit. An emphasis is put on the major problem, which occurs when dealing with extremely small signals, as the ones produced by a semiconductor detector. This problem concerns the low-noise operation of the front-end amplifiers.

The second part contends with the transmission of the data from this read-out devices to the first data buffer, which is located outside the detector about 50 to 100 m apart. It describes a device, which main task is the synchronization of these data to an external timing reference. Again, system and performance conditions urge the implementation as an integrated circuit.

- Chapter 1 gives a brief introduction to the context and the motivation for building this new high-energy physics experiments and describes the boundary conditions and the environment, the devices will have to work in.

- Chapter 2 reviews the fundamentals of semiconductors, relevant for its use as radiation detectors, and looks into the generation of signal charge, created by a traversing particle and the properties of the signal as seen by the readout amplifier. The chapter concludes with the characteristics of silicon strip detectors, significant for the design of the front-end electronics.

- Chapter 3 describes the requirements for an electronic device to deal with the signal delivered by a Silicon strip detector in terms of electrical properties of the signal itself and of the detector. In this context, we emphasize on the crucial problem of the noise performance of an amplifier to be used with semiconductor detectors.

A derivation of a complete expression for the electronic noise of a charge-sensitive amplifier including noise filtering, starting from the basic noise mechanisms, is presented. In order to improve the accuracy of this model, the theory of noise correlation in bipolar junction transistors, first predicted by A. Van der Ziel in 1955 [57], is adapted. Comparisons with experimental results confirm the quality of the derived model.

- Chapter 4 deals with the requirements and the specifications for the on-detector electronics in terms of environmental and system conditions concerning the use of the device within a large experiment like ATLAS/LHC. Subsequently, a 128-channel analog readout ASIC for semiconductor detectors (SCT128A) is presented and architecture and functionality described in detail.

  Results of functionality tests and performance measurements, carried out on the chip in a laboratory environment as well as using CERNs particle beam facilities, demonstrate that the SCT128A meets all specifications to be a feasible candidate for analog readout in LHC experiments. An absolute calibration of the front-end amplifier with monochromatic photons allows an accurate determination of the signal charge, released by a minimum ionizing particle (MIP) in the silicon strip detectors foreseen to be used within the ATLAS Inner Tracker.

- Chapter 5 describes the conception, establishing of the specifications, and implementation of a mixed-signal data receiver/synchronizer ASIC. The main task of the device is the synchronization of the data stream, sent by the readout chips, to an external time reference and the controlling of the A/D conversion of the analog data in the stream.

  The functionality requires an accurate Phase-to-Digital conversion with a resolution of 1 nano second. The demands on the nonlinearity of the converter and the jitter of the output signal (in the range of tens of pico seconds) are accordingly strict. In order to achieve the required performance independently of process variations, operating temperature and load capacitance, an auto-calibration circuit was implemented in the chip. The entire design flow from the concept to the final product is documented. Results of functionality tests and performance measurements on the prototype verify the design.

Kurzfassung

Den Rahmen der vorliegenden Arbeit stellt die Entwicklung elektronischer Komponenten für zukünftige Hochenergiephysik-Experimente dar.

Der erste Teil beschäftigt sich mit dem Entwurf und der Realisierung einer elektronischen Einheit zur Detektion, Verarbeitung und Zwischenspeicherung von Signalen, die durch geladene Elementarteilchen in Halbleiterdetektoren hervorgerufen werden. Einsatzgebiet und Arbeitsumgebung stellen sehr rigorose Anforderungen an die Schaltung in Bezug auf Schnelligkeit, Rauschverhalten, Leistungsverbrauch, Strahlungshärte und Größe sowie bezüglich der Systemkomplexität. Diese Rahmenbedingungen erzwingen eine Realisierung als integrierte Schaltung.

Eines der Hauptprobleme, das in diesem Zusammenhang auftritt, betrifft die extrem kleinen Signale, die ein Elementarteilchen in einem Halbleiterdetektor produziert. Ein Schwerpunkt in der Entwicklung liegt daher auf der Optimierung der Schaltung in Bezug auf ihr Rauschverhalten.

Der zweite Teil der Arbeit behandelt Probleme mit der Übertragung der Daten von diesen Zwischenspeichern zum ersten Datenbuffer außerhalb des eigentlichen Experimentes. Es beschreibt eine Einheit, deren Hauptaufgabe die Synchronisierung dieser Daten zu einer externen Taktreferenz darstellt. Wiederum drängen Leistungs- und Systemanforderungen auf die Implementierung als integrierte Schaltung.

- Kapitel 1 gibt eine kurzen, einleitenden Überblick und behandelt die Beweggründe für den Aufbau neuer Hochenergiephysik-Experimente. Weiters werden die Eigenheiten und Rahmenbedingungen der Arbeitsumgebung beschrieben, die für die Entwicklung der elektronischen Komponenten maßgeblich sind.

- Kapitel 2 wiederholt die Grundlagen der Halbleiter, relevant für ihren Einsatz als Teilchendetektoren. Behandelt wird die Erzeugung der Signalladung, ausgelöst von einem, den Detektor durchquerenden Teilchen, und die Eigenschaften dieses Signals aus der Sicht des Ausleseverstärkers. Das Kapitel schließt mit den für die Entwicklung der Auslese-Elektronik bedeutenden Eigenschaften der Silizium-Streifendetektoren.

- Kapitel 3 beschreibt die Anforderungen an die Auslese-Elektronik, betreffend die elektrischen Eigenschaften des Signals und des Detektors. In diesem Zusammenhang wird auf das wichtige Problem des Rauschverhaltens eines Verstärkers für die Auslese von Halbleiterdetektoren detailiert eingegangen.

  Die Ableitung eines kompletten Ausdruckes für das elektrische Rauschen eines ladungsempfindlichen Verstärkers mit Bandpaß-Filter wird dargestellt. Um die Genauigkeit dieses Modells zu verbessern, wird die Theorie der Rauschkorrelation in bipolaren Sperrschicht-Transistoren, bereits im Jahre 1955 vorausgesagt von A. Van der Ziel [52], benutzt. Vergleiche mit experimentellen Resultaten bestätigen die Qualität des berechneten Modells.

- Kapitel 4 beschäftigt sich mit Anforderungen und Spezifikationen für die Auslese Elektronik in Hinblick auf ihren Einsatz innerhalb eines großen Experimentes wie ATLAS/LHC. Anschließend wird ein 128-Kanal Analog-IC für die Auslese von Halbleiterdetektoren vorgestellt und Architektur und Funktionalität im Detail beschrieben. Das Kapitel schließt mit Resultaten von Funktionalitätstests und Messungen, die an dem fertigen Chip durchgeführt wurden,.

  Eine absolute Kalibrierung des Verstärkers mit monochromatischen Photonen erlaubt eine genaue Ermittlung der Signalladung, die von einem minimal ionisierenden Teilchen (MIP) in den, für den Einsatz im ATLAS Spurendetektor vorgesehenen Silizium-Streifendetektoren freigesetzt wird.

- Kapitel 5 beschreibt Konzept, Spezifizierung und Implementierung eines Empfängers und Takt-Synchronisierers für gemischt analog-digitale Datenpakete. Die Hauptaufgabe der Einheit ist die Synchronisierung des Datenstromes, kommend von den Auslesesystemen, auf eine externe Zeitreferenz, und die Steuerung der Digital-Wandlung der analogen Daten.

  Für die angestrebte Funktionalität wird eine hoch-genaue Phasen-Digital-Wandlung mit einer Auflösung von 1 Nanosekunde benötigt. Die Anforderungen an die Nichtlinearität des Wandlers und den Zeit-Jitter der Ausgangssignale (in der Größenordnung von einigen 10 Picosekunden) sind entsprechend hoch. Um die angestrebten Leistungsdaten unabhängig von Prozeßparametervariationen, Umgebungstemperatur und Lastkapazität sicherzustellen, wurde eine Selbstkalibrierung in den Chip integriert. Der gesamte Designfluß vom Konzept zum fertigen Prototyp ist dokumentiert. Resultate der Messungen und Tests an dem Prototyp demonstrieren die korrekte Funktion und die Einhaltung der angestrebten Spezifikationen.

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Chapter 1

Introduction

The origin of mass is one of the most fundamental topics in modern physics. In the Standard Model (SM), which is the theoretical foundation of high energy physics (HEP), elementary particles acquire their mass through spontaneous symmetry breaking. This process is known as the Higgs-mechanism and gives rise to the existence of a new massive particle, the Higgs boson, which has not yet been observed experimentally. Although the SM does not predict the mass of the Higgs boson, theoretical arguments indicate that either one or more Higgs bosons with a mass below about 1TeV should exist, or that a more complex scenario of new physics will be found at the TeV energy scale.

In current HEP experiments, sub atomic particles are accelerated to energies of hundreds of billions of electronvolts (>100 GeV), corresponding to velocities very close to the speed of light, and than brought to collision either with each other or with fixed targets. When such a collision takes place, a part of the particle's kinetic energy may convert into mass according to the Einstein relation, creating numerous particles of mostly very short lifetime. CERN, the European Center for Nuclear Research, houses the world's largest particle accelerator complex. LEP, the biggest machine at CERN at present, is a 27 km circular electron-positron collider that reaches a center-of-mass collision energy of 200 GeV. This value constitutes probably an upper limit for circular electron storage rings of that size due to synchrotron radiation energy loss from the circulating beams. Since the radiation losses decrease with the fourth power of the mass of the particles[1], one possible solution to overcome this limitation and push the collision energy into the TeV range, is to accelerate particles with higher rest mass, like hadrons. A proton - proton collider offers a feasible possibility of exploring this energy range in the nearer future.

In order to gain new experimental insight and to test and enlarge our understanding of elementary particle physics at the TeV scale, CERN approved in 1994 the proposed Large Hadron Collider (LHC). Scheduled to be operational by the year 2005, this new machine is a proton - proton collider with a projected center - of - mass collision energy of 14 TeV. The collisions between the bunches of

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[1] Emitted SR power P per turn for a given radius R: $P = (4\pi E_0 r_e I/3eR)(E/E_0)^4$, with energy of the particle E, rest energy E_0, electron radius r_e, electron current I.

protons will recreate the state of the very early universe just 10^{-12} seconds after the "Big Bang", the beginning of space and time, when the temperature was 10^{16} degrees.

The energy available for acceleration of the particles is mainly limited by the strength of the bending magnets. With the radius being fixed by the LEP tunnel, LHC needs a bending field of 8.36T, delivered by 1232 superconducting dipole magnets operating at 1.9 K. In addition to p-p operation, the LHC will be able to collide heavy nuclei (Pb-Pb) produced in the existing CERN accelerator complex, resulting in an energy of 1150 TeV in the center of mass.

The accelerating RF system consists of eight single-cell cavities per beam. Each cavity is driven by a separate 400 MHz klystron rated at 300 kW. The maximum operating voltage is 2 MV per cavity, thus leading to an overall RF voltage of 16 MV during the ramping up phase. The energy gain equals to 485 keV per turn, the stored beam energy will be 334 MJ. The wavelength corresponding to a RF frequency of 400 MHz is 0.75 m or 2.5 ns. Every tenth RF bucket will be filled obtaining bunches separated by 25 ns. This value of the bunch separation is well suited for the experiments and at the same time gives the optimum overall performance of the machine for two high-luminosity experiments taking data at the same time.

Four different experiments are currently planned for LHC. Two of them, ATLAS and CMS, are general purpose proton-proton experiments and are designed to exploit the full LHC physics potential. The other two experiments, LHC-B and ALICE, are dedicated to B-physics and to heavy ion (Pb-Pb) physics, respectively.

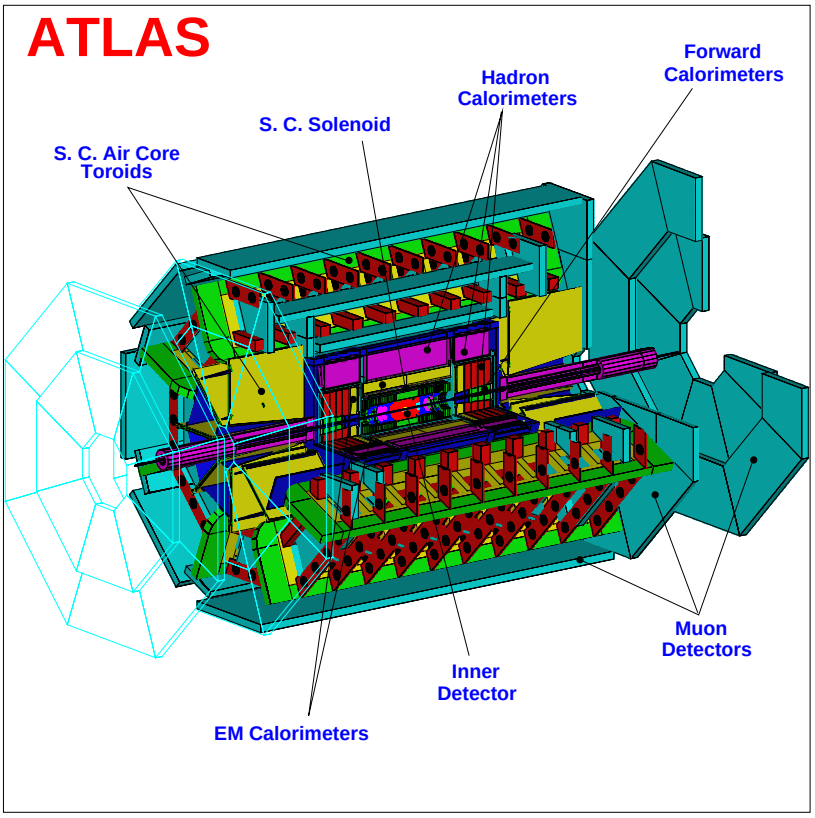

Figure 1. Cut view of the ATLAS detector

ATLAS, A Toroidal LHC ApparatuS, is one of the two general-purpose proton-proton collider experiments foreseen for LHC. A design description is presented in the ATLAS Technical Proposal [1]. The detector geometry follows the common tracker-calorimeter-muon chamber configuration. A three-dimensional view of the ATLAS detector installed in the underground hall is shown in Figure 1. With an overall length of 42 m (including the third layer of the forward muon chambers mounted on the cavern wall), a diameter of 22 m and a weight of 7000 tons, the ATLAS detector is enormous even if compared to the largest of today's high energy physics collider experiments.

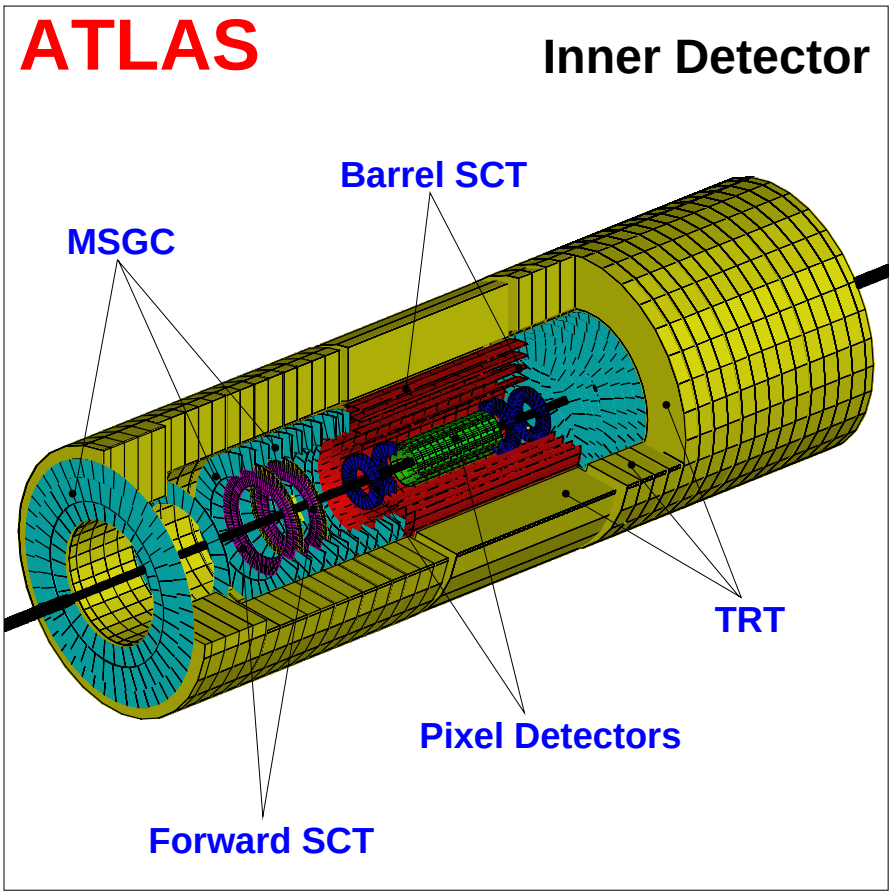

Figure 2. ATLAS inner detector

The purpose of the Inner Detector is to track the particle from the collision point to the electromagnetic calorimeter. Pattern recognition, momentum and vertex measurements, and enhanced electron identification are achieved with a combination of discrete high-resolution pixel and strip detectors (Semiconductor Tracker, SCT) in the inner part and continuous straw-tube tracking detectors with transition radiation capability (Transition Radiation Tracker, TRT) in the outer part of the tracking volume. The Inner Detector is housed in a 6.8 m long cavity of radius 1.15 m within the barrel cryostat of the electromagnetic calorimeter, which contains also the superconducting solenoid providing the axial 2 T field for the tracking. The large track density expected at LHC and the momentum and spatial resolution targets require the use of precision tracking layers with a fine

granularity. However, the number of such layers is constrained by the tolerable amount of material, and their granularity is limited by the power consumption and by the high cost of the readout electronics.

Depending on the required radiation hardness, which is determined primarily by the distance from the beam pipe, different detector technologies are used, namely silicon pixel detectors at the lowest radii and in the forward direction, where highest radiation hardness is required, and silicon strip detectors above a radius of 30 cm. The barrel SCT consists of two silicon pixel detector layers at radii of 11.5 cm and 16.5 cm, complemented by eight pixel disks for the forward direction and of four silicon strip detector layers at radii of about 30 cm, 40 cm, 50 cm, and 60 cm. Since material in the inner detector degrades the momentum, the amount of material is another important performance criteria.

The LHC bunch crossing frequency of 40 MHz, combined with the large number of 10^8 electronics channels in the ATLAS detector, results in a very large data rate: All subdetectors together produce data at a rate of ~ 50 – 100 TB/s, which are written into the detector's front-end pipeline memories. This data rate must be reduced to about 10 MB/s to 100 MB/s before being recorded for the subsequent offline analysis. This challenging task will be taken on by the three-level trigger architecture. The level-1 (L1) trigger accepts data from the calorimeter and the muon trigger chambers at the full LHC bunch-crossing rate (BCO) of 40 MHz. During the L1 latency (i.e. the time required to collect and process the data, and to distribute the trigger decision) of 2.5 μs, the data from all sub-detectors are stored in the pipeline memories. Upon reception of a positive L1 trigger decision, which occurs at a maximum rate of 100 kHz, the full event data are transferred from the pipeline memories to the L2 buffers, which corresponds to a data rate of about 130 GB/s.

The work described in this document deals with the design and evaluation of an electronic device for reading, processing and storing the signals, provoked by the traversing particles in the strip detectors of the SCT. This device has to work within the above described environment, which imposes very rigorous requirements in terms of data processing speed, noise performance, power dissipation, radiation hardness and size as well as in terms of system complexity (Chapter 4). An emphasis is put on the major problem, which occurs when dealing with extremely small signals, like the ones produced by a semiconductor detector (Chapter 2). This problem concerns the low-noise operation of the front-end amplification (Chapter 3). The last section deals with the transmission of the data from this read-out devices to the first data buffer outside the detector. It describes a device that takes care of the synchronization of these data to an external timing reference (Chapter 5). Test and measurement results are presented in order to demonstrate the functionality and performance of both devices.

Chapter 2

Signals From Semiconductor Particle Detectors

The nature and properties of semiconducting materials, as silicon, germanium, gallium-arsenide or diamond, allow them to being used as active components in particle detectors.

As described in the previous chapter, the ATLAS Semiconductor Tracker SCT will use silicon strip and pixel detectors in the barrels as well as in the forward regions. This section discusses the generation of signal charge by a traversing particle and the properties of the signal as seen by the readout amplifier. The characteristics of silicon strip detectors, significant for the design of the front-end electronics, will be reviewed

Signal Generation In Semiconductors

As an energetic particle traverses through a semiconductor, it continuously looses fractions of its kinetic energy via several kinds of interactions. The predominant type is the electromagnetic interaction with the electrons of the lattice atoms. As a result, electrons are excited and raised from the valence band to the conduction band, ionizing the lattice atoms and creating excess charge concentration. These additional charge carriers can be detected under certain circumstances.

The mean energy loss *dE* of a moderately relativistic particle over a path length *dx* can be calculated according to the Bethe-Bloch formula

$$-\frac{dE}{dx} = k \cdot z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2 \cdot m_e \cdot v^2 \cdot \gamma^2}{I^2}\varepsilon_{\max}\right) - \beta^2 - \frac{\delta}{2}\right] \qquad (2.1)$$

using the following symbols:

β relative speed

v velocity of the incident particle

c light speed in vacuum

$\gamma = \sqrt{\frac{1}{1-\beta^2}}$

k	parameter, proportional to the properties of the target material
m_e	electron rest mass
ε_{max}	maximum transferable energy, proportional to the mass of the incident particle
I	excitation potential per atomic electron
Z	atomic number of target material
A	atomic mass of target material
z	charge of incident particle
δ	density effect correction

The parameter k calculates to $4\pi \cdot N_A r_e^2 m_e c^2 = 0.307 MeV g^{-1} cm^2$ with r_e being the classical electron radius[1], the maximum transferable energy is determined using the relation

$$\varepsilon_{\max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e / M + (m_e / M)^2} \qquad (2.2)$$

with M being the mass of the incident particle. The relative speed is the velocity of the incident particle divided by the speed of light in vacuum ($\beta = v/c$). The parameter δ corrects for the density effect: The electric field of the incoming particle modifies the field present in the semiconductor. This results in a weakening of the oncoming interactions, hence reducing the transferred energy. The density effect becomes especially important for ultra relativistic particles. A general expression for δ as a function of the particle momentum has been given in [54].

[1] $r_e = (2.817940 \cdot 10^{-10}$ m).

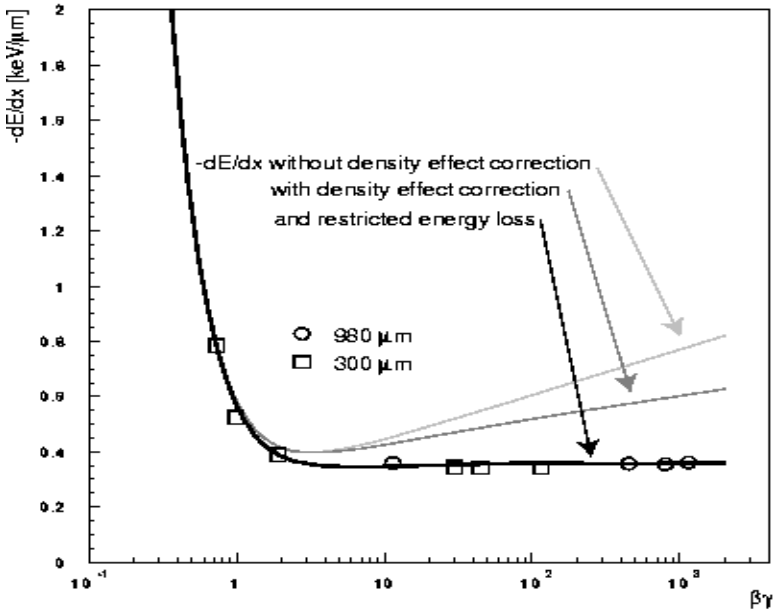

Figure 3. Mean energy deposition in silicon as a function of particle energy. The density effect correction and the restriction of the energy loss to 0.5 MeV become important at high energies. The circular data were taken with a 980 μm thick detector and are reported in [31], the rectangular are calculated from measurements of the most probable energy with a 300 μm thick detector[9].

dE/dx initially falls with $1/\beta^2$, then reaches a broad minimum at $\gamma = 3.2$ almost independently of the material. Particles with energy losses close to this minimum are called minimum ionizing particles (MIPs). The number of created, electron-hole pairs equals to the deposited energy divided by the ionizing energy of the material. This charge concentration in excess of the equilibrium ($n \cdot p > n_i^2$) represents the detectable signal. It returns to thermal equilibrium through recombination of the charge carrier pairs with a time constant equal to the minority carrier lifetime.

The mean energy deposition according to (2.1) is equivalent to the most probable energy deposition for relatively thick layers of absorber material where the number of collisions is large. Here the energy loss is *Gaussian* distributed. This follows directly from the *Central Limit Theorem* for a large number of statistically distributed events. In the case of thin[2] layers, the probability of interactions with high energy-transfer is highly reduced. Consequently, the most probable energy deposition is smaller than the mean deposition and the distribution function shows a long tail towards higher energies due to these rare events. *Landau* [36] established a theory for the energy deposition in thin layers, hence the energy loss of this type is designated as being *Landau*-distributed. All semiconductor detectors relevant for this work can be classified 'thin'.

[2] A layer of a thickness for which the mean energy loss is small (less than 1%) compared to the maximum energy loss allowable in a single collision are considered as 'thin' in this context [36].

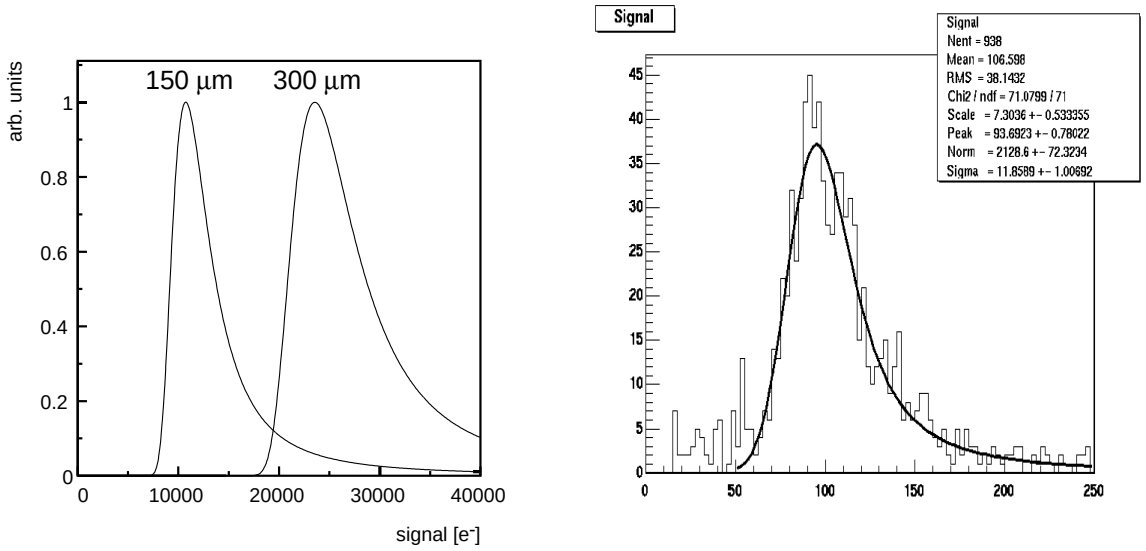

Figure 4. Landau distribution, approximated with equation (2.7) for a 300 µm and a 150 µm thick silicon detector, and measured for a 300 µm silicon strip detector and ^{109}Ru beta particles. A convolution of a Landau and a Gauss distribution is used as the fit function rather than a pure Landau due to the imperfections of the measurement process like for example the electronics noise of the readout amplifier. The vertical scale is the number of events for the given energy, the horizontal scale is in mV for an amplifier of a gain of about 25mV/fC.

The number of created charge carrier pairs can be calculated in a straightforward way from the deposited energy as the predominant interaction is the ionization of the atom resulting in the creation of an electron-hole pair. The *Landau*-distribution can be approximated by the following normalized distribution of the number of created carrier pairs:

$$\phi(\lambda) = \frac{1}{2\pi i}\int_{-i\infty}^{i\infty} \exp(\lambda s + s\cdot \ln s) ds \qquad (2.3)$$

The parameter λ takes the most probable charge generation q_{mp} and the *FWHM*[3] of the experimentally measured distribution into account and has the following relation with the generated charge q:

$$\lambda = \frac{q - q_{mp}}{FWHM} \qquad (2.4)$$

Figure 4 shows the *Landau* distribution derived according to the equations above using experimental data from [30] for q_{mp} and *FWHM* for 150 µm and 300 µm thick silicon.

[3] Full-Width-Half-Maximum (FWHM) denotes the full width of the distribution function at 50% of the peak value.

Charge Collection

In order to use semiconductor material as particle detectors, the excess charge created by the traversing particle has to be collected and measured. This charge collection can be done by applying an electrical field via electrodes across the bulk of the semiconductor. The electron-hole pairs will separate and start drifting towards their respective electrodes, thereby exciting mirror charges at the electrodes, which can be detected and measured. Applying an appropriate field across the semiconductor does not raise a problem in case of high-band gap material like diamond or for usual semiconductors (Si, GaAs) at cryogenic temperatures where practically no free charge carriers are available. Operating semiconductors like silicon at room temperature in this configuration requires the removal of nearly all free charge carriers from the bulk by other means in order to prevent the flow of a substantial DC current. The necessity for this precaution can be illustrated by the following consideration: A 1 cm^2 large and 300 μm thick silicon detector made of pure intrinsic silicon contains in total about $4.4 \cdot 10^8$ free electron-hole pairs. This number is further increased by the unavoidable presence of impurities in the crystal lattice. A traversing MIP looses an average of 116 keV of its energy in such a detector. Together with an ionization energy of 3.62 eV per carrier pair in silicon, this results in a total detectable signal of 32000 electron-hole pairs. The most probable energy loss corresponds to ~24000 electron hole pairs. This, in comparison with the total amount of free charge carriers, very small signal would sink into insignificance besides the fluctuation of the current through the detector. One possible and feasible method of removing the free charge carriers from the silicon bulk is, to use doped silicon in a reverse biased pn-junction-diode configuration. The junction of a reverse biased diode allows applying an electric field for the charge collection and creates a blocking barrier against the flow of majority carriers. Carrier diffusion establishes a region around the junction, which becomes depleted of free charge carriers. The depth of this so-called space charge region increases with the reverse bias voltage. For detector applications, it is desirable to extend the depletion region over the entire device depth, thus increasing the sensitive volume for radiation detection. Moreover, the higher electrical field across the bulk also provides a more efficient charge collection due to increase of the drift velocity. The maximum voltage, which can be applied, is given by the breakdown point of the junction.

Leakage Current And Detector Capacitance

The DC current flowing through a reversed biased pn-junction, called diode leakage current, is a sum of several effects, among which the most important are thermal generation of minority carriers in the depletion region, diffusion of minority carriers from the neutral region and surface effects. For planar silicon pn-junctions, the surface leakage current is generally much smaller than the generation current in the depletion region. A simplified expression for the generation current density can be obtained [55]

$$J_{gen} = \frac{qn_i W}{\tau_e} \qquad (2.5)$$

where W is the depletion-layer width and τ_e the effective carrier lifetime. At a given temperature, the current density is proportional to the depletion-layer width, which is itself dependent on the applied reverse bias. The diffusion current for a fully depleted silicon detector is negligible. The leakage current through a semiconductor detector constitutes a significant source of noise for the readout electronics. Therefore, the mastering of the leakage current is one of the major issues in detector design.

Another source of noise is the effect of the capacitance of the detector seen by the input amplifier of the readout electronics. The equation for the capacitance of a reverse biased planar pn-junction is equivalent to the equation for the capacitance of a parallel plate capacitor, where the distance is replaced by the depth of the depletion layer [36]:

$$C_{\text{det}} = \varepsilon\varepsilon_0 \frac{A}{d} \qquad (2.6)$$

This expression, however, is only accurate for capacitors where the depletion depth is much smaller then the lateral extension of the implant. For highly segmented detectors like that will be described in the following section, also the capacitance between two adjacent implants has to be taken into account. Depending on the layout the contribution of this capacitance can even become dominant.

The Signal Current At The Electrodes

The drifting charge carriers in the detector bulk induce image charges at the electrodes [25]. The resulting signal current is a function of the motion of the charge carriers from their point of generation to the respective electrode. The resulting current is the sum of two components, originating from the motion of the two charge carrier types, electrons and holes, respectively. For a planar junction and assuming constant carrier mobility and constant charge generation per unit length, the total current can be denoted as [53]:

$$\begin{aligned} i(t) = Q_{gen} \cdot \frac{v_n}{2}\left[\left(1+\frac{V_{od}}{E_{\max}\cdot d}\right)\cdot \exp\left(\frac{-v_n t}{d}\right) - \frac{{V_{od}}^2}{{E^2}_{\max}\cdot d^2}\cdot \exp\left(\frac{v_n t}{d}\right)\right]\cdot \sigma\left(t_{n\max}\right) + \\ + Q_{gen} \cdot \frac{v_p}{2}\left[\left(1+\frac{V_{od}}{E_{\max}\cdot d}\right)\cdot \exp\left(\frac{-v_p t}{d}\right) - \frac{{V_{od}}^2}{{E^2}_{\max}\cdot d^2}\cdot \exp\left(\frac{v_p t}{d}\right)\right]\cdot \sigma\left(t_{p\max}\right) \end{aligned} \qquad (2.7)$$

with

$$\begin{aligned} t_{n\max} &= \frac{d}{v_n}\cdot \ln\left(1+\frac{E_{\max}\cdot d}{V_{od}}\right) \\ t_{p\max} &= \frac{d}{v_p}\cdot \ln\left(1+\frac{E_{\max}\cdot d}{V_{od}}\right) \end{aligned} > V_{od} > 0 \qquad (2.8)$$

and the unit step function

$$\begin{aligned} \sigma(t_{n\max}) &= 1 \quad 0 \le t \le t_{n\max} \\ \sigma(t_{p\max}) &= 1 \quad 0 \le t \le t_{p\max} \\ \sigma(t) &= 0 \quad \textit{elsewhere.} \end{aligned}$$

Q_{gen} is the total charge per unit length, generated by the traversing particle in the bulk, E_{max} represents the maximum electric field at full depletion, v_n and v_p are the charge carrier drift velocities, d is the detector thickness. V_{od}, the over depletion voltage, is the voltage in excess of the voltage necessary for full detector depletion. t_{nmax} and t_{pmax} denote the total charge collection time for electron and holes respectively. It has to be mentioned here, that the diffusion of the carriers is neglected in this approximation and only the drift component due to the electric field is taken into account.

The two terms are nonzero only for the time where moving charge carriers are present in the bulk, which is accounted for by the unit step functions $\sigma(t)$. Hence, the detectable output signal is a current pulse with a rise time of typically a few pico seconds[4]. This is the time, the incident particle

[4] In case of a usual detector thickness of a few hundred micrometers. The traverse time calculates from the detector thickness divided by the speed of light in the medium (detector material) for relativistic particles.

needs to traverse through the entire detector bulk and to create the maximum number of electron-hole pairs. Immediately after their creation, the charge carriers start drifting in the electric field towards their respective electrodes, where they are absorbed on arrival. At the time when the last carrier reaches its electrode, the current becomes zero. Thus, the fall time of the signal pulse is proportional to the drift velocities of the charge carriers and therefore dependent on the electric field across the detector bulk and the mobilities of the electrons and holes in the semiconductor. As holes have usually a different (lower) mobility than electrons, the falling edge of the pulse signal is divided into two parts. After the last hole has reached its electrode, the output current becomes zero. The length of the falling edge for a moderately overdepleted 300 μm silicon detector is in the range of 25 ns (see Figure 7 for the charge collection time versus overdepletion voltage). Figure 5 shows the pulse shape according to (2.11).

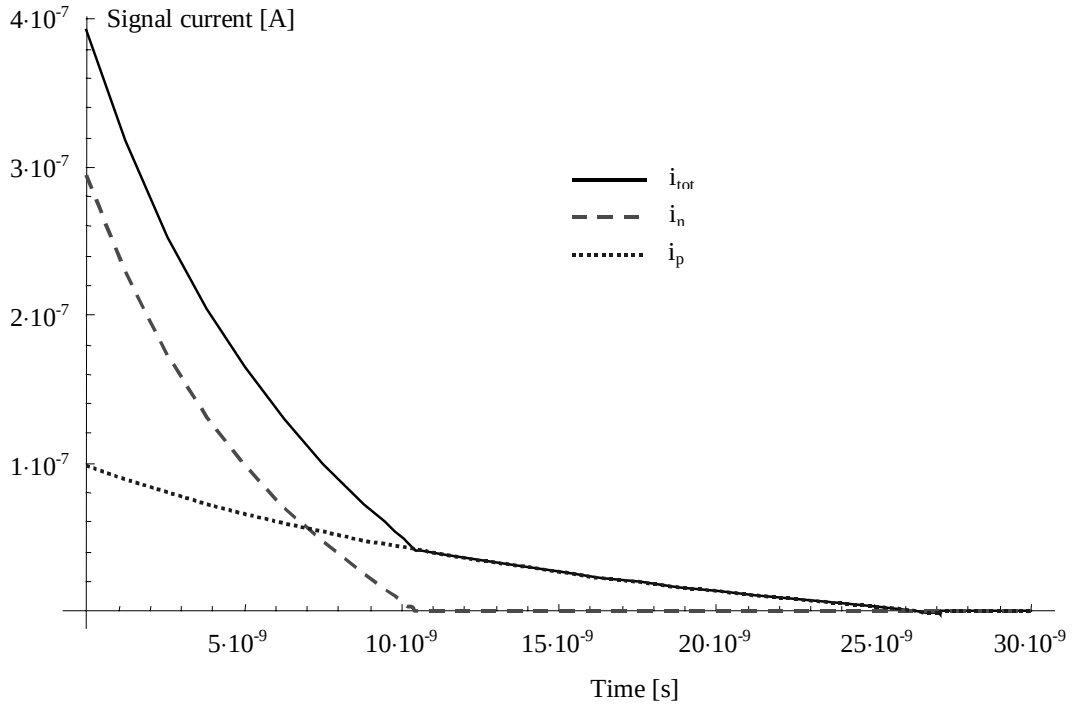

Figure 5. Current vs. time for 300 μm substrate doped at 10^{12} cm^{-3} with an overdepletion of 20 V. The total charge generated was assumed 24000 electron-hole pairs (1 MIP), the carrier mobilities 1300 and 500 cm/Vs respectively.

The contribution of each charge carrier to the total detectable charge in the output pulse depends on the place of its creation inside the detector, hence the further it travels before it reaches the electrode, the more it contributes. For that reason, a certain number of electron-hole pairs induce only half of the charge they carry themselves on the electrodes. The contribution as a function of the drift distance can be denoted as an infinite sum, which converges to one half for each of the charge carrier types [2]. A traversing MIP, creating 24000 electron-hole pairs in 300 μm silicon, gives rise to 24000

q of signal charge. Integrating (2.11) with respect to time yields the collected charge as a function of time [53], (Figure 6).

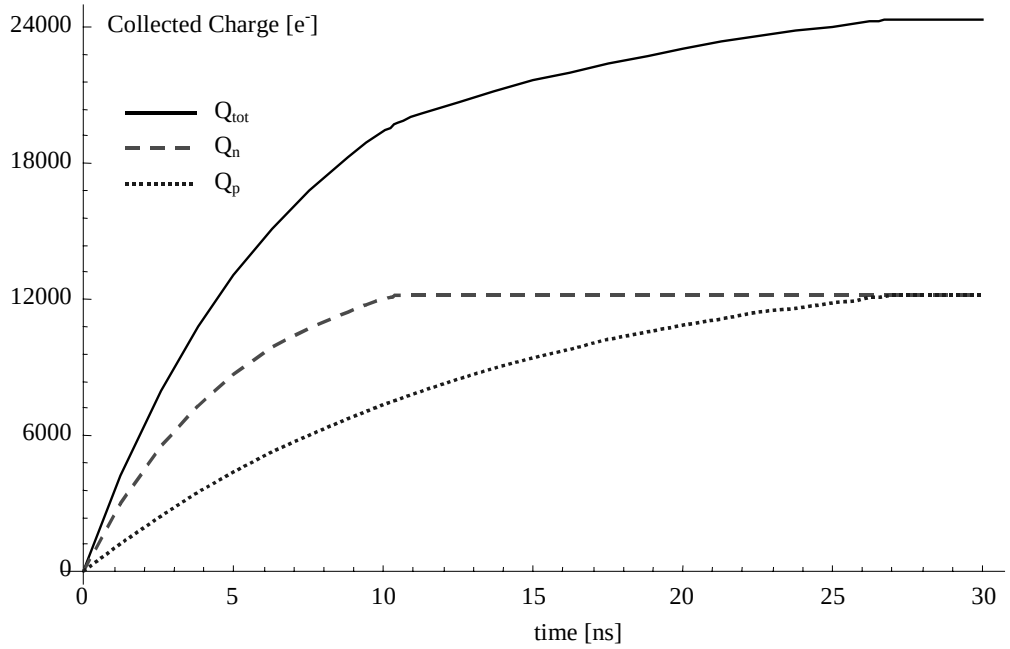

Figure 6. Collected charge as a function of time for the same conditions as in Figure 5.

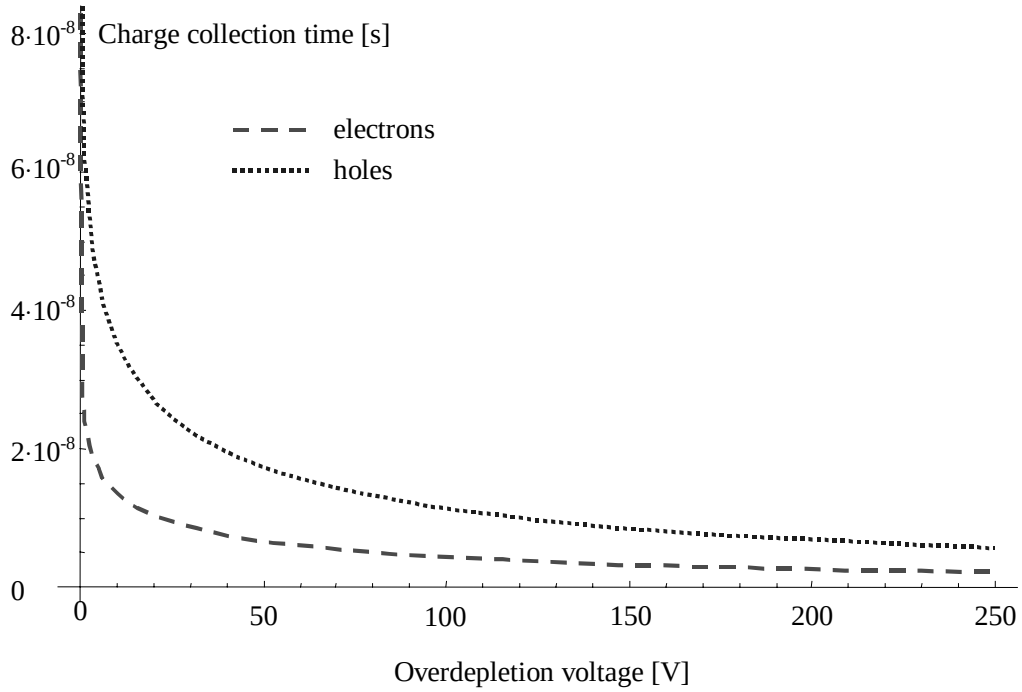

Figure 7. Charge collection time versus overdepletion voltage according to equation (2.12) for 300 μm silicon substrate doped at 10^{12} cm^{-3}.

The Silicon Strip Detector

The following list summarizes the desirable characteristics of a semiconductor particle detector material:

- Efficient energy to charge conversion
- Long charge carrier lifetimes for low leakage current and high charge collection efficiency
- High charge carrier mobilities for large signal amplitude and short signal pulse decay time
- High resistivity to enable full detector depletion
- Surface quality to minimize surface leakage

In current high-energy physics experiments, tracking detectors use mainly silicon as the detecting material, but also different semiconductors like germanium, gallium-arsenide or diamond are presently under investigation for their application as active substrates in radiation detectors. The main advantage of silicon is, besides its attractive characteristics (Table 1), that it has the most advanced techniques for the production of high quality crystals and is the most commonly used semiconductor material for various electronics application and for integrated circuits. The choice of other semiconductor materials might be motivated by special requirements, but their superiority over silicon has rarely been proven in practice. Table 1 summarizes some important properties of silicon [36].

Table 1. Some physical properties of silicon:

Atomic number	14	
Atomic weight	28.09	
Density	2.328	g/cm^3
Dielectric constant (relative)	11.9	
Intrinsic resistivity	235	$k\Omega cm$
Energy gap E_G (300K)	1.12	eV
Electron mobility (300K)	1350	cm^2/Vs
Hole mobility (300K)	480	cm^2/Vs
Carrier saturation velocity (300K)	$8 \cdot 10^6$	cm/s
Intrinsic carrier density	$1.5 \cdot 10^{10}$	cm^{-3}
Breakdown field	$3 \cdot 10^5$	V/cm
Energy per electron-hole pair	3.62	eV
Minimum dE/dx	1.66	$MeV \cdot g/cm^2$

Position sensitive detectors for multi particle tracking usually consist of one or two-dimensional arrays of detection elements. This is obtained by dividing the p-n diode into smaller segments that act as individual independent electrodes. Besides pad and pixel structures, the microstrip detector is the most widely used architecture in modern tracking devices.

Microstrip detectors are segmented in 10 to 50 μm wide parallel diode strips, which can be several centimeters long. Every strip can be connected to its own readout channel or intermediate strips can be left floating and only capacitively coupled to the readout strips. Depending on the precise geometry and signal processing the spatial resolution can be as good as < 1 μm in one dimension [15]; there is no sensitivity along the strip. A schematic view of a microstrip detector is shown in Figure 8. To achieve a two dimensional position information two microstrip detectors are mounted back to back rotated against each other. Only single tracks are unambiguously reconstructed. For n tracks, the n^2 possible combinations of the hits in the individual planes introduce considerable ambiguities called ghost hits. Combining several of these double microstrip planes and an iterative track finding program can partially or fully resolve the ambiguities and reconstruct the real tracks.

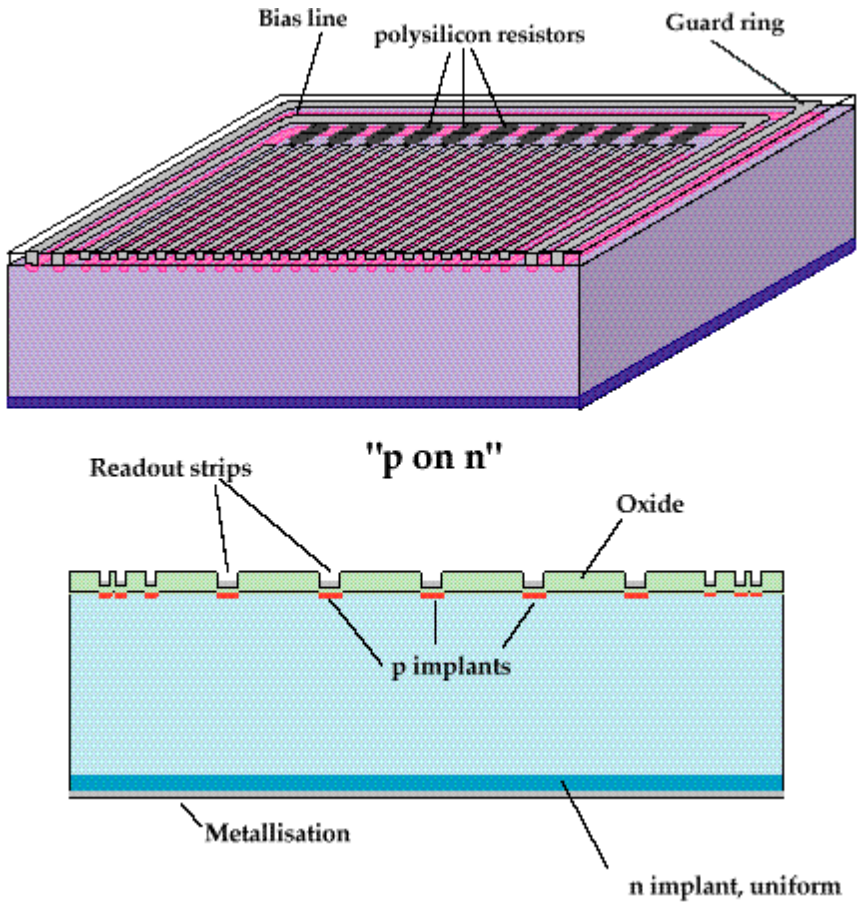

Figure 8. Cut views of a single sided p-on-n microstrip detector with capacitive (AC) coupled aluminum readout strips. The p-type implants are isolated from the readout strips through silicon oxide.

In addition to segmenting one side of the detector, the backplane can be segmented as well. This allows two dimensional position information from one silicon plane, hence reducing the material the particles have to traverse and can help to resolve the ambiguities by correlating the signal heights in the strips on the front and the back side.

For the ATLAS tracker, single sided p-on-n silicon strip detectors are foreseen. Each detector has an active area of approximately 6 cm by 6 cm, containing 768 strips. All strips are read out. The implant strip dimensions are 20 μm width, 62 mm length and 80 μm pitch[5]. A bias resistor supplies a DC path from each implant strip to the bias line allowing all strips to be held at the same potential. The resistor value should be large in order to achieve a maximum isolation between the individual strips and to keep its contribution to the system noise low (Chapter 3). On the other hand, the resistors cannot be made arbitrarily large as the inevitable variation of the actual resistor values would cause a too big variation of voltage drop, influencing the potential of the individual strips. The readout strips are AC coupled aluminum lines deposited on top of the oxide layer. The backplane consists of a metallized n^+-layer. The detector bias voltage is applied between the bias line and the backplane. The detector bulk thickness is 300 μm.

Table 2 summarizes some important electrical properties of the ATLAS prototype strip detector, which are crucial for the design of the read out electronics.

Table 2. ATLAS strip detector electrical properties

Resistivity p-implant	<200	kΩ/cm
Resistivity aluminum strip	<15	Ω/cm
Bias resistors (polysilicon)	1.5±0.5	MΩ
Load capacitance per strip	<1.2	pF/cm
Coupling capacitance	>20	pF/cm
Depletion voltage	<100	V
Initial leakage current @ 20°C (no irradiation)	<6	μA @ 150 V
	<20	μA @ 300 V
	<100	μA @ 500 V
Leakage current after irradiation	<1.5	mA @ 500 V

[5] The pitch denotes the distance between the centers of two adjacent strip implants.

Chapter 3

Processing The Signals From Silicon Strip Detectors - The Front-End

In order to utilize the information of the signal induced by traversing particles on the readout electrodes of a silicon strip detector, it needs to be taken care of by some signal-processing unit.

The following section describes the requirements for an electronic device to deal with the signal delivered by a Silicon strip detector in terms of electrical properties of the signal itself and of the detector. In this context, we emphasize on the crucial problem of the noise performance of an amplifier to be used with silicon detectors.

In integrated signal processing systems such as detector readout systems, electrical noise is a fundamental limiting factor. It represents a lower limit to the size of the electrical signal that can be handled by an electronic circuit without significant deterioration in signal quality. In position sensitive detector systems, the ratio between signal charge and noise determines the position resolution and even the detectability of the signals and indirectly determines the readout speed and the number of readout channels required. For a silicon strip detector and using pulse height readout, the position resolution at a given strip distance is directly proportional to the system's signal-to-noise ratio [47].

For the design of such a system, it is of crucial importance to optimize the noise performance of the preamplifier or input stage, as in a well designed systems the overall noise performance is always dominated by the preamplifier noise. The signal source in semiconductor detector systems is of a reactive rather than a resistive type, which means that the signal source at the input of the preamplifier can be represented by a capacitance in parallel with a current source. In order to achieve wideband noise matching, this fact has to be taken into account.

Unfortunately, noise is not the only performance parameter to be optimized for wideband amplifiers matching reactive sources. In addition, there are many other constraints to be met such as precise gain, bandwidth, power dissipation, distortion, stability, dynamic range, etc. For the application of the semiconductor detector readout, some of those, like low power dissipation are crucial, while others, such as large dynamic range or precise gain are less important.

The goal of this section is, to derive a complete expression for the noise performance of an entire detector readout system in terms of design parameters and conditions imposed by the environment.

The Preamplifier

The front-end for the readout of signals from silicon strip detectors, as well as from other types of particle detectors, can be divided into three sub-blocks: The input stage or preamplifier, which is the main source of electronics noise, the shaper, a bandpass filter to reduce the noise bandwidth, and some type of output buffer, that drives the signal from the shaper into subsequent stages.

The first step in the design of a preamplifier is the choice of the appropriate input device, which dominates the noise performance of the entire system. Possible candidates for this type of application are bipolar-junction-transistors (BJT) and the field-effect-transistors (MOSFET and JFET). There is only one noise source for each device type, which is related to the amplification mechanism and determined uniquely by the fundamental parameters of the device. This is thermal noise in the case of FETs and collector current shot noise for the BJT, which can be represented as an equivalent white noise voltage generator in series with the control electrode (base, gate). All other noise sources (for example "parallel" sources such as resistors at the input and leakage current into the input) are a result of imperfections. This type of noise can be reduced by improvements in technology and circuit design. The superiority of one device over the others in terms of noise performance depends on the selected amplifier configuration as well as on the requirements of the application. In the following, the noise performance of the BJT as the input device for a charge sensitive preamplifier will be derived and compared with the performance of a MOSFET transistor.

Feedback Configurations

There are three types of preamplifier configurations commonly used for the amplification of charge signals from particle detectors. Those are the integrating transimpedance amplifier with capacitive feedback ("charge sensitive amplifier", CSA), the current amplifier configuration and the voltage amplifier configuration. A detailed description of those architectures as charge amplifiers and a performance comparison are given in [27]. Subsequently, only the transimpedance configuration will be studied.

As discussed in Chapter 2, pp. 11, the detector output signal can be represented as a short current pulse, for a thin silicon detector in the range of up to 30 ns. The total charge Q_s contained in this pulse i_s is proportional to the energy deposited in the detector.

$$E \propto Q_s = \int i_s dt \qquad (3.1)$$

This charge is integrated onto a small feedback capacitor C_f by means of a low noise transimpedance amplifier, giving rise to a voltage step at the output with an amplitude Q_s/C_f. The step signal is fed into another integrating amplifier, which performs the pulse shaping, respectively noise filtering, primarily to optimize the signal-to-noise ratio of the readout system. The pulse shaper is being investigated in the section "Equivalent Noise Charge (ENC) And The Shaper Circuit", pp. 28.

Figure 9 shows the block diagram of a charge-sensitive transimpedance amplifier configuration (CSA). With the amplifier voltage gain $V_o / V_i = -A$, the voltage across C_f becomes $V_f = (A + 1) \cdot V_i$ The charge integrated onto C_f can be written as $Q_f = C_f \cdot V_f = C_f \cdot (A + 1) \cdot V_i$. Assuming the charge into the amplifier $Q_i \cong Q_f$, the charge gain A_Q calculates to:

$$A_Q = \frac{V_o}{Q_i} = \frac{V_o}{C_f (A+1) \cdot V_i} = -\frac{A}{A+1} \cdot \frac{1}{C_f} \approx -\frac{1}{C_f} \qquad (3.2)$$

The effective ("dynamic") input capacitance is $C_i = Q_i / V_i = C_f \cdot (A + 1)$. The amount of signal charge which actually flows into the amplifier input and the fraction which remains on C_d is determined by the ratio C_d / C_i :

$$\frac{Q_i}{Q_s} = \frac{Q_i}{Q_d + Q_i} = \frac{C_f V_f}{C_d V_i + C_f V_f} = \frac{C_f (A+1)}{C_d + C_f (A+1)} = \frac{C_i}{C_d + C_i} = \frac{1}{1 + \frac{C_d}{C_f (A+1)}} \qquad (3.3)$$

For example, assuming a feedback capacitance of 100 fF, a detector capacitance of 10 pF and a voltage gain of 1000, the fraction of signal charge that actually flows into the amplifier is 91%.

The feedback resistor R_f serves to discharging the capacitor C_f. It has to be large enough to minimize its contribution to the amplifier noise and small enough to discharge C_f fast enough to prevent tail pile-up.

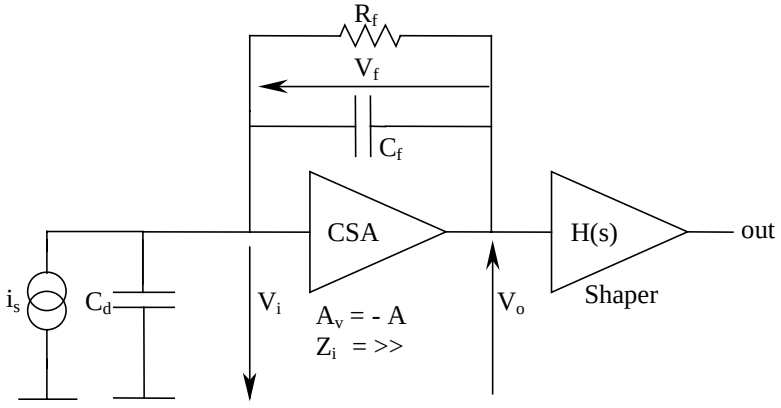

Figure 9. Block diagram of the charge sensitive amplifier (CSA) configuration.

Noise Sources In Bipolar Junction Transistors

In the following sections, the noise sources which appear with the use of a BJT as the input device for a CSA, will be revisited and the noise behavior of the whole system, from the detector to the shaper output, derived. Subsequently, the noise performance will be compared to the noise performance of a similar system, using a FET as the input device.

First, the basic noise mechanisms will be summed up, for a detailed discussion refer to excellent sources like [13], [39] or [46]. Noise can be characterized by its frequency spectrum, its amplitude distribution, and the physical mechanism responsible for its generation. There are two irreducible forms of noise which are generated according to physical principles, *shot noise* and *thermal* (or *Johnson*) *noise.* Real devices (transistors, resistors) in addition show various sources of "excess noise". This excess noise often exhibits a *1/f* spectrum, therefore called *1/f-noise*. Measured noise voltage (or current) depends on the measurement bandwidth, thus it is convenient to define a RMS noise voltage (current) spectral density:

- *Thermal noise* is generated by random thermal movement of the charge carriers in any conductive material. The noise voltage spectrum of a resistor, for example, is proportional to its resistance and to the absolute temperature and is frequency independent, thus showing a "white" noise spectrum:

$$v_t = \sqrt{4kTR\Delta f} \tag{3.4}$$

  A noisy resistor can be represented by an equivalent circuit, composed of a noise-free resistor and a noise voltage source in series[1] with a noise voltage density according to (3.4).

- *Shot noise* occurs due to the fact that an electric current is the flow of discrete electrical charges. Any current flowing across a potential barrier, like for example a pn-junction, shows a statistical fluctuation, giving rise to a random pulse train of current pulses of unit charge. The spectrum is, like for thermal noise, white:

$$i_n = \sqrt{2qI_{DC}\Delta f} \tag{3.5}$$

  The equivalent circuit representation for a shot noise source is a current generator according to (3.5).

- *1/f noise* in the case of the BJT manifests itself only in a frequency region that can be several orders of magnitude lower than that in MOSFET transistors. Therefore, from a practical low-noise design point of view, *1/f noise* in bipolar transistors has only little significance.

[1] According to Norton's Theorem, this series arrangement can be replaced by a current generator in parallel to the ideal resistor, with a noise current density of $i_t = \sqrt{4kT\Delta f / R}$.

In a bipolar transistor in the forward-active region, minority carriers diffuse and drift across the base region to be collected at the collector-base junction. Minority carriers entering the collector-base depletion region, are accelerated by the field existing in this region, and swept across into the collector. The time of arrival of the drifting carriers at the collector base junction is a purely random process and hence the BJT‘s collector current consists of a random series of current pulses, therefore showing *shot noise* behavior.

$$i_{nc}^2 = 2qI_c\Delta f \tag{3.6}$$

The base current I_b appears due to recombination in the base and base–emitter depletion regions and due to carrier injection from the base into the emitter. I_b exhibits *shot noise*.

$$i_{nb}^2 = 2qI_b\Delta f \tag{3.7}$$

In addition to the shot noise sources, associated with the terminal currents, BJTs show also *thermal noise* due to series resistances at each terminal. Among the three resistances r_{bb}, r_c and r_e, the base-spread resistance r_{bb} is the most important one, because it appears at the input terminal for most cases. The noise voltage caused by the base resistance is

$$v_{nb}^2 = 4kTr_{bb}\Delta f \tag{3.8}$$

Although there is no exact theoretical description of *1/f noise* in BJTs, it was shown [39] that the appropriate power spectrum can be expressed as

$$i_{nf}^2 = \frac{2qf_L I_B^\gamma}{f} \tag{3.9}$$

with the technology dependent parameters f_L and γ. The parameter f_L stands for the noise corner frequency of the specific device, while γ is a constant factor between 1 and 2, usually close to 1.

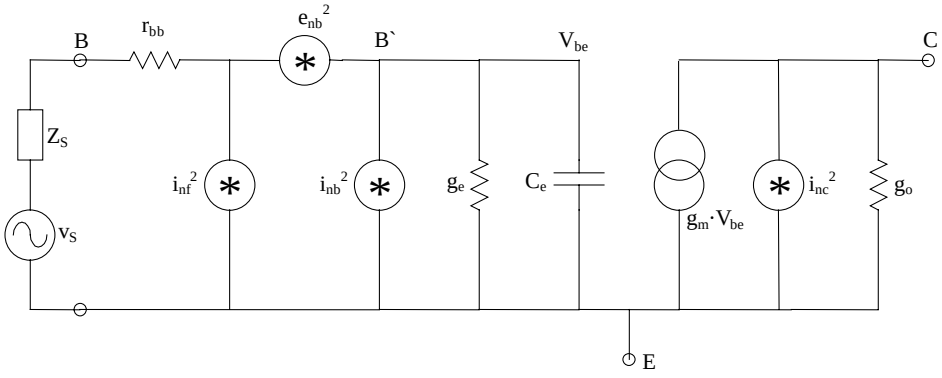

Figure 10. Hybrid-π small signal model of a BJT transistor, modified to include noise sources.

Figure 10 shows the hybrid-π small signal model of a BJT transistor, including the above described noise sources. The two elements g_e and C_e represent the significant portion of the transistor input impedance. The amplification property of the device is represented by the dependent current generator $g_m \cdot V_{be}$, where V_{be} is the signal potential between $B`$ and the emitter terminal E, the element g_o represents the dynamic output resistance of the transistor. The short-circuit current gain β can be derived from the model. Assuming a short circuit between C and E and considering low-frequency operation, β can be expressed as

$$\beta = \frac{g_m V_{be}}{g_e V_{be}} = \frac{g_m}{g_e}, \qquad (3.10)$$

with g_m derived from the diode equation relating I_c and V_{be}:

$$g_m = \frac{qI_C}{kT} \qquad (3.11)$$

Amplifier Noise Model

In general, the noise performance of any two-port network can be represented by two equivalent input noise generators e_n and i_n. e_n represents a zero impedance voltage generator in series with the input port, i_n a infinite impedance current generator in parallel with the input. A complex coefficient C (not shown) implies possible correlation between the two noise sources. It can usually be neglected. The thermal noise of the signal source resistance is represented by the noise generator e_t. An *equivalent input noise* generator e_{ni} can be used to represent all three noise sources. As the noise generators are assumed to be uncorrelated, they are summed up by adding their mean square values:

$$e_{ni}^2 = e_t^2 + e_n^2 + i_n^2 R_s^2 \qquad (3.12)$$

The correlation term would add to the right-hand side of this equation in the form $2Ce_n i_n R_s$.

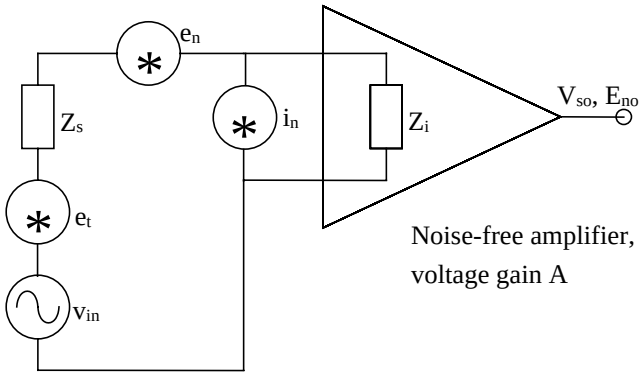

Figure 11. Amplifier noise model

In order to determine an overall signal-to-noise ratio of the preamplifier, we need to refer all transistor noise mechanisms to the input port. First, we express e_{ni}, e_n and i_n in (3.12) in terms of the noise sources, associated with the BJT transistor (3.6 – 3.9), then calculate the total noise at the transistor output, the gain from the source to the output, and finally divide the output noise by the gain.

With the output shorted in Figure 10., the output noise current is

$$i_{no}^2 = i_c^2 + (g_m V_{be})^2 \tag{3.13}$$

For an input signal V_s, the output short-circuit signal current is

$$I_o = g_m V_{be} = \frac{g_m V_s Z_e}{r_{bb} + R_s + Z_e} \tag{3.14}$$

With the transfer gain $K_t = I_o/V_s$, the equivalent input noise becomes:

$$e_{ni}^2 = \frac{i_{no}^2}{K_t^2} \tag{3.15}$$

Substituting (3.13) and (3.14) in (3.15) and introducing the expressions for the noise generators (3.6 – 3.9), leads to an expression for the equivalent input noise in terms of transistor parameters, temperature, operating-point currents, frequency and source resistance:

$$e_{ni}^2 = 4kT(r_{bb} + R_s) + 2qI_B(r_{bb} + R_s)^2 + \frac{2qI_C(r_{bb} + R_s + \beta r_e)^2}{\beta^2} + \frac{2qf_L I_B^{\gamma}(0.5r_{bb} + R_s)^2}{f} + 2qI_C(r_{bb} + R_s)^2\left(\frac{f}{f_T}\right)^2 \tag{3.16}$$

Starting from this complete expression for e_{ni}, we can derive the "series" noise voltage e_n and the "parallel" noise current i_n. Rewriting (3.16) for $R_s = 0$ gives, by definition, the noise voltage e_n. With the assumption $r_{bb}^2 << \beta \cdot r_e^2$, we get:

$$e_n^2 = 4kTr_{bb} + 2qI_C r_e^2 + \frac{2qf_L I_B^{\gamma}(0.5r_{bb})}{f} + 2qI_C r_{bb}^2\left(\frac{f}{f_T}\right)^2 \tag{3.17}$$

For R_s very large (specifically $2qI_b > 4kTR_s$), and with assuming $I_C / \beta^2 << I_B$, (3.16) yields the noise current i_n:

$$i_n^2 = 2qI_B + \frac{2qf_L I_B^{\gamma}}{f} + 2qI_C\left(\frac{f}{f_T}\right)^2 \tag{3.18}$$

Simple limiting noise conditions for the midband region can be obtained from these two equations by removing all frequency dependent terms. This region is also called "shot noise region" because the shot noise sources dominate in a well-designed circuit.

$$\boxed{\begin{aligned} e_n^2 &= 4kTr_{bb} + 2qI_C r_e^2 \\ i_n^2 &= 2qI_B \end{aligned}} \qquad (3.19)$$

With $r_e = 1 / g_m$ and $g_m = qI_c / kT$ (3.19) can be rewritten as

$$\boxed{\begin{aligned} e_n^2 &= 4kT\left(r_{bb} + \frac{1}{2g_m}\right) = 4kT\left(r_{bb} + \frac{kT}{2qI_C}\right) \\ i_n^2 &= 2qI_B \end{aligned}} \qquad (3.20)$$

Two mechanisms limit the *series voltage noise*, the thermal noise of the base resistance and the shot noise of the collector current times the emitter resistance, while the *parallel current noise* is determined only by the shot noise of the base current. Figure 12 plots the equations of (3.19) as a function of the collector current I_C.

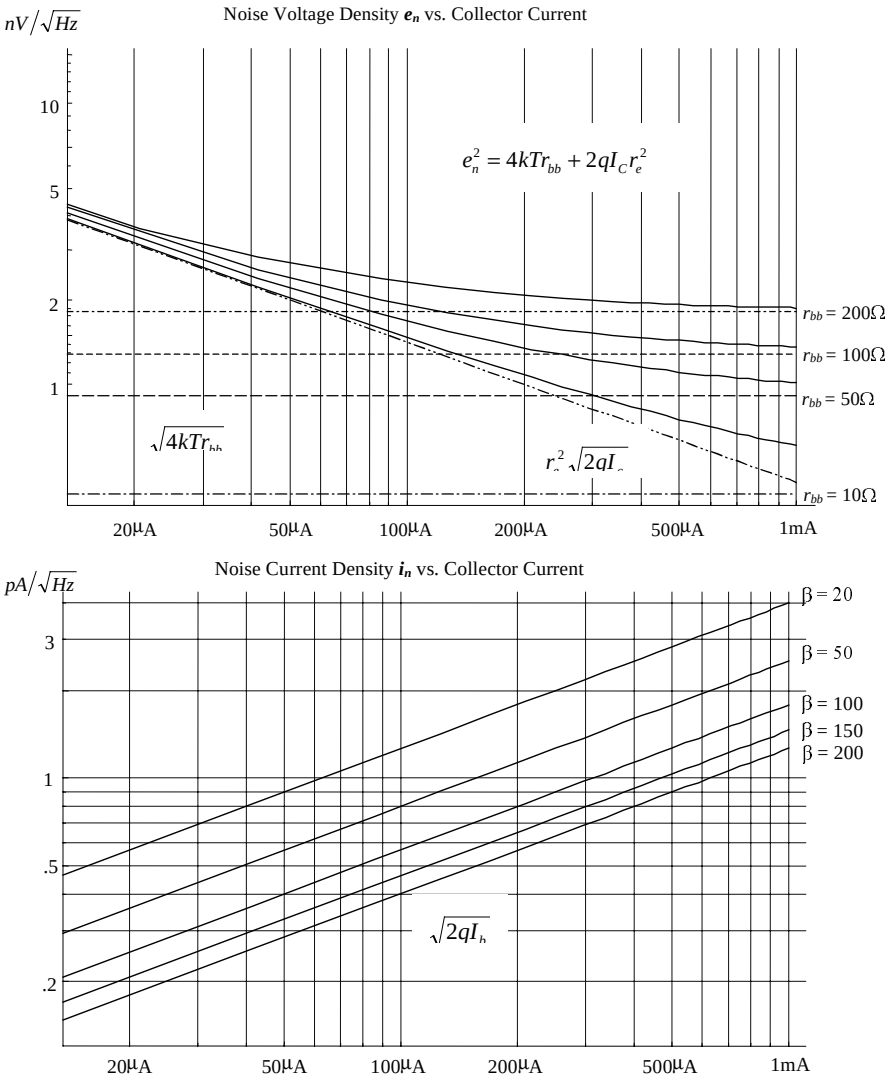

Figure 12. Voltage and current noise spectral densities versus collector current. The respective parameters are the base spread resistance r_{bb} and the transistor current gain β .

After having derived the equivalent noise sources for the case of a bipolar transistor as the input device, we will look at the complete signal path including the detector, the preamplifier with its feedback configuration, and the pulse shaper (noise filter), in order to estimate the noise performance of the entire system. A complete circuit diagram can be obtained by combining the two diagrams of Figure 9 and Figure 11:

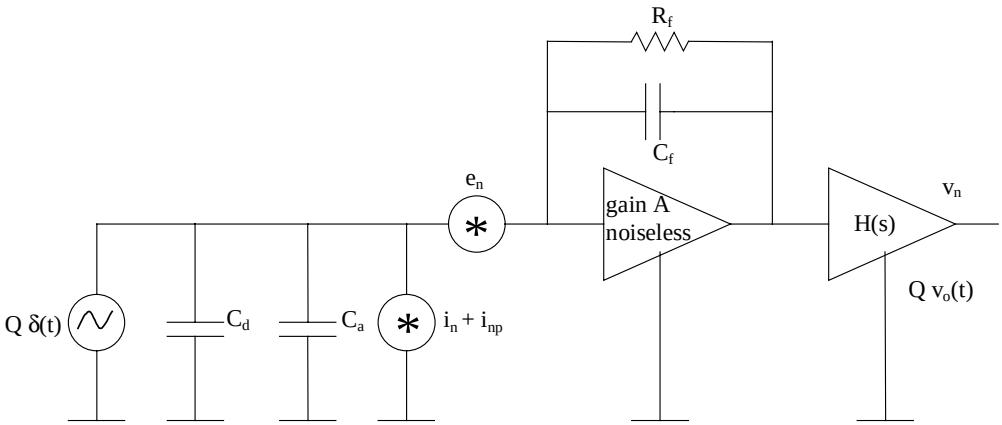

Figure 13. Detector – ideal charge amplifier – shaper, including noise sources

As mentioned earlier, the detector signal can be represented by a δ-Impulse of charge Q, the capacitances are C_d, the detector capacitance, C_a, the amplifier input capacitance and C_f, the feedback or integrating capacitance. Subsequently, the influence of the, compared to C_d, very small C_f will be neglected, however it can always be included by adding it to $(C_a + C_d)$. The equivalent current noise generator i_n which currently represents the base current shot noise, will be extended to include influences of the feedback resistor R_f [2] and the detector leakage current I_D:

$$i_{n,tot}^2 = i_n^2 + i_{np}^2 = 2qI_B + \frac{4kT}{R_f} + 2qI_D \qquad (3.21)$$

It will be accordingly assumed that, using a bipolar transistor in the midband region as the active input device, all power spectral densities in Figure 13 are independent of the frequency, thus show a white noise power spectrum.

Equivalent Input Noise Spectral Density

With the assumption that the input device dominates the noise performance of the entire system, the total equivalent noise current spectral density at the input can explicitly be written as a function of the basic design parameters of the input transistor. Merging (3.19) and (3.21) into the equivalent current expression of (3.12), yields the input noise current density:

[2] The contribution of the detector bias resistor, which appears in parallel to *Rf*, will be neglected as it is usually at least one order of magnitude larger.

$$i_{ni}^2 = e_n^2 \cdot \omega^2 (C_a + C_d)^2 + i_{n,tot}^2 = 4kT\left(r_{bb} + \frac{kT}{2qI_C} \right)\omega^2 \left(C_a + C_d\right)^2 + \frac{2qI_C}{\beta} + \frac{4kT}{R_f} + 2qI_D \qquad (3.22)$$

In the above expression, the base spread resistance r_{bb}, current gain β, and collector bias current I_C are the three transistor parameters to be optimized. In order to minimize the noise contributions of the base resistance and base shot noise, the input transistor has to be designed to have a small base resistance r_{bb} and a large current gain β. For a given technology r_{bb} is mainly concerned with layout techniques (p. 41, [22]), while the current gain, under normal operating conditions, is more or less constant (p. 47) and depends only on technological parameters. Figure 14 plots the dependencies of the input noise current with respect to the main design parameters, assuming the following values: C_a = 0.5 pF, C_d = 20 pF, r_{bb} = 50 Ω, β=100, T = 300 K, I_D = 1 nA, R_f = 80000 Ω at a frequency of ω = 40 MHz.

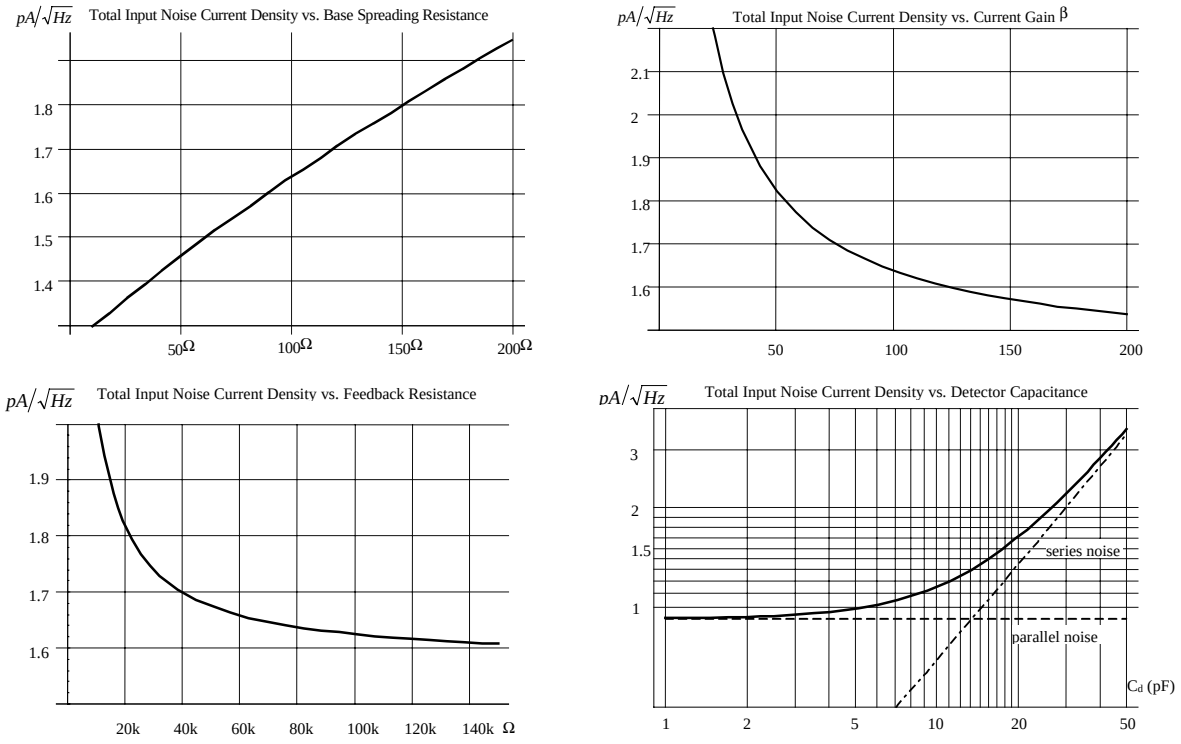

Figure 14. Equivalent input noise variations with respect to the main design parameters at ω = 40 MHz.

The main free parameter for the circuit designer is the collector bias current I_C, therefore noise optimization is equivalent to optimization of the collector current. The derivative of (3.22) with respect to I_C gives the optimum collector current:

$$I_{C,opt} = \frac{kT}{q}\sqrt{\beta}\left(C_a + C_d\right)\cdot\omega \qquad (3.23)$$

Assuming a current gain β of 100 and a detector capacitance of 20 pF and for a center frequency of ω = 40 MHz , $I_{C,opt}$ can be estimated to be in the order of ~200 μA according to (3.23). Figure 15. is a plot of the equivalent input noise current according to (3.22) for three different detector capacitances at ω = 40 MHz, Figure 16 shows a double logarithmic plot of the noise voltage density.

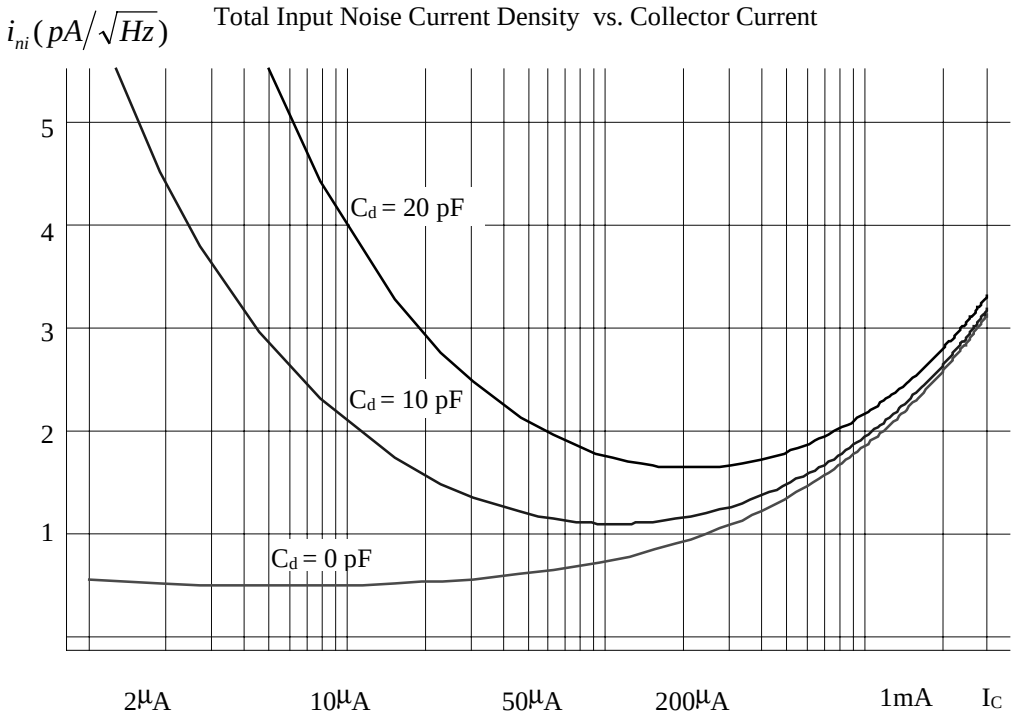

Figure 15. Equivalent input noise current according to (3.22) vs. I_C for three different load capacitances.

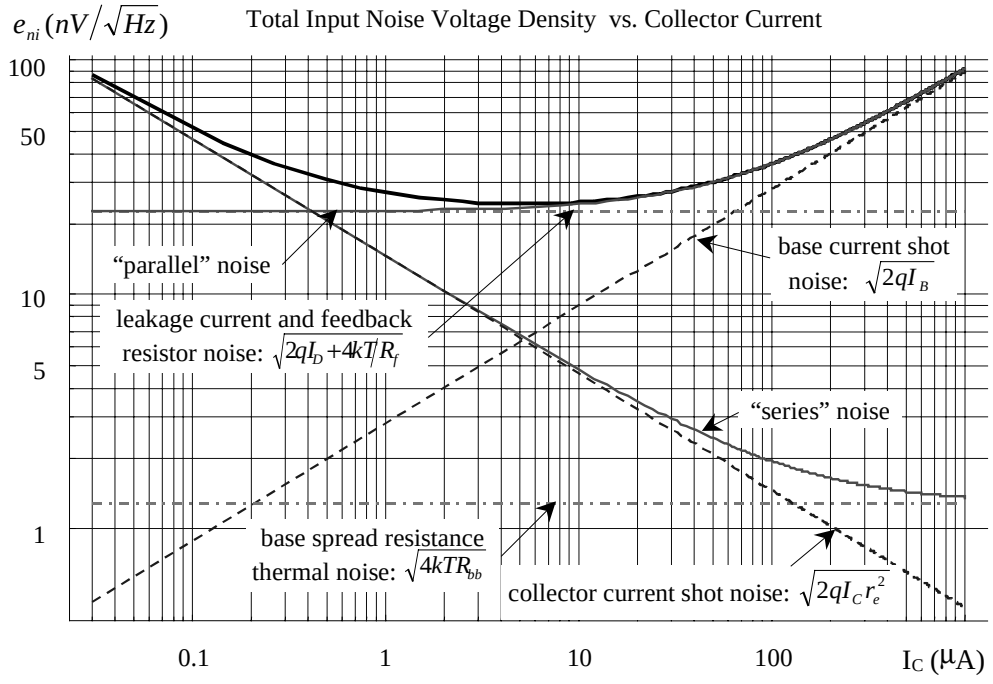

Figure 16. Equivalent input noise voltage according to (3.22) vs. I_C for a load capacitance of 500fF.

Equivalent Noise Charge (ENC) And The Shaper Circuit

As the input signal coming from the detector is a charge signal, it is convenient to express also the preamplifier noise in terms of electrical charge referred to the amplifier input. This *Equivalent Noise Charge* (ENC) can be defined as the variance of a *Gaussian* distribution at the amplifier output resulting from an infinitely narrow probability density function of detector charge at the input. ENC is typically expressed in RMS electrons. In order to calculate the noise performance of the entire system, also the filter transfer function *H(s)* of the shaper circuit has to be taken into account. *H(s)* is the *Laplace Transform* of the response of the shaper to a *Dirac*-impulse. The system response to a detector current signal $Q\cdot\delta(t)$ can thus be written as:

$$v_o(t) = L^{-1}\left[\frac{1}{s}\cdot\frac{Q\cdot A}{C_d + C_a}H(s)\right] \tag{3.24}$$

with L^{-1} denoting the inverse *Laplace Transform*. As $v_o(t) = 0$ for $t < 0$ and returns to zero at a finite time, it has at least one maximum. We want to assume that the voltage signal is sampled at the largest absolute value of these maxima $Q\cdot max[v_o(t)]$, and this value being used as the information on the respective event in further stages of the signal chain. With $N(\omega)=A^2e^2_{ni}$ as the total output noise power spectral density, the RMS noise at the output of the network can be described as

$$v_{no}^2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} N(\omega)\left|H(j\omega)\right|^2 d\omega \tag{3.25}$$

Substituting (3.20) with (3.21) into (3.25) yields

$$v_{no}^2 = \frac{1}{2\pi}A^2\int_{-\infty}^{\infty}\left(e_n^2 + \frac{i_{n,tot}^2}{\omega^2(C_a + C_d)^2}\right)\left|H(j\omega)\right|^2 d\omega \tag{3.26}$$

The signal-to-noise ratio can therefore be expressed as the quotient of (3.24) and (3.26):

$$SNR = \frac{\dfrac{Q\cdot A}{C_d + C_a}\cdot \max L^{-1}\left[\dfrac{H(s)}{s}\right]}{\left\{\dfrac{1}{2\pi}A^2\displaystyle\int_{-\infty}^{\infty}\left(e_n^2 + \frac{i_{n,tot}^2}{\omega^2(C_a + C_d)^2}\right)\left|H(j\omega)\right|^2 d\omega\right\}^{\frac{1}{2}}} \tag{3.27}$$

The equivalent noise charge ENC is defined as the value of *Q* which yields *SNR = 1*. This means that ENC is the value of charge which, injected across the detector capacitance, produces at the output a signal whose amplitude equals the output RMS noise. Applying this definition to (3.27) gives the

final expression for the ENC, including all noise sources of the input device (BJT) and the amplifier architecture, and valid for all types of shaper transfer functions:

$$ENC = \frac{\left\{ \frac{1}{2\pi} \int_{-\infty}^{\infty} \left(e_n^2 \left(C_a + C_d \right)^2 + \frac{i_{n,tot}^2}{\omega^2} \right) \left| H(j\omega) \right|^2 d\omega \right\}^{\frac{1}{2}}}{\max L^{-1}\left[\frac{H(s)}{s} \right]} \qquad (3.28)$$

The unit of this expression is RMS Coulombs. To get the ENC in RMS electrons, the result has to be divided by the unit charge.

The role of "pulse shaping" or "noise filtering" is to minimize the measurement error with respect to the noise, and at high event rates to minimize the effects of pulse overlap or pileup. The effect of different transfer functions *H(s)* of the shaper/filter circuit on the signal-to-noise ratio respectively the ENC, has been studied in detail in [26], [24], [51], [52]. We will restrict the investigation to two time-invariant filter functions, the triangular and the *CR-(RC)*^{n} shaping. The first, although it is not ideally realizable, is simple and often being used for noise performance estimations. The second is very common for practical implementations of readout electronics for particle detectors. The *CR-(RC)*^{n} filter contains one high-pass section, followed by *n* low-pass sections, all having the same time constant. The configuration is also known as *quasi* or *semi-Gaussian* filter, because its response to a step input approximates the shape of the *Gauss* error curve.

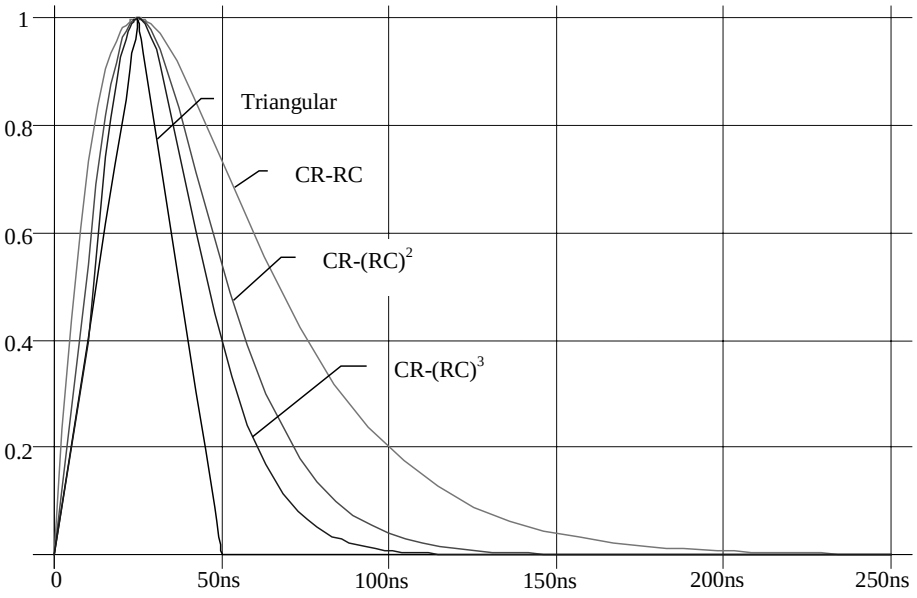

Figure 17. Pulse Shapes for triangular and CR-RC, CR-(RC)^2 and CR-(RC)^3 filter functions with peaking times of 25 ns and the peak amplitudes normalized to unity.

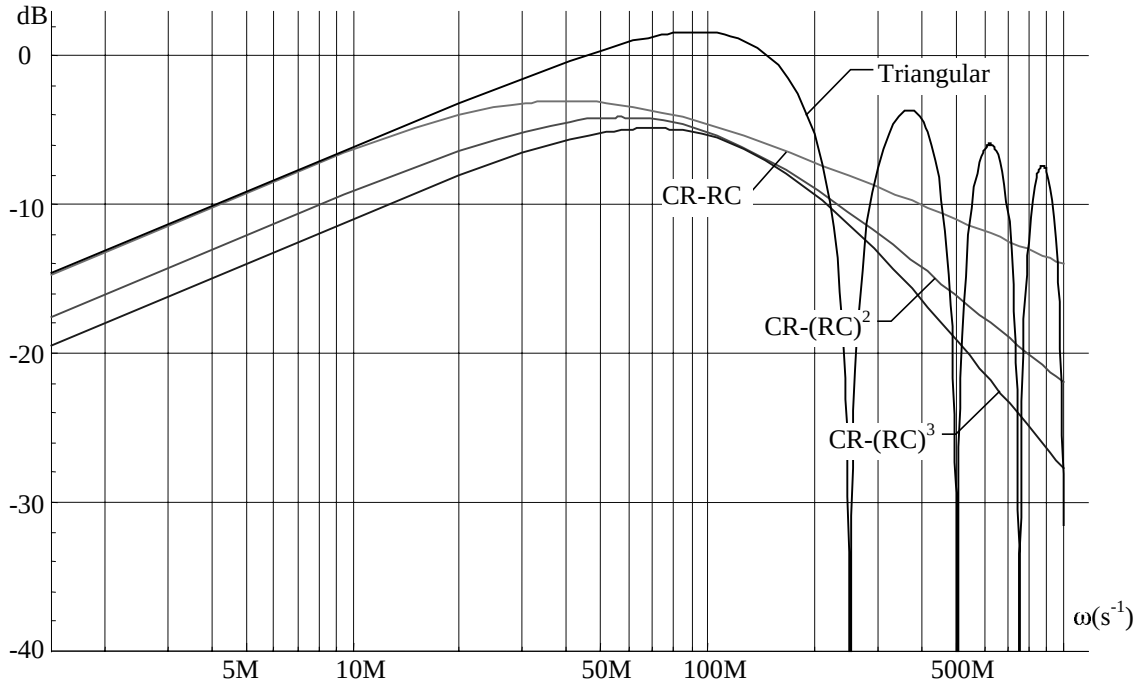

Figure 18. Double logarithmic plot of the filter functions of Figure 17 in the frequency domain.

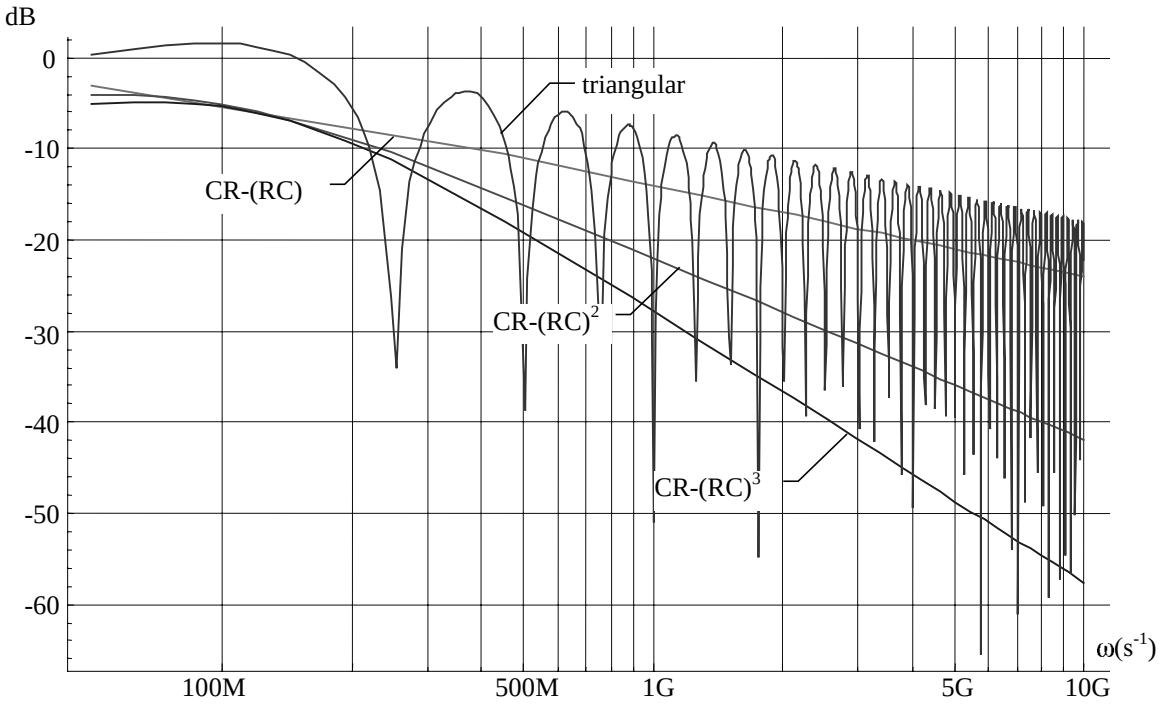

Figure 19. Lowpass slope of the filter transfer functions of Figure 18. The CR-(RC) function drops by 10 dB/decade, CR-(RC)^2 by 20 dB/dec., CR-(RC)^3 by 30 dB/dec. towards higher frequencies.

The determination of the signal-to-noise ratio requires the evaluation of the peak amplitude of the δ-response of the whole system and that of the noise integral in the denominator of (3.27). The *Laplace Transform H(s)* of the *CR-RC* shaping function with peaking time T_p is given by

$$H(s) = \frac{sT_p}{(1+sT_p)^2} \tag{3.29}$$

which leads, according to (3.24) to

$$v_o(t) = \frac{A}{C_d + C_a} \cdot \frac{t}{T_p} \cdot e^{-t/T_p} \tag{3.30}$$

with a peak value of $\frac{1}{e} \cdot \frac{A}{C_d + C_a}$.

The integral in the denominator is given by:

$$e_n^2 \int_{-\infty}^{\infty} \frac{\omega^2 T_p^2}{(1+\omega^2 T_p^2)^2} d\omega + \frac{i_n^2 T_p^2}{(C_d + C_a)^2} \int_{-\infty}^{\infty} \frac{d\omega}{(1+\omega^2 T_p^2)^2} \tag{3.31}$$

With the definite integrals of the types $\int_{-\infty}^{\infty} \frac{x^2}{(1+x^2)^2} dx$ and $\int_{-\infty}^{\infty} \frac{1}{(1+x^2)^2} dx$ producing π/2, the SNR of equation (3.27) and ENC of equation (3.28) result in:

$$SNR_{CR-RC} = \frac{(2/e)Q}{\frac{1}{\sqrt{2}}\left[(C_d + C_a)^2 \frac{e_n^2}{T_p} + i_{n,tot}^2 T_p\right]^{\frac{1}{2}}} \tag{3.32}$$

$$ENC_{CR-RC} = \frac{e}{2\sqrt{2}}\left[(C_d + C_a)^2 \frac{e_n^2}{T_p} + i_{n,tot}^2 T_p\right]^{\frac{1}{2}} \tag{3.33}$$

The *Equivalent Noise Charge ENC* for a charge sensitive preamplifier with a bipolar input transistor followed by a CR-RC shaper in terms of basic transistor and design parameters, given in RMS electrons, is expressed by the following equation:

$$ENC_{CR-RC} = \frac{e}{2\sqrt{2} \cdot q} \sqrt{\frac{4kT\left(r_{bb} + \frac{kT}{2qI_C}\right)(C_d + C_a)^2}{T_p} + \left(\frac{2qI_C}{\beta} + \frac{4kT}{R_f} + 2qI_D\right)T_p} \tag{3.34}$$

A similar procedure yields an expression for the *ENC* in case of triangular shaping:

$$ENC_{triangular} = \frac{1}{q} \sqrt{\frac{4kT\left(r_{bb} + \frac{kT}{2qI_C}\right)(C_d + C_a)^2}{T_p} + \left(\frac{2qI_C}{\beta} + \frac{4kT}{R_f} + 2qI_D\right)\frac{T_p}{3}} \tag{3.35}$$

The calculations of the *RC-(CR)^n* filter functions for *n = 1,2,3* are summarized in Table 3. The columns contain the *Laplace Transform* of the function, the solutions for the definite integrals in (3.31), the maximum value of the pulse, the factor in front of the square root and the multipliers for the voltage and current noise densities.

Table 3. Factors for the calculation of the ENC for RC-(CR)^n filter functions with n = 1,2,3.

Filter function	*Laplace Transform*	Integral 1	Integral 2	Pulse MAX	Mult. Factor	Series Multiplier	Parallel Multiplier
CR-RC	$\frac{sT_p}{(1+sT_p)^2}$	$\frac{\pi}{2}$	$\frac{\pi}{2}$	$\frac{1}{e}$	$\frac{e}{2\sqrt{2}}$	$\frac{1}{T_p}$	T_p
CR-(RC)^2	$\frac{s(T_p/2)}{(1+s(T_p/2))^3}$	$\frac{\pi}{8}$	$\frac{3\pi}{8}$	$\frac{2}{e^2}$	$\frac{e^2}{8\sqrt{2}}$	$\frac{2}{T_p}$	$\frac{3T_p}{2}$
CR-(RC)^3	$\frac{s(T_p/3)}{(1+s(T_p/3))^4}$	$\frac{\pi}{16}$	$\frac{5\pi}{16}$	$\frac{9}{2e^3}$	$\frac{e^3}{36}$	$\frac{3}{T_p}$	$\frac{5T_p}{3}$

From various studies on the influence of different shaping functions on the ENC of detector readout systems [16], [21], [24], [26], [46], [51], [52], it can generally be concluded, that the exact shape of the filter function is of less importance than the rise/fall time, respectively the slopes, and the width or FWHM of the pulse. In order to evaluate the performance of the filter functions, embedded in (3.34) and (3.35) for the envisaged application, we want to compare their characteristics, setting the environmental parameters to values according to the ATLAS and LHC specifications and the technological parameters to values, typical for modern bipolar/BiCMOS processes.

Table 4. Typical application parameters

Parameter	Symbol	Value
Detector Capacitance	C_d	20 pF
Peaking Time	T_p	25 ns
Detector Leakage Current	I_D	0.5 nA
Feedback Resistance	R_f	80 kΩ
Base Spread Resistance	r_{bb}	50 Ω
Amplifier Input Capacitance	C_a	0.5 pF
Current Gain	β	100
Collector Bias Current	I_C	200 μA

This set of parameter values was already used throughout most of this chapter, and will be kept for the remaining parts, unless otherwise stated. Figure 20 shows the ENC as a function of the collector current I_C according to the equations (3.34) and (3.35).

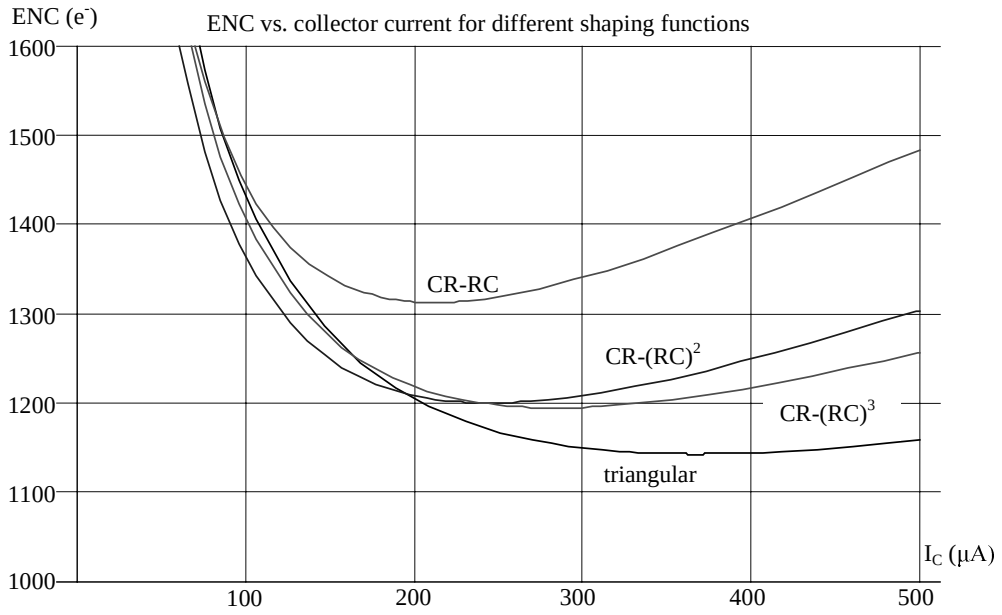

Figure 20. Comparison of the ENC functions in (3.34), (3.35) for a set of parameter values typical for the ATLAS SCT readout: ENC vs. I_c

From this plot and from the underlying equations it is clear, that there exists an optimum value for the collector bias current $I_{C,opt}$ for each filter function and set of parameters. Derivation of (3.34) for the CR-RC case yields [compare (3.23)]

$$I_{C,opt} = \frac{kT}{qT_p}\sqrt{\beta}\left(C_a + C_d\right) \qquad (3.36)$$

which gives $I_{C,opt}$ = 212 μA for the parameters of Table 4.

Another usually free parameter is the peaking time T_p of the pulse shaper, although it has to be mentioned here that a lower limit is imposed by the charge collection time in the detector (see Figure 6, Chapter 2). If the collection time is not adequately short compared to T_p, ballistic deficit may impair the measurement accuracy. For detailed discussion on ballistic deficit, refer to [24] and [48]. An upper limit to T_p is usually given by the counting rate, respectively the required double pulse resolution of the experiment (see Chapter 4). The optimum peaking time in terms of noise performance, again derived from (3.34) for the RC-CR case, can be written as

$$T_{p,opt} = \frac{\left(C_a + C_d\right)}{g_m}\sqrt{\beta\left(2g_m r_{bb} + 1\right)} \qquad (3.37)$$

The equation above gives $T_{p,opt}$ = 35.3 ns for the parameters of Table 4.

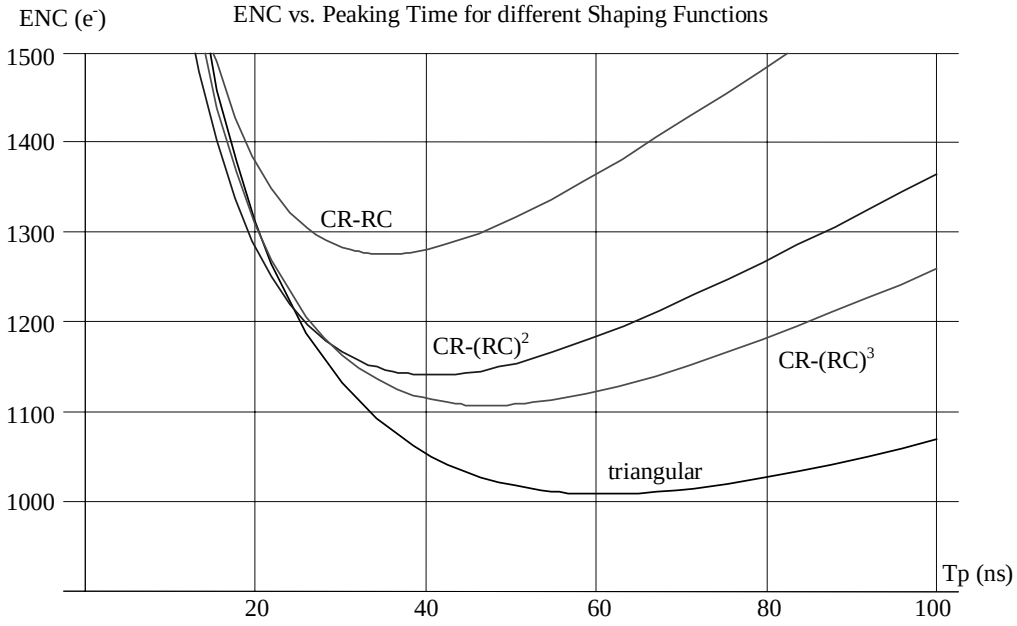

Figure 21. Comparison of the ENC functions in (3.34), (3.35) for a set of parameter values typical for the ATLAS SCT readout: ENC vs. T_p

As T_p is reduced below $T_{p,\,opt}$, the contribution to *ENC* due to voltage "series" noise dominates, while as T_p is increased above $T_{p,\,opt}$, the contribution to *ENC* from the current "parallel" noise grows in importance. Figure 22 shows how to choose the optimum I_C for a given T_p. For example, to obtain an ENC of 1200 at a peaking time of 25 ns, a collector current of at least 200 μA has to be chosen.

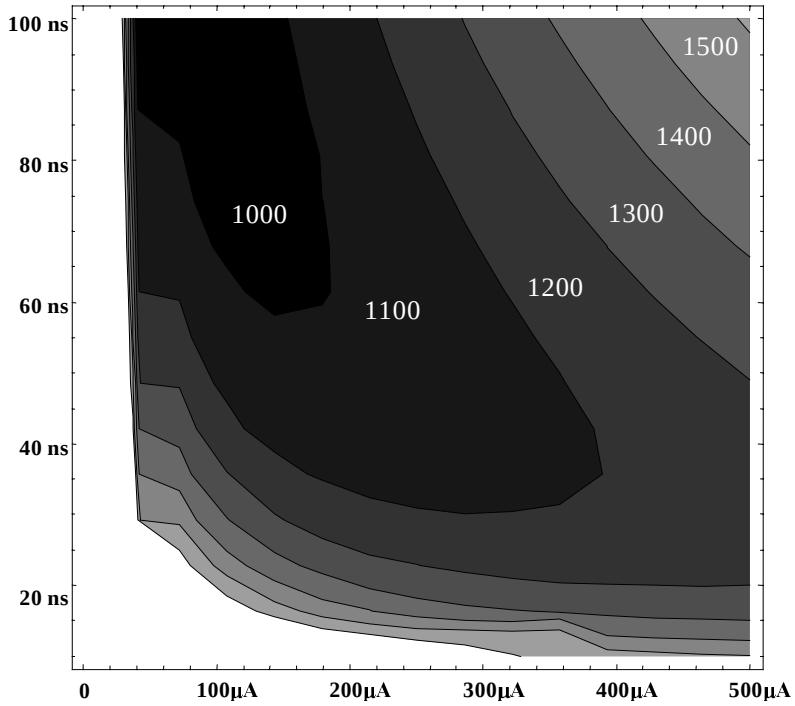

Figure 22. ENC contours versus collector current I_c and peaking time T_p.

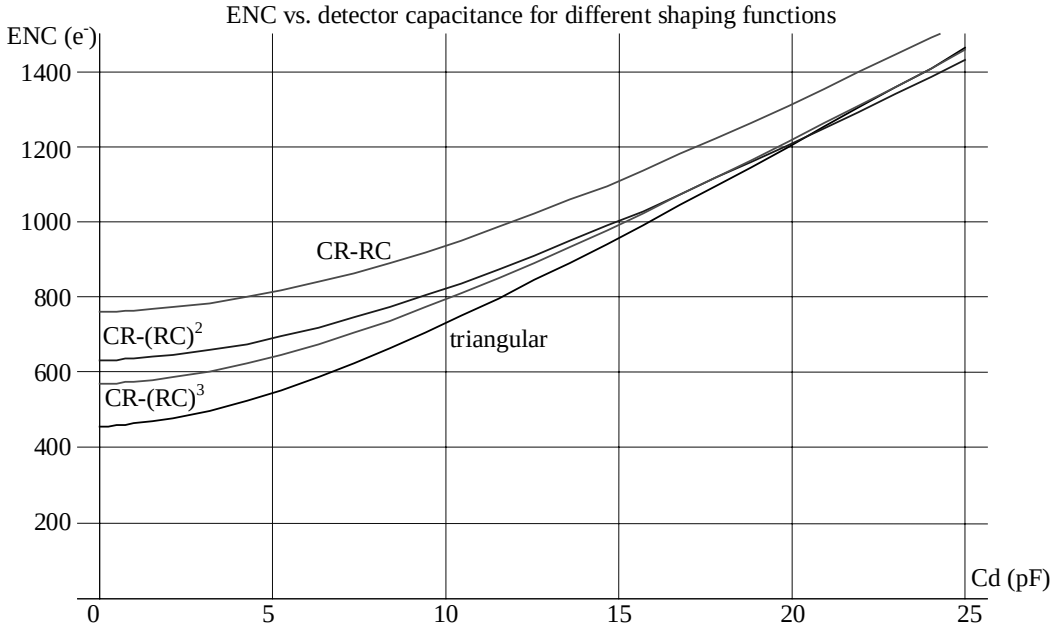

Figure 23. Comparison of the ENC functions in (3.34), (3.35) for a set of parameter values typical for the ATLAS SCT readout: ENC vs. C_d

Figure 23 plots the relation between the ENC and the detector capacitance, usually referred to as the "noise slope". This type of representation is especially expressive, because it shows the contributions of the two noise sources in a very obvious way. The "parallel" or current noise is given by the intersection of the trace with the *y*-axes, the additional noise from the "series" or voltage noise increases with detector and input capacitance.

The results, as expected, indicate that the ideal triangular shaping function suppresses noise more effectively in most cases compared to the realizable CR-$(RC)^n$ functions. The difference between CR-$(RC)^2$ and CR-$(RC)^3$ is not very large, indeed it can be shown [24], that a further increase of the RC-index *n* above 3 does not result in a substantial improvement of the noise performance. It has to be noted, that for the working point given by the parameters in Table 4, CR-$(RC)^2$, CR-$(RC)^3$ and Triangular result in a very similar ENC of ~1200 e^-.

Comparison Of Bipolar And MOS Input Device

In this section, we want to investigate, whether the MOS transistor behaves superior or inferior to the BJT in terms of noise performance as used as the input device.

The *NPN* bipolar transistor offers a higher g_m/I_c ratio and a lower input capacitance than the MOS transistor. For this reason, the *NPN* bipolar transistor is intrinsically the better input device for a low noise preamplifier when the series noise contribution dominates. For the comparison, we chose the simple triangular shaping, offering effective noise suppression for both series and parallel noise sources. Neglecting the influence of the feedback resistor and the detector leakage current in equation (3.35) leads to a simplified expression which was used in [5] for a comparison of the noise performance of front-end systems using bipolar and MOS input devices.

$$ENC = \frac{1}{q}\sqrt{\frac{4kT\left(r_{bb} + \frac{1}{2g_m}\right)\left(C_d + C_a\right)^2}{T_p} + \frac{2qI_C}{\beta}\cdot\frac{T_p}{3}} \qquad (3.38)$$

The contributions to the ENC of R_f and I_D are plotted in Figure 24. For typical values, a feedback resistance of 80 kΩ respectively a leakage current of 0.5 nA, as for a non-irradiated ATLAS type strip detectors, both contribute in the order of 30 e^- at a shaper peaking time of 25 ns, which can be neglected for most kinds of calculations.

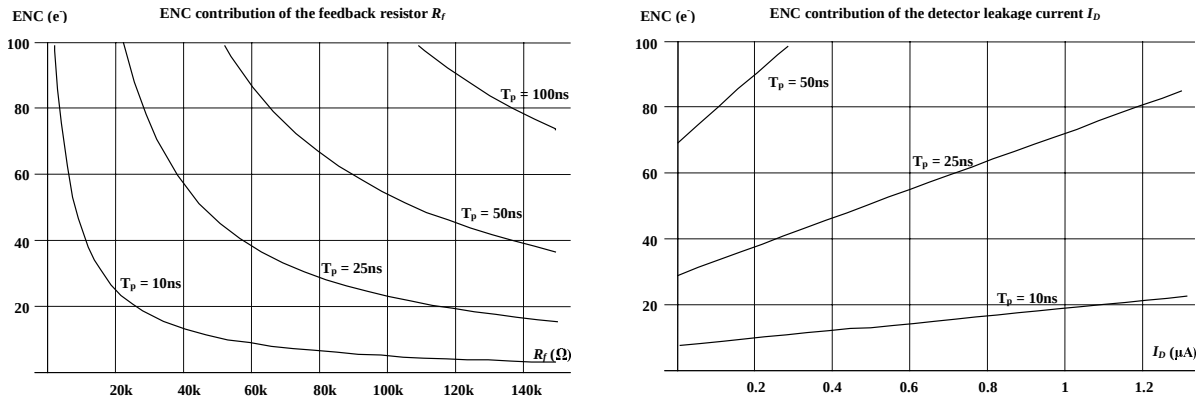

Figure 24. Neglecting the influence of feedback resistor and detector leakage current

As stated earlier, for a given peaking time, detector capacitance and current gain factor, an optimum value of the collector current can be found which results in minimum noise. Degradation of the β factor due to radiation damage of the bipolar transistors should be taken into account as this will result in some degradation of noise and a different optimum value of the collector current. The contour plot of constant ENC as a function of the collector current and β is shown in Figure 25.

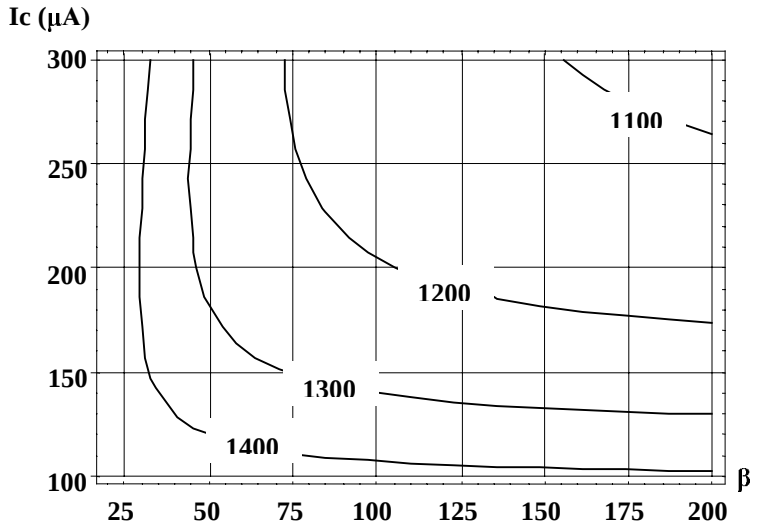

Figure 25. Contours of constant ENC as a function of the collector current I_C and gain β

The plot indicates that a noise below 1200 e^- RMS can be obtained for the usual parameter values. A degradation of β down to 50 due to irradiation causes only a minor increase in noise (up to 1300 e^- RMS).

For a MOS input device and triangular shaping the equivalent noise charge is given by [5]

$$ENC = \sqrt{4kT\frac{2\Gamma}{3g_m}(C_a + C_d)^2\frac{1}{T_p}} \qquad (3.39)$$

where g_m is the transconductance, Γ is the excess noise factor and C_a is the input capacitance of the MOS transistor. Compared with a bipolar transistor the amplifier input capacitance is not negligible since a large Width/Length ratio (W/L) for the input transistor is required to give a high transconductance. Given a minimum length allowed by the technology and short channel effect a large W/L can be obtained by increasing the width and so the total gate area. For a comparison of the noise vs. power figure of merit, it is important to notice that transconductance is proportional to collector current in a bipolar transistor while for a MOS transistor it is proportional only to the square root of the drain current. Thus for a given detector capacitance and shaping time there are two parameters, the width of the input transistor and the drain current which should be optimized in a system using MOS input transistors. The constant ENC contour plot for typical parameters of a PMOS transistor in a submicron technology is shown in Figure 26. The following assumptions were taken: Excess noise factor Γ = 1.5, effective gate length L_{eff} = 1.4μm, gate capacitance C_a = 1.5fF/μm^2, $g_m = \sqrt{2K'(W/L_{eff})I_D}$ with K' = 20 μA/V^2, detector capacitance C_d = 20 pF, triangular shaping with peaking time T_p = 25 ns.

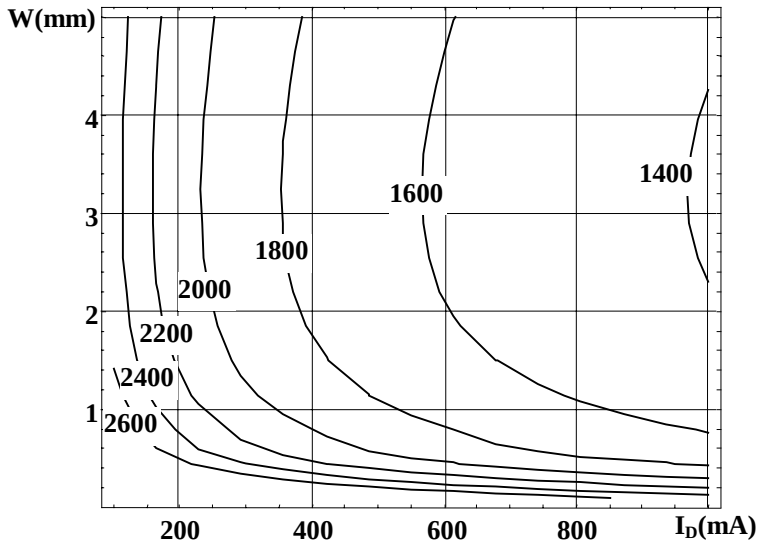

Figure 26. Contours of constant ENC as a function of the drain current I_D and the gate width.

The contour plot shows that an ENC of better than 1800 e^- RMS is achieved for a drain current of 400 µA and a gate width ranging from 2000 µm to 4000 µm. This result indicates that with a bias current twice higher in the MOS device, the minimum achievable noise is still 60% more than for a bipolar device. The lower series noise factor, 1/2 for a bipolar device compare to 1 for a p - channel MOS, and the lower input capacitance, 0.5 pF for a bipolar device and 5 pF for a large p - channel MOS input device explain this significant difference in noise performance.

A BiCMOS Front-End For Silicon Strip Detectors

The schematic of a front-end, designed for the readout of silicon strip detectors in the ATLAS Semiconductor Tracker, is shown in Figure 27. The design was done according to the specifications given in Chapter 4, and implemented in the radiation-hard DMILL 0.8μm BiCMOS process. This front-end was used in the SCT32A and SCT128B and early versions of the SCT128A readout chips.

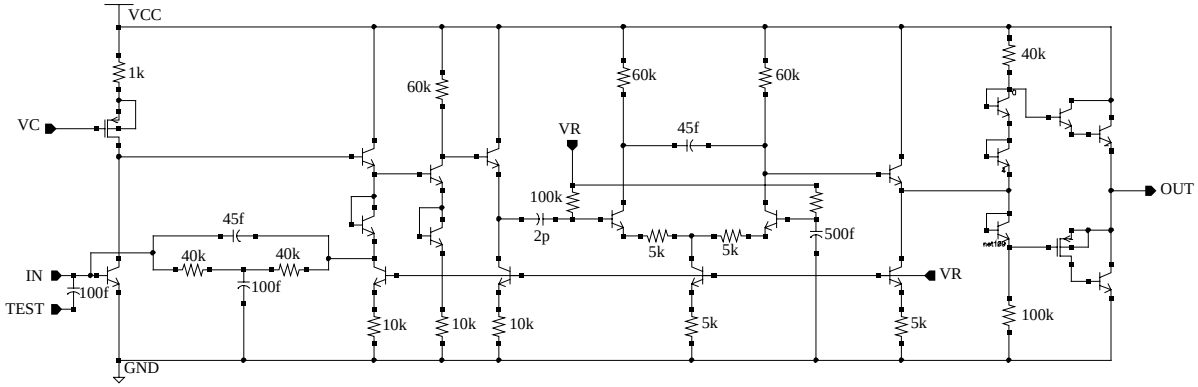

Figure 27. BiCMOS front-end for the readout of silicon strip detectors

Circuit Description

The front-end amplifier is a three-stage structure, comprising a fast transimpedance preamplifier, a differential integrator and a class AB output buffer stage. An additional gain stage is placed between pre-amplifier and shaper. All stages are separated by emitter followers.

The transimpedance pre-amplifier is built around a single ended NPN feedback pair circuit configuration, which offers a low noise characteristic as well as a sufficient gain-bandwidth product. A phase margin of about 70 degrees is achieved through a compensation network associated with the feedback resistor. The input device is a NPN bipolar transistor with an emitter area of $1.2\times20\ \mu m^2$. The load of the input transistor is built with a p-channel MOS degenerated current source, which offers a low output conductance and parasitic capacitance. A second PMOS transistor is used in the bottom branch of the push-pull output stage in order to form a PNP Darlington pair with another $1.2\times20\mu m^2$ NPN. All other transistors of the front-end are minimum size $1.2\times1.2\mu m^2$ NPN BJTs.

The input stage is followed by a single-ended gain stage with local emitter feedback and the shaper integrator, implemented with a differential pair. The circuit does not employ the ideal configuration with a transimpedance amplifier supplying a voltage step to a shaping amplifier, which contains all differentiating and integrating elements. The poles of the transfer function are introduced by all three amplifier stages so that the overall shaping function of the circuit corresponds to a triple integration, giving a transfer characteristics equivalent to a CR-RC^3 filter. Figure 28. shows SPICE simulations of the signals at the pre-amplifier output, after the gain stage and at the shaper output as a response to a 1 MIP signal, applied as a 35 mV voltage step to the on-chip 100 fF test input capacitor.

Note that these points are not accessible for measurements. The measured signal after the output buffer is compared with its SPICE simulation and an ideal calculated CR-$(RC)^3$ pulse shape, indicating that the overall response of the circuit can in fact be modeled with this function.

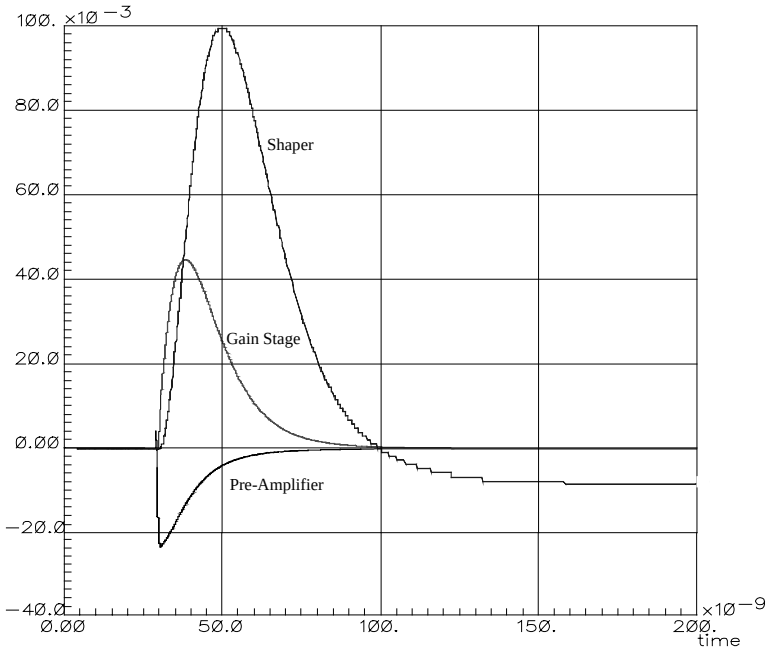

Figure 28. Simulated response of the front-end circuit to a 1 MIP input signal.

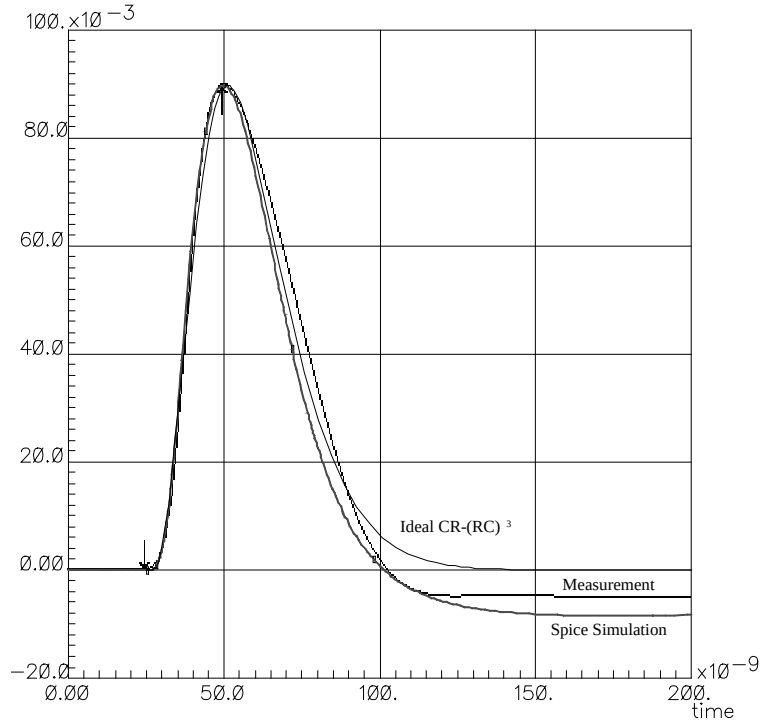

Figure 29. Pulse shape delivered by the front-end circuit.

The Input Transistor

As mentioned in the last section, a NPN bipolar transistor with an emitter area of $1.2\times20\ \mu m^2$ has been chosen for the input device. The size of the input transistor has to be optimized taking into account two effects, namely the series noise contribution from the base spread resistance and the parallel shot noise of the base current which increases after irradiation due to degradation of the current gain factor β. Radiation effects in DMILL bipolar transistors of various emitter areas have been studied ([43], [44], appendix A.2). Similar behavior of β, as observed for other bipolar technologies, has been found, i.e. the degradation of β due to radiation effects scales with the collector current density. From this point of view, a minimum geometry input transistor would be preferable, however, for such a transistor the noise originating from the base spread resistance would be significant. For the chosen geometry the base spread resistance is relatively low, of the order of 100 Ω, and β is expected to be above 50 after irradiation up to a total dose of 10 Mrad and an equivalent neutron fluence of 2×10^{14} neutrons/cm^2, as expected for the ATLAS-SCT. A chapter about the scaling of DMILL bipolar transistors and its influence on the base resistance can be found in [56].

Noise performance Of The SCT32A Front-End

The measurement of the ENC of detector readout systems is different than the general noise spectrum measurement method. One method, which was used in the characterization of the SCT32A front-end, is directly based on the definition of the ENC. The procedure starts with the measurement of the total integrated RMS noise v_{RMS} at the shaper output (or buffer output) with a RMS volt-meter or a DSO[3]. The next step is to determine the output pulse amplitude due to one elementary charge q. This is done by applying a block pulse of known amplitude V_s to a test capacitor C_T at the input of the charge sensitive preamplifier and measuring the output pulse amplitude V_o. The product of $V_s \cdot C_T$ represents the total input signal charge. Subsequently, the output amplitude due to one elementary charge q is given by $V_o / V_s \cdot C_T$ and hence, the ENC can be written as

$$ENC = \frac{v_{RMS} V_S C_T}{q V_o} \qquad (3.40)$$

The main drawback of this method is that it depends on the absolute values of the input pulse and the test capacitor. Figure 30 shows a measurement of the ENC versus collector current, done in the above-described way. For the calculation, the total input capacitance (transistor, stray capacitances, bond pad, etc.) was assumed to be 1 pF, the base resistance 100 Ω and β = 100; the shaper with a *CR-(RC)*^{3}-function and a peaking time of 25 ns. The optimum I_C for this input capacitance lies between 10 and 20 μA according to both, measured and calculated curves, showing a good agreement in this

[3] Digital Storage Oszilloscope

point. The lower measured curve assumes the test-input capacitance to be 10% below the nominal value. Note that the calculated curve rises faster with I_c than the measured one, predicting lower ENC in the region of small I_C and higher ENC after a certain point (~ 200 μA in this case) than shown by the measured results. This discrepancy will be addressed in the following section.

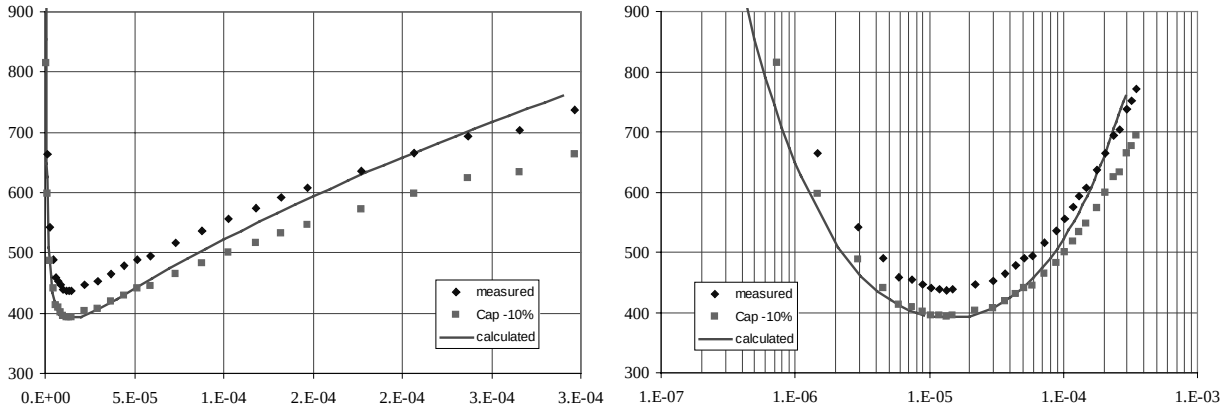

Figure 30. Measured and calculated ENC of the SCT32A front-end with floating input as a function of the collector bias current I_c (linear and logarithmic scale).

The signal amplitude and the RMS noise voltage vs. collector current are shown in Figure 31. The gain is constant over a wide range of I_c, the RMS voltage noise shows the expected behavior (compare Figure 15.)

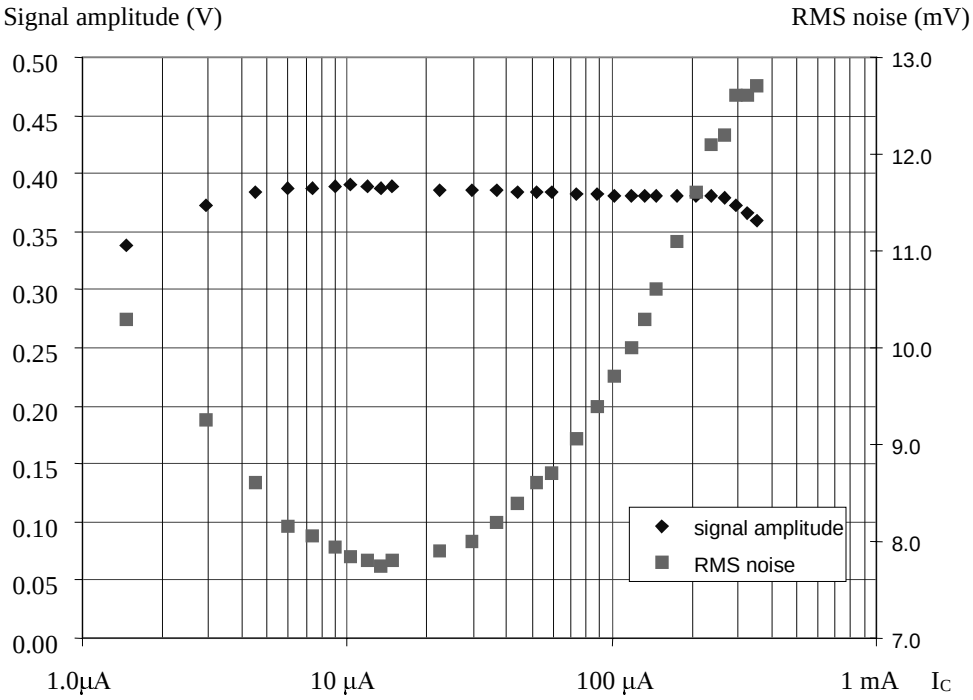

Figure 31. Signal amplitude and RMS noise voltage vs. collector current.

Noise Correlation In Front End Circuits With BJT input device

The intrinsic noise sources in a bipolar junction transistor can be modeled as two current sources in parallel with the two PN junctions (i_{n1}, i_{n2}). The contributions of these noise sources to the terminal currents can be regarded as being uncorrelated, which yields a good approximation at low frequencies. At higher frequencies, however, the correlation can produce a significant contribution to the noise and should not be neglected for accurate calculations.

For a transistor in common emitter configuration, the two noise sources can be represented by a current generator $i_{nb} = i_{n1} - i_{n2}$ in parallel with the base-emitter admittance $Y_{be} = Y_e - Y_{ce}$ and a current generator i_{nc} between emitter and collector. The noise power spectral densities are the shot noise of base and collector current respectively. The correlation term $i_{nb}^* \cdot i_{nc}$ is composed of the shot noise of the collector current proportional to the ratio of the complex HF transfer admittance Y_{ce} and its low-frequency value, the transfer conductance g_m. The frequency dependent part of Y_{ce} is proportional to the collector junction capacitance C_c.

In addition, the intrinsic junction capacitances C_c and C_e vary with the bias current in the device. The noise contribution of the noise voltage source v_{nb} in connection with the base spread resistance r_{bb} is a function of the ratio between the load capacitance C_d and the emitter junction capacitance C_e. As a consequence, the standard theory, assuming the noise term $4kTr_{bb}$ to scale linearly with the load capacitance, overestimates the noise in the range of high bias current I_C.

A theory of shot noise in junction diodes and bipolar junction transistors has been developed by *A. Van der Ziel et al.* and *W. Guggenbuehl et al.* and has been published between 1955 and 1958. [57], [58], [59] and [28]. A summary appears in *Van der Ziel's* text book [60] in 1970. The complete theory without neglecting noise correlation was first applied to a charge sensitive amplifier (CSA) with a BJT input device by *W. Dabrowski* and the results presented in 1997 [18]. In this section, we want to apply this theory to derive a complete expression for the Equivalent Noise Charge of a CSA with third order noise filtering [CR-$(RC)^3$] in a way that is consistent with the derivation of the standard expression for the ENC *(3.34)* in Chapter 3, pp. 20 – 31.

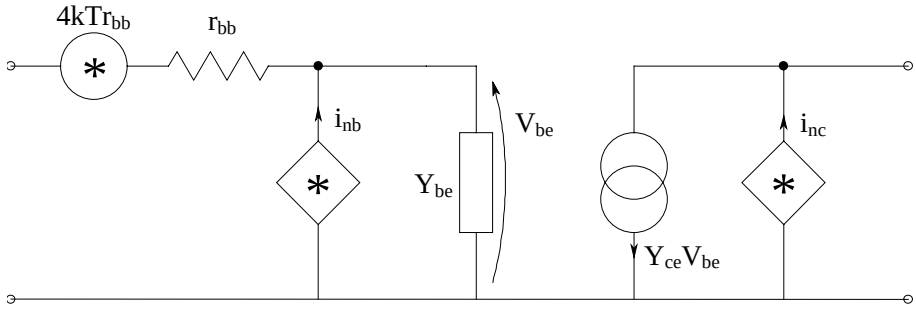

Figure 32. Equivalent circuit of common emitter transistor

The power spectral densities associated with the noise sources can be written as [18]:

$$\begin{aligned} i_{nb}^2 &= 2qI_B + 4kT\left(g_{ce0} - \mathrm{Re}\{Y_{ce}\}\right) + 4kT\left(g_{be} - g_{be0}\right) \cong 2qI_B \\ i_{nc}^2 &= 2qI_C \\ i_{nb}^* \cdot i_{nc} &= 2kT\left(Y_{ce} - g_{ce0}\right) \end{aligned} \qquad (3.41)$$

with g_{ce0} being the low frequency transfer conductance, usually referred to as the transconductance, denoted by g_m.

$$g_{ce0} = g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{kT} = \beta \cdot g_e \qquad (3.42)$$

The complex Y_{ce} will accordingly be called Y_m.

It is usually assumed, that $g_{ce0} - Y_{ce}$ and $g_{be} - g_{be0}$ are negligible, reducing *(3.41)* to Giacoletto`s equations $i_{nb}^2 = 2qI_B$ and $i_{nb}^* i_{nc} = 0$. Subsequently, we will neglect the terms in the equation for i_{nb} but not in the cross – correlation term.

The cross – correlation term in *(3.41)* can be written, replacing the noise current source i_{nc} by an equivalent noise voltage source e_{nc} with Y_m.

$$i_{nb} \cdot e_{nc}^* = i_{nb} \cdot \frac{i_{nc}^*}{Y_m^*} = 2kT\left(\frac{Y_m}{Y_m^*} - \frac{g_m}{Y_m^*}\right) \qquad (3.43)$$

Introducing the collector capacitance C_C into the small signal model of the BJT (compare Figure 10) yields the following circuit and relations:

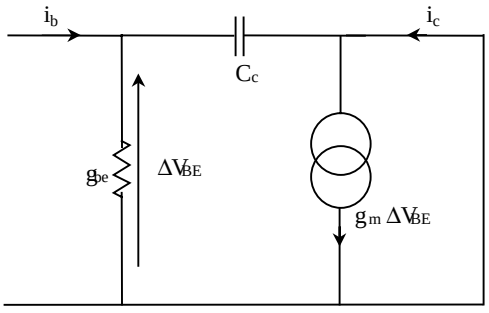

Figure 33. BJT small signal model with collector capacitance

$$i_c = \beta \cdot i_b \quad and \quad i_b = V_{be} g_{be} - V_{be}\left(j\omega C_c\right) \quad \Rightarrow \quad i_c = \beta V_{be} g_e - \beta V_{be}\left(j\omega C_c\right) \qquad (3.44)$$

The complex HF transfer conductance can be calculated therefrom:

$$Y_m = \frac{\partial i_c}{\partial V_{be}} = \beta \cdot g_{be} - \beta j\omega C_c \quad with \quad \beta \cdot g_{be} = g_m \quad \Rightarrow$$
$$Y_m = g_m\left(1 - j\omega\frac{\beta \cdot C_c}{g_m}\right) \tag{3.45}$$

Merging *(3.45)* and *(3.43)* yields the cross – correlation term

$$i_b \cdot v_{nc}^* = -2kT\frac{j\omega\frac{\beta \cdot C_c}{g_m}\left(1 - j\omega\frac{\beta \cdot C_c}{g_m}\right)}{1 + \omega^2\left(\frac{\beta \cdot C_c}{g_m}\right)^2} \tag{3.46}$$

The output noise voltage density v_{no} for a transimpedance amplifier configuration with a $R_f \| C_f$ feedback loop and purely capacitive input load can be derived from Figure 34:

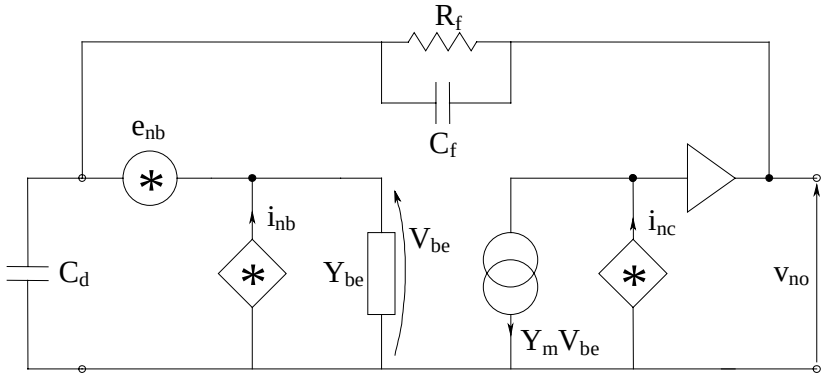

Figure 34. Transimpedance amplifier with capacitive input load C_d

$$v_{no} = i_{nb}Z_f \oplus e_{nb}\frac{Z_d}{Z_d + Z_e}\cdot\frac{Z_f}{Z_d} \oplus \frac{i_{nc}}{Y_m}\cdot\frac{Z_f}{Z_d} \tag{3.47}$$

$$Z_e = \frac{r_e}{1 + j\omega r_e C_e}, \quad Z_d = \frac{1}{j\omega C_d}, \quad Z_f = \frac{R_f}{1 + j\omega R_f C_f} \tag{3.48}$$

Inserting the impedances from *(3.48)* into *(3.47)* produces

$$v_{no}^2 = \frac{R_f^2}{1 + \omega^2 R_f^2 C_f^2}\left[i_{nb}^2 + e_{nc}^2\omega^2 C_d^2 - 2\,\mathrm{Im}\left\{i_{nb} \cdot e_{nc}^*\right\}\omega C_d + e_{nb}^2\omega^2 C_d^2\frac{1}{1 + \omega^2 r_e^2\left(C_d + C_e\right)^2}\right] \tag{3.49}$$

The noise power spectral densities in *(3.49)* are:

$$i_{nb}^2 = \frac{2qI_C}{\beta} + \frac{4kT}{R_f} + 2qI_D \qquad (3.50)$$

$$e_{nb}^2 = 4kTr_{bb} \qquad (3.51)$$

$$e_{nc}^2 = \frac{i_{nc}}{Y_m} = 4kT\frac{kT}{2qI_C} \qquad (3.52)$$

$$-2\,\mathrm{Im}\left\{ i_{nb} \cdot e_{nc}^* \right\} = 4kTr_e \cdot \frac{\omega C_c}{1+\omega^2 r_e{}^2 C_c{}^2} \qquad (3.53)$$

The resulting equivalent input noise current density is

$$i_{ni}^2 = \frac{2qI_C}{\beta} + \frac{4kT}{R_f} + 2qI_D + 4kT\frac{1}{2g_m}\omega^2 C_d^2 + 4kTr_e\omega^2 C_c C_d \frac{1}{1+r_e{}^2\omega^2 C_c^2} + \frac{4kTr_{bb}\omega^2 C_d^2}{1+r_e{}^2\omega^2\left(C_d+C_e\right)^2} \qquad (3.54)$$

The complete expression for the output noise voltage including the transfer function of a filter is given by:

$$v_{no}^2 = \frac{1}{2\pi}A^2\int_{-\infty}^{\infty}\left[\begin{array}{l}\left(\frac{2qI_C}{\beta}+\frac{4kT}{R_f}+2qI_D\right)\frac{1}{\omega^2 C_d^2} + 4kT\frac{1}{2g_m} + \\ + 4kTr_e\frac{C_c}{C_d}\frac{1}{1+r_e{}^2\omega^2 C_c^2} + \frac{4kTr_{bb}}{1+r_e{}^2\omega^2\left(C_d+C_e\right)^2}\end{array}\right]\left|H(j\omega)\right|^2 d\omega \qquad (3.55)$$

The noise power spectral densities go into an equation of the type of *(3.28)*:

$$ENC = \frac{\left\{\frac{1}{2\pi}\int_{-\infty}^{\infty}\left(e_n^2 C_d{}^2 + \frac{i_n^2}{\omega^2}\right)\left|H(j\omega)\right|^2 d\omega\right\}^{\frac{1}{2}}}{\max L^{-1}\left[\frac{H(s)}{s}\right]} \qquad (3.56)$$

We use the filter transfer function of a $CR-(RC)^3$ shaper (Table 3)

$$\left|H(j\omega)\right|^2 = \frac{\omega^2\left(T_p/3\right)^2}{\left(1+\omega^2\left(T_p/3\right)^2\right)^4} \qquad (3.57)$$

and solve the definite integrals. The result is an expression for the ENC of a bipolar front-end with a CR-$(RC)^3$ – shaper, considering correlation of the BJT noise current sources i_{nb} and i_{nc} *(3.58)*:

$$ENC = \frac{e^3}{36q}\left[\begin{array}{l} 2kT\frac{kT}{qI_C}C_d^2\frac{3}{T_p} + \left(\frac{2qI_C}{\beta} + \frac{4kT}{R_f} + 2qI_D\right)\frac{5T_p}{3} + \\ + 4kTr_{bb}\frac{3C_d^2q^2I_C^2T_p}{\left(3\beta kT(C_d+C_e)+qI_CT_p\right)^4}\left(45\beta^2k^2T^2(C_d+C_e)^2 + 12\beta kTqI_CT_p(C_d+C_e) + q^2I_C^2T_p^2\right) + \\ + 4kTr_e\frac{3C_cC_dq^2I_C^2T_p}{\left(3\beta kTC_c+qI_CT_p\right)^4}\left(\left(6\beta kTC_c+qI_CT_p\right)^2 - \frac{27\beta^3k^3T^3C_c^3}{q^2I_C^2T_p^2}\left(3\beta kTC_c+4qI_CT_p\right)\right) \end{array}\right]^{\frac{1}{2}} \quad (3.58)$$

Junction Capacitances And Current Gain As Functions Of The Collector Current

Until now, the amplifier input capacitance C_a and the current gain β were considered constant. In reality, all capacitances as well as the current gain are dependent on the DC conditions in the device.

The two junction depletion capacitances C_c and C_e vary with the DC potential between the terminals. In the forward active region, the C-B junction is a reverse biased diode while the E-B junction is a forward biased diode. The voltage dependence for the collector junction depletion capacitance C_c therefore is that of a reverse biased diode.

$$C_c = \frac{C_{jc0}}{\sqrt[m]{\left|1 - \frac{V_{CB}}{V_{bic}}\right|}} \quad (3.59)$$

where C_{jc0} is the capacitance of the zero biased junction, V_{bic} the intrinsic potential of the B-C junction and m a doping factor (1/3 for linear, 1/2 for uniform doping).

The expression for the E-B junction capacitance is similar with identical definitions for the parameters.

$$C_e = \frac{C_{je0}}{\sqrt[m]{\left|1 - \frac{V_{EB}}{V_{bie}}\right|}} \quad (3.60)$$

As the E-B junction is a forward biased junction, it has, in addition to the depletion capacitance, a diffusion capacitance like any forward biased diode. From the known expression for a diffusion capacitance $C_D = G_0(\tau_p/2)$, we find for the E-B diffusion capacitance the following relation:

$$C_b = \frac{qI_E}{kT}\tau_t \cong g_m\tau_t \quad (3.61)$$

where τ_t is the base transit time, the average time it takes a minority carrier to traverse the base region on its way to the collector.

The capacitance C_π between the intrinsic base and the emitter is the sum of the depletion and the diffusion capacitances $C_\pi = C_e + C_b$, the total input capacitance at the base terminal is given by $C_{inb} = C_\pi + 0.6 \cdot C_c$. For the amplifier input capacitance, the sum of C_{inb} and the feedback capacitance, as a function of the collector current, we find:

$$C_a(I_C) = C_f + \tau_t \cdot \frac{qI_C}{kT} + \frac{C_{je0}}{\sqrt[3]{1-\frac{V_{EB}}{V_{bie}}}} + 0.6\frac{C_{jc0}}{\sqrt{1-\frac{V_{CB}}{V_{bic}}}} \qquad (3.62)$$

The relations $V_{EB}(I_C)$ and $V_{CB}(I_C)$ need to be found for each circuit individually. In case of the SCT32A front-end, one can make the following assumptions:

$$V_{CB}(I_C) \cong 2V_T + \frac{I_C}{\beta} R_f \qquad (3.63)$$

$$V_{EB}(I_C) \cong V_T \qquad (3.64)$$

All parameters, which are necessary to evaluate *(3.62)* can be found in the SPICE model delivered by the foundry for each process. Figure 35 shows the total amplifier input capacitance as a function of the collector current for the SCT32A front-end.

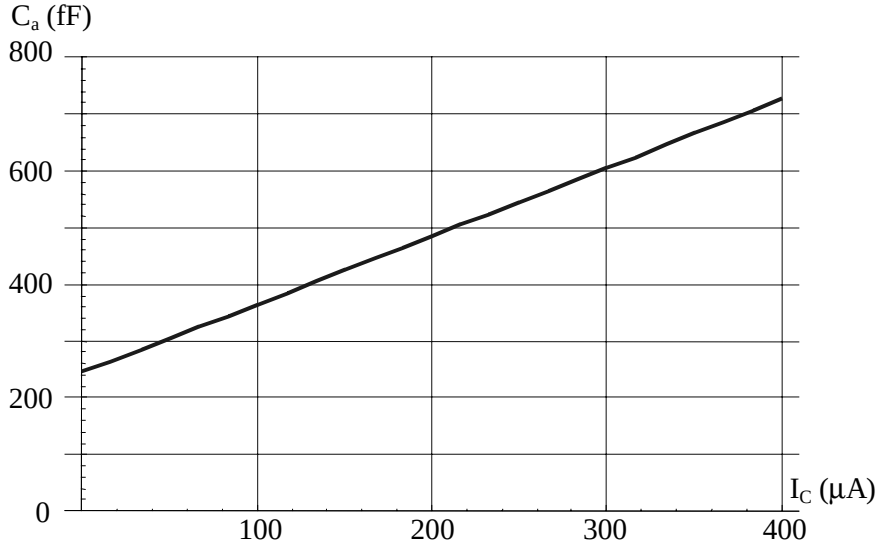

Figure 35. Amplifier input capacitance as a function of the collector current [equation (3.62)]

A model for the current gain $\beta(I_C)$ was derived from measurements on 10 samples of the actually used input transistor by taking the average over the 10 sets of parameters that were fitted to the measured curves. It was found, that for the interesting region of collector current 1 µA – 400 µA, the gain can very accurately be modeled by simple logarithmic functions in two sub-regions:

- Region 1: Ic [1uA – 40uA]: $\beta(I_C) = 0.87 \cdot Ln(I_C) + 110.9$
- Region 2: Ic [20uA – 400uA]: $\beta(I_C) = 1.41 \cdot Ln(I_C) + 116.5$

ENC Considering Noise Correlation And Capacitance Scaling

Now we can compare the expressions for ENC with and without consideration of noise correlation and capacitance scaling [equations *(3.34)* and *(3.58)*]. Figure 36 shows the ENC curves at three different detector capacitances for I_C from 10 µA – 300 µA, while Figure 37 plots the region of higher collector current from 100 µA – 2mA. The graphs indicate the following effects.

First, the extended equation gives wrong results in the region of low current densities, because some assumptions apply only for high current injection (refer to [28] and [57] – [59]). The correlation term [the last term in equation *(3.58)*] becomes dominant and goes negative below a certain value of I_C. Assuming the parameters of Table 5, the correlation model yields sensible results above a current of ~ 50 µA.

Second, for zero load capacitance, both models yield almost identical results above a certain I_C (~30 µA for the parameters given in Table 5). The difference becomes more and more significant with increasing C_d. This behavior is predictable, as with C_d decreasing to zero, all "series noise" – terms, including the correlation term, become negligible. The remaining "parallel noise" – term is identical in both models.

Third, at a certain current, depending on the value of the load capacitance, the positive contribution due to the correlation and the negative effect of the decreasing ratio of C_d and C_e cancel out. Above this point, the correlation model yields lower noise than the standard theory, because the decrease of noise contribution from the base spread resistance becomes the dominant effect.

Summing up, it can be concluded that in the region of small currents and load capacitances, the standard theory underestimates the noise because it does not consider the correlation of the intrinsic noise sources. At higher currents and load capacitances on the other hand, the noise is overestimated due to the assumption of linear scaling of the base resistance noise with load capacitance.

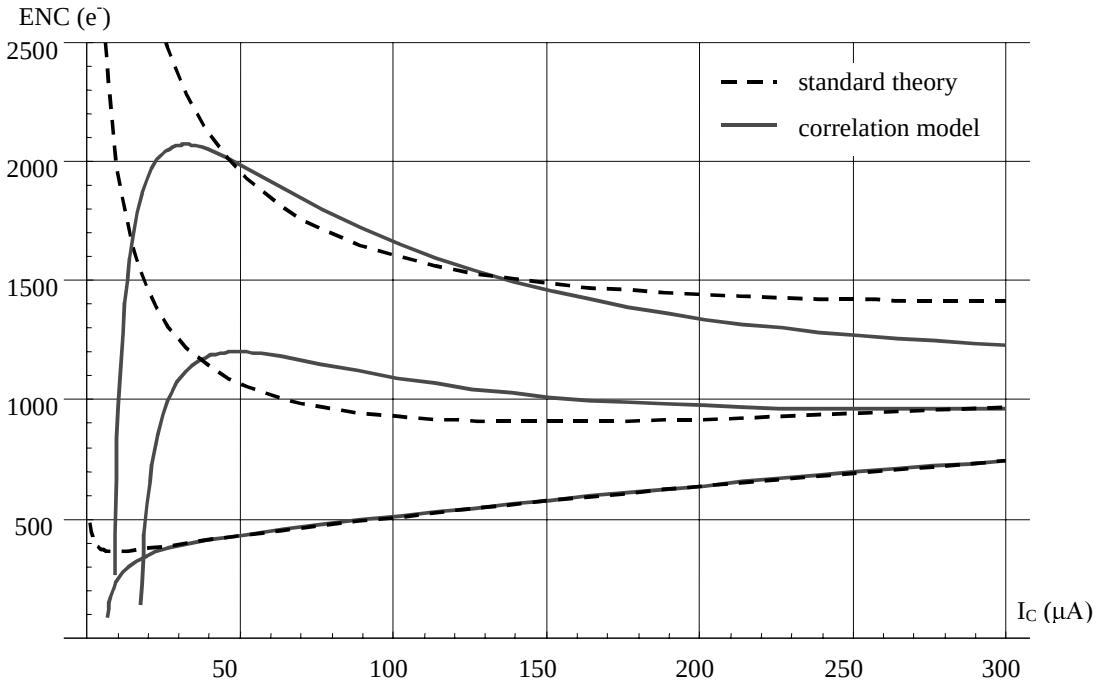

Figure 36. ENC vs. I_C for C_d = 0.1, 10 and 20 pF – low current region

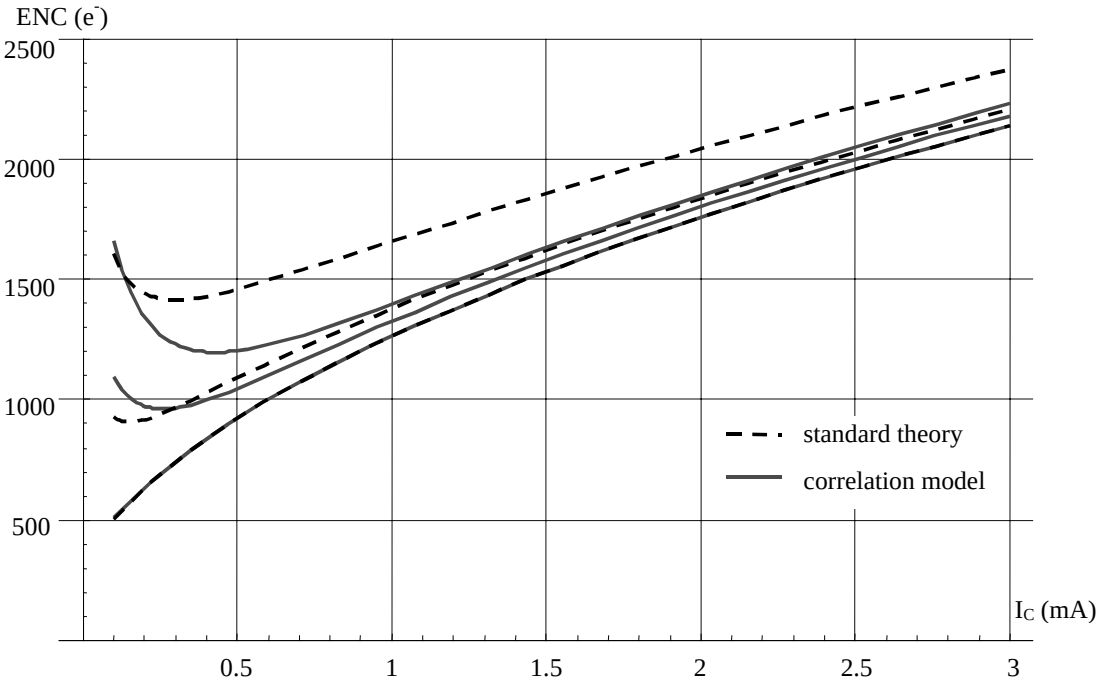

Figure 37. ENC vs. I_C for C_d = 0.1, 10 and 20 pF – high current region

The plot in Figure 37 shows the region of higher currents. The ENC function without correlation overestimates the noise, while in the region of moderately small collector current and detector capacitance, the extended function yields higher noise.

The above discussed behavior can also be observed by looking at the "noise slope". Figure 38 plots the ENC as a function of the detector capacitance for both expressions at I_C = 160, 200 and 260 µA. The correlation expression yields the more or less straight lines. Again, the standard theory predicts lower noise in the region of low capacitance than the correlation theory. At a certain point, depending on the current, the curves cross and from this point on, the standard theory rises faster and predicts higher ENC than the correlation model. In Figure 38, the crossover points are indicated by the vertical lines at 11.2 pF, 14.2 pF and 17.2 pF.

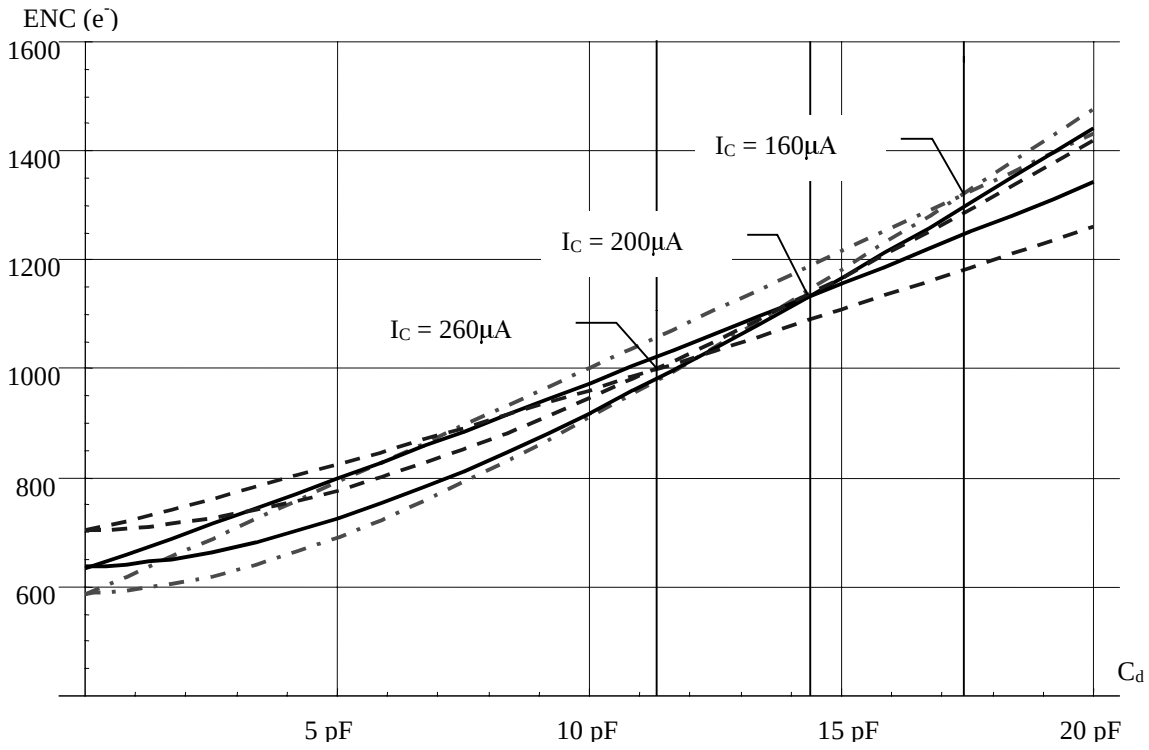

Figure 38. Noise slope: ENC vs. C_d for I_C = 160, 200, 260 µA

In order to evaluate the quality of the noise correlation model, we want to compare the predictions of both, the simple standard theory and the noise correlation extension, with actual measurement results.

Comparison With Experimental Results

Figure 39 shows the results of measurements on the SCT32A front-end from Figure 30. For values of I_C above 50 µA, the correlation theory achieves a clearly better agreement with the experimental results. The calculation was done, assuming a 600 fF additional capacitance at the input due to interconnects and bond pad. Also for the noise slope of Figure 40, which was measured with discrete capacitances at a collector current of 220 µA, the better agreement between results and theory using the correlation model is obvious.

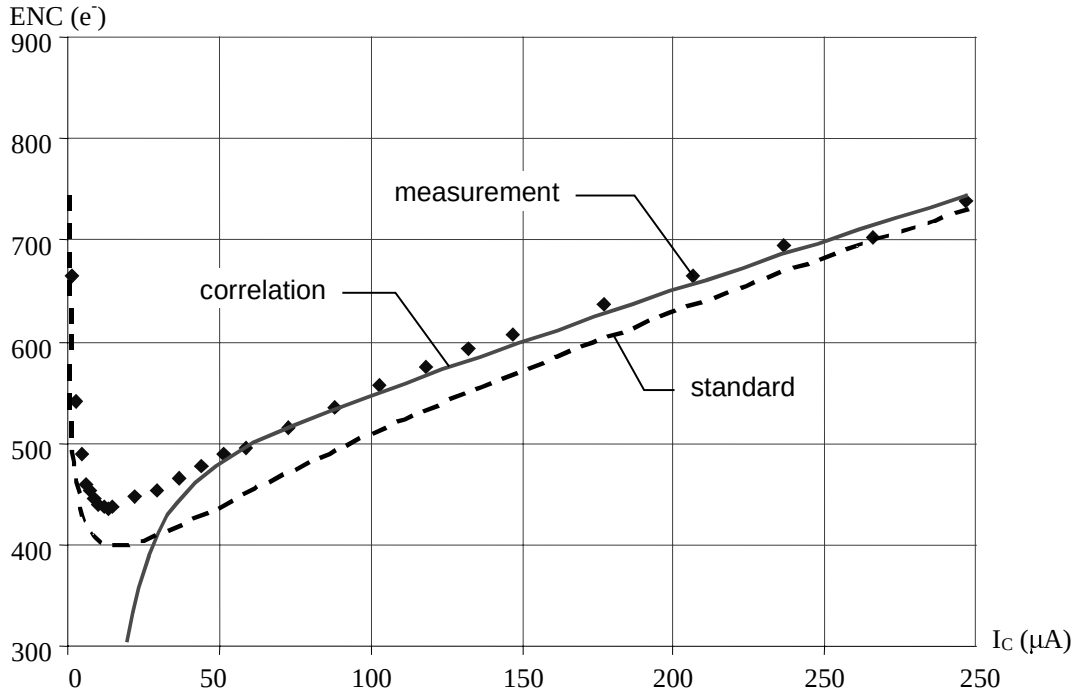

Figure 39. ENC vs. I_C of the SCT32A front-end (compare Figure 30).

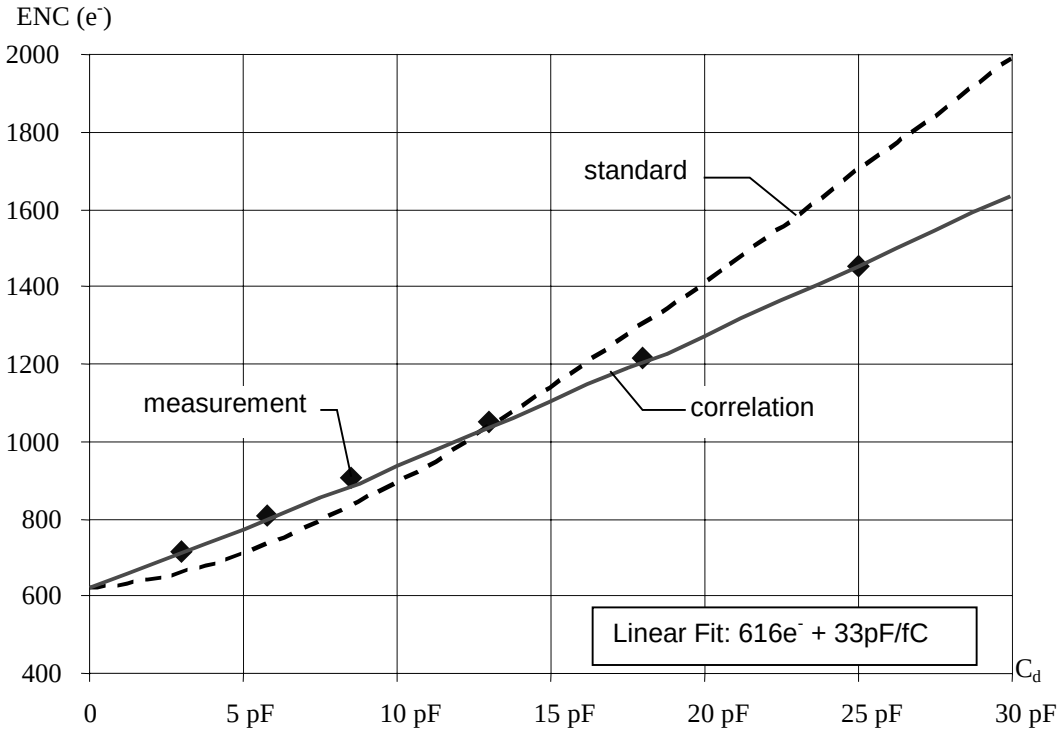

Figure 40. Noise slope of the SCT32A front-end measured at I_C = 220 μA

For all calculations in this section, the following set of parameters was used. The transistor parameters are taken from the SPICE model delivered by the foundry TEMIC.

Table 5. Transistor and circuit parameters and constants used in the above calculations

Parameter	symbol	value
Zero biased collector junction capacitance	C_{jc0}	164 fF
Zero biased emitter junction capacitance	C_{je0}	68 fF
Base spread resistance	r_{bb}	100 Ω
Minority carrier base transit time	τ_t	$32 \cdot 10^{-12}$
Feedback resistor	R_f	80 kΩ
Feedback capacitor	C_f	45 pF
Elementary charge	q	$1.602 \cdot 10^{-19}$
Boltzmann constant	k	$1.38 \cdot 10^{-23}$
Temperature	T	300 K
Shaper peaking time	T_p	25 ns
Detector leakage current	I_D	400 nA / 786

Chapter 4

A Readout ASIC For Silicon Strip Detectors In LHC Experiments

Read Out Electronics For LHC Experiments - System Aspects

This section describes the requirements and the specifications for the on-detector electronics in terms of environmental and system conditions for the use of the device within a large experiment like ATLAS/LHC. Subsequently, a 128-channel analog readout ASIC for semiconductor detectors is being presented and design and functionality described in detail. The chapter concludes with results of functionality tests and performance measurements carried out on the chip in a laboratory environment as well as using CERNs particle beam facilities. An absolute calibration of the front-end amplifier with monochromatic photons allows an accurate determination of the signal charge, released by a MIP in the Silicon strip detectors foreseen to be used within ATLAS SCT.

As mentioned in Chapter 1, the ATLAS Inner Tracker will contain ~ 20.000 silicon strip detectors covering an active silicon area of ~ 63 m^2. This leads to a total of ~ 6.5 million detection elements and the same amount of electronics channels. At the LHC bunch-crossing rate (BCO rate) of 40 MHz, an enormous amount of data is being produced which can be neither transmitted nor stored at this speed. From a particle physics point of view, most of these data will not contain “interesting” events[1]. The task of the read out electronics is on one hand to read the charge signals from the silicon strip detectors and convert them into a transmittable format, and on the other hand to reduce the amount of data being transmitted without losing interesting information.

The data reduction is done in conjunction with the trigger, which monitors incoming data from the different sub-detectors for “interesting” events[2]. The Level 1 Trigger (L1), the first of three trigger levels in ATLAS, is designed to reduce the event rate from the 40 MHz BCO rate to a rate of ~100kHz. The trigger latency, which is the time between a BCO and the corresponding L1 decision (event to be read out or not), has a fixed value of 2.5 μs. Thus, the device needs to store all of the data,

[1] An interesting collision will occur at a rate of ~100kHz.
[2] No data from the tracker are used for the L1 trigger generation.

which come in permanently at a rate of 40 MHz, for at least the time of the trigger latency. After that, the data are either transmitted off-detector or discarded. A data storage or memory structure, subsequently referred to as the pipeline, is therefore a crucial part of the device. The pipeline must be capable of storing at least 100 events. General ATLAS design considerations have resulted in the necessity of a deadtime-less readout, which forces simultaneous read-write operations on the pipeline.

The average L1 trigger rate can be estimated, while the exact time (BCO) of occurrence is stochastical. As described later, the transmission of the data of one event to the outside world takes much longer than the minimum possible time distance between two L1 events[3]. That means that a L1 trigger can occur during a data transmission cycle or even before the data of the last L1 accepted event started to be sent off. A second storage facility, which holds the data of several L1 accepted events, or at least pointers to this data, is necessary. This device, called de-randomizing buffer, is a FIFO type storage. It can be shown that a memory depth of 8 locations is sufficient to meet the ATLAS specification of 99% efficiency[4] [29].

The transmission of the data corresponding to L1 trigger accepted events from the tracker to the first data processing stage off-detector will be carried out using optical links. In order to reduce the amount of fibers, a certain number of channels are time multiplexed and put out in series. It is foreseen to use the LHC machine clock to control the multiplexers which leads to a time slot of 25 ns per channel. Thus, the transmission of a 256 channel data packet would take approximately 6.4 μs, which lies well beyond the L2 data acceptance[5] rate of 100 kHz. Each data packet has to contain additional information in order to relate it to a specific event. The backend protocol uses the BCO number and the L1 trigger number to supply a unique distinctive feature for the event builder.

Nature of silicon strip detectors necessitates that the read out electronics is mounted immediately at the detector electrodes. This indicates that the electronics, sitting in the active volume of the detector, must be of low mass. The available space and the power consumption per electronics channel is strictly confined; the power dissipation per channel is specified to be <3.8mW. Inaccessibility of the readout electronics requires high reliability and a certain amount of redundancy wherever possible to minimize the amount of data loss due to single point failure.

One of the most prominent technological challenges to the design of the readout electronics is the radiation environment within the ATLAS inner tracker. The expected radiation dose for the planned lifetime of the experiment of 10 years corresponds to $2 \cdot 10^{14}$ 1MeV-equivalent neutrons/cm^2 and 10 Mrad(Si) of ionizing radiation respectively in proximity of the collision point. Electronic components used in this environment have to survive effects (displacement damage, ionization) due to these radiation doses without significant degradation in performance.

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[3] The minimum time between two positive L1 trigger decisions is specified 2 BCOs (or 50 ns).
[4] Not more than 1% of the events may be lost due to data overflow.
[5] The Level2 trigger uses tracker data.

As no commercially available devices can meet all the above listed requirements, the design of ASICs (Application Specific Integrated Circuits) is a necessity. Table 6. summarizes the requirements for the on-detector readout electronics for silicon strip detectors in the ATLAS semiconductor tracker.

Table 6. Summary of silicon strip readout electronics requirements for the ATLAS SCT:

- The characteristics of the input signal and the electrical properties of the detector such as leakage current and detector capacitance require an input stage with certain attributes.
- The performance of the input stage has to meet certain criteria in terms of speed and signal-to-noise ratio (SNR).
- Data storage and reduction has to be accomplished according to the boundary conditions given by the system parameters BCO rate, L1 trigger rate, L1 trigger latency, L2 data acceptance rate and efficiency.
- The data transfer to the first data processing stage off-detector requires time multiplexing. Data format and protocol have to be implemented in accordance to the ATLAS data acquisition system.
- The operating environment imposes additional requirements in terms of radiation hardness, power consumption, operating temperature, size and channel density.

Basic Readout Architectures Proposed For ATLAS

Several architectural options are being investigated for the ATLAS SCT on-detector electronics. Two important issues determine the overall concept of the readout system: Whether or not to use pulse height information from the Silicon strip detectors and how to divide the necessary functionality between on-detector and off-detector electronics.

The present baseline architecture is the binary readout scheme, while the analog scheme is developed in parallel as a fall back (forward, sideways) solution. The digital readout scheme, incorporating the Analog-to-Digital conversion into the front-end chip, is no longer a candidate for being used within the ATLAS tracker. In the following sections a short description of the binary and the analog readout scheme plus a performance and feasibility comparison is given.

The Binary Readout Architecture

The analog front-end chain in the binary solution consists of an input amplifier, a noise filter (shaper) and a discriminator, providing only hit/no-hit information from the strips for a given beam crossing. The binary data are stored in a clock driven digital pipeline for the time of the L1 trigger latency. The position resolution is essentially given by the geometrical patterning precision of the silicon detector and does not rely on analog amplitude interpolation.

Efficiency and occupancy are determined by the signal-to-noise ratio of the amplifiers and threshold uniformity of the discriminators. The binary architecture needs to provide a sufficiently high signal-to-noise ratio in order to avoid noise hits and to keep the discriminator threshold low and the

efficiency high. Any threshold non-uniformity effectively adds to the system noise. One of the major concerns of the binary readout scheme is the vulnerability of the system due to common mode noise, which cannot be taken care of by the offline data analysis as it is the case for analog readout.

System performance monitoring becomes less transparent, however it has been demonstrated successfully that pulse height information and noise measurements can be obtained by scanning the discriminator threshold [21].

The Analog Readout Architecture

The analog readout scheme stores the full pulse amplitude information in an analog storage implemented as a switched capacitor array. The front-end chain contains the same components as the binary architecture with the discriminator replaced by a sampling buffer that drives the analog signal to the storage cells. The most obvious advantage of the analog approach is the direct access to pulse height information, which allows in principle for more flexible data processing, in particular for corrections of gain and pedestal[6] variations and for common mode noise.

The nature of silicon strip detectors implies possible charge sharing between neighboring strips due to diffusion[7] and particles crossing the detector plane under an angle other than orthogonal. This results in a distribution of the signal charge onto two or more adjacent strips (cluster) and therefore a reduced signal amplitude for the single strip. The influence of charge sharing on spatial resolution as well as signal-to-noise ratio depends on the chosen readout architecture.

In this section, some important features of the analog readout of silicon detectors and particular reasons for the use of the analog solution within the large LHC experiments like ATLAS will be covered.

Readout of the full signal charge

A hit is recorded, when the signal at one strip exceeds a certain threshold, which is usually defined in multiples of the RMS system noise σ. A commonly used value for the "seed cut" (the threshold above which a signal is regarded to be the main part of a cluster) is 4 σ. The signal at the neighboring strips is then examined whether they contain charge originating from the same particle incident and have to be added to the cluster (the threshold for neighboring strips is usually set to 2σ). The signals from all strips are finally added and divided by the single strip noise, giving the cluster signal-to-noise ratio. In addition, a cluster threshold, which is higher than the individual trigger

[6] DC baseline of each readout channel.

[7] During the drift towards their respective potentials in a silicon detector, electrons and holes diffuse through multiple collisions. The charge distribution of a MIP in 300 μm silicon shows a Gaussian-like shape with a FWHM of 5–10 μm. For a detector of a strip pitch larger than the diffusion width, the position information is achieved by one strip responding to the hit. The resolution is then given by a rectangular distribution with $\sigma = p/\sqrt{12}$ where *p* denotes the pitch (distance between two strip implants) of the detector (typically 50-80 μm). σ is the maximum spatial resolution which can be achieved using the binary readout architecture.

threshold, can be added. That results in a reduction of the noise occupancy, compared with a single threshold method, with no loss in efficiency. An additional feature of the cluster analysis is the identification and possible suppression of excessively large clusters which can be caused by δ electrons or shallow tracks and which are generally useless events for the track reconstruction. Reference [42] gives a detailed description of the treatment of experimental raw data in terms of clustering and cut thresholds.

Spatial resolution

Making use of the pulse height information, provided by the analog readout architecture, it is possible to extend the maximum achievable binary resolution[7], which is limited by the geometrical properties of the detector, by applying "centroid"-finding algorithms to the signal distribution pattern. This charge distribution over multiple strips can be used to calculate the location of the particle hit much more precisely, thus highly enhancing the spatial resolution. Introduction of capacitive or resistive coupled intermediate strips[8] further enhances the resolution without increasing the number of readout channels. The effect of these additional strips is to linearize the charge sharing and make the centroid finding more precise. Using analog readout, a spatial resolution of < 1 μm was obtained with 50 μm readout pitch detectors having one intermediate strip [15]. Conversely, assuming a given resolution specification, the number of readout channels in the analogue architecture can be reduced compared with the binary case. One disadvantage of charge sharing in this context is that some charge is always lost by capacitive coupling to the backplane, which may affect the efficiency. Detailed descriptions of charge sharing, intermediate strips and effects on spatial resolution can be found in references [6], [7], [15], [19], [20], [23], [46], [47]. An overview over centroid finding algorithms is given in [48], the commonly used *eta*-algorithm is described in detail in [7].

Monitoring of the detector performance

Perhaps the primary reason for advocating analogue readout at LHC is the fact that it is conservative with regard to safety. The risk of losing segments of the detector due to radiation damage is real and yet not well quantified. Analogue readout allows for continuous monitoring of the detector performance during the normal running of the experiment. Regions of high leakage current, dead areas or 'microdischarges' can immediately be discovered.

The analog solution is also relatively insensitive to many of the processing variations, which would disable the binary option completely. Pedestal and gain variations and common mode pick-up can be corrected for at the off-detector electronics level or even in off-line data analysis, provided that the dynamic range of data transmission and AD conversion are set accordingly [49].

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[8] Intermediate strips are normal, properly biased strip implants which are just not connected to a readout channel.

Pattern recognition

Pulse height information may be used to discriminate against unwanted events, such as δ rays which are emitted and then impact the detector again due to the magnetic field, or the above mentioned internal δ electrons which cause artificially large clusters. The information may also be used to see hits on top of 'loopers' or shallow tracks, which cause many strips to exceed the seed cut. In stiff, dense track regions, a calorimetric approach may be taken to count the likely number of particles, even if they cannot be individually separated [49].

Table 7. Advantages and features of the analog readout architecture

- Signal charge is fully collected by reading out every strip in a cluster, thus maximizing the signal-to-noise ratio.
- Resolution is enhanced for a given strip pitch, respectively the number of channels may be reduced for a given resolution
- Monitoring of the detector behavior is transparent and continuous.
- Pattern recognition is enhanced by using pulse height discrimination algorithms

An Analog Readout ASIC For LHC: SCT128A

This section gives a detailed description of an analog readout ASIC for silicon strip detectors, designed to being used within the ATLAS Inner Tracker. Conception, establishing of the specifications and design of the chip were done according to the above mentioned requirements. After an outline of the chip architecture, experimental results and data of functionality tests and performance measurements are presented. A section concerning ASIC design techniques can be found in Chapter 5.

Specifications

The tables below list the functional and electronical specifications for the final 128 channel ATLAS SCT analog readout chip. They consist of a mixture of parameters, which are strictly imposed by the LHC data and of parameters that are derived from the experiment and the environmental conditions.

Table 8. SCT128A - basic functional specifications

Requirement	**Associated parameter**	**Specification**
Synchronous sampling of analog data at LHC BCO frequency for 128 input channels	Min. clock speed	40MHz
	Channels / readout chip	128
Selective (sparsified) readout of analog pulse height values to a single serial output port	Pipeline length	128 locations
Minimum event loss due to data overflow	de-randomizing buffer	8 locations
	Efficiency	99%
Duration of one readout cycle shorter than the average time between two L1 trigger events	Maximum average L1 trigger rate	100kHz
	Minimum output MUX clock	40MHz
Double pulse resolution according to minimum L1 trigger spacing	Minimum L1 trigger spacing	2 BCOs (50ns)
	Two consecutive 35fC signals: resolution	50ns
Simultaneous read/write operation	Dead time	0
All signals of interest must be correlated to the correct BCO	Time tag resolution	1 BCO
Environment	Voltage compliance	± 5% of nominal
	Operating temperature	± 2.5 °C of nominal
	Functionality temperature range	-15 °C to +30 °C
	Power dissipation	< 3.8 mW / channel
	Radiation total dose	$2 \cdot 10^{14}$ neutrons/cm^2 10 Mrad (Si)

Table 9. SCT128A - additional functional specifications

Minimum number of external control signals: One clock input, one serial interface port for trigger and commands (LVDS standard)
Programmability of internal biasing conditions and operation modes through serial communication port
On chip generation of test pulses (0.5 – 16 fC) to each channel (calibration mode)
Readout of 4 and 8 consecutive cells of the pipeline
Output multiplexer speed adjustable (main clock divided by 1, 2, 4, 8)
Attachment of trigger L1 number, BCO number and FIFO overflow flag to each data packet
Testability: Additional output pads for evaluating performance of the bias DACs, status of internal registers, status of the command decoder

Table 10. SCT128A - analog specifications

PARAMETER	SPECIFICATION
Preamplifier type	Transimpedance amplifier
Pulse shaper (noise filter) type	semi gaussian (CR-RC type)
Shaper peaking time	25 ns
Dynamic Range (linear response)	16 fC (~ 4 MIPs)
Coupling detector-readout channel	AC
Nominal detector capacitance (C_d)	20 pF
Noise @ C_d	< 1500 e^- RMS

Architecture And Basic Principles

The SCT128A comprises five basic building blocks: front-end amplifier, analogue pipeline, control logic for the pipeline including a derandomizing FIFO buffer, command decoder and output multiplexer. Three 5-bit D/A converters for the biasing of the analog part (front-end amplifiers) of the chip have been implemented, one 8-bit DAC controls the internal calibration circuit. The front-end circuit is a fast transimpedance amplifier followed by an integrator, providing a semi-gaussian shaping with a peaking time of 25 ns, and an output buffer. The peak values are sampled at 40 MHz rate and stored in the 128 - cell deep analog pipeline. The readout sequence is initiated by an L1 trigger transmitted through the command lines in coded format. Once the trigger signal arrives, the pointed physical address of the 128 - channel memory column with the sampled analogue values is stored in a derandomizing FIFO. The column containing the data written in the pipeline at the time of the trigger gets a flag and will be skipped by the read pointer until the event has been read out or the pipeline has been reset. Up to 8 events can be stored in the derandomizing FIFO. In case of overflow the control logic issues the overflow bit which is bundled with the physical data and the chip needs to be reset. Since 8+2 columns of the ADB is spent on the derandomizer buffer, the overall delay of the ADB is 118 clock cycles. With the start of the readout sequence, the analogue data from the corresponding time slot in the ADB are sampled in the S&H buffer and sent to the analog multiplexer which produces a serial data stream and builds a data packet according to the backend protocol (see Chapter 5). The SCT128A can be configured to share a common data line with a second chip in a master-slave mode. The second front-end chip on the same fiber waits for the first chip to finish simply by pausing the appropriate number of clock cycles before sending the data.

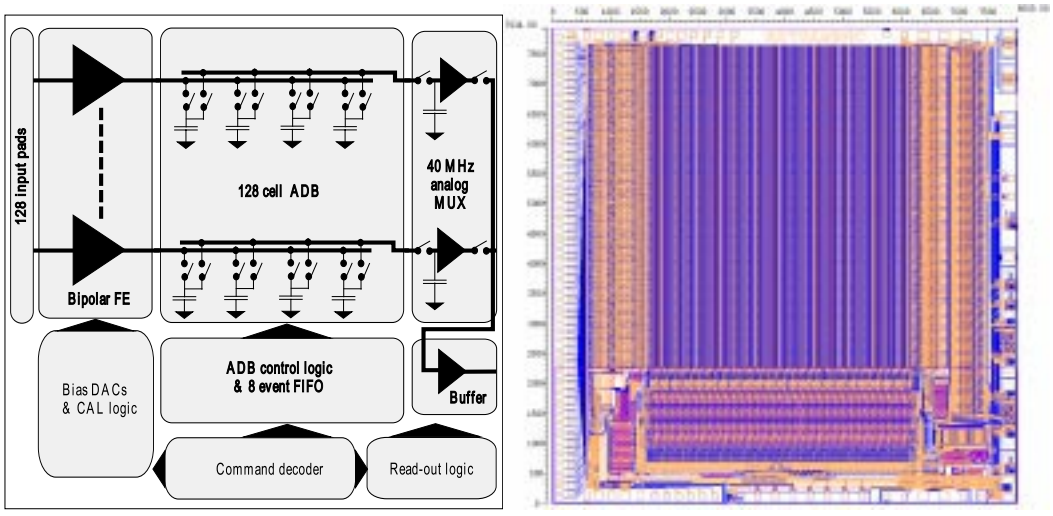


Figure 41. SCT128A block diagram and layout

Layout

Figure 41 shows the layout of the SCTA128HC chip. The front-end channels and the analogue pipeline are laid out with a pitch of 42 μm. Input bonding pads are laid out with 60 μm pitch. The bond pads for supply voltages and control signals are located on both sides of the chip to assure a symmetric distribution of the supply and ground return currents. The analogue and the digital part of the chip are surrounded by two separate guard-rings. The die area is 7.9×8.0 mm^2 of which about 30% is occupied by the storage capacitors in the ADB.

The SCT128A Front - End

Compared to the SCT32A, the front-end circuit was slightly modified. The input transistor was reduced in size by a factor two to gain higher f_t and reduce noise correlation. Furthermore, it has been found out, that smaller transistors suffer less from radiation effects (β-decrease). The noise contribution of the base spread resistance turns out to not being significant enough to force the use of large transistors.

The active load of the input transistor, PMOS plus source resistor, was replaced by a double width PMOS, the diodes in the first emitter follower and the gain stage were suppressed. Both outputs of the differential shaper circuit are now connected via switches to the output buffer in order to adapt for the polarity of the input signal. The output buffer itself, a push-pull Darlington structure, was replaced by a simple emitter follower. The main reason for the new buffer was the high sensitivity of the bottom-branch Darlington pair to changes in the threshold voltage of the PMOS transistor due to radiation. However, the basic topology of the front-end circuit remained unchanged, practically exhibiting the same transfer characteristics and signal properties.

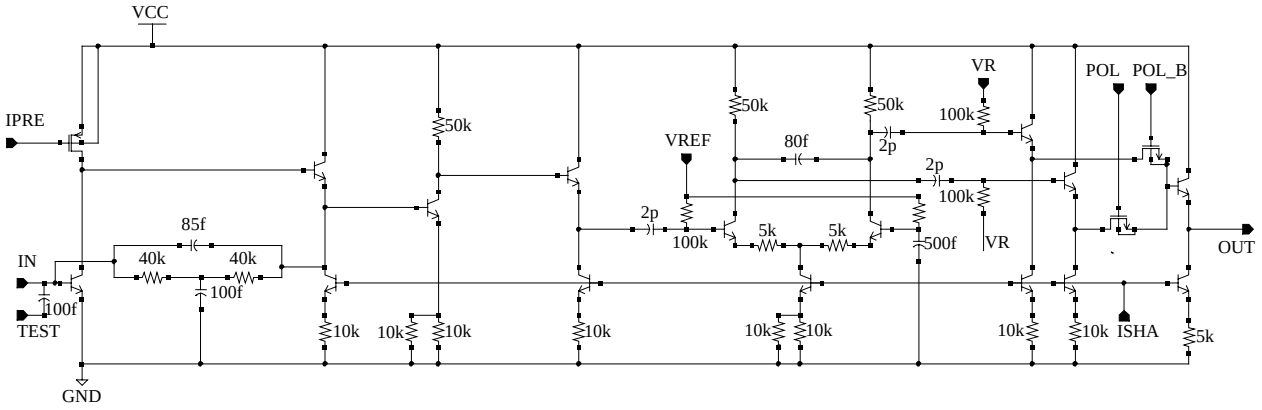


Figure 42. SCT128A front-end

Two versions of the front-end (LC and HC) have been designed in order to optimize the noise performance for low and high detector capacitances respectively. The main difference between the two versions is the nominal gain, which is twice as high for LC version. The designed peaking time for both versions is 25 ns. The front-end circuit is designed such a way that it can be used with either

polarity of the input signal. The given polarity is selected by switches, controlled from the external pads POL and POL_B.

Three 5-Bit D/A converters were implemented that allow for setting the bias currents in the different stages of the analog part of the chip. The first DAC controls the input transistor collector bias current I_C. As the optimum I_C that provides the maximum SNR for a given load capacitance depends on the value of the current gain β as well as on detector leakage current and bias resistor, the possibility of adjustment of this current is crucial. Furthermore, degradation of β due to irradiation throughout the lifetime of the experiment will require additional readjustment of the collector current in situ and even during data taking. In the HC front-end, the current can be set within the range of 0 to 310 μA with a resolution of 10 μA. For a detector capacitance of 15 to 20 pF, a nominal current of ~ 200 μA is foreseen. The second DAC provides a reference current which is used to control bias currents in shaper and output buffer. The shaper current can be set within a range of 0 to 77.5 μA with a resolution of 2.5 μA. A third DAC controls the bias current in the readout amplifier. VR and VREF denote a reference voltage levels.

Description Of The Readout Logic

A diagram of the readout logic is shown in Figure 43. On reception of a trigger, the 4 - bit counter is incremented. The sequencer starts producing the necessary readout control signals provided that the counter (which reflects the buffer occupancy) is not zero, and a “stop” is not being generated by the start/stop logic. The start/stop logic arbitrates the destination of the read-bit according to the chip address (first or second chip on fiber) and the number of readouts to be performed. The read-bit either passes to the multiplexer shift register, thus sequentially outputting the analogue information, or is used to generate the “stop” signal to indicate that a new sequence should not be generated yet. When one readout sequence is completed, the 4 - bit counter is decremented, reflecting the fact that the buffer has had one event removed.

The command decoder receives the data from the serial command line input and translates the codes into internal signals for controlling the DACs, registers and sets operating modes and multiplexer speed. Also the L1 trigger command is initially received by the command decoder.

The ADB and S&H logic controls the organization of the pipeline memory and the read and write pointers.

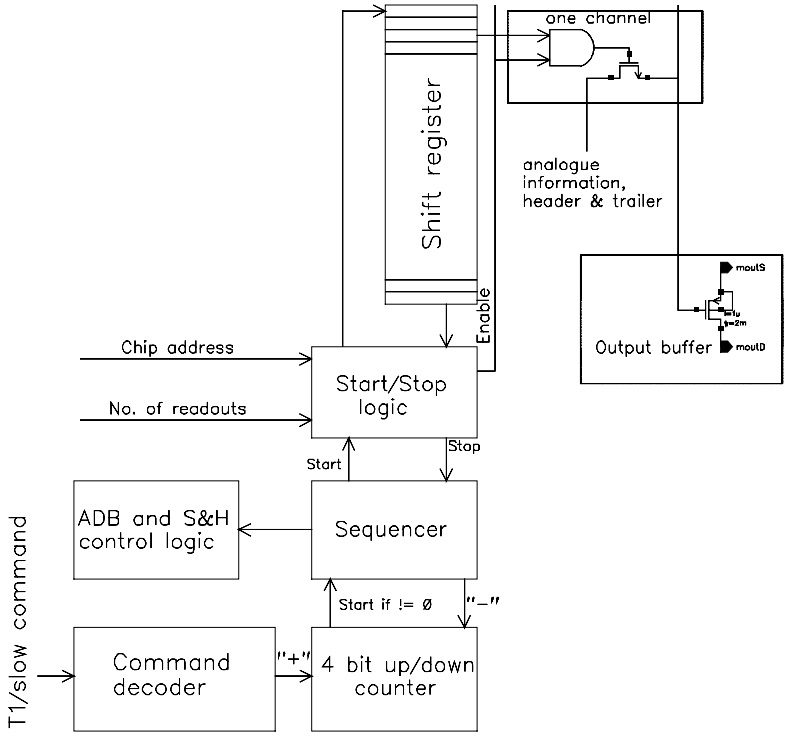


Figure 43. Block diagram of the SCT128A readout logic

Calibration Circuit

Each channel of the front-end circuit is provided with a calibration capacitor of 100 fF allowing the injection of test pulses. The test signals are distributed via four calibration lines so that every forth channel is connected to one calibration input. The four calibration lines can be pulsed either from the external calibration inputs or from the internal calibration circuit. The calibration circuitry comprises an 8-bit D/A converter (calibration DAC) providing dc current, address decoder, delay chain and a chopper circuit. In response to the calibration strobe signal the chopper circuit generates a voltage step pulse across a resistor by switching the dc current provided from the calibration DAC.

The amplitude of the calibration pulse can be set within a range from 0 to 160 mV with 8-bit resolution, i.e. 0.625 mV/step. For the calibration capacitor of 100 fF this corresponds to a range of 16 fC and a resolution of 0.0625 fC/step. The duration of the strobe signal is fixed and equal to 200 ns while the delay relative to the clock phase is controlled by the delay register and can be tuned within a range of 50 ns with a 5-bit resolution, i.e. 1.56 ns/step. Since the delay circuit is realized as a series of inverters the overall delay is strongly dependent on the process variation and therefore has to be cross-calibrated using the external clock signal. It is therefore required that in an extreme case of process variation the overall delay covers at least one clock period of 25 ns.

Readout Protocol

An analogue signal package from one chip consists of a four bit header (0101) followed by the three analogue samples supposed to be used for calibration of the optical links, 128 analogue samples with physical data from the detector, a one bit buffer overflow flag, a four bit BCO counter and a four bit trigger L1 counter. The above format of the data is independent of mode of readout (single or two chip readout). The total time for readout on one fiber for two chips is 2 x (4+3+128+1+4+4) x 25ns = 7.2 µs. The four bit BCO counter and L1 counter returned by the chip can be used for unique association each trigger with the physical data from the detector.

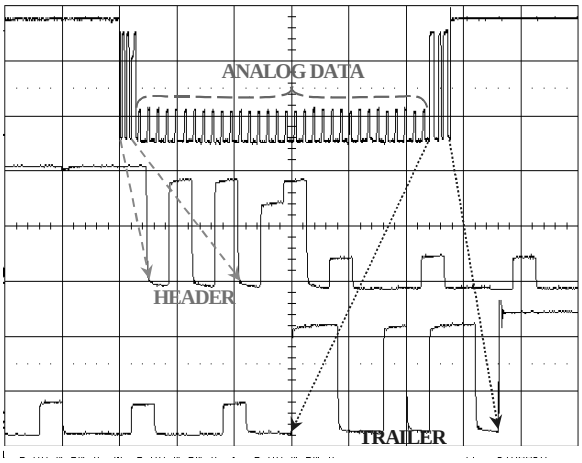


Figure 44. Scope view of a data packet of the SCT128A front-end chip; test pulses are applied to every fourth channel

In the case of overflow of the readout buffer the control logic issues an overflow bit which is sent with the data packet. After detection of the overflow error the chip should be reset by means of the soft-reset command.

The maximum clock rate of the multiplexer and the readout circuit is the same as the rate of sampling the data, i.e. 40 MHz. The chips can be read out with a lower rate (40 MHz divided by 2, 4 or 8) which is programmable. All communication with the chip i.e.:

- sending the level 1 triggers,
- sending the software reset,
- loading the DACs,
- issuing the internal calibration pulses
- programming the speed of the output MUX

is executed via the fast 40 MHz serial command interface.

Lab Tests And Measurements On The SCT128A

In order to evaluate the behavior and performance of the chip in a real-life scenario, its input pads were wire-bonded to several different types of semiconductor detectors. Particularly ATLAS SCT prototype silicon strip detectors, which are foreseen to be used within the ATLAS tracker, were employed. These modules were exposed to particles from various radioactive sources in the lab or directly put into beams of CERN's accelerators facilities. The following section gives a summary of the results obtained from these measurements. It will be demonstrated, that the SCT128A meets all the necessary specifications to be a feasible candidate for analog readout in LHC experiments.

Test And Data Acquisition Setup

In the lab environment, single or multiple readout chips are mounted onto printed circuit boards (PCBs), which contain power supplies, additional buffer amplifier and all necessary connectors to carry control and data signals to and from the chip. The detectors are wire-bonded to the input pads. Radioactive sources, e.g. β-sources like Ruthenium (^{106}Ru) and γ-sources like Americium (^{241}Am), provide the particles, which are sent through the detector. A scintillator-photomultiplier, placed underneath the detector, supplies a synchronous trigger for β-particles.

Figure 45. shows 6 SCT readout chips mounted on a ceramic carrier. All control and data signals to and from the chips are transmitted via a low-mass kapton cable between the PCB and the carrier. The chips are wire bonded to the carrier and to a 6×12 cm silicon strip detector (composed of two 6×12 cm detectors in series) .

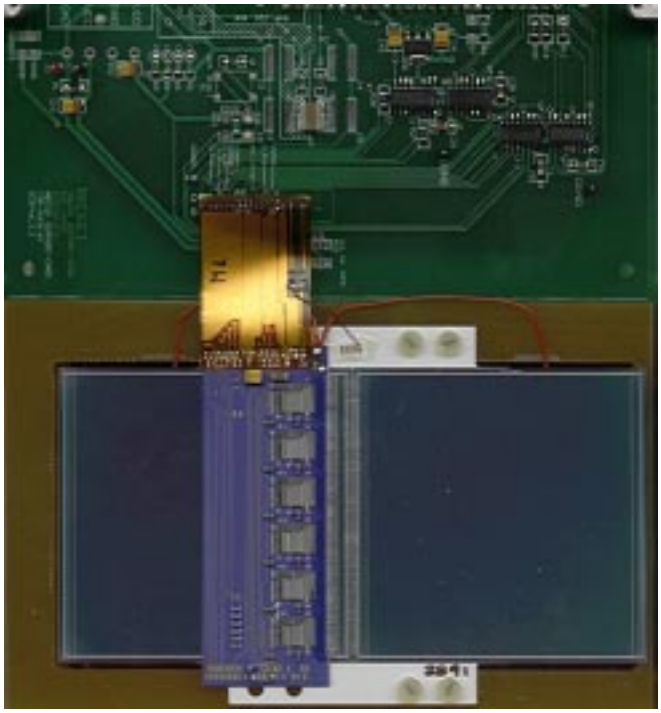


Figure 45. 6 readout chips on a ceramic carrier wire-bonded to a 6 × 12 cm silicon strip detector

The recording of an event takes place in the following way. A particle crosses the detector, creating signal charge in the semiconductor bulk (see Chapter 2), and eventually is caught in a scintillator that produces a short pulse in a photomultiplier diode. This pulse is converted into a NIM-type trigger pulse and is sent to the command generator, a unit that communicates with the readout chip via the serial command interface and also produces the main 40 MHz clock. The pulse from the scintillator is encoded into the L1-trigger command by the command generator and sent to the chip. On reception of the trigger, the SCT128A starts the readout sequence, multiplexing out a data packet (Figure 44), which is sent to a fast A/D converter. Subsequently, the converted analog data are stored onto a disk via a VME bus interface. The system is ready for the next event. The maximum data rate achievable with this setup, up to 250 kHz[9] limited by the processing speed of the controller, is approx. 1000 events/sec. The software that runs the system communicates with the chip via the command generator. It allows for running different types of test cycles with variable settings of parameters like test pulse amplitude or the timing delay between L1 trigger reception and sampling-point of the write amplifier. Variations of the bias settings in the front-end between data runs are also supported. Results of tests and measurements, carried out on this very flexible test setup, are presented in the next section.

[9] maximum event rate of the SCT128A at 40 MHz operation (1 data packet ~ 3.6 μs)

Readout Of Silicon Detectors

Channel 1 – 20 and 109 – 128 were bonded to a ATLAS prototype silicon strip detector. The detector was fabricated by CSEM with the following parameters: size 2.8 6.6 cm, 50 µm readout pitch with one intermediate strip, 350 µm thick, nominal depletion voltage V_{dep} = 60V, FOXFET biasing. The capacitance as seen by the preamplifier at full depletion is approximately 9.5 pF.

Test Pulse Measurements: Noise Performance, Gain and Timing Scans

The internal calibration circuit applies test pulses of variable amplitude to the on-chip test capacitors at the input of every channel. Noise and signal amplitude as a function of the collector current were measured for three different input load situations (Figure 46).

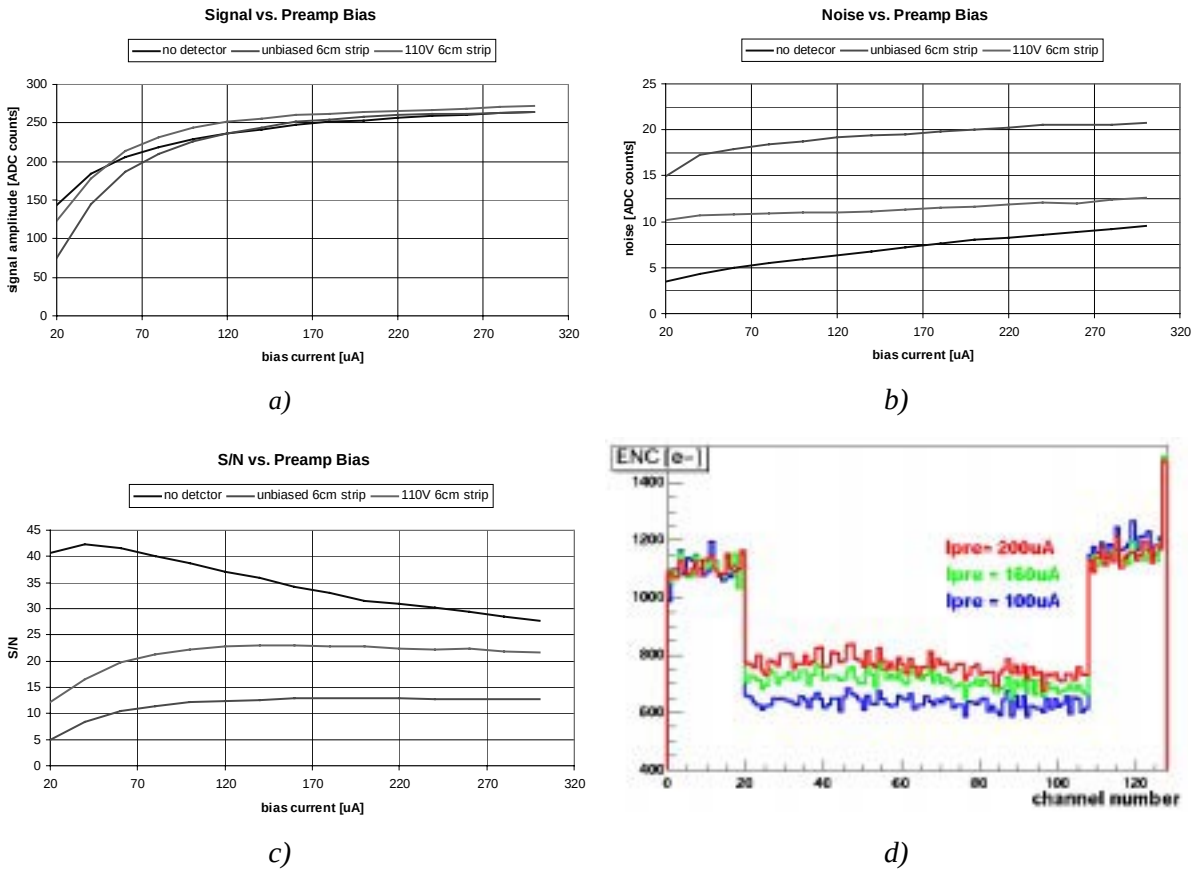


Figure 46. a) Amplitude of a test pulse as a function of the collector current I_C for three different input load capacitances (floating, fully depleted detector, unbiased detector) averaged over all channels, b) RMS noise measured for the same input loads (averaged), c) calculated Signal-to-Noise Ratio, d) ENC of each channel for three different bias currents (Ipre = I_C). The low-noise region of floating inputs covers channels number 20 to number 108.

Floating input results in an input capacitance of ~ 500 fF, resulting from the metal lines and the bonding pad. A 6 cm strip detector of this type produces, when fully depleted, approximately 9.5 pF. The unbiased detector has a capacitance which is difficult to determine, one can expect at least 30 pF. Figure 47 shows the ENC measured and calculated according to (3.34).

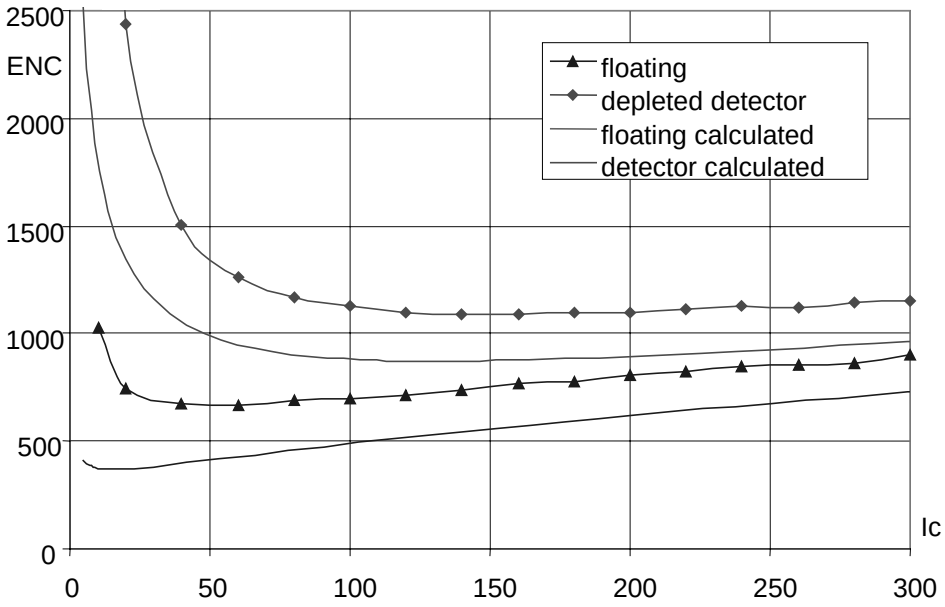


Figure 47. ENC for channels floating and bonded to fully depleted detector (~9.5 pF) as a function of the collector bias current. The plotted curves are mean values of the 40, respectively 68 channels. The discrepancy between the measured and calculated curves is due to clock pick-up and switching noise of the digital parts in the order of 200 e^-.

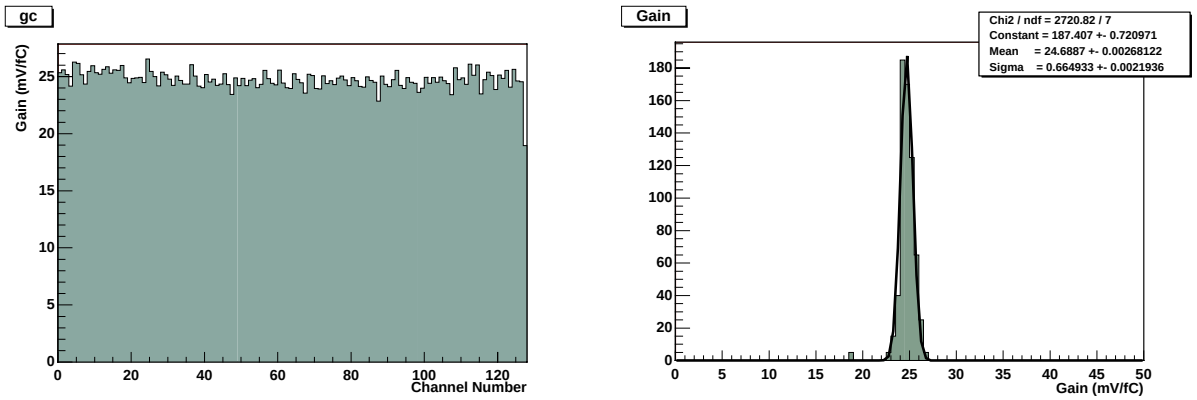
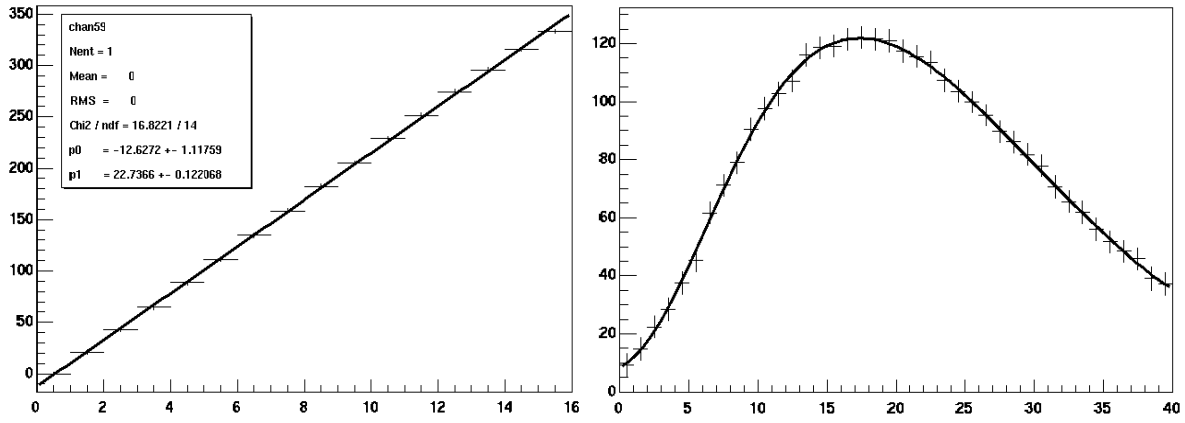


Figure 48. The mean gain of the SCT128A front-end is in the order of 24.7 mV/fC. This chip shows a channel-to-channel gain variation with a sigma of 0.66 mV/fC.



a) *b)*

Figure 49. a) Linearity of the front-end amplifier for an input signal range from zero to 16 fC. b) Pulse shape at the multiplexer output, obtained by scanning the L1-trigger to sampling delay. The vertical scale in both pictures is mV, the horizontal scales fC and ns respectively.

Performance Of The Analog Memory (ADB)

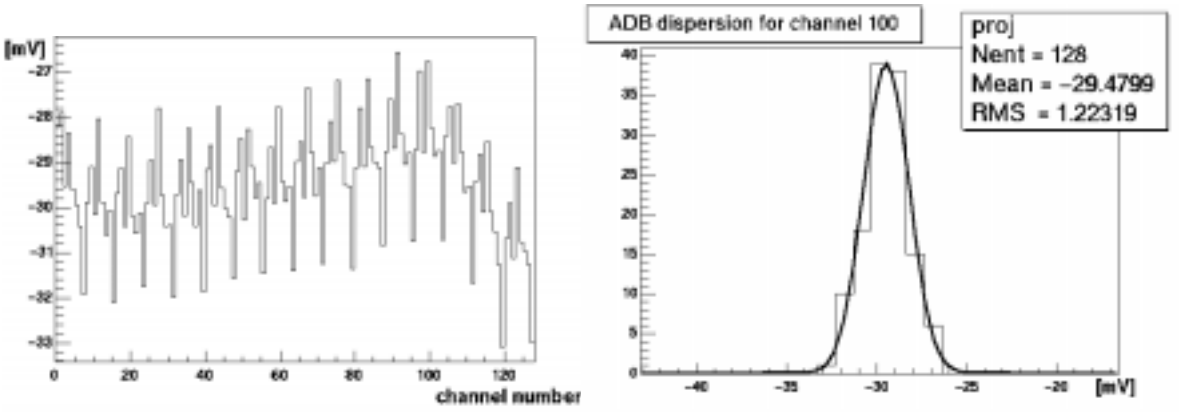
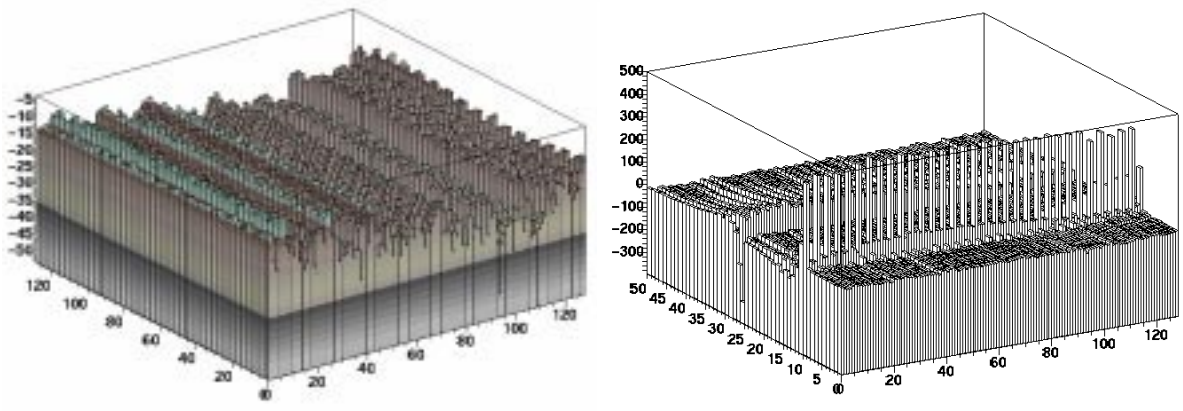


Figure 50. Pedestal distribution across a column of the ADB, hence the baselines for one readout event. The distribution shows a sigma of 1.22 mV corresponding to ~ 300 e^-.



a) *b)*

Figure 51. a) Pedestal map of the 16384 storage cells of the analog memory (ADB). The peak-peak variation is approximately 25 mV. b) A 400 ns - 16 fC test pulse applied to every fourth channel in the ADB.

Calibration with gammas from a ^{241}Americium Source

As the energy deposition of β-particles in silicon is statistically distributed, they are not favorable for an absolute calibration of the gain and the ENC of a readout system. β-particles are emitted by the source with different kinetic energies and also interact with the detector material in a non-uniform way, thus producing the *Landau* spectrum (Chapter 2). Photons, like the γ-particles from a ^{241}Am source, interact with the detector through the photoelectric effect, thus always releasing the same amount of energy. This results in very narrow lines at known energies. ^{241}Am emits monochromatic photons at different fixed energies. The two most probable lines are

- 59.5412 keV @ 35.9 %
- 26.3448 keV @ 2.4 %

The more abundant ones will produce about 16500 electron-hole pairs, corresponding to 2.65 fC. With an expected gain of 25 mV/fC, the line should appear at 66.25 mV.

In contrast to β-particles, photons deposit all their energy and are annihilated through the interaction, thus do not cross the detector. It is therefore not possible to trigger on the same particle that created the signal in the detector. However, the readout chip needs precise timing in order to produce a signal proportional to the released charge. One possible solution is to trigger the chip randomly and running the "8 consecutive triggers – mode". This means that on reception of a trigger, 8 consecutive columns of the ADB pipeline are written to the FIFO and read out immediately. 8 time slots correspond to 200 ns. Having a pulse width of less than 100 ns, there is a good probability to find complete pulses, sampled at 25 ns intervals, in these 200 ns time windows (Figure 52). Because of the undersampling (a signal with an upper –6dB bandwidth of about 40 MHz is sampled with 40 MHz), it is impossible to restore the exact signal properties. However, due to the fact that the function of the pulse shape is known (the CR-(RC)^n – functions, see Chapter 3), one possible workaround is to fit that function to the 8 sample points, leaving the peak amplitude and the time of the peak within the 200 ns – window, as free parameters. As a result, this fit returns the peak value of the signal as if sampled with the correct timing of a synchronous trigger.

In order to minimize the amount of data written to the disk, at each event, the 8 consecutive time slots were analyzed *on-line* in order to determine the presence of a strip with a signal over noise greater than 5.5 in any of the slots. Only events with one of those strips were stored on file for a posterior analysis. Given that the acquisition rate is determined by the speed of the processing of one event, which is constant, we were reading always the same cells in the pipeline. In consequence, pedestals and noise had to be calculated for each of the eight time slots acquired independently.

At the *off-line* analysis stage, strips with a signal-to-noise ratio (SNR) greater than 4 were searched for. If found they were used as seeds to build a cluster around them. All the consecutive neighbors were scanned and added to the cluster until one of them had a SNR of less than 2. That

defined a cluster with signal being the sum of the signals of the components and SNR also defined as the sum of the SNR of the components. A cluster is accepted if the SNR was greater than 6.5. That procedure was repeated until all the channels are scanned. An event was rejected if it had more than one cluster in any of the time slots or if that cluster had more than 4 channels in it. Figure 52 shows the fit to a three strip cluster with strip 1 containing the seed and strips 0 and 2 being the two neighbors.

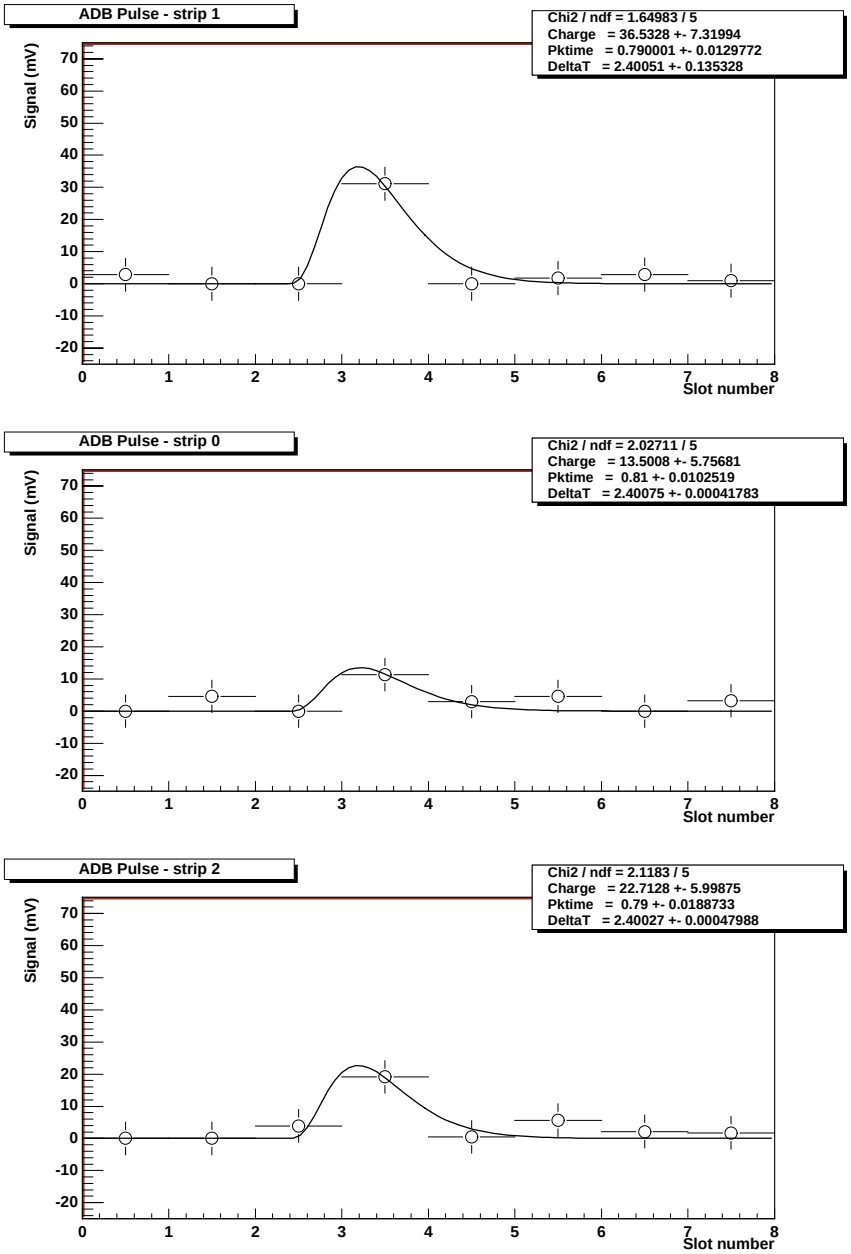


Figure 52. Fit of the filter function to the sample points corresponding to a 3-strip cluster

In order to gain additional information on the true behavior of the shaper circuit, generic CR-$(RC)^n$ functions were fitted to pulse shapes, acquired by scanning the L1-trigger-to-sampling delay. The free parameters are the peaking time T_p, the filter order n and the peak amplitude. Results of the

fits for the parameters T_p and n across all channels of one SCT128A are shown in Figure 53. According to these fits, the shaper peaks at ~ 22 ns for floating input and at ~ 26.5 ns when connected to a 9.5 pF detector. The order of the filter function equals to 3.3 and 5 respectively. The so obtained values were used to build the fit functions for the sampled data (Figure 52).

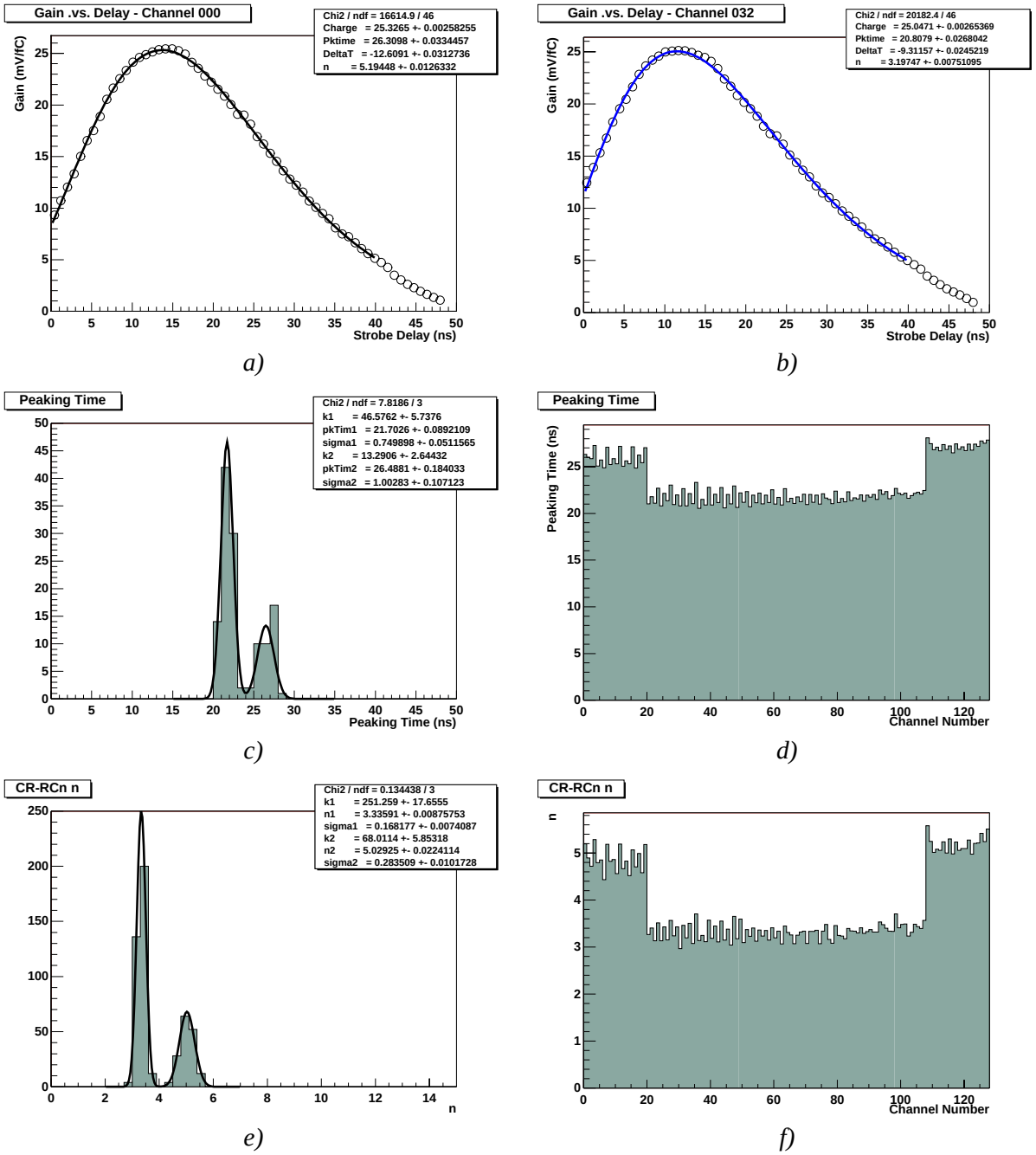


Figure 53. Results of the fit of the CR-RC^n function (a) to a channel, connected to the detector, (b) to a floating input channel. (c) Peaking time distribution obtained from the fit, and (d) spread across the channels. Order of the filter: (e) distribution and (f) across the channels.

The results of applying this procedure to the raw data of one ^{241}Am run is shown in Figure 54. The peak of the Americium 59.54 keV – line, widened by the system noise and the inaccuracy of the fit procedure, lies at 64 mV, which is very close to the expected value. The sigma of the distribution is 13.7 mV. These data allow an absolute calibration of the detector-readout system.

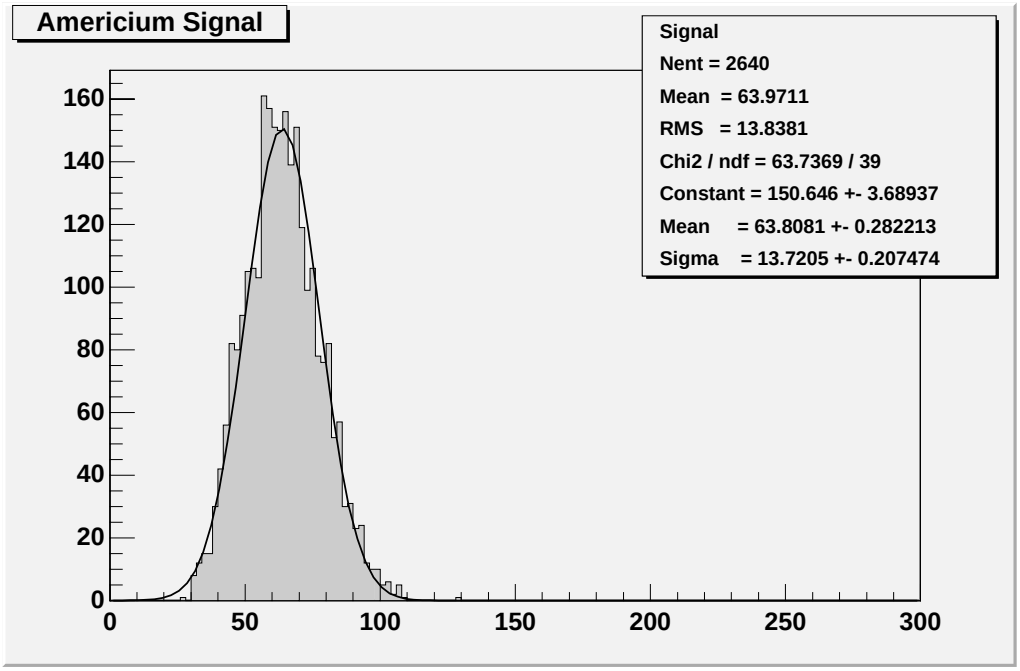


Figure 54. Americium peak

Table 11. Parameters for the calibration of the detector – readout system

Parameter	Value
Energy per electron/hole pair in silicon	3.62 eV
Most probable ^{241}Am line (35.9%)	59.5412 keV
Signal peak	63.8 mV
Avg. RMS noise	4.75 mV
Collector bias current	155 μA
Shaper bias current	68.5 μA
Detector bias voltage	140 V
Detector capacitance	~ 9.5 pF
Detector depletion voltage	60 V
Preamplifier open loop gain	1000
Preamplifier feedback capacitance	85 fF

From the energy per electron/hole pair in silicon and the value of the ^{241}Am line, we calculate the induced signal charge to 16448 e^- which corresponds to a charge of 2.635 fC. With a detector

capacitance C_d of 9.5 pF, a preamplifier feedback capacitance C_f of 85 fF and a preamplifier open loop gain A of 1000, we can estimate the actual signal charge into the amplifier according to (3.3):

$$\frac{Q_i}{Q_s} = \frac{1}{1+\frac{C_d}{(A+1)C_f}} = 0.9 \equiv 90\% \quad \Rightarrow \quad Q_i = 14805\, e^- \equiv 2.372\, fC$$

Gain and ENC are calculated[10] from these data giving

$$Gain\ (Am): \qquad A = \frac{63\ mV}{2.372\ fC} = 26.6\ mV/\ fC$$

$$Noise\ (Am): \qquad ENC = \frac{14805\, e^-}{13.4} = 1100\, e^-$$

for the bias conditions summarized in Table 11.

The gain differs by 1.9 mV or 7 % in comparison to the electronic calibration (test pulse).

Readout The Signals From β - Particles In Silicon Detectors

The energy deposited by β-particles in silicon is *Landau* distributed as discussed in Chapter 2. We use the same detector as for the Americium run, and use this time a ^{106}Ru–source. ^{106}Ru is a radioactive isotope of Ruthenium, which decays to Rhodium under emission of an electron with a half-life time of about 1 year and at an endpoint energy of 3541.100 ± 6.325 keV. The mean energy of the β is about 1450 keV. Figure 55 shows the electron range and the energy loss of electrons in silicon. From this graph we can assume safely that the majority of electrons will cross the 350 μm of silicon and reach the scintillator. We therefore run the setup with a synchronous trigger.

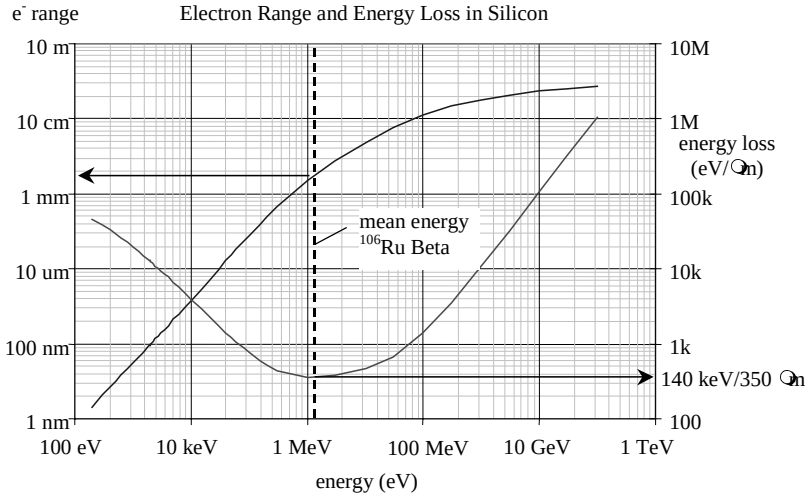


Figure 55. Electron range and the energy loss of electrons in silicon

The mean energy loss of a ^{106}Ru β - particle in 350 μm silicon is approximately 140 keV (from Figure 55), yielding a most probable energy loss of about 90 keV[11]. This value, which is for a ^{106}Ru β - particle very close to 1 MIP (Minimum Ionizing Particle), is corresponding to 25000 e^-. The results of a Ruthenium run at the same bias conditions as for the Americium calibration (I_c = 160 μA, I_{SHA} = 60 μA, V_{det} = 150 V) is shown in Figure 56. The *Landau* peak of the signal, which is proportional to the deposited energy, lies at 93.7 mV, the S/N peaks at 21.156, the mean RMS noise is ~ 4.42 mV for the connected channels. The majority of all recorded events contains 2-strip clusters.

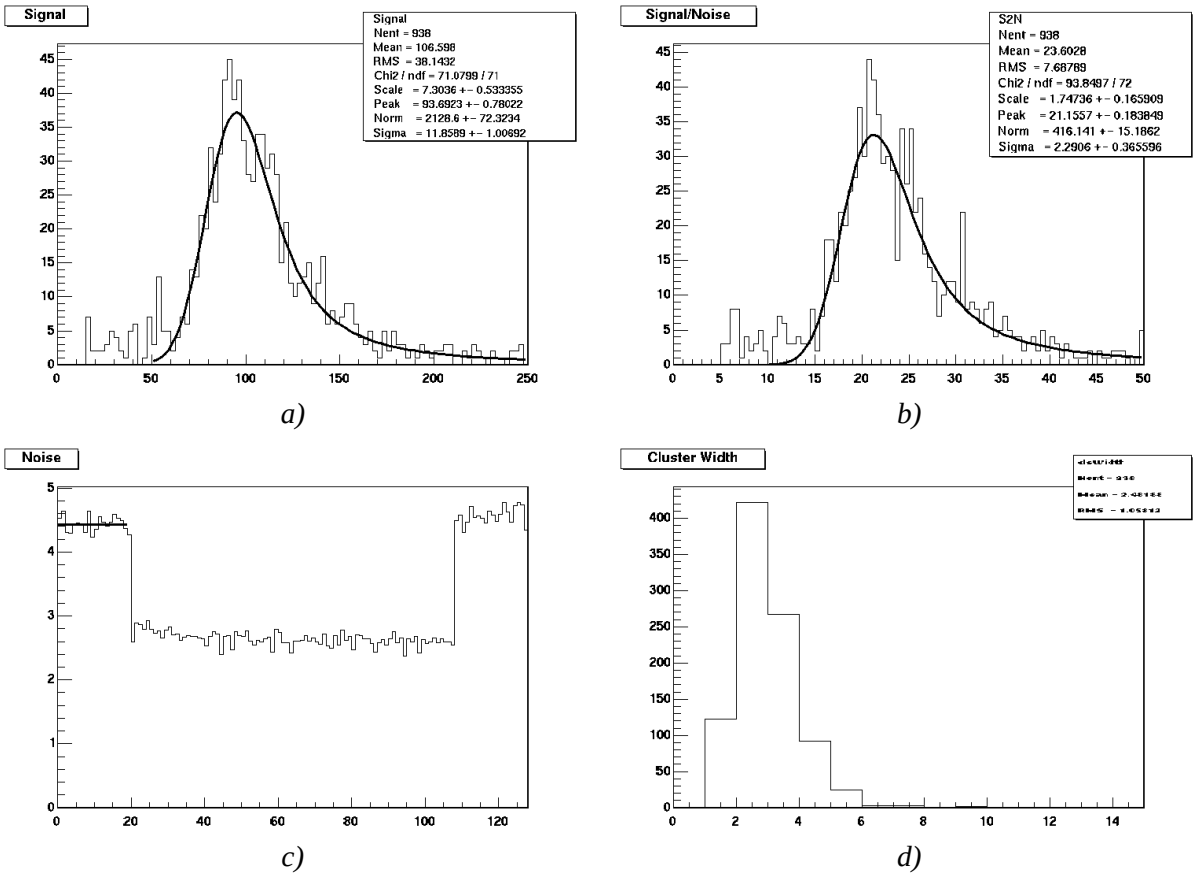


Figure 56. ^{106}Ru run with a 350 μm silicon detector at I_c = 160 μA, I_{SHA} = 60 μA, V_{det} = 150 V. a) Landau spectrum of the deposited energy in mV, b) S/N spectrum, c) noise (mV) spread across the channels, d) cluster multiplicity.

[10] Gain = signal peak / input charge, ENC = input charge [e^-] / (S/N)
[11] 2/3 rule of thumb

Using the gain value, derived from the Americium calibration, we can now derive the number of electrons, created by one MIP[12] in ATLAS – type 350 μm and 300 μm Silicon strip detectors with 25μm(50μm) pitch:

$$1\ MIP_{350\mu} \cong 1\ ^{106}Ru\text{-}\beta_{350\mu} = 24200\ e^-$$
$$1\ MIP_{300\mu} \cong 1\ ^{106}Ru\text{-}\beta_{300\mu} = 20750\ e^-$$

Assuming the gain to be the same in both the runs, we can calculate the noise in the Ruthenium run:

$$ENC = \frac{22000\,e^-}{21.16} = 1040\,e^-$$

This value, which corresponds to 4.43 mV RMS[13], compare Figure 56 c), is very consistent with the noise measured in a great number of further data runs (see next section) and with the result of the electronic (test pulse) calibration of 1090 e^-. The electronic (test pulse) and the Americium calibration show a good agreement. Table 12. gives a summary of the obtained results:

Table 12. Summary: Calibration of the SCT128A-HC detector-readout system with the biasing parameters of Table 11.

Calibration	^{241}Am	electronic
Gain	26.6 mV/fC	24.7 mV/fC
ENC	1100 e^-	1090 e^-
ATLAS p-type 25 μm(50 μm) strip detector:		
1 MIP (350 μm)	24200 e^-	
1 MIP (300 μm)	20750 e^-	

Another type of detector, which is widely used in radiation detection systems, is the "pad detector". This detector consists, like strip detectors, of thin silicon bulks in a reverse biased p-n configuration. The readout side is segmented into squared or rectangular "pads". A main advantage of this detector type is the highly reduced intersegment capacitance, which results in much smaller charge loss due to capacitive coupling, and, also dependent on the pad size, a significantly reduced load capacitance towards the readout amplifier input. Figure 57 shows the results of a Ruthenium run

[12] created charge carriers = peak signal / gain = 3.523 fC = 22000 e^- + 10 % = 24200 e^- actually generated charge carriers.

with a SCT128A connected to a SINTEF silicon pad detector with the following characteristics: Thickness 300 μm, pad size 1×1 mm^2, depletion voltage ~ 60 V, operating bias voltage 150 V, load capacitance ~ 1 pF. The preamplifier bias current was set to 150 μA.

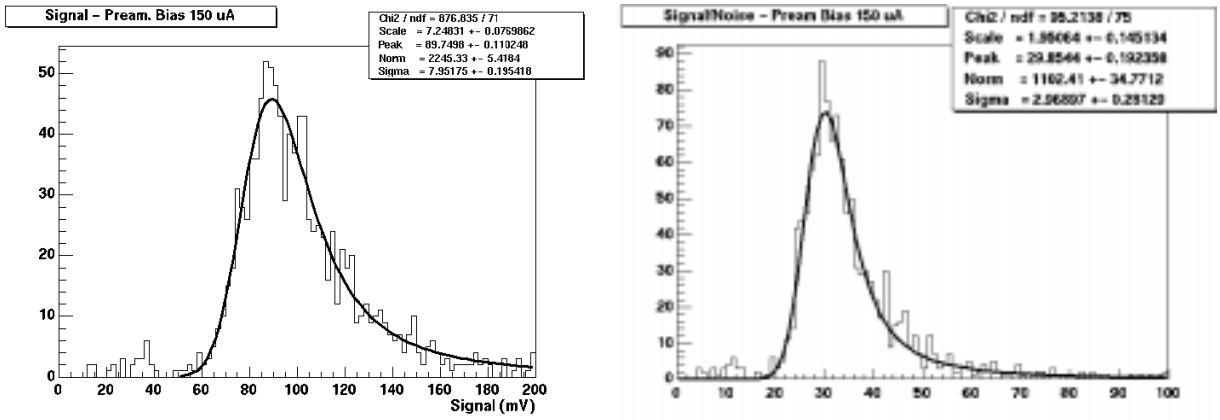


Figure 57. Signal and S/N distributions for ^{106}Ru β's in a 300 μm silicon pad detector

Applying the gain, derived from the Americium calibration, we calculate the deposited charge from the signal peak: Q_i = 89.74 mV / 26.6 mV/fC = 3.374 fC. This charge corresponds to 21050 electrons. Because of the very small charge loss due to capacitive coupling, this value is close to the charge created by 1 MIP in 300 μm of silicon ($Q_s = Q_i + 1.1\%$):

Charge carrier pairs in Silicon:	
1 MIP (300 μm)	~ 21260 e^-

It may be concluded, that the charge loss in ATLAS p-type 25 μm(50 μm) 6cm strip detectors due to capacitive coupling amounts to ~ 500 electrons.

The SCT128A-HC Performance At Varying Bias And Detector Settings

The behavior of the SCT128A-HC front-end was further evaluated by recording Ruthenium data runs with the CSEM strip detector at different settings of the bias current of the preamplifier (IPRE = I_C of the input transistor) as well as for the reference current of the gain stage, the shaper integrator and the output buffer (ISHA). The plots show the *Landau* peak of the signal amplitude and of the S/N distribution as well as of the RMS noise voltage as functions of the bias currents.

In order to investigate the effect of the "ballistic deficit", all measurements were redone at different detector bias voltages above full depletion.

The first set of plots (Figure 58) shows measurements, done at the same collector current as the calibration runs of the last two sections, I_C = 155 μA. The data are directly comparable. The left

[13] RMS noise [mV] = ENC · electron charge · gain: $1040 \cdot 1.602 \cdot 10^{-19} \cdot 26.6 \cdot 10^{-3} \cdot 10^{15}$ = 4.43 mV

column contains the peak signal, the RMS noise voltage and the S/N peak versus detector bias voltage, the right column versus ISHA. Figure 58 a) indicates that for ATLAS prototype silicon strip detectors, readout with a 25 ns shaping time front-end, the ballistic deficit [22], [41] saturates at ~ 140 V (or 80 V over depletion). Figure 58 b) shows the increase of signal amplitude with rising reference current ISHA. The RMS noise voltage remains constant with increasing overdepletion voltage (c), as the detector capacitance does not rise anymore after reaching full depletion. On the other hand, noise grows by 25% over the range of ISHA (d). However, the increase in noise is relatively bigger than the rise of the signal amplitude. The best S/N is therefore reached at low ISHA (e), (f).

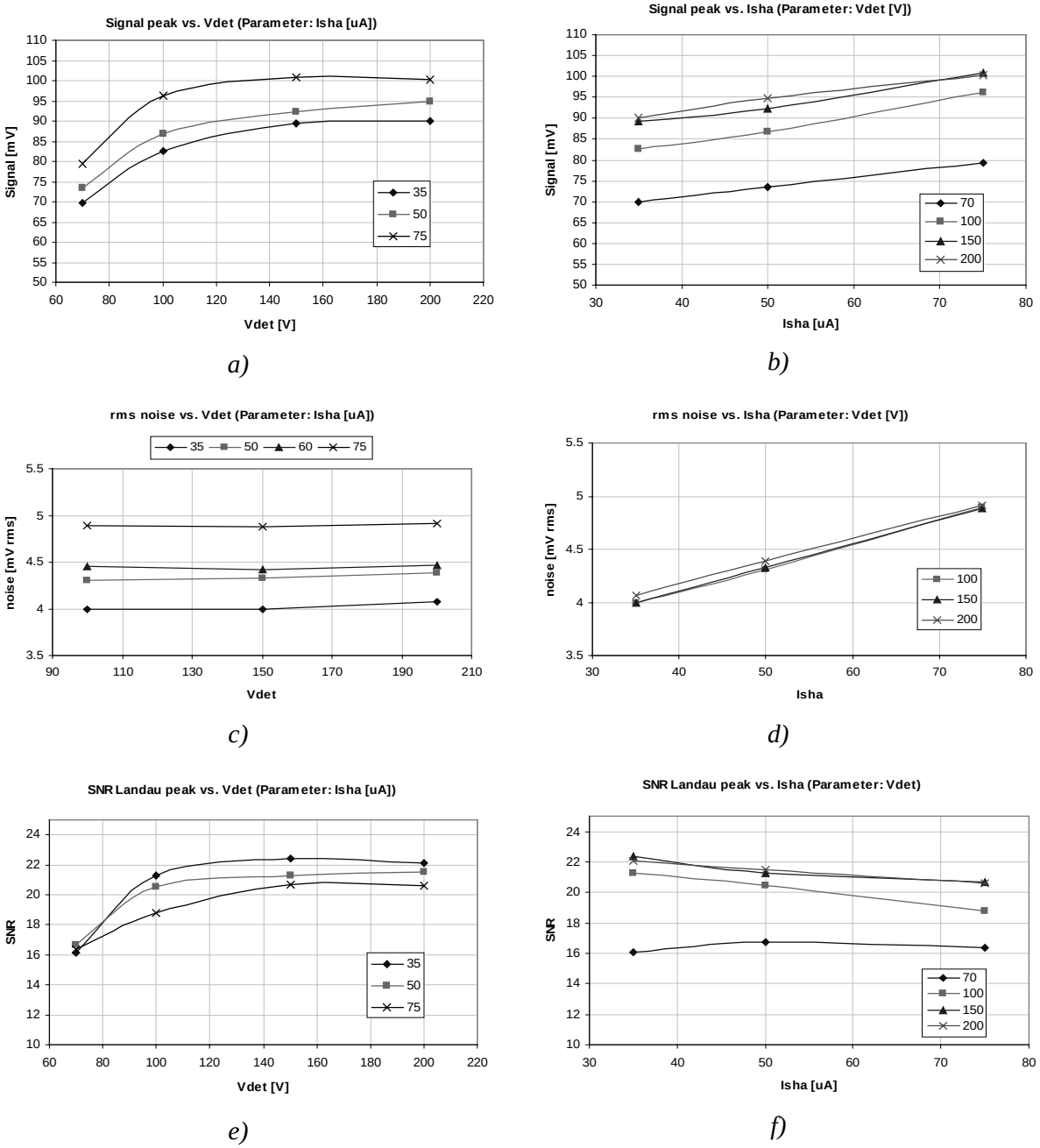


Figure 58. Signal, noise and S/N as functions of the detector bias voltage Vdet (left column) and the reference current ISHA (right column).

The plots of Figure 59 show the dependency of the same parameters on the preamplifier bias current I_C (or I_{pre}). The left column shows signal amplitude and RMS noise increase with rising I_{pre} at a shaper reference current of 50 µA, the right column at a detector bias voltage of 200 V. The relative increase of both signal and noise, is almost equal, yielding a rather small rise in S/N ratio over a preamp current range of 100 µA to 220 µA. This result stands in very good agreement with theoretical predictions and test pulse measurements. (see Figure 47).

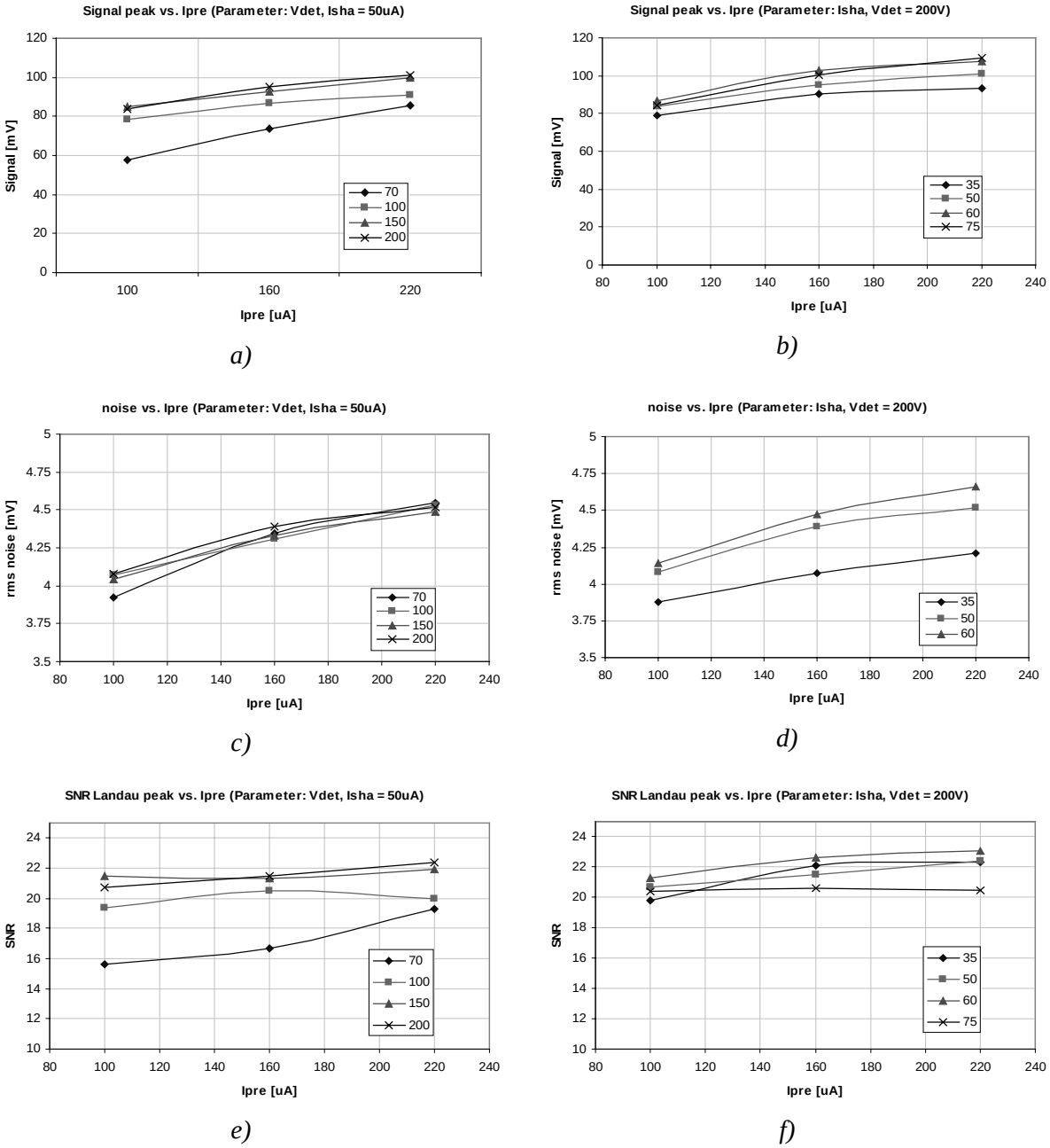
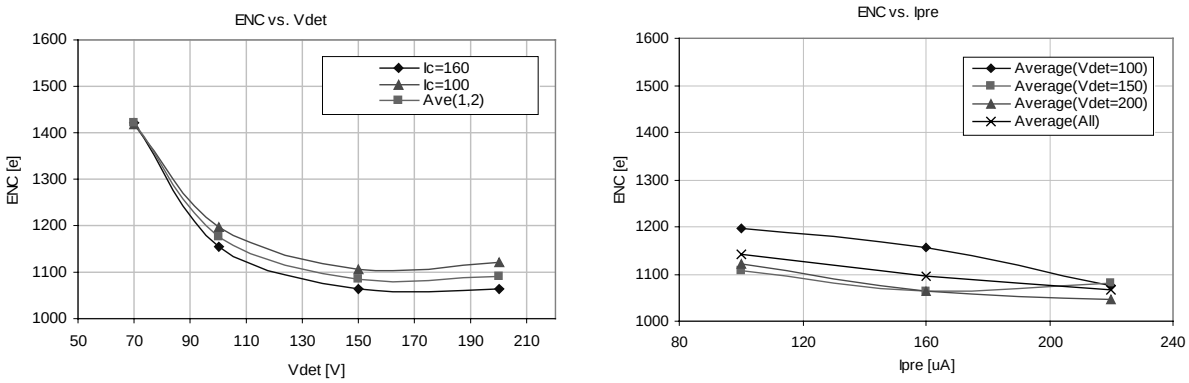


Figure 59. Signal, noise and S/N as functions of the preamp bias current at reference current ISHA = 50µA (left column) and at detector bias voltage V_{det} = 200 V (right column).

Figure 60 plots the ENC versus detector bias voltage (a) and preamp bias current (b). Again, at a detector bias above ~ 140 V, all available charge from a 300 μm – 6 cm silicon strip detector is collected by a front-end with 25 ns peaking time. ENC decreases slightly with increasing I_{pre}.



a) *b)*

Figure 60. ENC versus detector bias and preamp current

The mean ENC, averaged over all data runs at V_{det} = 150 and 200 V, turns out to be 1085 e^-. The correspondence to the Americium and the electronic (test pulse) calibrations are good.

^{241}Am	1100 e^-
Avg. ^{106}Ru	1085 e^-
Electronic	1090 e^-

Chapter 5

A/D Conversion For The ATLAS Analog Readout Scheme

The data, sent from the SCT modules are serial data streams, organized in packets. At each readout cycle, the multiplexer of the readout chip sends a mixed-signal data packet consisting of a digital header pattern, analog data values and a digital trailer, time multiplexed at 40 MHz (thus the length of one time slot is 25ns). The receiver is the so-called the Read Out Driver (ROD), which is situated off-detector in the cavern typically around 50 to 100 meters from its front-end chip. Optical fibers serve as the data links. On reception at the ROD, a defined phase relation between the data packet and the local copy of the machine clock has to be established in order to ensure proper A/D conversion of the analog data. Furthermore, the additional information on the data has to be extracted out of the trailer of each data packet and distributed to their respective receivers.

Requirements And Specifications For A Mixed Signal Data Receiver/Clock Synchronizer

The local clock at ROD level and the front-end multiplexer clock will both be derived from the LHC machine clock, which is generated centrally and distributed to all sub-detectors and counting rooms by the TTC (Timing, Trigger and Control distribution) system. One single laser will send the clock signal[1] via a hierarchical structure of passive optical splitters to receiver ASICs (TTCrx) which sit close to each readout module and also in the counting rooms. The ROD local clock frequency therefore will be exactly the same as the one of the incoming data stream, however it is difficult to predict the phase of the data packet relative to the clock. Moreover even if the absolute phase was known this would not be useful as the absolute phase of the incoming streams will be determined by differing delays in the readout cables and drive electronics plus different delays in the clock distribution system. Also, any clock skew correction scheme at the front-end modules will initially start in an uncorrected state and will need to be corrected using data readout from the front end.

The phase of the conversion clock of the A/D converter determines the sampling point of the data. Ideally, each time bin of the data stream should be sampled as late as possible before the

transition, to allow for rise time effects and settling time. As an analog data stream is difficult to delay, the need is to produce a sampling clock for the A/D converter, which precedes the data transition by a few nano seconds. A maximum deviation from the selected sampling point of $< \pm 1$ ns has been decided to be acceptable for a time slot of 25 ns.

Furthermore, as the converter type is not yet known, it would be desirable to be able to select a certain phase relation between clock and signal phase according to the requirements of the ADC. Finally, to avoid problems from coherent clock pick up, the phase of the sampling clock must be constant during the sampling of a complete data packet. As the radiation level in this part of the experiment is sufficiently low [1], a commercial ADC can be used.

The second task is the generation of a minimum set of control signals for the ADC and subsequent data processing stages at ROD level and the extraction of the digital data out of the trailer of the mixed signal data packet. As it is designed to work primarily together with the SCT128A analog front end chip, the unit should be fully compatible with the SCT128A mixed signal data format and meet the LHC/ATLAS timing specifications in terms of speed and timing resolution. It also has to be compatible with one-chip and daisy chained two-chip readout cycles.

A block diagram of the system is shown below (Figure 61). For different reasons, mainly the high speed operation and accuracy, and also space and power constraints, it has been decided to implement the functionality into an ASIC. Table 13 below summarizes the tasks and design specifications for the unit, named Clock Synchronizer Circuit (CSC) [45].

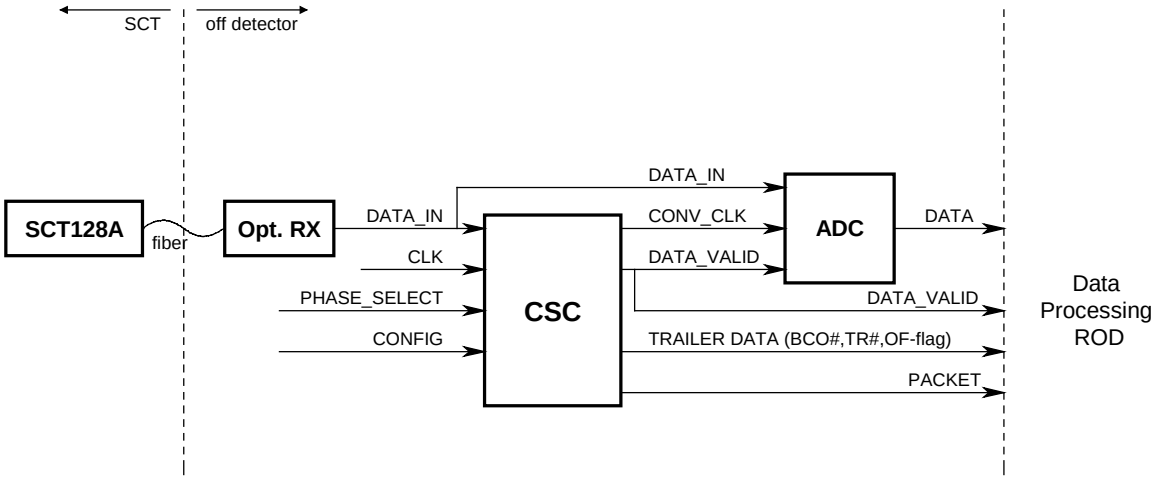


Figure 61. A/D conversion for the ATLAS analog readout scheme: system overview

[1] Besides the main clock, also the L1 trigger signal and other general control signals will be distributed via the same data line using biphase mark encoding.

Table 13. CSC tasks and specifications

- Monitoring of the data line at the output of the optical receiver for the mixed signal data packets sent by the analog front-end chips.
- Detection of the digital header pattern, synchronization on the data and creation of an encode clock of correct phase for the A/D converter.
- Extraction of additional information, bunch crossover (BCO) number, trigger L1 number and data overflow flag, from the digital trailer at the end of each data packet.
- Generation of control signals for A/D converter and further data processing stages at ROD level.
- Additional functionality: Programmable output clock phase selection, configurable for one-chip or two-chip readout cycles.

Parameter	SPECIFIED VALUE
Nominal clock frequency	40 MHz
Phase-to-digital converter (PDC) time resolution	1 ns
Maximum timing error (@ sampling point)	± 1 ns
Nominal power consumption	100 mW
Single power supply	+5V
Target process	0.8 μm standard CMOS

Input signals
CLK: 40MHz LHC machine clock
DATA_IN: Data line from the optical receiver
CONFIG: sets the CSC to 1-chip or 2-chip readout cycles (1 bit)
PHASE_SELECT: 5-bit serial input, selection of output phase
RESET: Master reset line (all registers, DLL, FSM)

Output signals
CONV_CLK: Phase corrected ADC strobe
PACKET: Indicates the start of a conversion cycle (25ns pulse)
DATA_VALID: Active (high) for the time analog data are present at the ADC input
BCO_TR1: Active (high) for the time digital data (trailer) are present at the DATA_OUT output
DATA_OUT: Digital data restored to internal CMOS levels (0, 5V)
PD_DOWN: Indicates DLL lock

VLSI Design Methods

The design description for an integrated circuit may be described in terms of different levels of abstraction. From the top down, these levels are

- architectural or functional (behavioral) level
- register transfer level
- logic level
- circuit level
- physical description (layout)

In each of these levels there are a number of design options that maybe selected to solve a particular problem. Depending on the type of circuit (analog, mixed-signal, digital logic), different design flows are preferable or even necessary. Other constraints, as optimization for high speed operation, low power or small area as well as economical motivations (time-to-market) can influence the choice of the design method. On top of that, the need for scalability or flexibility for the transfer to different processes or even the availability of design tools can play a role. Within one design, for example a mixed-signal ASIC, different design flows for the different sub-blocks can be employed.

Three basic design methods can be distinguished, however a combination of two or all three of them is sometimes a feasible or even necessary approach.

Full Custom Design

Full Custom Design is the most fundamental design technique. The designer has total control over the geometrical properties of every physical layer on the silicon, thus controlling the exact behavior of each device (transistor, capacitor, …) by creating it, defining the geometry, size and location of every diffusion area or polysilicon gate. The routing is done by manually placing contacts and drawing metal interconnects. This design method is used for analog circuitry as well as if optimization for noise, power, speed or area is crucial. However, it is the most complex and also time consuming technique, and requires the highest level of experience and expertise from the designer.

Simulations can only be done in an analog way (SPICE type), requiring a vast amount of time and computing power. Thus only small circuits or sub circuits of larger systems can be verified.

Semi Custom Design

Semi Custom or Standard Cell Design relies on a library of common sub blocks (logic gates, flip-flops, inverters, sometimes also OP-amps, comparators, ADCs, DACs, …) provided by the foundry. The circuit is constructed, using the functionality of the predefined cells. The layout can be done by hand, hence placing the cells and draw the interconnects, or using automatic Place&Route tools. For the cells, the foundries usually provide transistor-level netlist and high level functional descriptions in one of the common hardware description languages (VHDL and Verilog), including timing

information, load and drive properties. Thus, behavioral (functional) as well as analog (SPICE) simulations are possible. So called mixed-mode simulators provide an interface between high-level and analog simulators, giving the possibility to run different simulators on different sub-blocks of a design simultaneously. Functional simulation and timing verification of large systems is possible.

The main disadvantage of this design approach is, that the cells are usually not optimized in any respect, e.g. for performance or silicon area.

High Level Design And Synthesis

High Level Design With Synthesis represents an expansion on standard cell design. This technique allows top-down design of sub-blocks or entire ASICs, starting from behavioral (functional) description to the final layout. Synthesis tools create circuitry from the high-level description code using the standard cell library of the target process. Place&Route tools conduct the floorplanning, placing and connecting of the cells and I/O pads, routing of the power nets, down to the final layout. Post layout simulation and final verification (Design Rule Check, Layout-Versus-Schematic comparison) is done on the automatically generated layout. The simulation possibilities are the same as with Semi Custom Design.

Depending on the quality of the HDL code, synthesis can result in good, fast circuitry as well as in weird constructions and/or big, complicated circuits. Anyhow, optimization of synthesized schematics by hand is possible. The most prominent advantage of this method is the possibility of fast design of large and complex logic systems. The main drawback is again the lack of custom optimization.

Figure 62. shows the design flow for full custom design and high level design with synthesis.

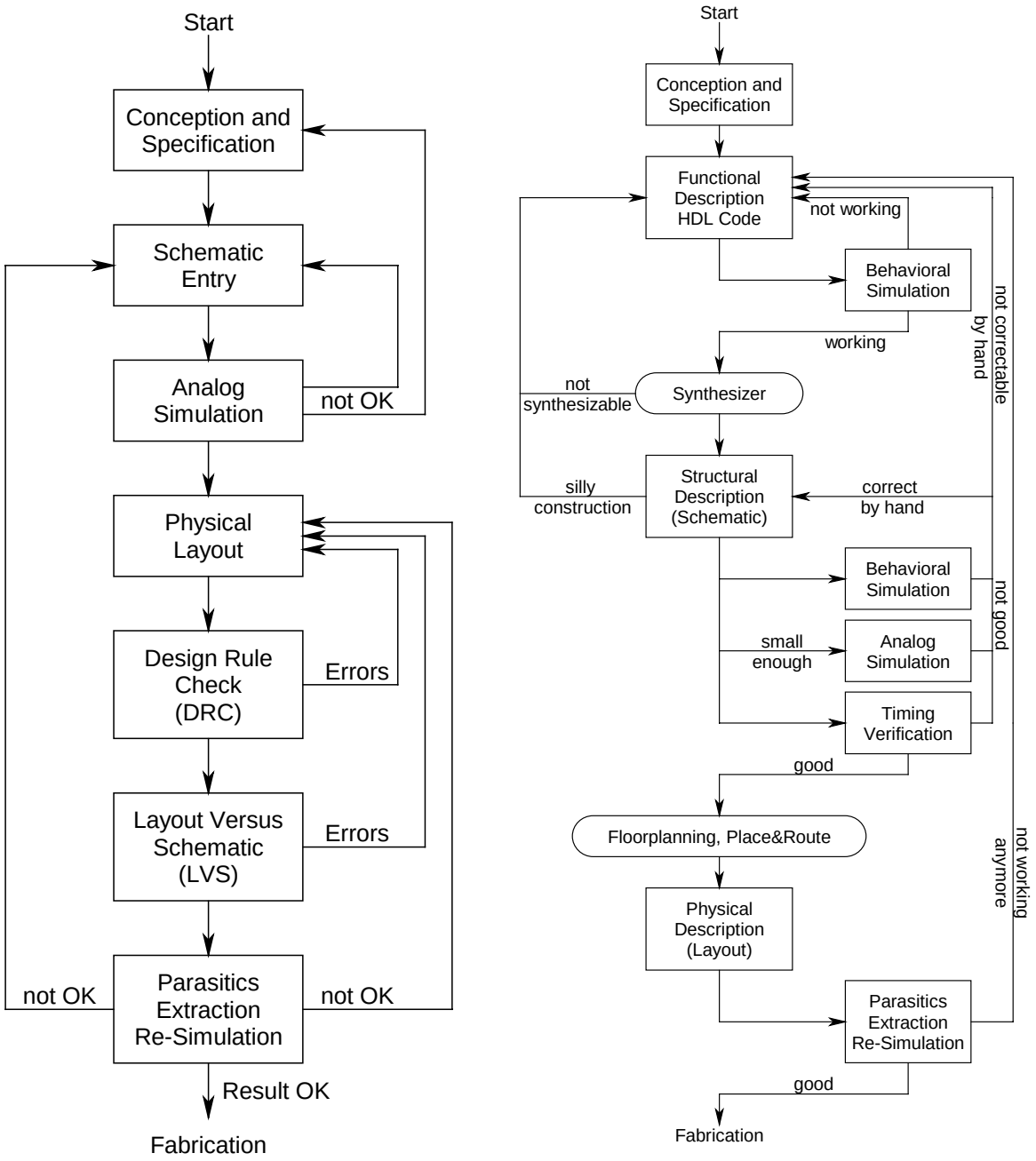


Figure 62. Design flow for full custom design (left) and high level design with synthesis (right)

CSC Architecture

Figure 63 shows the block diagram of the CSC chip architecture. The main building blocks comprise a delay locked loop (DLL), a finite state machine (FSM) for the header identification, the phase detection and clock selection units and a self calibration circuit using a dummy loop. A 9-bit counter organizes the generation of the control signals.

The design was started with a behavioral description of the entire system, using the *Verilog* Hardware Description Language (HDL). The specified functionality was verified by means of behavioral simulation. In principle, this code could have been applied directly to a circuit synthesizer. However, the result would haven been, assuming successful synthesis, a very complex and inaccessible construction, impossible to optimize or correct. Thus, the functionality has been divided into several sub-blocks, which were treated independently and connected together manually. Furthermore, the generator of the timing reference, chosen to be a delay-locked-loop structure, is not synthesizable at all.

For the design of the individual sub-blocks, all above described design methods were employed, depending on the type of the sub-block. The delay-locked-loop, as it is an analog circuit, was implemented in full custom design. The header identification FSM as well as the clock selection unit were synthesized from Verilog code. For the design of the phase detection circuit and the counter, the standard cell design method was used. The dummy structures for the auto calibration circuit, again, were done in full custom.

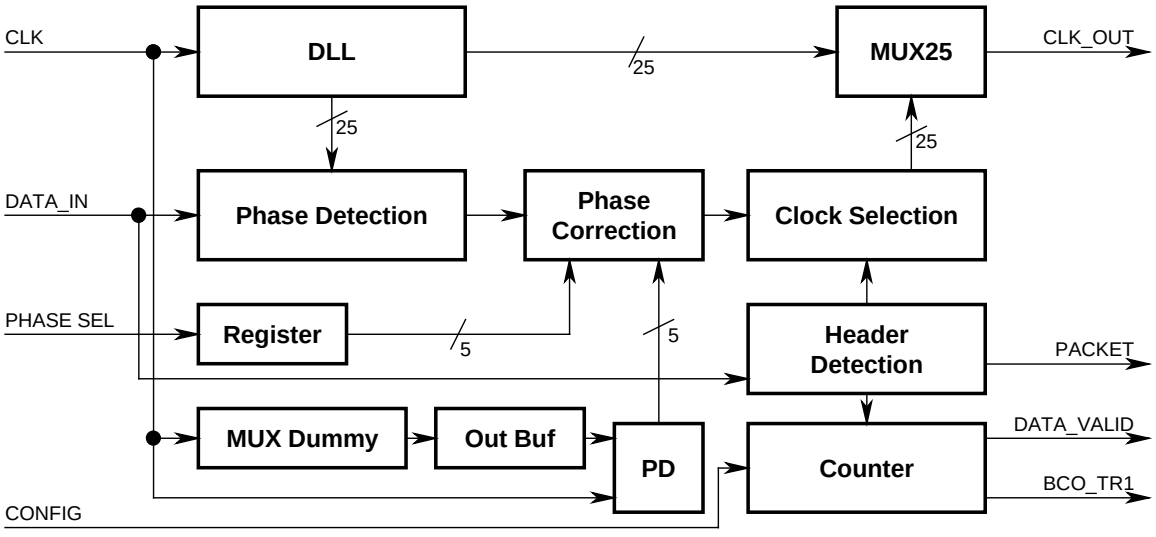


Figure 63. CSC block diagram

The Building Blocks

Phase Detection (Phase-to-Digital Converter)

The delay-locked-loop derives 25 copies from the incoming 40 MHz clock with phases equally spaced by 1 ns, thus covering one complete clock cycle. The phase detection units uses these reference clock signals to latch the incoming data into a row of 25 static D-flip-flops. The outputs of these cells are clocked into a second row of static D-flip-flops by the master clock. This procedure yields a "thermometer code" for the position of each transition edge on the data line relative to the phase of the master clock. The phase information is turned into 1-of-25 code by means of sequential logic (Invert, shift-by-one, AND) and subsequently encoded into 5-bit binary. In case of a successful header identification, these data are sent to the clock selection circuit, which updates the phase of the output conversion clock. Thus, the output phase is readjusted for each data packet.

This building block constitutes a 5-bit Phase-to-Digital Converter with an LSB of 1 ns. The full scale range is 25 ns, resulting in 7 missing codes or an effective number of 4.65 bits. The RMS quantization error can be calculated to

$$\sigma_Q = \frac{LSB}{\sqrt{12}} \cong 290\,ps \quad (1.16\%\ of\ \ full\ scale) \qquad (5.1)$$

Integral and differential non-linearity were measured. The results can be found on pp. 103. Due to the locked-loop architecture, there is no offset or gain error. The nominal conversion rate is 40 MHz.

The clock selection circuit chooses the phase of the output clock, depending on the data from the edge detection unit, the measurement of the auto-calibration loop, and the contents of the programmable phase selection register.

Header Identification

The mixed signal data packet sent by the front-end chip (SCT128A) consists of a 4-bit digital header pattern, 3 calibration levels (used for calibration of the analog optical link), 128 channel-data and a 9-bit digital trailer (Figure 64).

The CSC uses a finite state machine (FSM) with "one-hot" encoding for header detection and identification. In order to start a conversion cycle, the consecutive reception of a correct bit pattern (4 bit, "0101") is required. This decreases the probability of detecting non-existing data packets due to noise and spikes on the data line. After a successful header identification, a short pulse (1 clock cycle) is put out on the HEADER_DETECT line and the unit goes into an idle state in order to avoid false triggers due to misinterpretation of signals from the analog part or the trailer of the data packet. At the end of the data transmission, the FSM goes back to its active state, monitoring the input line for the next data packet.

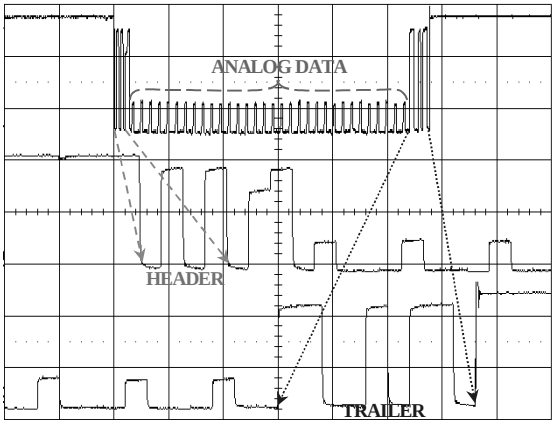


Figure 64. Scope view of a data packet of the SCT128A front-end chip; test pulses are applied to every fourth channel

Generation Of Control Signals

A readout cycle is triggered by a HEADER_DETECT pulse, sent by the header detection FSM. On arrival of the pulse, a 9-bit counter is initialized and starts operating depending on the mode, set by the CONFIG bit. The DATA_VALID signal goes active on the first rising edge of the clock after the header detection. At the beginning of the trailer, DATA_VALID is reset and the signal indicating the trailer (BCO_TR1) becomes active. The 9-bit trailer data, restored to CMOS levels, can be accessed on the DATA_OUT line. This constitutes the end of one readout cycle and the CSC goes back to its initial state.

In two-chip mode, 2 data packets from adjacent front-end chips are joined together sequentially. In this case, the trailer of the first packet and the header of the second packet are being ignored by the CSC. The DATA_VALID signal goes low during this period and becomes active again at the beginning of the analog data sequence of the second chip. The additional information is extracted out of the second trailer (both trailers contain identical data).

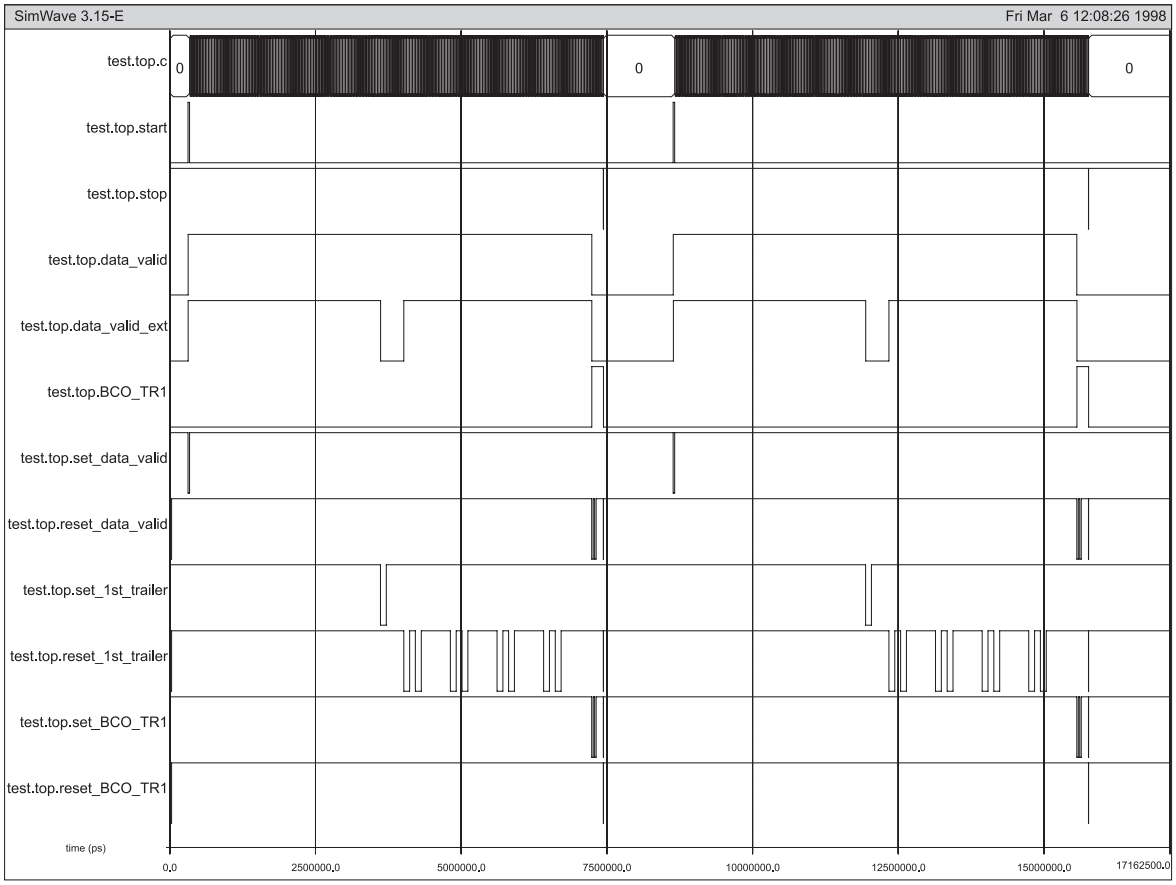


Figure 65. Generation of the control signals in two-chip mode

Figure 65 shows the result of a functional simulation of the control signal generator in two chip mode. The first signal *top.c* represents two incoming data streams, each composed of the data packets of two SCT128A readout chips. *top.start* contains the start commands, sent by the header detection unit at reception of the packets. *top.data_valid_ext* is the signal which appears at the DATA_VALID output pin. It is active (HIGH) at presence of analog data. Note the LOW phase during the trailer of the first packet and the header of the second in the middle of the combined data stream. *top.BCO_TR1* is HIGH at the end of the stream for the extraction of the second trailer. *top.stop* is the stop-bit, generated by the counter. The other signals *top.set._** and *top.reset_** are internal and serve to check for the correct function of the control signal generator.

The Timing Reference: Delay Locked Loop (DLL)

In order to generate an accurate low-jitter timing reference for a PDC – resolution of 1ns, a delay locked loop (DLL) structure was chosen. It consists of a voltage controlled delay line, a phase detector, a loop filter and a charge-pump [33], [14]. The delay line is a chain of 2 times 25 current-starving inverters. The delay of each individual inverter is controlled by the loop control voltage V_c. The signal edge coming out at the end of the delay line is compared against the incoming clock signal through a phase-detector, deriving a binary decision whether the signal delay was longer or shorter

than one period of the reference clock (25 ns at 40 MHz). The phase detector is implemented as a balanced flip-flop. The decision of the phase detector (either *early* or *late*) is used to control a charge-pump, which increases or decreases the charge on the loop-filter capacitor, thus changing V_c and its associated delay value.

Delay line architecture

Every tap of the delay line, corresponding to a nominal delay of 1 ns, consists of two identical current starving inverter cells. The output of each of these inverters connects to another inverter acting as a buffer between the delay line and the multiplexer. The schematic of a current starving inverter delay cell is shown in Figure 66. The basic current starving inverter structure consists of an ordinary CMOS inverter (T1, T2) being connected to the supply rails via voltage controlled current sources (T3 and T4, with gate voltages V_p and V_n. Two shunt transistors (T5, T6) were added to linearize the delay vs. voltage characteristic of the delay cell and to assure a finite delay time even if the starving transistors are cut off.

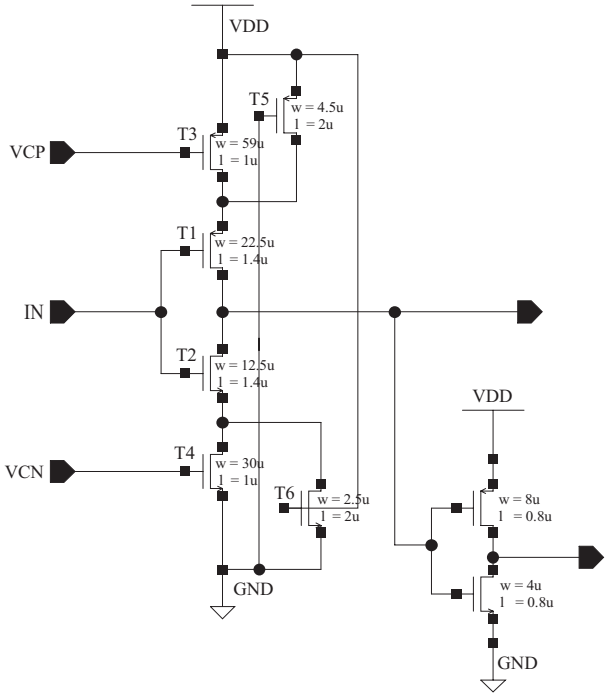


Figure 66. Current starving inverter cell

Figure 67 shows the delay vs. voltage relationship. The nominal delay value of 1 ns will be achieved within all process corners. The ratio of the delay times for slowest and fastest case is about a factor of 2.7. The plot indicates that a clock frequency range from 12 MHz to 80 MHz should be achievable for typical process parameters. By scaling down the power supply voltage V_{DD}, additional slowing down of the inverters is possible, extending this range further down.

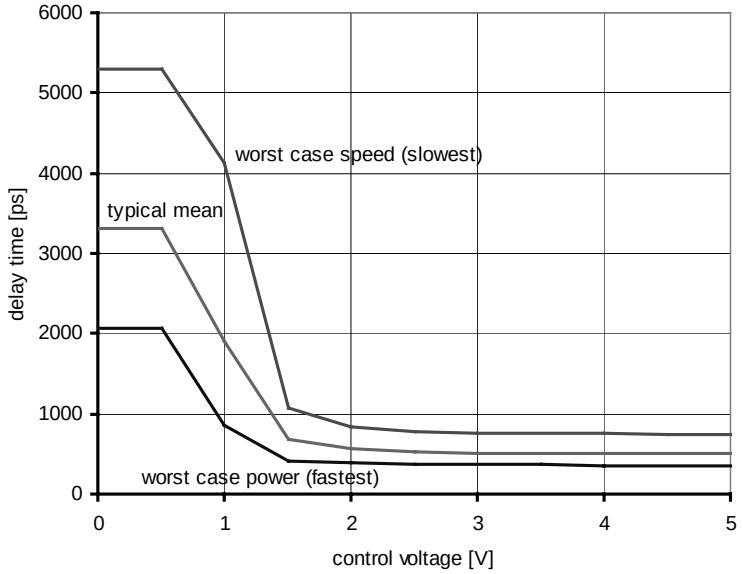


Figure 67. Delay time versus control voltage (Spice simulation) at typical mean and two process corners

Phase detector and charge pump

The DLL uses a balanced flip-flop as a phase detector [33], which samples the delayed signal with the non-delayed clock. The decision of the phase-detector is maintained during a whole clock period. Dummy cells have been used in order to ensure equal capacitive load for both input signals.

The charge pump conducts small currents to and from the loop capacitor, according to the decision of the phase detector. Driver circuits convert the control voltage at the output of the loop filter to the gate source voltages V_n and V_p of the NMOS and PMOS starving transistors. To avoid long oscillation cycles in the control loop, it is necessary that the gate voltages change as fast as possible. Using big transistors result in small timing constants and fast transient behavior, but also in high consumption of static power. So there is a trade off between power consumption and jitter. In this design, the time constant of the starving transistor drivers is approximately one clock cycle (25 ns). The second function of the starving transistors drivers is to provide buffering between the control voltage V_c and the gate-source voltages of the delay stages, thus avoiding coupling from the delay channels to the integration capacitor. Another limiting factor to the jitter is the value of the loop capacitor. As integrated capacitors are very area consuming, they cannot be made arbitrarily large. Therefore, there is another tradeoff between jitter and area. Figure 68 shows an analog simulation of the lock-in process of the DLL. The upper trace shows the input clock (dashed) and the DLL output clock after 25 delay cells. The lower trace is the voltage V_C, which controls the charge pumps.

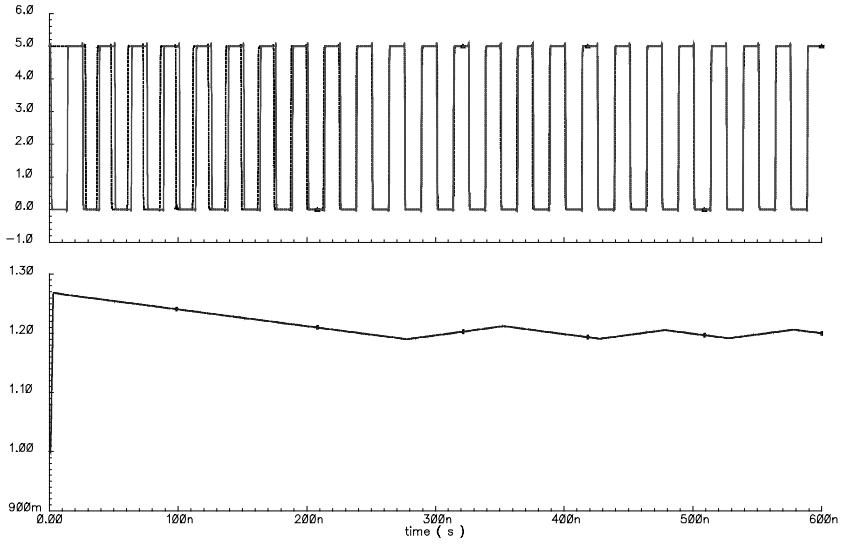


Figure 68. SPICE simulation of the lock-in process of the DLL.

Auto Calibration And Numerical Phase Correction

In order to correct the phase of the output conversion clock for changing delays due to temperature or process parameter variation or different load capacitances, a self-calibration structure was incorporated in the chip. It consists of a dummy signal path that represents the path of the conversion clock through the chip including the output buffer. From the output pad, which can be loaded with the actual load capacitance, the signal is fed back into the chip. A second phase detector permanently measures the signal delay in multiples of 1ns and stores the result as 5-bit binary code. This number is utilized to tie the positive edge of the output clock to approx. 1 ns before the end of each data time slot.

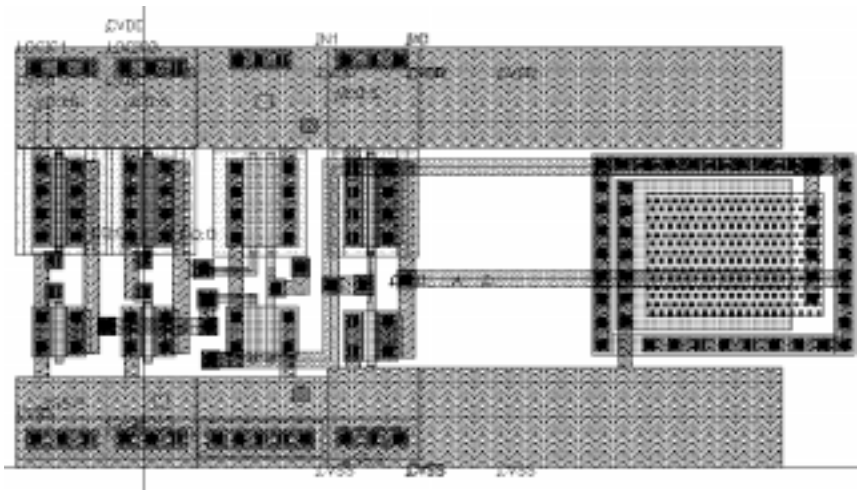


Figure 69. Part of the dummy signal path, representing the multiplexer. The clocked inverter in the middle is loaded with the output capacitances of 24 inverters of its type. The poly-poly capacitor on the right side provides this capacitance.

The contents of a 5-bit register can be used to select earlier clock phases in 1ns steps to accommodate timing requirements of different A/D converters. The register can be loaded any time and has a separate reset line.

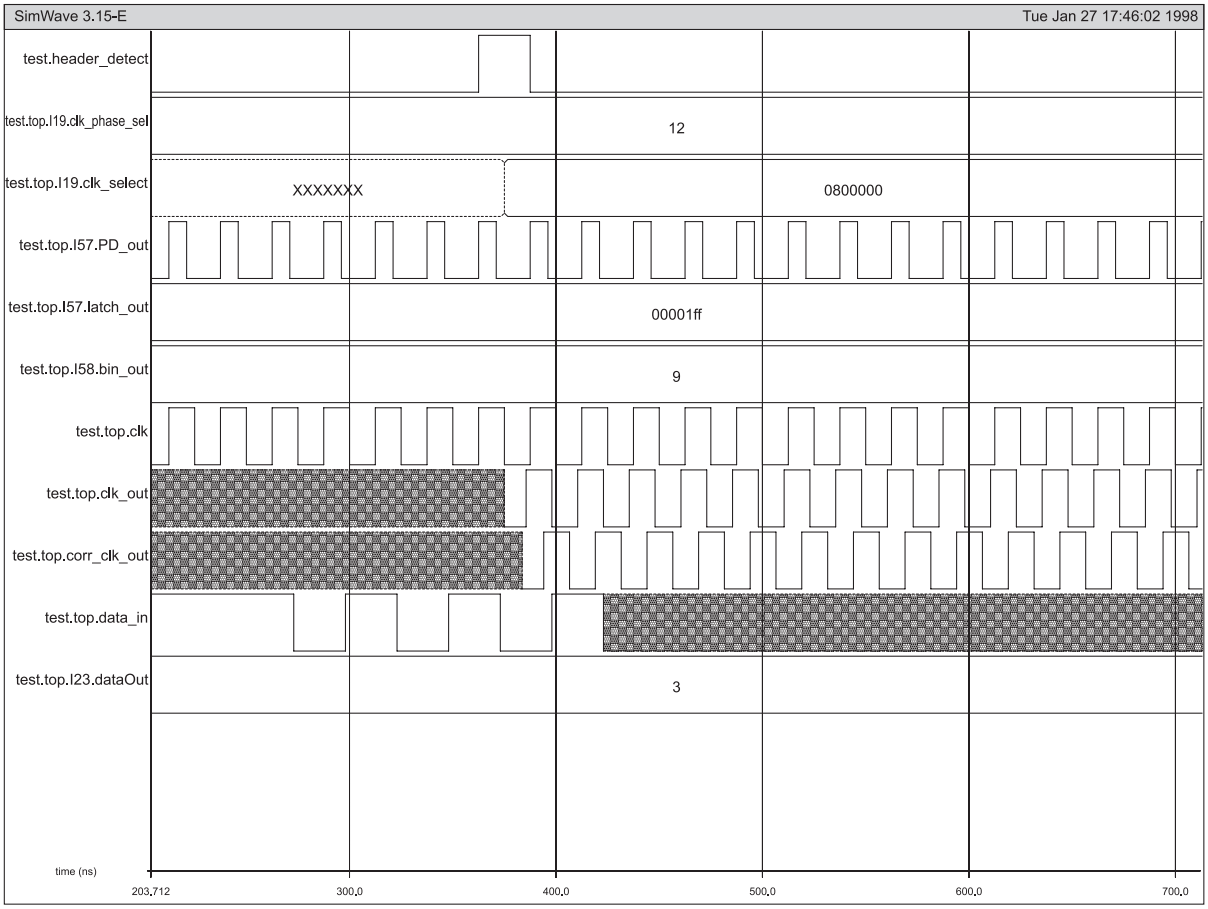


Figure 70. High-level simulation of the auto-calibration and phase correction circuit

Figure 70 shows the result of a high-level (Verilog) simulation on the auto-calibration and phase correction circuit. The trace *top.data_in* contains the input stimulus, a simulated data packet, which arrives at an arbitrary time of ~ 275 ns after time zero. The "0101" bit pattern, representing the header plus a further "01" pair to clarify the exact time of transition after the header, is followed by "unknown state" for the time of the analog data. The delay of the signal path through the chip, including the output buffer, is arbitrarily set to 8564 ps. The phase selection register content is set to 3 (*.top.I23.dataOut*).

The first trace *.header_detect* shows the pulse, sent by the header detection FSM in answer to the incoming data packet at the first rising edge of the main clock *.top.clk*. Trace 4 (*.top.I23.PD_out*) is the output of the phase detector of the calibration loop. The width of each pulse represents the signal delay through the loop, measured once per clock cycle. Trace 6 contains the result of this delay measurement in 5-bit binary. The result, 9 ns (the loop delay was set to 8,564 ns), indicates the correct function of the unit. This number is added to the contents of the phase selection register ("3") and

applied to the clock selection unit, which selects the phase of the output clock accordingly (*.top.I19.clk_phase_sel*). Traces 7 through 9 show the input clock (*.top.clk*) and the derived signals. Trace 8 (*.top.clk.-out)* contains the clock phase, as it would have been chosen without the auto-calibration loop, trace 9 (*top.corr_clk_out*) is the final clock, as it actually appears at the CONV_CLK output pad. Note the first rising edge of the correct clock *top.corr_clk_out* being ~ 3 ns before the "01" transition after the header as selected, while the clock phase without correction (*.top.clk.-out*) would be wrong by the mentioned 9 ns.

Self Unlock

Verilog simulations and timing verification of the entire system unveiled certain, though unlikely, situations where parts of the system would fail due to lock-up or undefined-state situations. Two self set-reset circuits have been implemented in the phase detection unit and the header identification state machine.

Data-Latch<0> Set

It was discovered that for a certain phase relation between main clock and incoming data, the edge detection circuit would fail to respond with the correct state, leaving all flip-flops of the data_sync register in the zero state. This state was found to correspond to the situation where clock and data have almost exactly the same phase, thus bit 0 of the clock-select bus should be in state HIGH. A circuit was implemented into the edge detection unit, which produces a short pulse at each rising edge of the main clock if all data_sync latches are in LOW state. This pulse is sent to set the asynchronous set input of the edge-detection-latch corresponding to bit 0 in the moment the header detect pulse is active, thus bringing the system back to its correct state. The self correction circuit is shown in Figure 71.

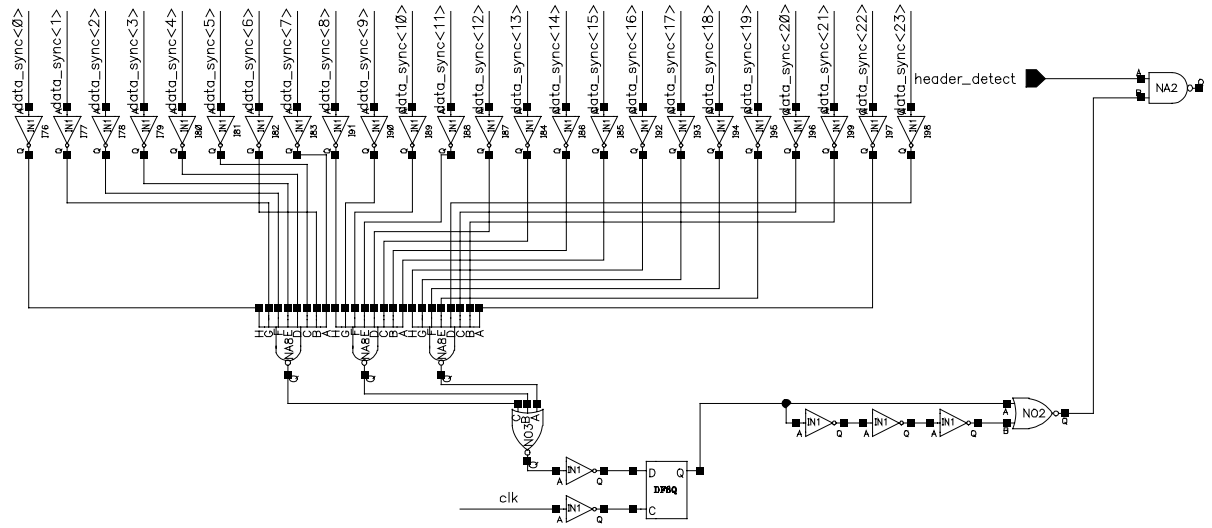


Figure 71. Self correction circuit of the edge detector for the equal-phase failure

Auto Reset Of The State Machine

The header detection state machine uses one-hot encoding, thus forbidden states occur if more than one of the state flip-flops is active. The circuit showed faulty behavior for certain input signal conditions. An auto reset circuit for the “state-zero” flip-flop has been incorporated that sets the FSM to a valid state whenever a faulty state is detected.

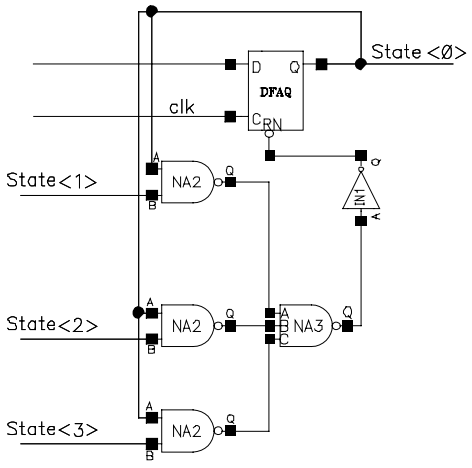


Figure 72. Auto Reset of “State<0>” in the header detection FSM

After implementation of the two corrective circuits, no further system failure has been detected by high-level simulation and timing verification, scanning the phase relation between clock and data packet in steps of 10 ps over the entire range.

In total, 9 buffer amplifiers were inserted or replaced to overcome load violations, detected throughout the verification process.

System Simulation

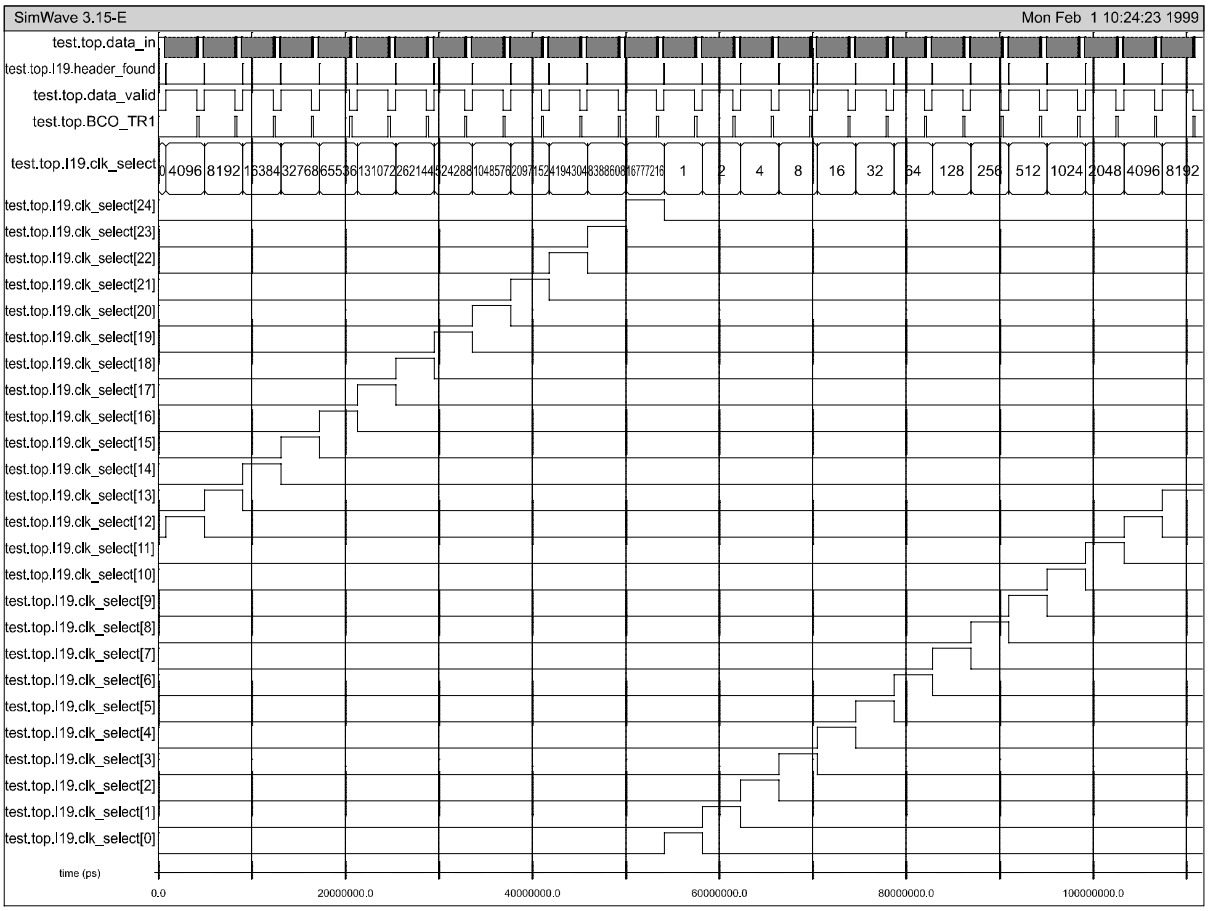


Figure 73. High-level simulation of the entire system, including the corrective circuits

Figure 73 shows a high-level simulation of the entire system, including the corrective circuits. The first trace (*.top.data_in*) contains the stimulus, consisting of 26 consecutive data packets. The phase of each packet relative to the clock is set back by 1 ns with respect to its predecessor. The second trace (*.top.header_found*) shows the header detection pulse for each packet, traces 3 and 4 (*.top.data_valid* and *.top.BCO_TR1*) the respective control signals. Traces *.top.I19.clk_select[0]* to *.top.I19.clk_select[24]* contain the selected output phase for each data packet in 1-of-25 code. The clock phase select register content is set to "3" and the signal delay through the auto calibration loop to "10", summing up to "13". The first data packet arrives in-phase with the clock, yielding the output phase "12" (= 25 – 13). The subsequent packets, each arriving with 1 ns phase shift, produce the desired clock select code. The simulation also demonstrates the cyclic behavior of the system. Other simulation of the same type were done, using steps of 100 and 10 ps for the phase shift between the packets. The results did not unveil any failure of the system, due to timing violations, logic race or lock-up conditions.

As a last and final verification, an analog SPICE-type simulation was carried out on the complete system. Although the size of the ASIC is rather small (~ 10.000 transistors), the simulation of the first

600 ns after a reset with a data packet arriving at 340 ns, took 14 hours on a state-of-the-art UNIX workstation[2]. The result of the simulation is shown in Figure 74. *PD_DOWN*, a signal from the Phase Detector of the DLL, indicates successful lock. The trace *PACKET* contains the header detection pulse of the FSM in answer to the data packet, shown in trace *DATA_IN*. *DATA_VALID* goes active and the chip starts putting out the conversion clock with the correct phase. Also shown are the main clock (*CLK*), the *DATA_OUT* signal and the reset line (*RESET*). As this type of simulations uses device models rather than derived behavioral descriptions and/or timing models, the results are as close as possible to reality. Successful analog simulation indicates the highest possible chance of a working design.

For all simulations, CMOS level (0, +5 V) input signals were assumed.

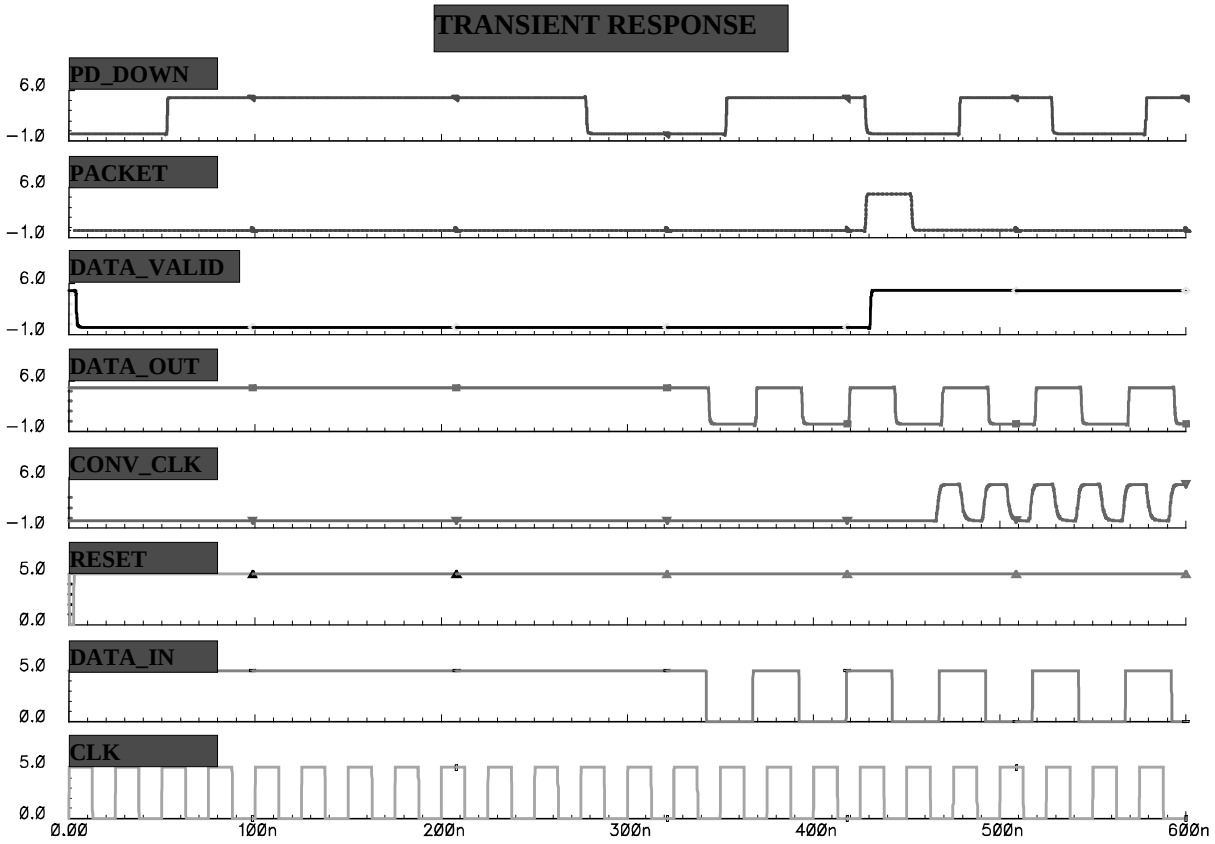


Figure 74. Analog (SPICE) simulation of the complete system. First 600 ns after a reset with a data packet arriving at ~ 340 ns.

[2] For large designs, one has to trust in the results of high-level simulation.

Layout

The target process was chosen to be a standard 0.8µm CMOS process, for it combines the required performance with a moderate price. The operating location of the CSC, close to the ROD in a low radiation environment, did not force the use of a radiation hard or tolerant process. The AMS double-metal, double-poly CMOS process "0.8 µm CYE" was found suitable for the CSC design. Although a very generous power supply routing was chosen, using 6 core and 4 peripheral power supply pads and double concentrical core power rings, the layout turned out very compact. With 8 input and 6 output pads, yielding a total of 24 pads, and a gate count of ~ 10.000 transistors, the die size, including scribe lines, is 2105 2695 µm^2. Two 20 pF decoupling capacitors were placed close to the power connections for the analog DLL block to minimize the effects of digital switching noise. The layout is shown in Figure 75.

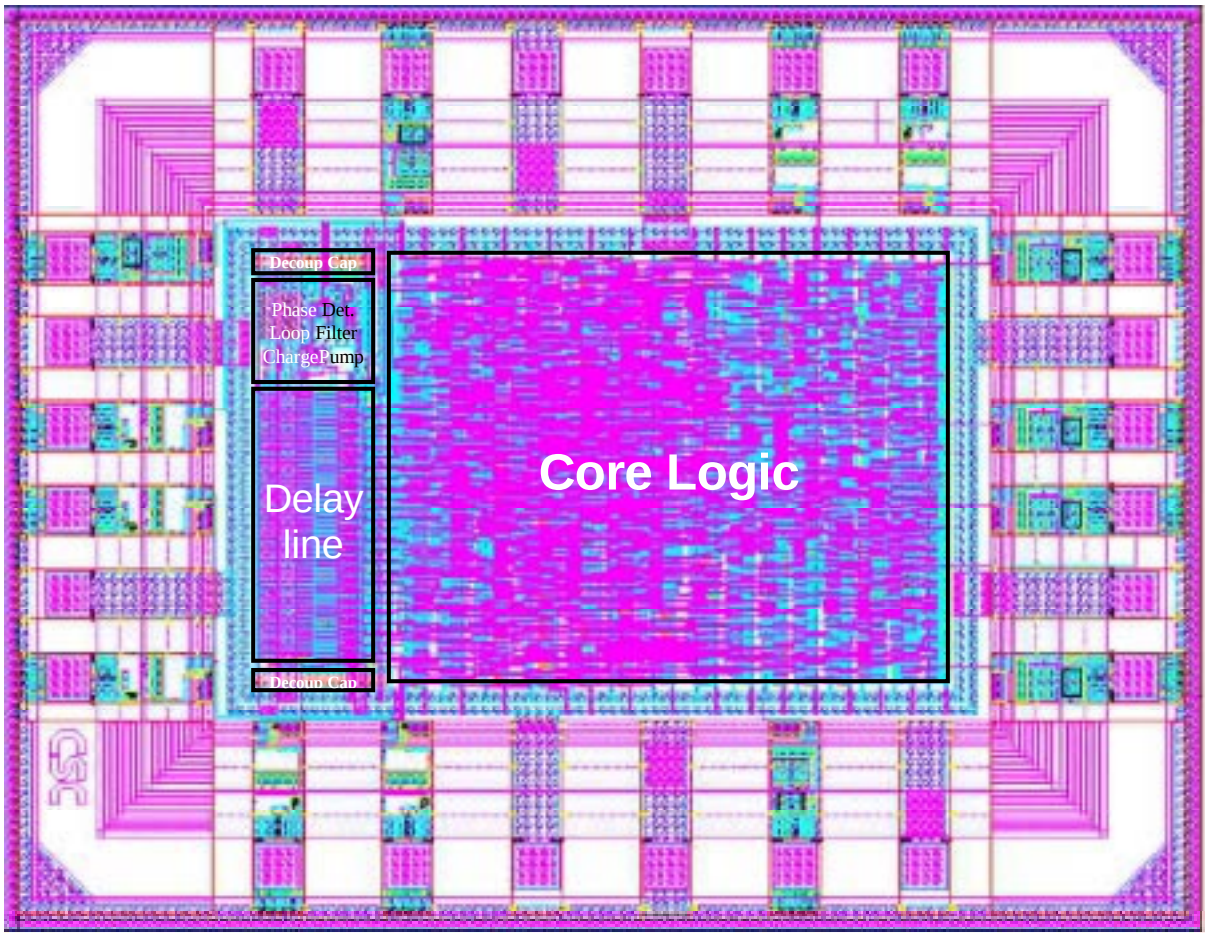


Figure 75. CSC layout

Testing and Measurement Results

Functionality tests and measurements were carried out on prototype samples after fabrication at AMS. The chip was glued to a custom made chip carrier, connecting the metalized backplane substrate contact to ground. All pads were wire-bonded, the inputs terminated with 50 Ω chip resistors on the carrier.

The laboratory test setup consists of a programmable pattern generator for composing the signals to be sent to the chip, a reset generator, power supply and a DSO (digital storage oscilloscope). The entire setup is controlled by a PC via GPIB bus. Input signals were either taken from the pattern generator or directly from the multiplexer output of a SCT128A, running on a test-bench next to the setup.

Functionality

For the functionality tests, all environmental conditions were set to nominal values:

- 40 MHz input clock frequency
- +5 V power supply
- CMOS type input signals

The prototype shows full functionality, all internal logic blocks work according to their specifications and to the simulations.

The performance of the header detection FSM, the block which has to deal first with the input data, is dependent on the signal quality of the incoming headers. A large variation of the width of the consecutive time slots, containing the header, can result in the loss of a data packet. This could happen, if the bandwidth of the data link between the readout chip (SCT128A) and the CSC is too small. However, this situation will not appear in the real experiment and furthermore, a failure would only occur under certain additional circumstances (phase of the clock and the data packet very close to each other). Another restrictions, concerning the header detection, was discovered experimentally. By scanning the entire range of possible phase relations between clock and data, it was unveiled that for a data packet, arriving between 0.7 ns before and 2.7 ns after the rising edge of the clock, no stable edge detection could be accomplished. Under certain circumstances, this would even send the header detection state machine into a lock-up state, where it needs a reset in order to resume normal operation. That means, that a fraction of about 3.4 ns (~ 13 %) of the whole phase range is dangerous. A possible solution for this problem is given in “Suggestions For The Redesign”, p. 107.

No further functionality failures were discovered.

Power Consumption, Power Supply Range And Clock Frequency Range

Figure 76 shows the power consumption of the CSC as functions of the clock frequency and the supply voltage. The nominal power consumption (f = 40 MHz, V_{DD} = 5 V) is < 140 mW.

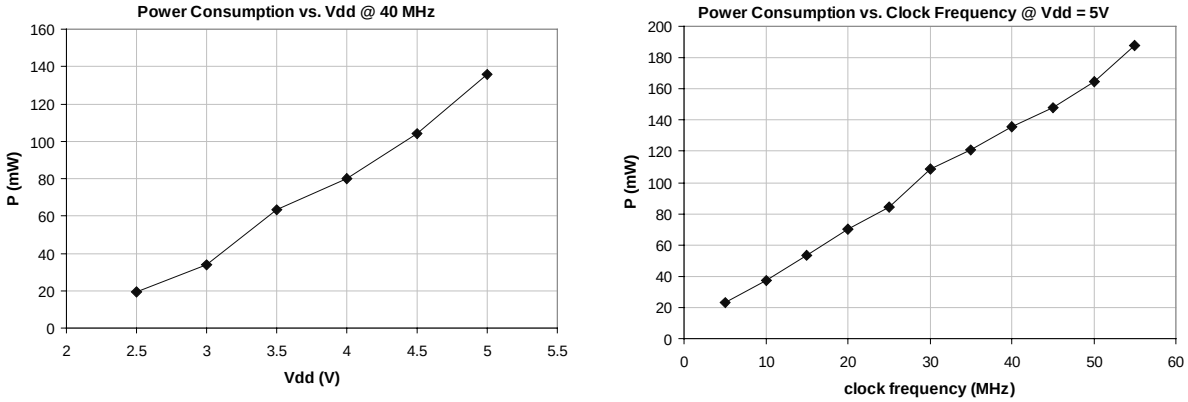


Figure 76. CSC power consumption

Full functionality could be achieved within a clock frequency range of 15 MHz to 80 MHz. Reduction of the power supply voltage, resulting in a down-scale of the process speed, yields an absolute minimum clock frequency of 5 MHz.

CSC is able of exhibiting full 40 MHz operation down to a power supply voltage of 3.3 V.

Clock Jitter And Phase-to-Digital Converter Performance

Performance measurements on the PDC verify that the desired timing resolution can be obtained with sufficiently low jitter and good linearity. The output clock jitter scales linearly with the delay cell number and is mainly caused by the up-down cycles in the feedback loop. The jitter was measured to range from 17 ps for the first to 185 ps RMS for the last delay cell (Figure 77). The mean value μ_J = 109 ps.

The integral nonlinearity of the PDC, the deviation of the values of the reference levels from their ideal values, is shown in Figure 78. The maximum integral nonlinearity measures 325 ps or ~ 1/3 LSB. The distribution exhibits a sigma of ~ 120 ps. The scope view shows the nonlinearity (center of the traces) as well as the jitter (width).

The step width varies from 500 ps to 1375 ps showing a Gaussian-like distribution with a sigma of 154 ps, providing a measure for the differential nonlinearity of the phase detector (Figure 79). Due to the locked loop architecture, there is no gain error in the transfer function (the mean of all delay step values is 1).

A measure for the RMS error of the converter can be defined:

$$\sigma = \sqrt{\sigma_Q^2 + \mu_J^2 + \sigma_{DNL}^2} = 345 \; ps \; RMS \qquad (5.2)$$

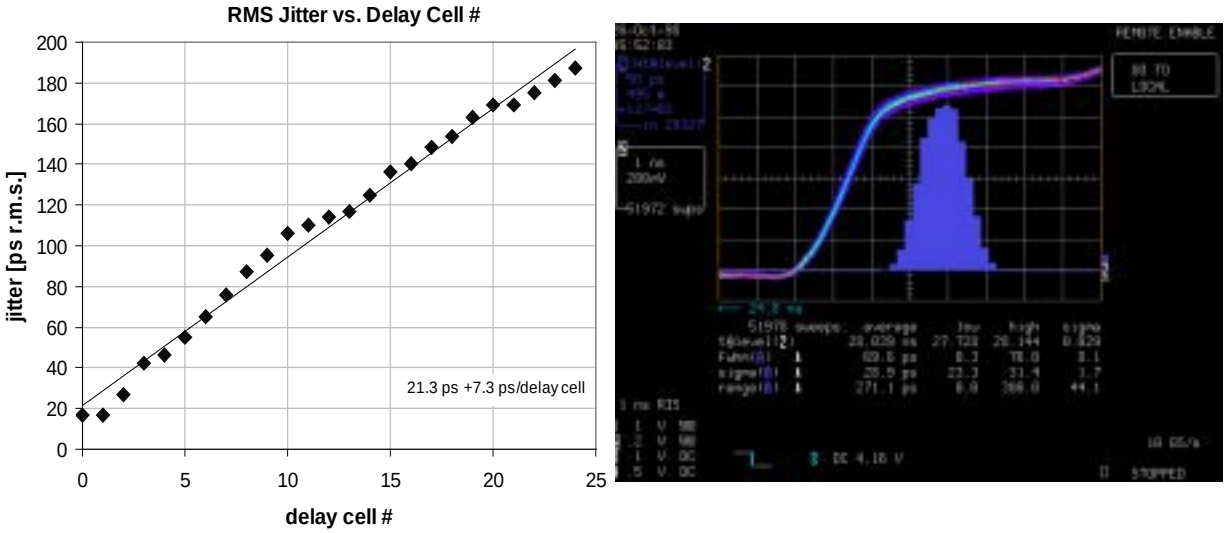


Figure 77. Output clock jitter. The scope view on the right hand side shows the trace of the clock edge #3 in persistence mode and the histogram. The sigma of this distribution yields the data point in the plot.

`sigma(A)  28.9 ps`

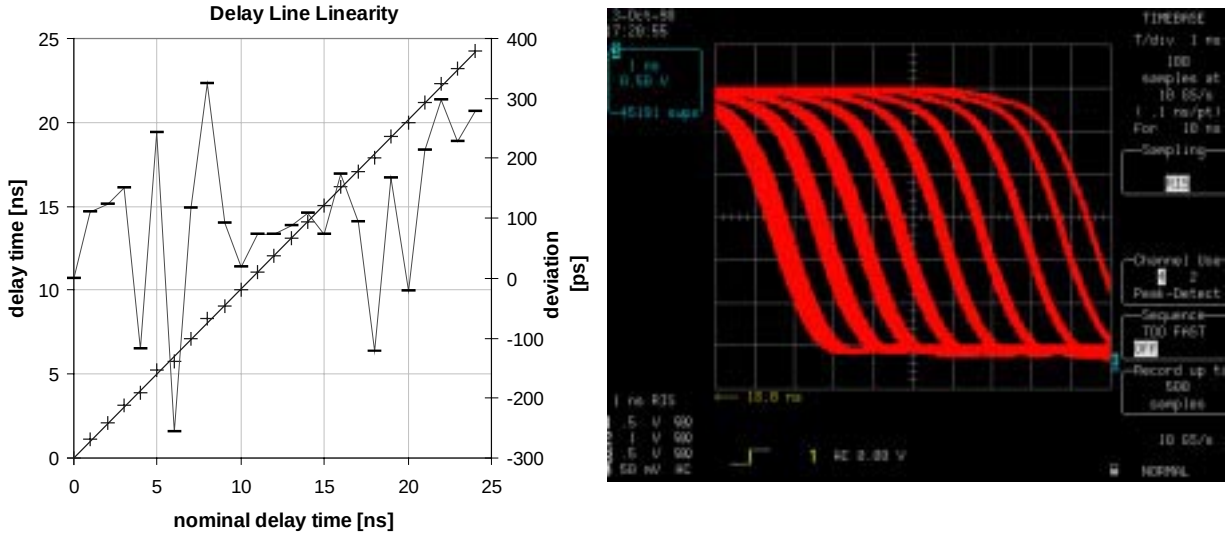


Figure 78. Integral nonlinearity of the PDC. The squared data points follow the ideal straight line with slope 1. The second set of points show the deviation for each level of its ideal value in ps (right scale). The right hand side picture is a scope view of the first 9 clock edges in persistence mode.

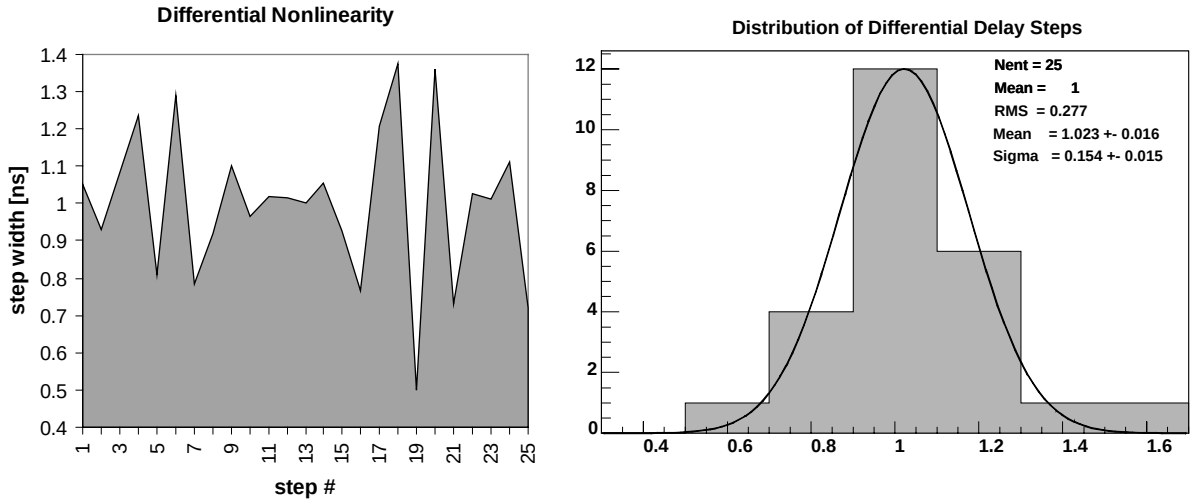


Figure 79. Differential non-linearity of the phase detector and distribution of the differential delay steps.

Behavior Of The Auto Calibration Loop

The characteristic curve of the auto-calibration circuit in Figure 80 shows the correction of the output clock phase as a function of the load capacitance at the EXT_CAP pad. The data points which lie in the middle between two steps represent values of load capacitances where the calibration circuit chose the steps equally likely. A linear fit to the data points exhibits a slope of 0.09 ns/pF. The AMS CYE data book gives for the used output pad OB33 a signal delay versus load capacitance characteristic according to: $t_D(C_L) = t_{D0} + 0.1\ ns/pF$.

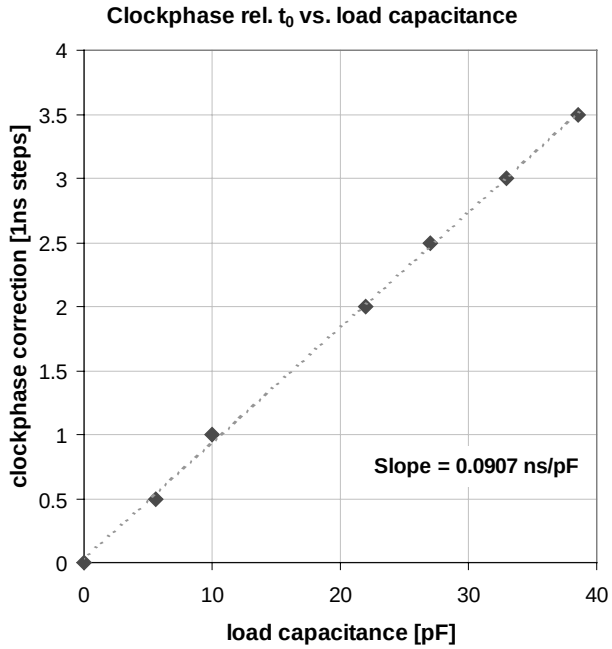


Figure 80. Calibration loop characteristics

Suggestions For The Redesign

Improved Header Detection

In order to overcome the problem concerning the header detection state machine, which was described above, one possible solution would be the over-sampling of the incoming data (sampling at a higher frequency). A simple and robust approach is to employ a second header detection unit, which samples the incoming data with a phase shift of 180 degrees (at the falling edge of the clock). After successful identification of a header, each state machine puts out the *header_detect* pulse and sends a reset to the other one. The outputs are simply OR connected. In this case, each of the units had only to cover 50 % of the input phase range, while a single one already covers 87 %. In addition, the sensitiveness to time slot variations would be reduced to a large extent.

Additional Functionality

In addition to the basic functionality, described throughout this chapter, the conversion itself and parts of the data processing that needs to be done at ROD level, could be incorporated into the CSC. A flash-type ADC with a nominal conversion rate of 40 MHz is and a resolution of 8 bit is realizable with the chosen technology. A hardware implementation of cluster-building and zero-suppression algorithms, before as well as after the conversion, is possible, but complex. The present design can be translated into the BiCMOS version of the process, if additional functionality would require bipolar devices.

Furthermore, all signal I/O could be equipped with LVDS (Low Voltage Differential Standard) translators, as this standard may become the common signal format for LHC experiments. An automatic gain controlled (AGC) input stage would be desirable for the data input from the optical receiver.

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