Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects

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Abstract

We discuss design issues related to the extensive use of Enclosed Layout Transistors (ELT's) and guard rings in deep submicron CMOS technologies in order to improve radiation tolerance of ASIC's designed for the LHC experiments (the Large Hadron Collider at present under construction at CERN). We present novel aspects related to the use of ELT's: noise measured before and after irradiation up to 100 Mrad (SiO_2), a model to calculate the W/L ratio and matching properties of these devices. Some conclusions concerning the density and the speed of IC's conceived with this design approach are finally drawn.

I. Introduction

Enclosed Layout Transistors (ELT's, also called elsewhere edgeless transistors) have already been used in the early days of CMOS [1,2] and their effectiveness together with guard rings in preventing leakage currents in irradiated integrated circuits is well known [3,4]. In that case, the total dose tolerance of the design was limited by the radiation effect in the gate oxide. The ultra thin gate oxide of deep submicron technologies is inherently more tolerant to total dose effects than the thicker oxides encountered in less advanced technologies [5,6]. Deep submicron processes are therefore attractive for the design of ASIC's for the radiation environment of the LHC experiments, which is composed of pions, protons and other charged hadrons and neutrons. In such an environment, SEE's can occur only through nuclear interaction of the hadrons with the material constituting the IC's or in their close environment. In this paper we will address only total dose issues; a study of SEE's in a 0.25 μm technology is presented in [7]. The total dose tolerance required over a life cycle of 10 years varies from less than 10 Krad in the experimental cavern to a maximum of 30 Mrad in the detector closer to the beam interaction point. The use of ELT's and guard rings in deep submicron technologies allows to satisfy these requirements, and using this approach we can profit at the same time from all the other advantages of these technologies, such as speed, reduced power consumption, high level of integration, high volume production (and consequently low cost) and high yield.

In the last three years we have designed several test chips that have been manufactured in some advanced commercial technologies available, from 0.7 to 0.25 μm. We have therefore accumulated experience in the new design issues arising from the extensive use of edgeless devices for the design of complex IC's. Such issues are discussed in this paper.

II. Experimental Details

A. Technology and Test Structures Description

We have chosen to implement the test chips in a 0.25 μm CMOS technology which is a purely commercial process, i.e. nothing is done by the foundry to harden the gate or the field oxides. The basic features of the selected technology are given in Table 1.

Table 1
Technology features.

VDD	2.5 V
Gate Oxide Thickness	5.5 nm
Process	Twin well CMOS
Device Isolation	Shallow Trench (STI)
Polysilicon gates doping	Dual (n^+ and p^+)
Ti salicidation	On n^+, p^+ polysilicon and diffusions
Interconnectivity	2 to 5 metal layers

The test chips that have been designed for this study contain the following test structures:

- single transistors (edgeless and standard, n-channel and p-channel) with different gate lengths;
- very wide (W = 2 mm) transistors for noise measurements, edgeless n-channel and normal p-channel, L = 0.36, 0.5, 0.64, 0.78 and 1.2 μm. Such a large W was chosen to have an high white noise density in current at the drain and because very wide transistors are often needed in the front-end IC's for High Energy Physics experiments;
- 5 matched edgeless n-channel transistor pairs with different gate lengths (L = 0.36, 0.5, 1, 2 and 5 μm);
- field oxide transistors with polysilicon and metal gate, diffusion to diffusion or diffusion to well, with or without guard rings;
- digital standard cells (inverters, nand and nor gates, flip-flops) laid out with the proposed approach.

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B. Static and Noise Measurements Setup

For the static measurements we use a Semiconductor Parameter Analyzer (HP4145B) connected to a Semiconductor Test Fixture (Keithley 8007) through a Switching Matrix (Keithley 707); everything is controlled by a PC running a custom developed Labview program. This allowed to minimize the time to perform the high number of measurements required (especially for the matching study).

The noise current at the drain of the transistors is measured with a transimpedance stage using a low noise wide band op-amp followed by a second gain stage. A Spectrum Analyzer (HP3588A) is used to read the output of the second stage during the gain, noise and background measurement stages and to inject a known signal during the gain measurement. The noise is then referred to the gate after background subtraction dividing by the gain. The DUT is biased with batteries, except for the drain voltage during measurements in strong inversion (i.e. a drain current of 20 mA); in this case we use a power supply, as the noise introduced is negligible compared with the noise to be measured. The noise spectrum has been measured from 200 Hz up to 30 MHz.

C. Irradiation Procedure

To test the radiation tolerance of our devices and circuits we have used 10 KeV X-rays (with the Seifert RP149 irradiation system at CERN, using dose rates varying from 5 to 25 Krad/min) and a ^{60}Co source (the CNR/FRAE gamma cell in Bologna, Italy, with a dose rate of 3 Krad/min). All the irradiations have been performed under worst case bias, i.e. the bias conditions that really occur in a circuit and that maximize the irradiation effects. All the terminals are grounded for the p-channel transistors and all the terminal are grounded except for the gate which is biased at V_{DD} for the n-channel transistors.

Annealing has been performed on irradiated samples following the ESA/SSC Basic Specification No. 22900, i.e. 24 h at room temperature and 168 h at 100° C (under worst case bias).

III. Results and Discussion

A. ELT Parameter Degradation

Transistors (ELT and standard) irradiated up to 10 and 30 Mrad (SiO_2) under worst case bias have shown limited threshold voltage shifts: 15 mV for n-channel and -30 mV for p-channel after 10 Mrad, 35 mV and -70 mV after 30 Mrad. After the annealing these values were respectively 45 mV and -55 mV.

In deep submicron technologies the device isolation is generally made with shallow-trench isolation (STI). This successor of the LOCOS does not eliminate the problem of leakage currents from drain to source in standard n-channel devices (as proved by the curve A in Figure 1).

Results obtained with irradiated field oxide transistors have shown that STI does also not prevent leakage between devices, and that the use of guard rings is still necessary [8]. No leakage current has been observed after irradiation of edgeless devices, as shown in Figure 1, and measurements of the irradiated field oxide transistors with guard rings have shown similar results.

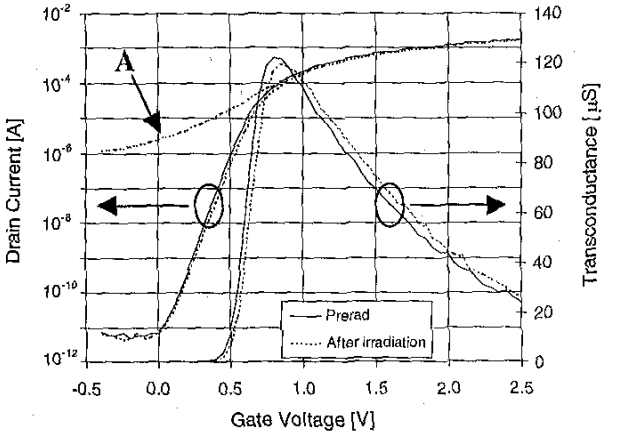

Figure 1: Drain current (log scale) and transconductance before and after 30 Mrad (SiO_2) for an edgeless n-channel (L = 0.28 μm) and drain current for a normal n-channel (L = 0.28 μm) after 1 Mrad (SiO_2) (curve A).

Very little degradation (less than 6%) of transconductance, mobility and subthreshold swing has been observed (Fig. 1), indicating very little creation of interface states after 30 Mrad (SiO_2).

These results confirm the intrinsic radiation tolerance of deep submicron technologies and the effectiveness of ELT's and guard rings in preventing leakage currents.

B. Noise measurements

Noise performance and its degradation are very important for analog design. We have therefore explored the noise in the 200 Hz – 30 MHz bandwidth, in weak, moderate and strong inversion.

At low frequency, the noise of MOS transistors is dominated by the 1/f (or flicker) noise, which can be expressed as [9]

$$\frac{\overline{dv_{1/f}^2}}{df} = \frac{K_a}{C_{ox}^2 WL} \cdot \frac{1}{f^{\alpha}} \qquad (1)$$

where K_a should be a constant, for a given technology, with two different values for n-channel and p-channel transistors, C_{ox} is the gate capacitance per unit area and α is a parameter close to 1. Measurements of the wide transistors (W = 2 mm) before irradiation have shown that 1/f noise of n-channel devices exhibits an unexpected noise increase for device lengths below 0.64 μm, as can be seen in Figure 2. Short n-channel

devices should hence be avoided in analog designs for better noise performances.

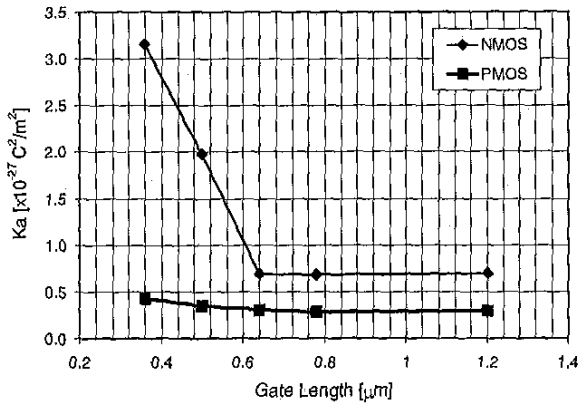

Figure 2: 1/f noise parameter K_a for n-channel and p-channel transistors as a function of the gate length.

We irradiated the devices up to 30, 60 and 100 Mrad (SiO_2) with 10 KeV X-rays. We have reached such a high dose, well beyond our goal (i.e. testing the radiation tolerance of our approach), to try to make a correlation between the increase of the oxide traps and of the 1/f noise. We have noted such a tendency after irradiation, but it was very difficult to make an exact correlation due to the small degradation of the transistor parameters even after 100 Mrad. After annealing, we have seen a decrease of the 1/f noise for n-channel transistors (Fig. 3), confirmed by an annealing of the oxide traps. For p-channel we have measured an annealing of the oxide traps whilst the 1/f noise seems to increase slightly (Fig. 4). A similar behavior has been observed in [10], where its origin was attributed to the positive bias during annealing.

The white noise increases after 100 Mrad by 15% for n-channel devices and 7% for p-channel's, and stays constant after annealing. The white noise at the input of a MOS transistor can be expressed as

$$\frac{\overline{dv_{w.n.}^2}}{df} = \frac{4kT}{g_m} \cdot \gamma \qquad (2)$$

where T is the absolute temperature, k is the Boltzmann constant and g_m is the transconductance. γ is equal to $2/3 \cdot \Gamma$ in strong inversion and $1/2 \cdot \Gamma$ in weak inversion, where Γ is the white noise excess factor. The increase in the noise, even if very small, was found to be higher than expected from the decrease in the transconductance.

Figure 3 and 4 show examples of the noise for two devices (one n-channel and one p-channel) before irradiation and after irradiation and annealing. The measurements shown have been made in the moderate inversion region (I_D = 500 µA) and in saturation (V_D = 800 mV). Comparable degradation of the noise parameters was measured in weak and strong inversion.

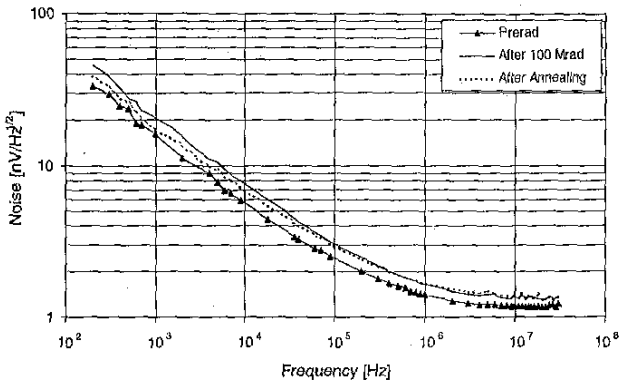

Figure 3: Noise spectrum for an enclosed n-channel (2000/0.5 µm), before irradiation and after irradiation and annealing.

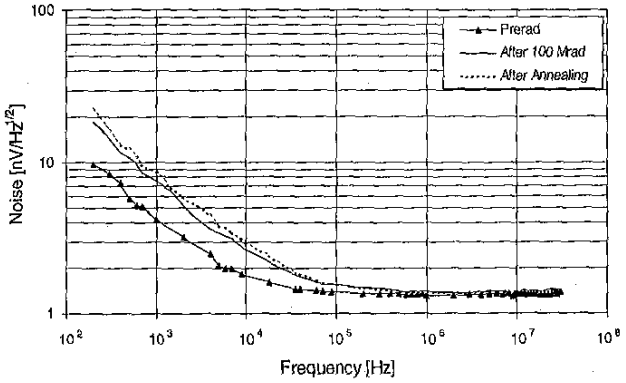

Figure 4: Noise spectrum for a standard p-channel (2000/0.5 µm), before irradiation and after irradiation and annealing.

From a designer's point of view we can conclude that the noise increase even after 100 Mrad is compatible with our low noise applications, and that short n-channel devices should be used carefully wherever low-frequency noise determines the overall noise performance of the circuit.

C. ELT Model

Our study of edgeless transistors, aimed at the design of radiation tolerant IC's, brought us to investigate unexplored issues for these devices. The main topics, whose knowledge is crucial for analog design, are the need for a good model to compute the aspect ratio, the limitation in the effective W/L ratio that can be achieved and the lack of symmetry in the device.

There are many different possible shapes for ELT's, e.g. square, octagonal, square with the corners cut at 45°, and each shape needs to be modeled separately. We have decided to adopt the shape shown in Figure 5, that is compatible with the design rules of many deep submicron technologies. The size *c* is kept small and constant varying the L, making the current flowing mainly in two orthogonal directions and ensuring in this way a better uniformity.

We will now focus on this shape for the modeling of the

W/L ratio; more information about modeling of a generic ELT can be found in [11].

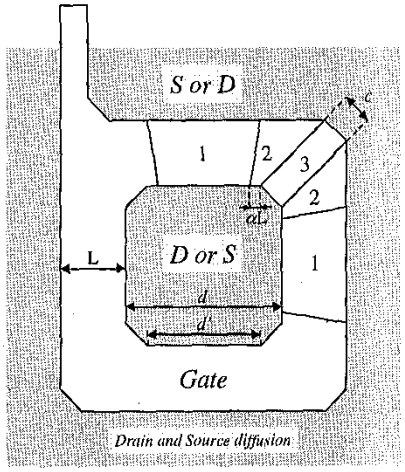

Figure 5: ELT shape. The transistor can be thought of as being formed by transistors of three different kinds in parallel, labeled in the picture 1, 2 and 3.

Studies of the electric field under the gate of the device, supported by simulations, lead to the following formula:

$$\left(\frac{W}{L}\right)_{eff} = \underbrace{4\frac{2\alpha}{\ln\frac{d'}{d'-2\alpha L_{eff}}}}_{1} + \underbrace{2K\frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5}\cdot\ln\frac{1}{\alpha}}}_{2} + \underbrace{3\frac{d-d'}{L_{eff}}}_{3} \quad (3)$$

where c, d, $d' = d - c \cdot \sqrt{2}$ and α are shown in Figure 5. L_{eff} is used in the formula to take into account for the gate length shortening due to underdiffusion, photolithography and etching. After testing on different CMOS technologies scaling from 2.5 μm to 0.25 μm, α has been found to be almost technology independent, 0.05 being the best fit to the experimental data. The above expression has been derived decomposing the transistors in three parts, labeled 1, 2 and 3 in Figure 5 and represented in the formula by three terms. The first part corresponds to the linear edges of the transistors, the second to the corners without the 45° cut, which is taken into account separately from the third part. Due to the presence of the polysilicon strip, necessary to integrate the gate contact outside the thin gate oxide region, the third term in the formula is multiplied only by 3. Since the polysilicon strip has a constant width, the parameter K is geometry dependent, being 7/2 for short channel transistors ($L \leq 0.5$ μm) and 4 for longer devices.

The good agreement between the formula and measured W/L ratios is shown in Table 2. The effective W/L of ELT's has been extracted by comparing their drain current with the drain current of standard devices with the same L for the same $V_{GS} - V_{th}$. The drain of ELT's was considered to be the inner contact.

Table 2
Calculated and extracted $(W/L)_{eff}$ for edgeless transistors.

L_{drawn} (μm)	Calculated $(W/L)_{eff}$	Extracted $(W/L)_{eff}$
0.28	14.8	15
0.36	11.3	11.2
0.5	8.3	8.3
1	5.1	5.2
3	3	3.2
5	2.6	2.6

The shape of the enclosed transistors does not allow aspect ratios lower than a certain value. To obtain high W/L values it is sufficient to stretch the device in one or two dimensions, without modifying the corners; the calculation of the obtained W/L is straightforward. To have low aspect ratios the only way is to increase the L keeping the minimum size for the distance d. Increasing L in the formula leads the terms 1 and 3 to decrease, and after a certain value of L the constant term 2 will dominate. In the case of the geometry of Figure 5 the minimum W/L achievable is ~ 2.26, and it is almost reached with L = 7 μm. Values close to this also imply a considerable waste of area, compared to the standard transistors, and should be avoided using different circuit topologies.

We have observed an asymmetry in the output conductance, related to the non-symmetrical geometry of the device. Since the gate is annular, the source and drain contacts can be chosen inside and outside the ring of the gate, or vice versa. Table 3 shows the measured values for the drain inside (G_{di}) and outside (G_{do}). The fact that G_{do} is lower can be explained as follows: the distance between the pinch off point and the drain, due to the conservation of the space charge region for the same bias potentials, will be smaller when the drain is outside. An increase of V_{DS} will in this case increase less the drain current, resulting in a lower G_{do}. The asymmetry between G_{di} and G_{do} increases with L as the outer perimeter of the gate increases with L, while the inner does not. We have also compared the output conductances G_{di} and G_{do} of ELT's with the one of normal devices (G_{dn}). We have found that for $L \leq 0.5$ μm $G_{dn} \approx G_{di}$, while for larger gate lengths G_{dn} values are close to the mean of G_{di} and G_{do} values. Therefore the output resistance achievable with ELT's is higher than for normal devices.

Table 3
Output conductance for enclosed n-channel transistors of different gate length. G_{di} = inner diffusion as drain, G_{do} = outer diffusion as drain. Difference = $(G_{di} - G_{do})/G_{di}$.

L_{drawn} (μm)	G_{di} (μS)	G_{do} (μS)	Difference (%)
0.28	11.89	9.62	19
0.36	7.17	5.55	23
0.5	4.10	2.73	33
1	1.68	0.79	53
3	0.57	0.17	70
5	0.41	0.10	75

Another asymmetry that needs to be considered in designing an integrated circuit is that the inner terminal capacitance is smaller than the one of the outer contact. This must be taken into account for example when pass-gates are used, because the charge injection towards the outer contact is higher.

D. ELT's Matching

Matching properties of transistors of identical geometry are critical for analog applications, as for example in differential pairs and current mirrors. We have studied the statistical properties of the difference in V_{th} (ΔV_{th}) and in β ($\Delta\beta/\beta$) for pairs of identically laid out edgeless n-channel transistors as a function of the gate area. We have measured 100 chips with 5 pairs each, extracted V_{th} and β for each transistor (with a procedure similar to the one proposed in [12]) and calculated ΔV_{th} and $\Delta\beta/\beta$ for each pair. The obtained histograms have been fitted with gaussian curves, and from them we have extracted $\sigma_{\Delta Vth}$ and $\sigma_{\Delta\beta/\beta}$. We have plotted these values as a function of the inverse of the square root of the geometrical area (S_g), as shown in Figure 6 for $\sigma_{\Delta Vth}$.

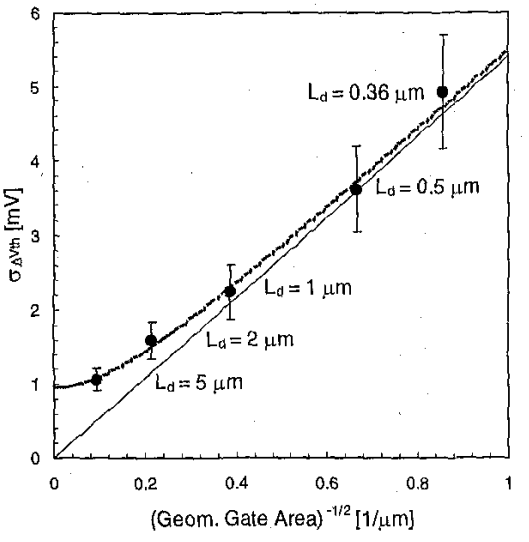

Figure 6: $\sigma_{\Delta Vth}$ values for five couples of enclosed n-channel devices of different gate lengths. The X axis is the inverse of the square root of the geometrical gate area. The straight line represents the theoretical behavior described in [13], and is the asymptote of the dotted line.

The values can be fitted by the following equation

$$\sigma_{\Delta V_{th}} = \sqrt{\left(\frac{A_{V_{th}}}{\sqrt{S_g}}\right)^2 + \sigma_0^2} \qquad (4)$$

The classical formula for $\sigma_{\Delta Vth}$ does not contain the parameter σ_0 [13]. In our case $\sigma_{\Delta Vth}$ values show a good linear slope for small devices, and a kind of "saturation" behaviour for larger devices. Best-fit evaluation leads to the following values for the equation parameters: A_{Vth} = (5.40 ± 0.38) mV·μm and σ_0 = (0.95 ± 0.12) mV. A_{Vth} fits well with the value based on the literature benchmark $A_{Vth} = K \cdot t_{ox}$ were t_{ox} is the gate oxide thickness (about 5.5 nm in a 0.25 μm technology) and K is a constant which is found to be around 1 mV·μm/nm for many different technologies [14].

The plot of $\sigma_{\Delta\beta/\beta}$ show the same kind of behaviour, and again the curve can be fitted with the equation

$$\sigma_{\Delta\beta/\beta} = \sqrt{\left(\frac{A_\beta}{\sqrt{S_g}}\right)^2 + \sigma_0^2} \qquad (5)$$

where the best-fit evaluation for the parameters leads to A_β = (1.49 ± 0.16) %·μm and σ_0 = (0.33 ± 0.05) %. A_β is comparable with the other technologies values found in literature [15].

E. Device Density and Speed Considerations

ELT's and guard rings decrease the device density that can be achieved with the technology. For analog design the area penalty is important only for long channel edgeless devices; if there are few of this kind of transistor in the circuit, the increase in area will not be significant. For digital design, a comparison has been made between several digital standard cells laid out with and without the proposed approach. The area penalty factor introduced was found to be between 1.5 and 3.5.

This loss in density is unavoidable if we want to use a standard deep submicron technology for our applications. On the other hand, the alternative to our approach is to use a radiation hardened technology; these technologies are some generations behind the most advanced commercial CMOS technologies. If we compare the density of a 0.25 μm technology using edgeless transistors and guard rings with, for example, a 0.6 μm standard technology (which is 2 generations older), the former still achieves a higher density, up to a factor of 3.2 (depending on the circuit). This comparison has been made designing circuits with our approach and with a 0.6 μm standard technology (an example is shown in Figure 7). We have seen that increasing the complexity of a digital gate the area benefit factor decreases, but in a complete digital circuit it is always at least 1.5. In all the designs we have only used two levels of metal, whilst in deep submicron technologies one could use more levels of metals and improve in this way the density.

Although the use of ELT's slows down digital circuits due to an increase in the node capacitances, it still remains faster than other less advanced technologies. For example, the delay of an inverter biased at 2V with fan-out of 1 is 2.4 times less than that of its standard counterpart in a 0.6 μm technology (biased at 3.3 V), and consumes 10 times less power.

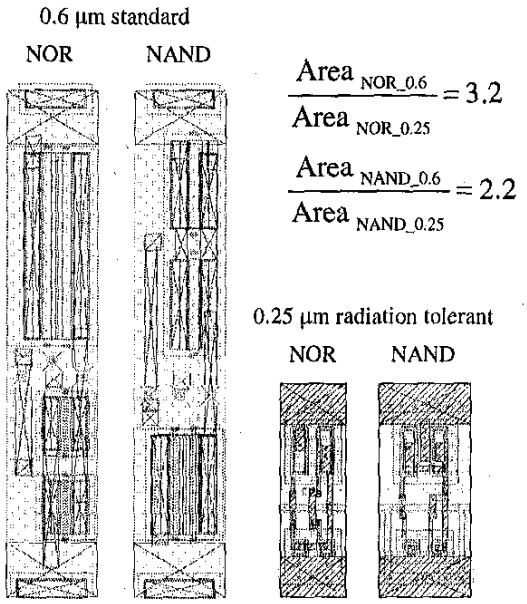

Figure 7: Comparison between areas of two digital gates laid out in a standard 0.6 μm technology and in a 0.25 μm technology with ELT's and guard rings.

IV. Conclusions

The very thin gate oxide of deep submicron technologies (~ 5 nm for a 0.25 μm) is inherently more radiation tolerant than the one of older technologies. We have verified that threshold voltage shifts, subtreshold slope and transconductance degradation after 30 Mrad (SiO_2) are small enough to be fully tolerable for our designs.

Nevertheless STI does not prevent post irradiation leakage in deep submicron technologies, and the use of Enclosed Layout Transistors (ELT's) and guard rings is still necessary. Test chips conceived with this design approach have proven its effectiveness.

To simulate and design an IC using ELT's, the characteristics of these devices are essential. We have derived a formula to calculate the W/L ratio which turned out to be very precise, and we have measured the output resistance and the noise as a function of the gate lengths. Noise characteristics are very important for front-end amplifiers for High Energy Physics, and we have also measured the noise degradation after irradiation: white noise increases by 15% for n-channel and 7% for p-channel after 100 Mrad (SiO_2), which is low enough to be compatible with our applications.

Finally, we have used the results of our study to design digital and mixed-mode circuits in a quarter micron CMOS technology which could tolerate total doses of 30 Mrad (SiO_2) [16]. To help in the design of complex digital IC's with the suggested approach, a digital library has been designed in a 0.25 μm technology. These circuits have allowed us to estimate the design density achievable with such design technique and have confirmed that our radiation tolerant design approach allows the use of standard deep submicron technologies for LHC applications.

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