

The ALICE dimuon trigger : Overview and electronics prototypes

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Abstract

ALICE is the LHC experiment (2005) dedicated to the study of heavy ion collisions. Amongst the ALICE sub-detectors, the muon spectrometer will investigate the dimuon production from heavy resonance ($J/\psi, \Upsilon$) decays, which is believed to be a promising signature of the QGP (Quark Gluon Plasma) formation.

For maximum efficiency of the spectrometer, a dedicated dimuon trigger is presently built. The detector part itself is based on RPCs operated in streamer mode and is the topic of another contribution to this conference. This paper gives the principle and the simulated performances of the trigger and is also focussed on the description of the electronics prototypes and future developments. The RPCs are read-out by X and Y orthogonal strips : the front-end chips are presently developed. The signals are sent to the trigger electronics which basically performs a p_t cut on the tracks to reduce the background. A prototype of fast (decision time 200ns) programmable electronics working in a pipelined mode at 40 MHz has been built and tested. This prototype handles simultaneously 160 digital information from the strips. The tests of the trigger card have required the construction of a pattern generator (160 bits at 40 MHz).

1 Trigger principle

The trigger has to select events of interest, containing a dimuon from the decay of a resonance J/ψ or Υ amongst all possible background sources. The main source of background is clearly the low p_t component of muons from pion and kaon decays.

For this reason, a cut on the transverse momentum of the tracks is performed by the trigger to reduce the background. The principle of this cut (on single tracks) is explained in Fig. 1. The magnetic deviation δY_2 between the two trigger stations MT_1 and MT_2 is measured by the trigger electronics. A cut on δY_2 increasing proportionally to R_f (radial position in the dipole middle-plane) is equivalent to a p_t cut, at first order.

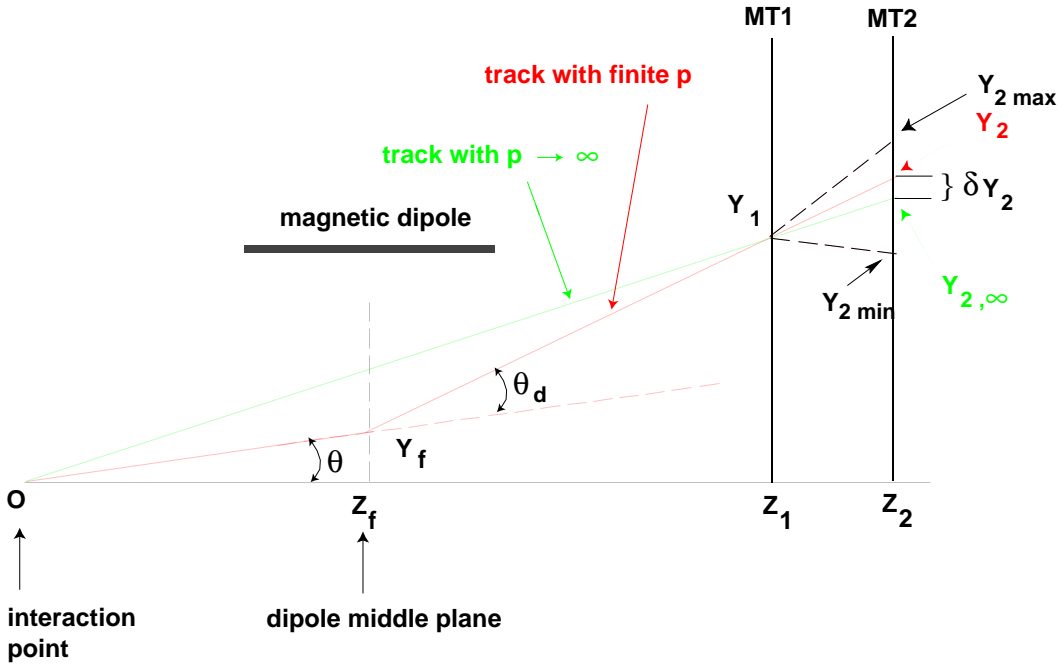


Fig. 1. Principle of the p_t cut performed by the trigger.

A *dimuon trigger* is issued if at least two tracks, with opposite signs essentially, above pre-defined p_t cuts, are detected in an event. The trigger decision has

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to be available very fast ($\leq 1 \mu s$) because the signal is used as an early strobe by the muon tracking chambers.

The R&D on the RPC detector, operated in streamer mode, is the topic of another contribution (1) to this conference. The aspects concerning the front-end and trigger electronics, prototypes and future developments are discussed in this paper. The simulated performances of the system are briefly presented. More details can be found in reference (2).

2 Overview of the trigger system

The trigger system is represented in Fig. 2. The muon trigger is generated using the information of two trigger stations (MT1 and MT2) located 16 m and 17 m away from the interaction point.

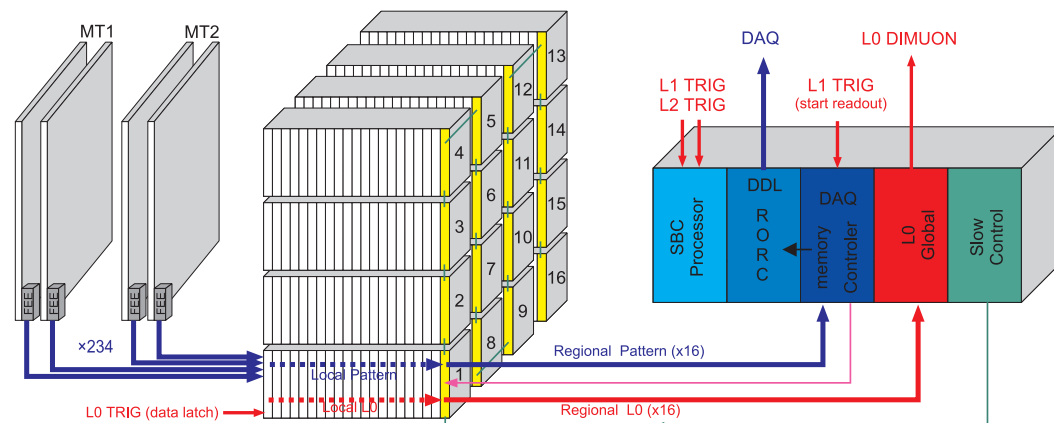


Fig. 2. Overview of the trigger system.

Each trigger station consists of two planes of single-gap RPCs, each plane providing an X and Y read-out. Y is in the bending direction (vertical) of the dipole magnetic field while X measures the position in the non-bending direction.

The information coming out from the front-end electronics (X and Y strip pattern of the 4 planes) is sent to the “local trigger electronics”, which purpose is to perform the p_t cut on single tracks. Two different p_t thresholds are foreseen, a low threshold in order to select the muons coming from the decay of the J/ψ and a high threshold for the Υ ones. The cuts will be pre-loaded in look-up tables located in the local trigger electronics. In the non-bending plane the track is required to point back to the interaction point.

This local information is then gathered on a “regional” level (1 per VME crate housing the local boards) which delivers a signal for single muons as well as for muon pairs. All these regional pre-triggers are then mixed to deliver the “global” dimuon trigger signal.

From the DAQ point of view, the patterns are transmitted in the same way to an interface card which further send the information to the ALICE DAQ system.

The numbers of channels and trigger boards are summarized in Table 1.

Number of X channels (strips)	14976
Number of Y channels (strips)	6016
Number of FE boards (8 ch./board)	2624
Number of local trigger boards	234
Number of regional trigger boards	16

Table 1

Total number of channels and trigger boards of the setup.

3 The Front-End Electronics (FEE)

The detector induced signals are collected on Aluminum strips 1-4 cm wide and less than 70 cm long. Each strip is connected at one end to a resistive termination and to a FEE channel at the other end. The signal pickup is done through the various layers of the readout planes (foam,...) by mean of special connectors developed for this purpose.

The FEE basically consists of a discriminator stage followed by a shaper. No amplification of the signal is needed in the streamer mode of operation of the RPC. The output signal must have a width of about 20 ns, less than the LHC bunch crossing interval of 25 ns. The FEE signals are sent in differential mode to the local trigger electronics through cables of about 15 m long.

The FEE prototype

A FEE prototype has been built and successfully tested on RPCs during runs at the GIF (Gamma Irradiation Facility at CERN). It is built around a commercial comparator in ECL technology (MAX9687 from Maxim or AD96687

from Analog Devices). The ECL technology is fast enough to handle RPC signals but the well known drawback is its large power consumption (200 mW/ch for this prototype).

The FEE chip

The development of a FEE chip in micro-electronics technology (BiCMOS 0.8 μm) has been started. A first design is available and software tests with CADENCE[©] have been performed. A reduction of a factor 2 of the power consumption is obtained as compared to the prototype one. Additional functions are presently implemented :

- a remote control delay, with a range of 50 ns;
- a “one-shot” which prevents the chip from re-triggering during 100 ns.

A LVDS output (instead of ECL) is currently under study to further reduce the power consumption. The present design includes a leading edge discriminator but more sophisticated techniques could be implemented in the future. A sketch of the circuit is presented in Fig. 3.

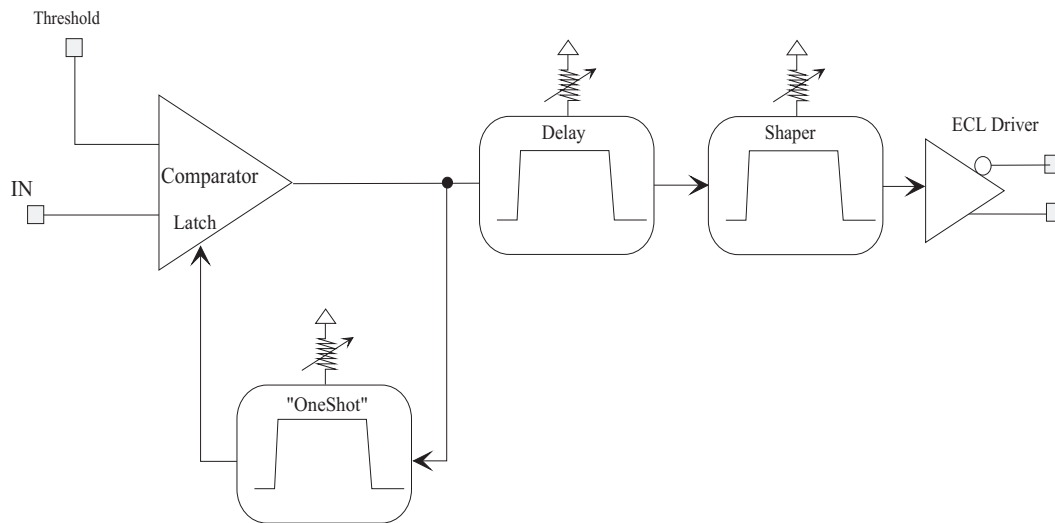


Fig. 3. Sketch of a channel of the FEE chip (first design).

4 The trigger electronics

The dimuon trigger is involved in the level 0 of ALICE triggers and should work in “pipelined” mode at a frequency of 40 MHz with a total latency less than 700 ns.

The local trigger electronics receives digital signals from the FEE called “bit-pattern” sequences. Two main functions are implemented in the local electronics :

- the backup of the input bit-patterns which are stored in a pipelined memory read out at the occurrence of an ALICE L1 trigger;
- the local trigger algorithm. The local L0 dimuon triggers - on single tracks - above low and high p_t thresholds are delivered on output.

The regional and then global trigger electronics collect the information of the various local boards. The trigger should finally limit the dimuon rate below 1KHz at low p_t and deliver a signal at low rate (≤ 100 Hz) for rare events like high p_t muon pairs.

Tests of the local trigger prototype

The prototype houses essentially two programmable ALTERA (FLEX 6016) chips which perform the L0-X (bending plane) and L0-Y (non-bending plane) local logic. As an example, a coincidence majority of 3/4 planes is required by L0-X and L0-Y to define a track. All output information needed for the p_t cut is available and can be read-out on the prototype but the look-up table is not yet implemented.

The prototype is designed to receive inputs from the RPC front-end electronics : 160 logical differential signals (a bit-pattern sequence) from X and Y strips are processed simultaneously at the clock frequency of 40 MHz. For test purposes, it is however more convenient to have the possibility to choose the input configurations. Hence a dedicated bit-pattern generator has been built (VME 9U board). Selected bit-pattern configurations are loaded in the memories (12 memories of 32 Kwords of 16 bits) of the generator and then transmitted to the trigger card at the clock frequency. The expected outputs are software computed and compared to the measured ones. The Labview[©] VME interface is used for loading the bit-pattern configurations in the generator as well as for the readout of the trigger card response, through a CAEN/V533 VME module. The test bunch is shown in Fig. 4.

The system allows up to 10^7 bit-pattern sequences to be tested per hour. The debug of the hardware (speed, short-cuts, ...) and of the software (reliability of the trigger algorithm) has been succesfully demonstrated.

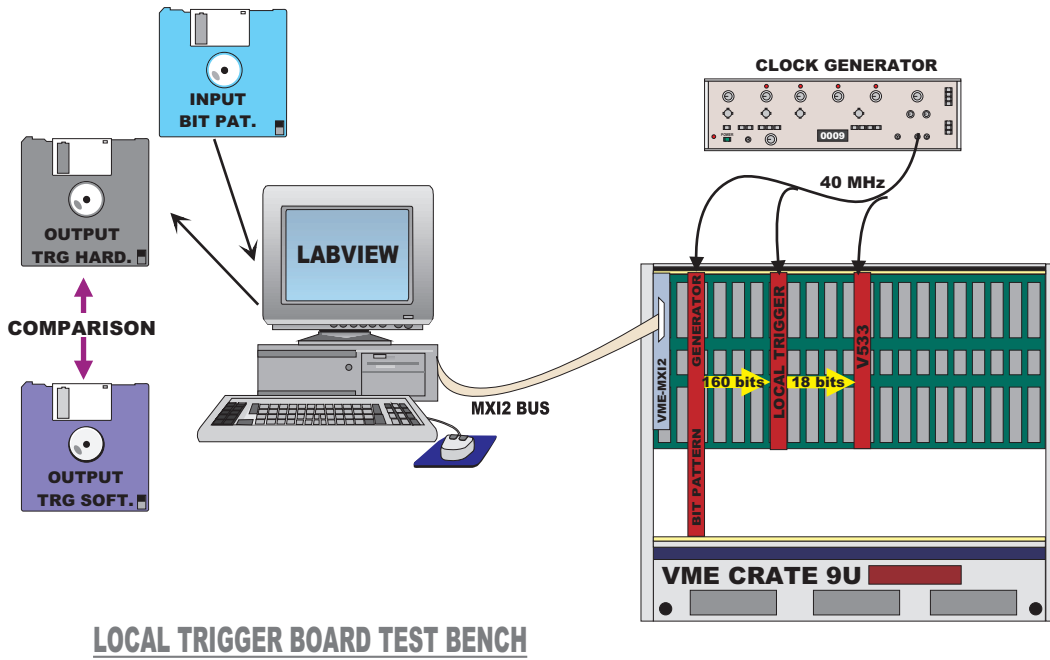


Fig. 4. Test bench of the local trigger board.

5 Simulated performances

The efficiency of the proposed setup has been simulated from events using the HIJING (3) code with nuclear effects turned on. The charm production, which contributes significantly to the trigger rates, is taken from PYTHIA (4) simulations with the structure function GRV-HO. The tracking of the muons up to the trigger is done with GEANT. The treatment of the hadronic showers in the absorbers and shields of the spectrometer uses the FLUKA (5) package (soft-background generation).

Examples of the dimuon trigger performances are presented in Table 2.

The trigger rates are given for the low and high p_t cuts which correspond respectively to 1 and 2 GeV/c at 50% efficiency and a J/ψ and Υ detection efficiency of 74% and 91%. The rates are calculated for minimum bias events at the nominal ALICE luminosities for the systems Pb-Pb, Ca-Ca and p-p.

It is observed that, in case of Pb-Pb events, a reduction of the minimum bias rate of about 1 and 2 orders of magnitude respectively for the low and high p_t cuts. The trigger efficiency is obviously better for the lighter systems where the background multiplicity on the trigger is low. In the last line of Table 2 we give the trigger rates accounting for a safety factor of 4 on the soft-background multiplicity predicted by FLUKA.

	Pb-Pb	Ca-Ca	p-p
Minimum bias	8000 Hz	$3 \cdot 10^5$ Hz	10^6 Hz
Low p_t cut	650 Hz	800 Hz	≤ 10 Hz
High p_t cut	90 Hz	60 Hz	≤ 10 Hz
Low p_t cut Soft-bckg $\times 4$	1100 Hz	1070 Hz	

Table 2

Simulated trigger rates for minimum bias events after the low and high p_t cuts and for the systems Pb-Pb, Ca-Ca and p-p. The last line indicates the trigger rates obtained with a safety factor of 4 on the soft-background multiplicity predicted by FLUKA.

6 Conclusion

We have briefly described the ALICE dimuon trigger setup and performances, with an emphasis on the electronics part. The front-end prototype developed for our R&D program is described. The development of a front-end chip for the streamer mode of operation of the RPCs is currently under study. The production is foreseen for year 2002. The first prototype of the trigger electronics for ALICE has been successfully tested after the construction of a bit-pattern generator. The production of the trigger electronics is planned for year 2003.

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