The Silicon Drift Detector readout scheme for the Inner Tracker System of the ALICE experiment

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The Silicon Drift Detectors (SDDs) provide, through the measurement of the drift time of the charge deposited by the particle which crosses the detector, information on the impact point and on the energy deposition. The foreseen readout scheme is based on a single chip implementation of an integrated circuit that includes low-noise amplification, fast analog storage and analog to digital conversion, thus avoiding the problems related to the analog signal transmission. A multi-event buffer that reduces the transmission bandwidth and a data compression/zero suppression unit complete the architecture.
In this paper the system components design is described, together with the results of the first prototypes.

1. Introduction and requirements

The silicon drift detectors are expected to provide high detection efficiency over the whole detector surface, a spatial precision of the order of 30 μm, a two–track separation down to O(600) μm. In addition the detector should provide a charge resolution such that the dE/dx resolution is dominated by Landau fluctuations, which the truncated mean of the four ITS dE/dx samples is around 10 % for M.I.P.

A M.I.P. releases about 4 fC in the SDD. For hits far from the anode pads the charge collected by one is typically one-third to one-half of the 4 fC; thus the tails of the hit signal, essential for the position determination, will consist of less than 1 fC. The range of useful signals is limited between the noise level (250 e^-) and 28-32 fC, but higher signals (up to 160 fC) are possible.

The charge generated by a particle crossing the detector, depending on the crossing point and therefore on the drift time, can be collected by one anode as a fast gaussian signal ($\sigma = 5\ ns$) or by several anodes (up to five) as a slower gaussian signal ($\sigma = 30\ ns$), due to the diffusion during the charge drift through the detector.

In order to obtain the required precision the signal has to be sampled at quite high frequency (around 40 MHz); the dynamic range is 10 bits while an 8 bit resolution is sufficient if a non linear readout is adopted.

Due to the high sensitivity of the SDD to temperature variations and the very stringent requirement on the material budget which does not allow a very massive cooling system, the allowed power consumption for the electronic readout is very low (below 5 $mW/channel$).

2. System architecture

In order to minimize the power consumption, the signals coming from the detector are not immediatly digitalized after the low noise preamplifier. Instead, they are continuously stored into an analog memory; only when the trigger signal is received the memory content is frozen and the data are converted and sent to a digital event buffer. In this way the most power demanding components work for a reduced pecentage of the time (below 10%) greatly reducing the power consumption.

After a local digital storage, which de-randomizes data for a lower transmission speed, the data have to be transferred to the acquisition system. Since the amount of data is very large (around 32.5 $MBytes/event$) and more than 95% of these data are zero, a data reduction is performed. In order to minimize information losses an Huffman encoder has been used, togheter with tunable filter functions which allow to reach the required compression factor in the presence of noise. Figure 1 shows the full readout architecture.

3. The front-end module

In the Inner Tracking System of the ALICE experiment the SDDs are placed on linear support structures called ladders. The front-end modules are placed on the ladders, near the detectors, and are based on two functional modules, named PASCAL and AMBRA architectures.

The PASCAL architecture

The PASCAL architecture performs the low noise preamplification, analog storage and A/D conversion. A fully CMOS, low noise transimpedance amplifier continuously write the SDD signals into a switched capacitor analog memory at 40 MHz. When the trigger signal is received, the memory cells contents are converted in digital through a charge redistribution successive approximation A/D converter.

Current prototypes of the PASCAL architecture are designed as separate ASICs in standard technologies (0.7-0.8 μm); the A/D prototype fulfils the specifications while the preamplifier, which has been succesfully tested in beam tests, has to be improved in term of dynamic range. Promising results has been obtained also with the analog memory. The final goal is to design the full architecture as a single chip using the new deep submicron technologies (0.25-0.35 μm).

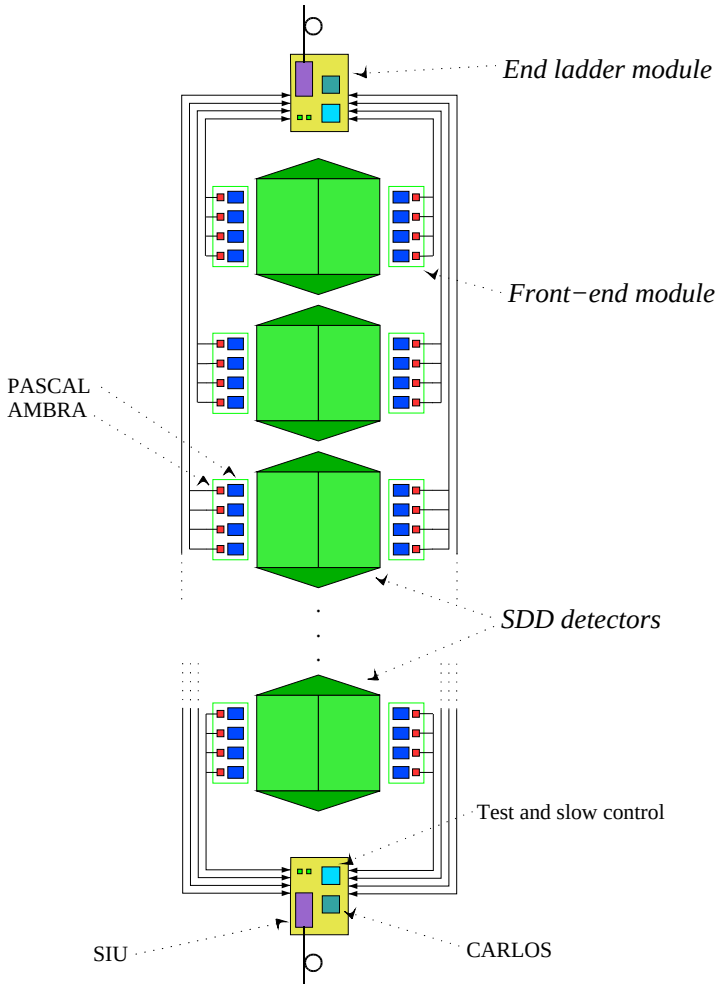

Figure 1. The SDD ladder readout architecture

The AMBRA architecture

In order to decrease the number of transmission wires from the detectors to the end ladder to a manageable number an event buffer strategy has been adopted. The events are temporarly stored in local digital buffers near the detectors; in this way the analog memory can restart the write mode faster thus reducing the dead time. It has been shown [1] that with only two event buffer the dead time due to event buffer overflow is around 0.1%. The current prototype of the AMBRA architecture is a single ASIC designed in 0.35 μm technology

4. The end ladder module

The end ladder modules are placed at both ends of the ladders, and contains the compression circuit, the optical interface to the data acquisition system and the control system.

The most important functional module is the CARLOS architecture. Its purpose is to

compress the signals coming from the front-end readout units to a size compatible with the requirements by the ALICE data acquisition system.

Data compression

The amount of data generated by the SDDs is 32.5 $MBytes/event$. Most of these data are zeroes, therefore a data compression is required in order to save space on tape. Since a simple zero suppression leads to an unacceptable information loss, several compression algorithms have been studied :

- Zero sequence encoding : sequences of zeroes are transmitted as a zero code followed by the number of consecutive zeroes. Since the occupancy is quite low, long zero sequences are highly probable.
- Simple threshold zero suppression : the data below a certain threshold, which takes into account noise and pedestal, are set to zero. This technique is very easy to implement and increases the number of zeroes by cutting non zero values due to the noise. Unfortunately this results in information loss.
- Differential encoding : instead of the samples, the difference between consecutive samples is transmitted. In this way any channel baseline value is translated into a zero sequence. On the other hand a differential encoding scheme is more sensitive on sample errors during transmission.
- Simple threshold tolerance : it is a simple threshold zero suppression applied after the differential encoding. It reduces the noise variations over a baseline, at the expense of information loss.
- Huffman encoding : since the probability of lower codes is much higher than the higher ones, using a variable length encoding leads to a lossless

  data reduction. This reduction depends on the sample statistics; the implementations is quite heavy in terms of hardware requirements.
- Multithreshold zero suppression : a sample is set to zero depending on its value and on the value of neighbour samples. In this way the information loss can be greatly reduced with respect to single threshold zero suppression.

An FPGA-based prototype of the first 5 algorithms, with software tunable parameters, has been realized and is currently under test with the data taken from the ALICE SDD beam tests [4]. The sixth algorithm is currently under evaluation. A detailed description of this alghoritm can be found in [5].

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