SIGNAL-INTEGRITY MEASUREMENTS ON VME320 BACKPLANE

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Abstract

Using high-speed buses in data-acquisition systems is widespread very much. The bus topology and performance is one of the key factors in the overall performance of the hole system. The limitation of the speed which can be achieved on a backplane-like bus is determined by the signal-integrity behaviour of the bus and the driver and receiver of the daughter cards. The paper deals with the profound evaluation of one of the latest VME-like backplanes. Measurement results are presented for the impedance profile, frequency-domain response, skew, eye-diagram and BER of the transactions.

1. INTRODUCTION

At the beginning of last year the VME community was surprised that a new type of VME backplane was announced which could handle data transfer up to 320Mbye/s: the VME320. In DAQ systems of experiments the VME is extensively used so it is very important to extend our knowledge in this new technology.

In this sub-project we would like to evaluate the latest VME backplane technology. The purpose of the measurements is to determine the limitations or weak points of this technology and to receive basic experiences to design high-speed boards and systems using this type of backplane.

2. LIMITATION OF BANDWIDTH

First of all we should find the reason of the bandwidth limitation on a VME backplane. The key factors are the followings:

- Data width, Handshake protocol
- Signal settling time, Backplane delay
- Backplane skew, Circuit delay and skew
- Set-up and hold time
- Synchronization time, Bus acquisition time, Interrupt response time

Several improvements were done on the VME backplane to achieve higher data throughput. In the latest draft standards describe up to 64 bit wide transaction with 2eVME protocol instead of the original BLT protocol. [1]

The electrical characteristics of backplane and bus drivers of the cards are very important to achieve clean, undistorted signal to reach the highest speed enabled by the protocol. The designing of such high-speed cards and systems require deep knowledge of the electrical properties of the system components and extremely careful design focusing on the signal-integrity problems.

3. VME BACKPLANE TOPOLOGIES

3.1 Traditional backplane

Conventional backplane design uses slot to slot wiring scheme. *Figure 1.* In this topology the backplane looks like a long transmission line from slot #1 to slot #21. The unloaded characteristic impedance is near 60-70 ohm but it can be as low as 20 ohm in a fully loaded system.

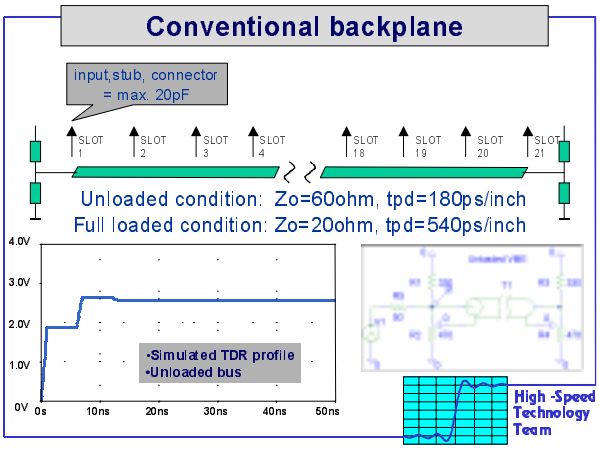


Figure 1.

The transmission is distorted by the reflection from the end of the long transmission line. [2] The main improvements use incident wave switching drivers with tighter input voltage range and limiting of the slew rate of the pulses driving the backplane. With the 160 pin connector which contains more ground pins we can reduce the crosstalk and ground bounce. The requirements can be seen in [3]. A lot of simulation and measurements were done which show that the system can be used to achieve high-speed data transmission and there are not any basic signal-integrity problems. [4] The theoretical data throughput is 160Mbyte/s with 64 bit wide data bus and 2eVME protocol.

3.2 The VME320 backplane

The new topology which is used by VME320 backplane instead of slot to slot wiring uses a star routing and all of the slots are directly connected to slot #11 at the centre of the backplane. [5][6] *Figure 2.*

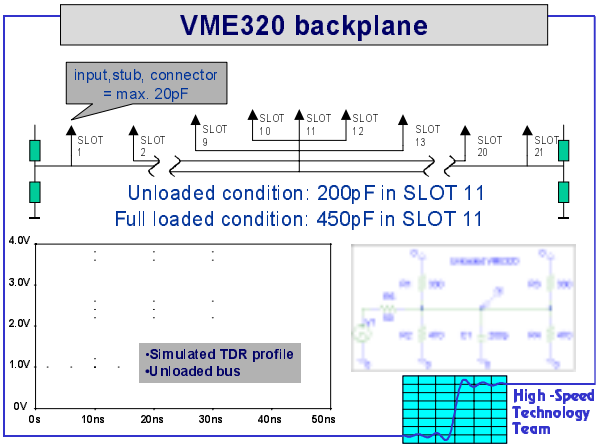


Figure 2.

With this new topology the backplane looks like a lumped capacitance at slot #11. In optimal case all of the problems -like reflection- which comes from the transmission line behavior of the backplane can be eliminated.

Beyond this new type of backplane a new protocol was suggested for higher speed: the 2eSST. [7]

4. BASIC MEASUREMENTS

4.1 The TDR measurement

The impedance profile was measured on the backplane with TDR oscilloscope. In slot #11 the response looks like a lumped capacitance. See *Figure 3.*

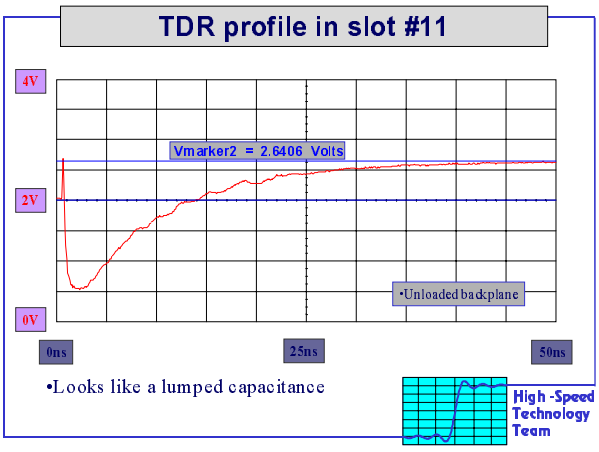


Figure 3.

The TDR profile was measured in all of the other slots. At the ends of the backplane we can see some additional delays before the lumped behaviour. *Figure 4.*

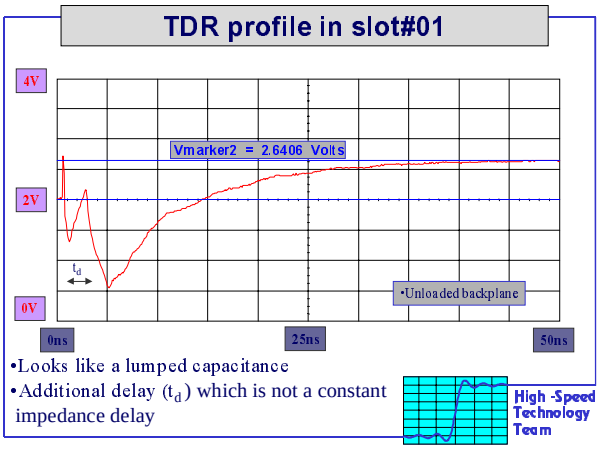


Figure 4.

4.2 The frequency-domain measurement

The transmission on the backplane was measured in frequency-domain, too. Basically we can see low-pass response which will help in decreasing the slew rate of the signals in the backplane. *Figure 5.*

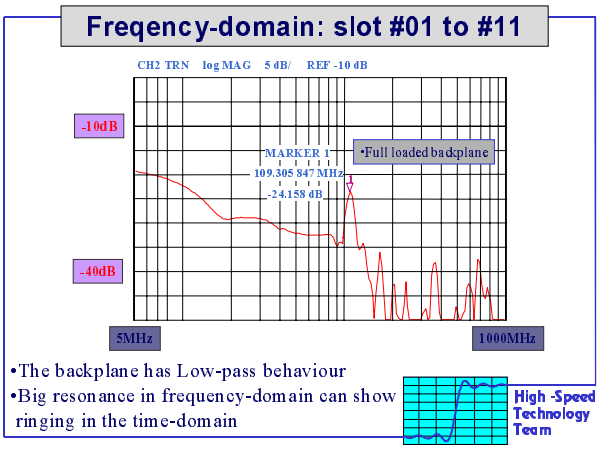


Figure 5.

In some connection combinations there is a peek resonance in the frequency domain response. This can show ringing in the time-domain. Basically the frequency of the resonance is higher than the signalling rate of the backplane and the low pass behaviour of the backplane attenuates the value signal which can generate the ringing.

This low-pass behaviour also can help to improve the EMC issues of the backplane and shows less radiation of the high-speed signals.

5. SKEW MEASUREMENTS

Using the 2eSST protocol requires a low-skew signal transmission to achieve a theoretical maximum speed.

For the skew and transmission measurements a 3U VME testcard was designed and manufactured. This card contains the ETL bus drivers with optionally installable RL filter network and it is compliant with VITA ETL draft standard. [3] Beyond the drivers there are some connectors for Pattern Generator and Logic Analyser which was used as a data source and receiver at the source and destination card respectively. The test set-up can be seen in *Figure 6*. Detailed information about the card can be found at our web: http://hstt.mht.bme.hu .

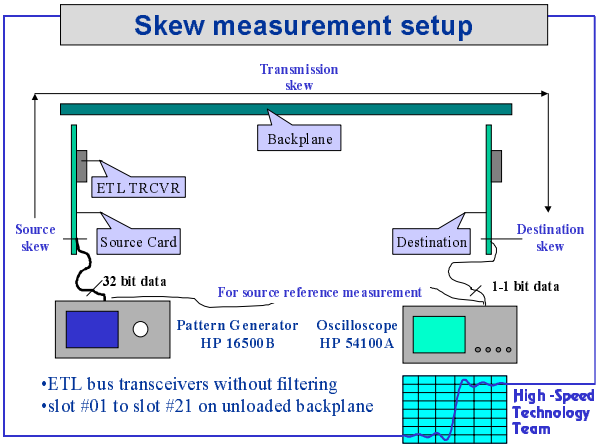


Figure 6.

With the test set-up two kinds of skew were measured and one was calculated on rising and falling edge of the signals. First the skew of the 32 output bit of the HP Pattern Generator was measured by measuring bit by bit delay to a reference clock signal. The skew was determined as the difference between the earliest and latest signal. The second measurements series were done at the output of the receiver on the destination card. See *Figure 7*. and *Figure 8.*

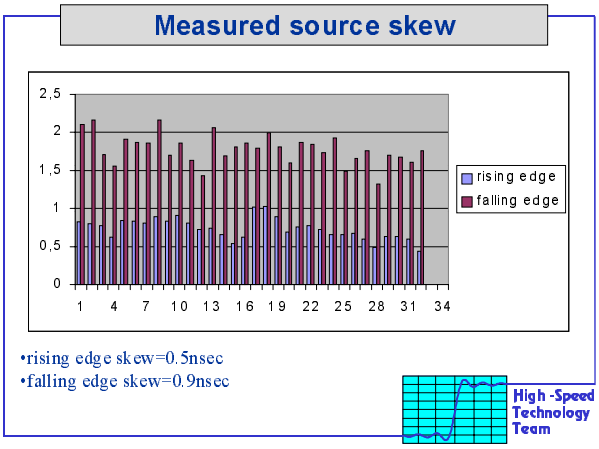


Figure 7.

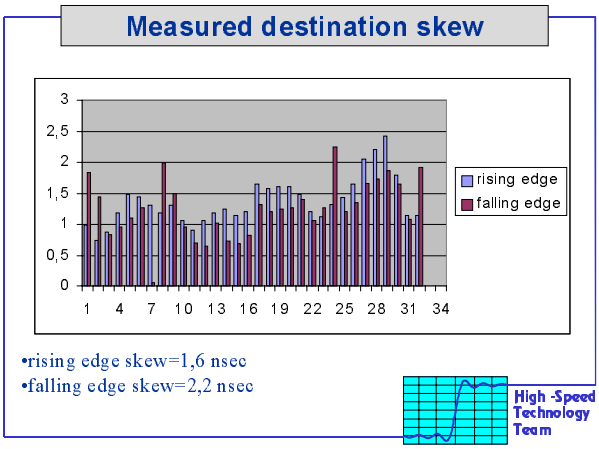


Figure 8.

The third skew was calculated from the two previous measurements. The base of the calculation was the subtraction of the delay of each bit. In this way we can give a delay of each bit from the source (the input of transmitter bus driver) to the receiver (output of receiver bus driver). The difference between the minimum and maximum is the total transmission skew caused by bus transceivers and backplane itself. The results are the followings:

SKEW [ns]		
	Rising	falling
source	0.5	0.9
Destination	1.6	2.2
Transmission	1.85	2.2

Table 1.

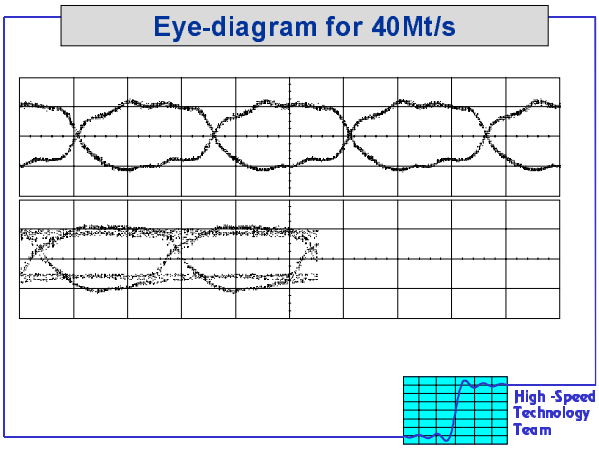
Please note that these kinds of skews are different from the skews which are determined by the 2eSST draft. [7] There we can see the source skew which should be measured by the output of the card (real data source plus transmitter driver), backplane and receiver skew.

We think that our explanation and measurements show a little bit more realistic picture about the real development problem. The 2eSST draft may be based on the hypothesis that the real source skew can not be minimalised to such a low level as it was in our measurements, so registers should be used in the output driver. (like ABT16646, ABT646 or V320) In this way, really the output skew of the backplane driver is the main determining factor. But we consulted our digital designer and the preliminary simulation showed that the output skew of the digital core logic could be minimized under 1ns with special high-speed design techniques in the FPGAs and ASICs. In this way it is possible to use bus drivers without registers. And with tight input

tolerance ETL can be used (ABTE16245, 246) really fulfilling the VITA ETL and 2eSST draft.[3][7]

On the receiver side the destination skew should be compared to the timing of the data strobe, setup and hold time of the receiver core logic FPGA or ASIC.

It should be ensured that the latest data bit arrives before one setup time of the earliest data strobe, and the earliest data is clocked at least one hold before the transition of the latest data strobe. The measurements show that the 1-3ns setup and hold time can be fulfilled easily and the transmission can be safe at the proposed 40Mt/s speed. But please note that it was only one measurement in one configuration and lot of other configurations should be checked.



6. WAVEFORM MEASUREMENTS

With the designed and manufactured test cards we can generate transaction up to 100Mt/s on the backplane. From the signal integrity point of view checking the clean and monotone rising and falling waveform is one of the most important measurements.

The waveform was measured on the receiver card at the pins of the 160 pin VME connector. The A1 and DS1* line was monitored and eye-diagram was collected synchronising to the master clock of the transmitter. This is the reason why we can see two data strobes because the scope was triggered at all rising edges of the master clock which has got double frequency as the data strobe. The eye pattern was made with a pseudo random bit pattern, so it gave us a view of the intersymbol interference (ISI) presenting in the system.

The transmission was stable up to 80Mt/s. As we can see from the scope pictures unfortunately the data strobe signal timing is not good. The transition of the strobe should be at the centre of the data window. This is the reason of transmission errors beyond 80Mt/s. The proper set-up time of the receiver cannot be fulfilled with this timing. With properly aligned data strobe the transmission can be stable far beyond 80Mt/s. See *Figure 9.-10.-11.* for eye-diagrams of different speed transmissions.