Test of Alice DDL: Test Setups and Test of ALICE DDL Integration to ALICE TPC Test System

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Abstract

The Detector Data Link (DDL) has been developed to constitute a standard interface between the ALICE sub-detectors and the DAQ system.

In this paper we present the test environment and the application software library made for supporting the DDL development and its integration into the ALICE detector system.

The test setups contain VME64 crates, MVME processor cards, a VMETRO analyser, a logic-analyser and Read-out-Receiver (RORC) and Destination-Interface-Unit (DIU) cards. They made possible to measure the maximum throughput of the full read-out chain and also to measure the transmission latencies. They support the functional and long-term stability tests as well.

1. INTRODUCTON

The ALICE Detector Data Link (DDL) [1] will interface the Front-end Electronics (FEE) of all the sub-detectors to the Data Acquisition System (DAQ). The DDL consists of a Source Interface Unit (SIU) connected to the FEE, a Destination Interface Unit (DIU) connected to the Read-Out Receiver Card (RORC) [2] located in the counting room, and a physical medium which is a duplex optical fibre. Instead of SIU-DIU configuration, DIU-DIU configuration can be used as well, so VME crates can be used at both sides. For test purposes we used the DIU-DIU setup.

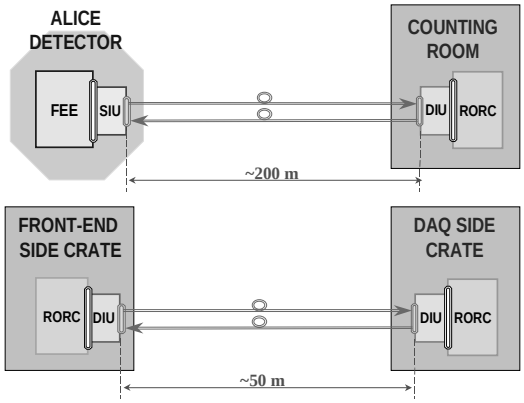

Figure 1: The DDL concept

2. THE AIM OF THE TEST TOOLS

The aim of the test tools developed in KFKI-RMKI is

- to support the debugging and the low level hardware tests of the DDL components, the RORC and the FEEs;
- to provide test routines for the complete functional tests of the DDL components and the RORC;
- to provide test procedures for the long term stability, the performance and the qualification tests of the complete DDL chain (the RORC is included);
- to provide library routines for the software developers of the front-end and the DAQ sub-systems of the TPC test system.

3. THE TEST SETUPS

The DDL developers and users can use the following setups to execute DDL functionality and stability test:

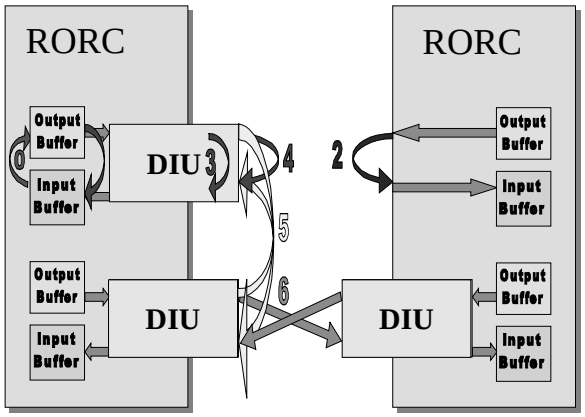

Figure 2: Test setups

The large numbers in figure 1. represent the different possible loop-backs and DIU-DIU connections:

1: RORC internal loop-back (temporary not implemented)

2: RORC external loop-back

3: DIU internal loop-back

4: DIU external loop-back

5: DIU to DIU, same RORC

6: DIU to DIU, different RORC

0: DDL loop-back, (not possible with **1**)

4. SUPPORTED HARDWARE

During our tests we used VME64 crate using two different single board computers running under three different operating systems:

- MVME2604 PowerPC under AIX 4.1
- MVME2604 PowerPC under LynxOS 2.5.1
- Motorola VME166-6840 under OS9 V24

5. STABILITY AND TIME MEASUREMENT TESTS

For the task-to-task stability and time measurement test we used the following setup:

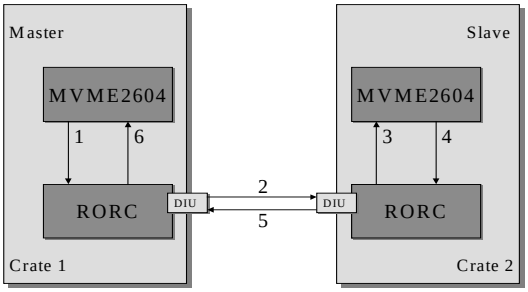

Figure 3: Stability and time measurement test setup

We made two different tests

- Data sent from the master to the slave processor (steps 1, 2, 3)
- Data sent from the master to the slave processor (steps 1, 2, 3) and back (steps 4, 5, 6).

In both case measured the transfer speed using three different VME modes:

- VME single cycle mode
- VME 32 bit BMA mode
- VME 64 bit BMA mode

Figure 4. shows the results we got in single cycle and 32-bit BMA mode.

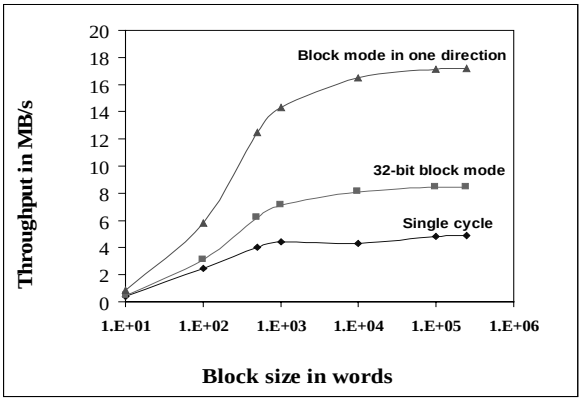

Figure 4: Time measurement results

In 64-bit block mode in one direction the maximum throughput was 34 MB/s.

During measurements several hundreds GBytes data have been transferred without any error.

We used different data patterns, such as:

- incremental data
- chess board pattern
- walking 0's and 1's
- random data.

For the average time for sending one command we got 6.4 μs.

We also made successful stability test with random data length.

6. STABILITY TESTS USING THREE RORCS

Figure 5. shows the test setup we used for three RORCs tests.

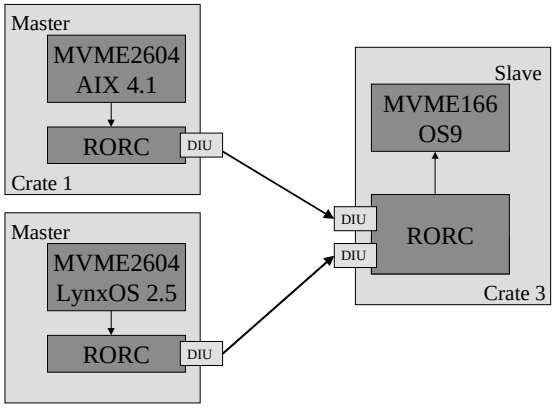

Figure 5: Test setup for 3 RORCs test

We used the above test setup because a similar configuration is to be used in ALICE TPC prototype test.

Several GBytes data have been transferred without any error.

Data patterns used:

- incrementing data
- walking 0's and 1's

We also made successful stability test with random data length.

7. DDL INTEGRATION IN ALICE TPC PROTOTYPE (NA49)

The first version of DDL will be integrated and tested in ALICE TPC prototype test beam run in September 1998 [3]. A DIU-DIU setup will be used as shown in figure 6.

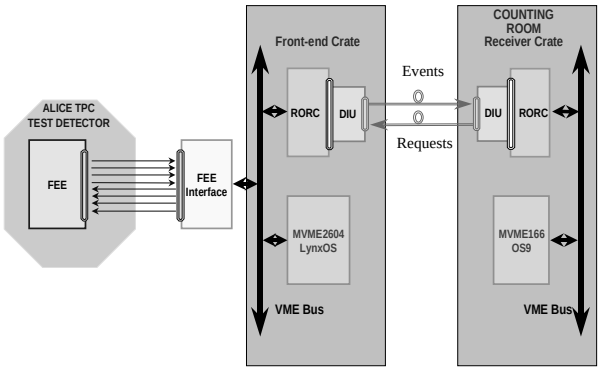

Figure 6: The DIU-DIU configuration used in DDL integration

The 2 versions of the integration setups:

Two different use of DDL will be possible.

Version 1.

- All (max. 32) events in one spill are measured and data stored with local event numbers in the Front-end Crate's LynxOS memory.
- When the central DAQ requires a given event the Receiver Crate's processor requests it and the Front-end Crate transfers it to the Receiver Crate's RORC memory, where the further move of the data is carried out by the central DAQ side.

Version 2.

- The Front-end Crate collects data when the trigger arrives
- and transfers this data to the RORC memory of the Receiver Crate automatically without any command from the Receiver side.

Results of time measurements using the integration setup:

We made time measurements for both possible use of DDL. We got the following results:

In the case of version 1 the time between the data request and event arrival into the Receiver Crate's RORC memory was measured:

Table 1: Transfer times for version 1

# of words	Time in ms
100	0.14-0.15
500	0.21-0.22
10000	27-0.28
50000.	88-0.89
10000	1.65
50000	7.75
60000	9.25

In the case of version 2 the time between the SW trigger and event arrival into the Receiver Crate's RORC memory was measured. This time contains two VME transfers and the DDL transfer time.

Table 2: Transfer times version 2

# of words	Time in ms
17665	8
66000	26

8. SUMMARY

We can summarise the results of DDL stability and integration tests as

- No problem found during functional and stability tests, all tests were successful.
- The transfer speed reached the limit of the operating systems and the hardware.
- ALICE TPC prototype integration requirements fulfilled: data arrives to DAQ side in 70 ms after the trigger.

REFERENCES:

[1] G. Rubin et al.: "The ALICE Detector Data Link Project", Proceedings of the 4th Workshop on Electronics for the LHC Experiments, Rome, September 21-25, 1998

[2] G. Rubin, J. Sulyán: "VME Read-out Receiver Card (RORC) for the ALICE-TPC test system." ALICE/97-14, Internal Note/DAQ, 05.05.1997.

[3] J. Baechler et al.: "Front-End Electronics for the ALICE TPC Detector", Proceedings of the 4th Workshop on Electronics for the LHC Experiments, Rome, September 21-25, 1998