# FPIX1: an Advanced Pixel Readout Chip

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## 1. INTRODUCTION

At Fermilab, a pixel detector for BTeV is proposed for installation a few millimeters from the beam. Its information will be used in on-line track finding for the lowest level trigger system. This requires a high-speed readout and immediate data transfer from the pixel chip to the trigger processor. It is also believed that a 2-4 bits of analog information is required to achieve the targeted spatial resolution [1] with 50μ wide pixels.

Our first prototype, FPIX0 [2], is now being used in a beam test to confirm physics simulations and to determine the required resolution of the analog "information".

Our 2nd prototype, FPIX1, is a 160X18 pixel readout chip compatible with the ATLAS family of detectors. We have build and tested 4 FPIX1-detector assemblies. FPIX1 is realized in the HP 0.5μ process. The main features of FPIX1 are:

- 2bit flash ADC on each cell for maximum speed.
- Triggered or stand alone operation.
- High speed sparse and time ordered Readout.

## 2. THE FPIX1 CHIP

The FPIX1 is a column based pixel chip with 50× 400 μm pixel cells arranged in an array of 160 rows by 18 columns. FPIX1 stores hit information awaiting readout in the pixel unit cells, and uses an indirect addressing scheme to reference the hits to BCO numbers held in registers at the end of each column. Instead of using pointers to accomplish the indirect addressing, as in [3], FPIX1 uses a command driven design, which is described below. The chip can be divided into three mutually dependent pieces: the Pixel Cell, the End-Of-Column (EOC) Logic and the Chip Control Logic ( Figure 1).

The responsibility of the Chip Control Logic is to control and maintain all features that are common to the chip such as the clocks, the "current" and "requested" BC0 numbers, and the status of off-chip communication. Each one of the eighteen EOC Logic cells controls one column.

The EOC Logic responds to information from the Chip Logic, and from the 160 pixels in a column by broadcasting commands to the Pixel Cells, and by arbitrating with the other EOC Logic cells for control of the on-chip data bus. Finally, each Pixel Cell connects to one sensor pixel and responds to commands from the EOC Logic. The commands used in this architecture are the following: the "input" command instructs a Pixel Cell to accept hits from its sensor pixel and to respond to a hit by alerting the EOC. In the absence of an input command, the hit is ignored. The "output" command instructs the Pixel Cell to prepare to write its information onto the bus. The "reset" command instructs the Pixel Cell to reset its contents. Finally, the "idle" command instructs the Pixel Cell to do nothing.

To buffer for 4 hits and decrease the column dead time, each EOC Logic cell consists of four EOC command Sets, each one capable of generating its own commands. When a Pixel Cell receives a hit, it immediately associates itself with whatever EOC Set is broadcasting the "input" command. From that point until it is reset or output, the Pixel Cell only responds to commands from its associated EOC Set. Meanwhile, the EOC Set holds the timestamp. The EOC Set can then issue the "output" or the "reset" command. The hit information is stored inside the Pixel Cell until readout.

The Chip Command Logic supports two readout modes. The first one, the "continuous" readout mode, requires no external trigger. This mode is expected to be used in the BTeV experiment. The other readout mode is the external trigger mode, in which an external system must provide the timestamp of the hits that should be read out. This mode is applicable for pixel detectors with external trigger, and for diagnostic purposes.

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## *2.1 Pixel Cells*

The pixel cells hold the front-end electronics and the digital interface with the EOC Logic.

The FPIX1 front-end is based on a design implemented in the FPIX0 and Pre-FPIX1 test chips. References [2,4] report in detail on measurements of FPIX0, both unbonded and bonded to an ATLAS test sensor. The front-end (Figure 2) contains a charge sensitive amplifier (CSA) and a second amplification stage. The DC feedback used in the CSA is similar to the one described in [5]. The average recovery time of the CSA can be adjusted from 50 ns to 1 ms by an external current source without requiring any reset signals to be transmitted across the sensitive analog region. The output of the second stage connects to a 2 bit flash ADC and a discriminator.

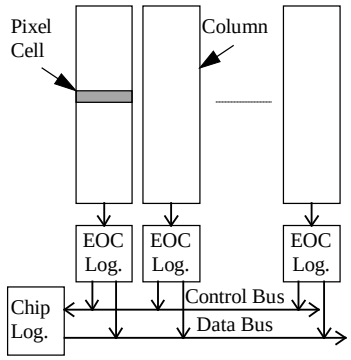


**Figure 1. FPIX1 Block diagram.**

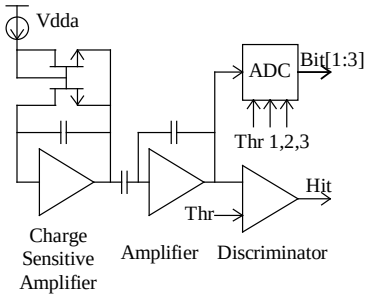


**Figure 2. Front-end Block diagram.**

The discriminator output Hit is asserted when the signal at the input of the discriminator is higher than the threshold (Thr). The flash ADC consists of three comparators directly connected to SR flip flops inside the pixel cell. The four thresholds (common for all pixel cells) are input to the chip as DC levels. During readout, tri-state buffers connect the outputs of the ADC flip flops to the EOC Logic, where they are encoded into two bits.

The digital interface of the pixel cell is depicted in Figure 3. It has two major components; the Command Interpreter, and the Pixel Token and Bus Controller. The Command Interpreter has four inputs, corresponding to the four EOC command Sets. Commands are presented by the EOC Logic simultaneously to all pixel cell Interpreters in a column. When an Interpreter is executing the input command and the Hit output from the discriminator is asserted, the Interpreter associates itself with the particular EOC Set that is issuing the input command. Simultaneously, it alerts the EOC Logic to the presence of a hit via the wire-or'ed HFastOR signal. After the association to a particular EOC Set has been made, the Interpreter ignores commands from all other EOC Sets. The pixel hit information is stored in the cell until the associated EOC Set issues an output or reset command.

When the associated EOC Set issues the output command, the Interpreter issues a bus request and asserts the wire or'ed RfastOR signal. This operation is executed independent of the master readout clock (Rdclk)[1]. The balance of the readout proceeds synchronous with the Rdclk. The EOC Logic provides a column token on the bottom of the column as a means to regulate bus access. The token quickly skips pixel cells with no information until it reaches a cell that is requesting the bus. This propagation to a hit pixel is done in less than one clock cycle, even if the pixel is the last in the chain. At the next rising edge of the Rdclk, the hit pixel with the column token loads its data onto the bus and drives it to the EOC logic for one clock cycle. In parallel, the column token is transmitted to the next hit pixel, pipelining the output of the Pixel Cell with the token passing. This allows the readout of one Pixel Cell per clock cycle, without any wasted Rdclk cycles. The data is composed of the ADC count Bits[3:1] and the row address Radd[7:0]. As the hit pixel is read out, it automatically resets itself and withdraws its assertion of the RFastOR. The RFastOR returns to its inactive state while the last of the hit pixels is being read out. This way, the EOC Logic is able to detect when the last hit pixel in the column is being output. At the next rising edge of the Rdclk, control of the on-chip bus is transferred to the next column with hit data.

[1] Rdclk is reffered to as MClk in figure 4.

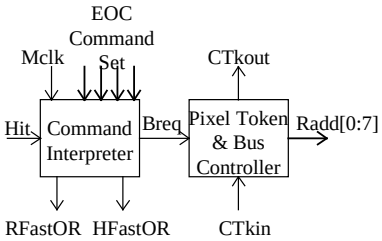


**Figure 3. Pixel Cell Digital Interface**

At any given time, only one EOC Set is permitted to broadcast the input command. This insures that hit pixel cells are associated with only one EOC Set. Pixel cells that have not been hit continue to monitor all four EOC Sets, waiting for a coincidence of hit and input commands.

### *2.2 End of Column Logic*

Figure 4 shows a block diagram of the EOC Logic. It consists of a Priority Encoder and four EOC command Sets. The EOC Sets themselves consist of a timestamp register, a state machine for generating the appropriate EOC commands, and two comparators.

The Priority Encoder selects one EOC Set to issue the input command. When there is a hit somewhere in the column, the HFastOR signal is asserted, and the state machine inside the assigned EOC Set responds by latching the Current BCO (CBCO) in its EOC timestamp register and by issuing the idle command at the next rising edge of the BCO clock. This ensures that all pixels in a particular column hit in the same clock period are associated with a single EOC Set. The Priority Encoder assigns the next EOC Set to issue the input command to the column (at the rising edge of the BCO clock). Since the EOC Logic has four EOC Sets, pixel cells in the column can be hit without loss of data in four different crossings before any data is read out.

A "hit" EOC Set waits for matches with its stored timestamp BCO (SBCO). If the match is between the Requested BCO (RBCO) and the SBCO, the EOC Set broadcasts the output command, and if the match is between the Current BCO (CBCO) and the SBCO, it broadcasts the reset command. Any of the bits in the comparison between CBCO and SBCO can be programmed to be ignored. This allows for a user defined reset delay. This feature is designed primarily for the externally triggered readout mode.

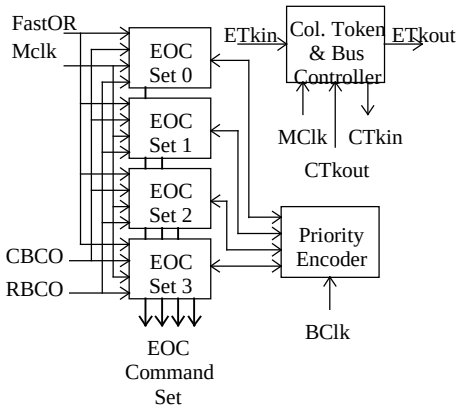


**Figure 4. End Of Column Logic**

A second state machine is implemented inside the Column Token and Bus Controller, to control the access to the EOC data bus. This access is arbitrated by an EOC token. As soon as there is a match between the RBCO and the latched CBCO, the Column Controller issues the CTkin token to the column, and waits for the EOC Token In (ETkin) from the Chip Logic. When the ETkin is asserted, the Column Controller enables the pixel data onto the internal data bus, and stays in this state until all hits in the column are read out. The Column Controller now passes the EOC token to the next EOC Logic by asserting ETkout. The early delivery of the CTkin to a column, even before the ETkin is received, allows for the pixel data to be asserted on the internal data bus as soon as the EOC token arrives at the EOC Logic. This, added with the assertion of ETkout as soon as CTkout is received by the Column controller, allows for full clock speed readout of the pixel data, even when the chip finishes the read out of one column and starts the read out of the next.

A more detailed description of the complete readout including the chip logic can be found in [6] and [7].

## 3. RESULTS

We have thoroughly tested the FPIX1 chip both with and without a detector. In this paper we will focus on chips bump bonded to detectors. We have bonded several chips to different types of detectors (All from the same wafer form Seiko) that were provided by the ATLAS collaboration. Figure 9 shows a chip-detector assembly on the test PCB.

The readout was found to work as expected, despite a minor bug. A typical output sequence of the FPIX1 RO is shown in figure 11 as captured from a logic analyzer. The data valid bit (DV) indicates the presence of a valid data, which should be strobed at each negative edge of the readout clock. First the chip outputs the chip ID and the time stamp then the addresses and the ADC values of all pixels hit during that time stamp.

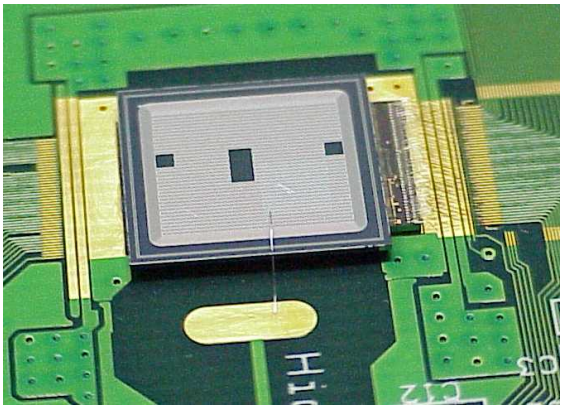

**Figure 5 FPIX1-detector assembly.**

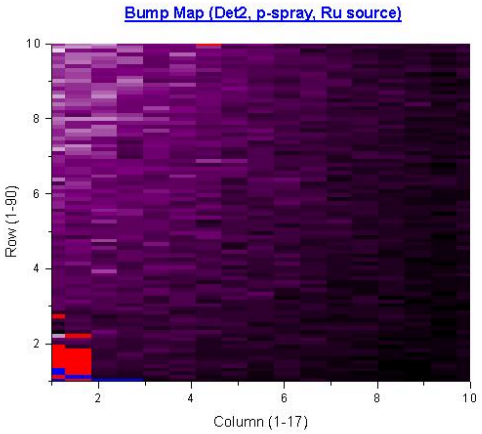


**Figure 10 Bump Map.**

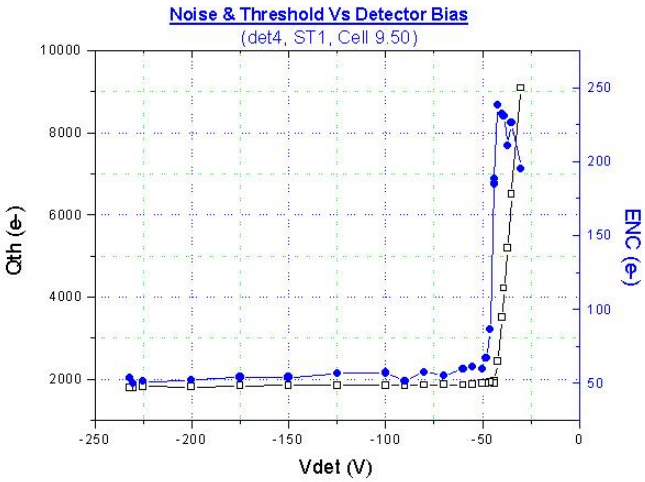


**Figure 8 Noise & Threshold Vs VDET.**

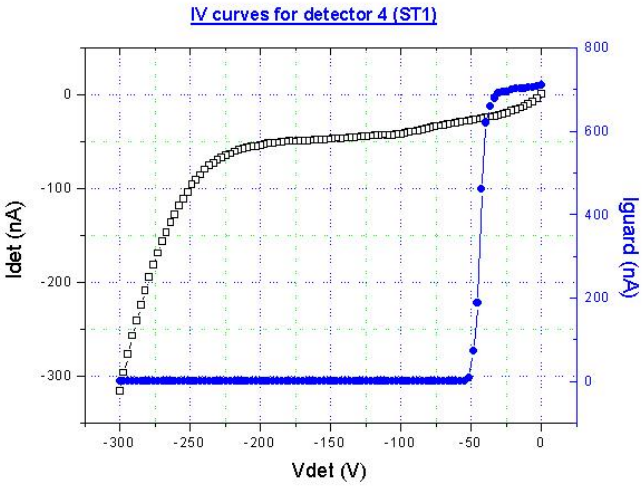


**Figure 7 IV characteristics of an ST1 detector.**

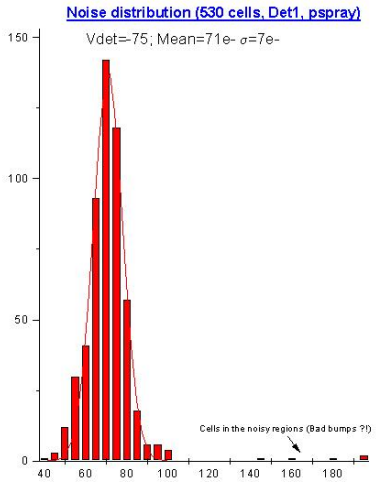


**Figure 6 Noise distribution.**

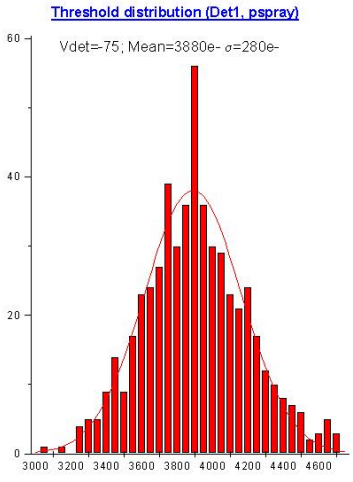


**Figure 9 Threshold distribution.**

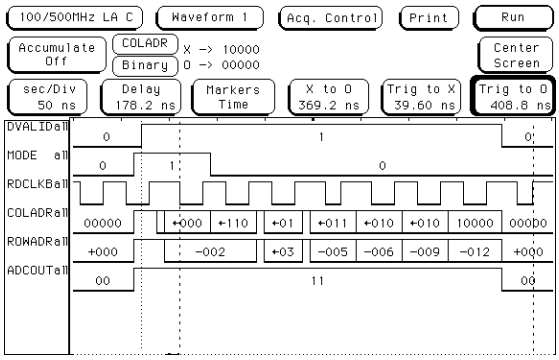


**Figure 11 A typical FPIX1 output sequence (6 pixels hit)**

Figure 7 shows typical DC characteristics of an assembled n-on-n detector in which the individual pixels are separated by individual floating p-implants (PSTOP). To precisely determine the full depletion voltage we plot the noise and the threshold (of a given channel at a given bias setup) versus the detector reverse bias voltage. Figure 8 depicts one such a curve. We have found that all detectors deplete at around 50V, but have differences as high as 100V in the breakdown voltages of detectors.

An important design criterion is threshold and noise dispersion within one chip. Without a detector, we consistently measured across several chips threshold dispersion of about 250e-, at low threshold setup. The noise averages about 40e- rms. with a standard deviation of less than 3e-. After bump bonding to a detector the threshold dispersion was about 300e- rms. and the noise reached about 70e- rms. After bonding the detectors we had to disable some extremely noisy pixels (about 25 in the bottom left corner of the detector as shown in figure 10) to perform adequate measurements. The excess noise is believed to be due to some bumps, being shorted together and/or to the guard ring.

Figure 9 and 6 depicts the threshold and noise distributions of an FPIX1 bumped to a p-spray detector. Similar results were obtained with the other type of detectors.

We were unable to detect any cell to cell cross-talk at a 2000e- threshold with the maximum input charge of 80000e-. The test was done by injecting only one cell and looking for any of its neighbors to fires. The test was performed at different locations across the chip. The result was the same for p-spray and p-stop detectors.

**Table 1 Summary of the main results.**

| | |
|---|---|
| Supply voltage | 3.3V (+/- 25%) |
| Analog supply current | 18μA/cell |
| Noise (ENC) | 70e- |
| Threshold dispersion | 280e- |
| Timewalk | 50ns |
| Dynamic range | 40ke- |
| Threshold control | 2ke- to infinity |
| Token skip delay | 192ps, 5.2GHz skip rate |
| Maximum RO clock | 30MHz |
| Cell to Cell Xtalk | None at 2ke- threshold. |

# 4. CONCLUSION

As summarized in table 1, most of the obtained results meet or exceed the preliminary specifications suggested by the BTeV collaboration. Our immediate plan is to beam test the described system and have a confirmation regarding the required resolution in the analog information. We are also planning to design a radiation tolerant quasi final chip next year. A small prototype front-end circuit has been already submitted for fabrication in a 0.25μ CMOS process.

# 5. REFERENCES


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