EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

NP Internal Report 73-15
28 September 1973

A TWO-CLOCK SENSING SYSTEM: A NEW TIME-TO-DIGITAL CONVERTER

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ABSTRACT

Nuclear physics experiments very often require time measurements down to some nsec and better.

In particular, because of the drift chamber becoming available as a particle detector[1,2], time measurement is gaining in importance[3,4]. The conventional techniques for performing time measurements are discussed in general together with their limitations. Then a new time measuring method is introduced which is free from the limitations set by the former methods.

Geneva - 27 September 1973

Generally, time-measuring problems can be described in the following way: the time between the leading edges of two pulses has to be expressed in digital form, and the measured value can be instantaneously (or not instantaneously) available for processing. The two pulses do not necessarily need to be on the same line.

1. THE SCALER AS A TDC

For many years the scaler has been applied as a time-to-digital converter (TDC). Although so well known, it is presented here in order to discuss its performance and limitations.

In Fig. 1 the switch S1 is supposed to respond (open → close) on the leading edge of the start pulse and S2 (close → open) on the leading edge of the stop pulse. The binary scaler counts the number of clock pulses with frequency 1/T between the two leading edges. The measured time is thus immediately available in the binary scaler and so the scaler is a real time device.

Because the scaler stops counting (S2), measuring cascaded time intetvals is not possible.

1.1 Timing errors due to the elements around the binary scaler

The scaler is switched on and off by means of two separate switches. Even if these switches were to be combined, it would still mean that two different functions, namely on → off and off → on, would have to be carried out using the one switch. However, the response time for opening and closing of one and the same switch does not need to be the same.

In practice these devices are more complex than a simple gate and thus response differences become more obvious.

The influence of these differences on the device is expressed in the timing diagram shown in Fig. 2. The "binary counter open time" differs by a value $(E_{on} - E_{off})$ from the true time interval to be measured.

One way to prevent this error is to make $E_{on} - E_{off} = 0$, but this might be prohibitive in price if the chain treating start/stop is long. A direct conclusion is that the same time interval measured with different units could produce two different binary open times. The classical remedy is to make $E_{on} - E_{off}$ similar for all units. Apart from complicated adjustment procedures, a long-term guarantee that $(E_{on} - E_{off})$ will remain constant might not be possible at nsec resolution.

1.2 Limitation in time resolution due to the toggle flip-flop itself

The difference between the actual counted clock pulses and the "binary counter open time" is called the time resolution of the scaler.

In Fig. 2 the five counted pulses can stand for any time interval between 4T and 6T. This time resolution (±T) is defined by the frequency limitation of the first flip-flop (FF). The FF in Fig. 3 is in the position Q = 0. The addition of a clock pulse must switch the binary FF to Q = 1. Thus the FF contains a feedback loop for routing the clock pulse to the correct input. Before the FF can again respond to a new clock pulse, the effect of the first clock pulse should be present on the input routing. Clearly the propagation delay in the loop is one of the serious limitations in the toggle frequency.

2. ANALOG TIME MEASUREMENTS (Fig. 4)

The analog time measurement method is indirect and overcomes the frequency limitations set by the binary FF used in the scaler method. A capacitor is charged with a constant current during the time interval to be measured, and then discharged with a constant current smaller than the charging current. During discharge a constant clock frequency is counted in a binary scaler.

This device is therefore a non-real-time device, as the measured value in digital form is only availabel some time after the stop pulse.

Errors due to $E_{on} \neq E_{off}$ are also present here, but are less important in some applications, as long as a one-to-one correspondence exists between input and output.

To make sure that one time interval measured with different limits will produce the same digital value requires close tolerance and high-stability components. Long-term stability might be difficult to achieve.

2.1 Real time analog TDC

As mentioned above, the device as discussed in Section 2 is a non-real-time device. Techniques exist (see MOTOROLA - Mecl. system design handbook 1971) for making it real time. In fact the rising edge of the voltage ramp over C (Fig. 4) can be measured by stacked discriminators, and thus the measured value is immediately available.

3. CONCLUSIONS

From the discussion of the various TDC, we can see that the following performance characteristics would be desirable:

i) simple circuit elements;

ii) fully digital;

iii) toggle flip-flop should not limit time resolution;

iv) start and stop must be functionally the same;

v) real time TDC;

vi) cascaded time measurements should be possible;

vii) recuperation of past time intervals should be possible.

Suppressing one of these points even temporarily would compromise a later recuperation. For example, the scaler as discussed here possesses points (i), (ii), and (v). In nsec resolution the omission of points (iii) and (iv) may compromise the time resolutions, etc.

A TDC based on a vernier principle[5] possesses points (ii) and (iii). Owing to the choice to fulfil point (iii), all other points are compromized. This remark can also be applied to the analog TDC.

In the following section a TDC is presented that would fill all seven requirements. This TDC is basically a two-clock sensing system, one clock with a time resolution of 2 nsec and one with 16 nsec.

4. GENERAL DESCRIPTION OF THE TWO-CLOCK SENSING SYSTEM

In the following description a ±2 nsec time resolution has been aimed at. This measuring method is basically a two-clock system. [By a clock is meant a cyclic changing code appearing on several parallel wires (Fig. 5).]

One clock is formed by the outputs of a 5-bit synchronous binary counter*). A crystal-controlled frequency changes the code every 16 nsec. One cycle is thus completed in $2^5 \times 16 = 512$ nsec.

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*) A synchronous counter is a counter where all the bits of the code have changed max. one FF propagation delay after the clock input leading edge.

A second clock works with the Johnson code. The input frequency to the 5-bit binary counter is fed into a one-shot multivibrator with an output pulse width of 8 nsec (50% duty cycle). The output of this one-shot is then fed into three parallel delay lines with 2, 4, and 6 nsec delay, respectively. The clock pattern obtained is thus a 4-bit Johnson code. (See timing diagram, Fig. 5.) These two clocks are working in parallel and are in principle common to a set of measuring devices.

Any one measuring device contains nine latches, constantly watching the two clocks (see JL_1/JL_4 and BL_0/BL_4 in Fig. 6). Whenever a time marker arrives (e.g. drift chamber signal) both clock positions are locked in the latches. This locked value is then transferred into a memory.

By subtracting consecutive values (in the computer or elsewhere), the individual time intervals can be obtained.

The following parts of the TDC are discussed in detail:

the time resolution of the Johnson clock;

the time resolution of the four latches JL_1/JL_4;

the binary clock;

liaison between the two clocks;

keeping clock reference with finite clock cycle time;

memory organization.

4.1 The Johnson clock

It is clear that the one-shot multivibrator must define a pulse width of 8 nsec every 16 nsec, as accurately as possible. Dependence on power supply and temperature variation should be minimal.

A further requirement is the capability to drive at least three delay lines.

It was thought to combine four measuring channels in one unit, in which case the one-shot would drive 12 delay lines in parallel. The one-shot capable of doing this is illustrated in Fig. 7.

The input pulse of the one-shot has leading and trailing edges of approximately 1 nsec. The pulse is narrower at the top than at the bottom.

Thus by changing the threshold point of the differential pair T_1/T_2 the output pulse width can be regulated. T_4 and T_5 are a differential pair of fast transistors (Philips BFR 91): T_4 senses the one-shot output pulse, while the input of T_5 is set on a fixed d.c. voltage. The signals on the collectors of the pair T_4/T_5 are integrated and compared by a d.c. comparater which regulates the input threshold of the one-shot. This one-shot makes it possible to obtain economically an accurate pulse width for a high-power pulse.

Clearly the advantage of this circuit is that the width is not defined by the power transistor itself, which would hardly be possible with high-current pulsed transistors but could be done by two fast low-power transistors.

4.2 The four latches locking the Johnson clock position

Toggle devices such as those used in scalers are combinations of two FF's, a master-slave combination.

The latch is a single FF with two inputs: a clock input and a data input. If the clock is, say, low, the output of the latch follows the data input. If the clock changes to high, the data input is locked out and the output holds the data input.

In fact if at a certain moment (the time threshold) with respect to the clock transient a data transient takes place, there is 50% chance that a logic "1" will be locked in the latch. One may define this "certain moment" as the "time threshold" of the latch.

Manufacturers specify "set-up times" and "hold times" as the times before and after clock transient during which the data is not supposed to change in order to guarantee that this data is locked by the latch (normal operation as a memory). The sum of "set-up time" and "hold time" can thus be seen as the device spread of the "time threshold" around the clock transient.

This behaviour holds also for the master part of a toggle FF. The information from the master is transferred to the slave part and thus to the output after a clock transient (the time threshold of master and slave are offset by a constant value).

In Section 1.2 it was stated that the propagation delay from input to output τ_{pd} limits the frequency of the toggle FF. The following figures have been taken from the MOTOROLA - Mecl I.C. Handbook and may serve as an example:

Toggle FF MC 10131

τ_{pd} = 4.5 nsec max.

t_{set-up} = 2.5 nsec max.

Toggle frequency max. 125 MHz (e.g. minimum clock spacing 8 nsec).

The data at the input routing (Fig. 3) should be 2.5 nsec (set-up time) before the next clock, so minimum clock spacing is the sum of (2.5 + 4.5 + + τ_{fb}). τ_{fb} is the propagation delay in the external feedback loop, and is here $\sim$ 1 nsec.

The latches as used with the Johnson clock suppress $\tau_{pd} + \tau_{fb}$, as the data presented at the data inputs of the latches does not depend on its previous state but on a quantity produced by the one-shot + cable delays.

The proper gain in time resolution compared with a toggle device can thus be expressed by the ratio:

$$\frac{(t_{set-up} + t_{hold})_{latch}}{(\tau_{pd} + \tau_{fb} + t_{set-up})_{toggle\ FF}} .$$

Further improvement can be obtained by using rise- and fall-times (1 nsec) that are faster than the one (2 nsec) for which t_{set-up} and t_{hold} are specified. In fact other bistable elements or temporary bistable elements can also be used.

The following cost comparison is significant:

Latch with typical $t_{set-up} + t_{hold}$ = 1.4 nsec, cost 1 unit

Toggle FF with typical $t_{set-up} + \tau_{pd} + \tau_{fb}$ = 1.87 nsec, cost 36 units.

Further improvement in time resolution for a latch can be obtained by individual adjustment of the cable delays producing the Johnson code.

In the TDC the four latches watching the Johnson code are normally not locked, e.g. the outputs follow the data input. The time marker (wire signal or time zero reference) will cause the latch to lock (Fig. 6) the position it has read.

The code presented by the position of the outputs then makes it possible to localize the time marker transient with a precision of $\sim$ 2 nsec within the Johnson clock cycle.

4.3 The binary clock (Fig. 5)

The max. phase error between the bits of the binary clock plus the max. phase error between the two clocks should be smaller than ±8 nsec. The use of a synchronous counter generating the binary code is largely sufficient to fulfil this requirement.

4.4 Liaison between the two clocks

The problem normally posed when synchronizing two clocks is the following. Say we have a digital clock (at present on the market) and we want to make a photograph to see what time it is; then we may read, for example, 3 hours 00 minutes. The question may now arise whether it is 3 o'clock or 4 o'clock.

In the liaison of the Johnson latches and the binary latches the result of what the Johnson latch has read is used to update the binary latch; so this ambiguity will not exist here.

Because start and stop are functionally the same -- both are time markers measured by the same TDC -- phase errors smaller than ±8 nsec between the two clocks will not add to the time resolution. It is clear that this improves the stability. Temperature or aging effects can never change the phase error within the time interval to be measured and the same time interval measured by different units gives the same result.

The output transient of the Johnson latch that falls in the middle of the smallest binary bit is selected to update the binary latches. Maximum phase error between the two clocks should thus be smaller than ±8 nsec.

4.5 Keeping clock reference with finite clock cycle (Fig. 8)

The 5-bit binary counter has a cycle time of $2^5 \times 16 = 512$ nsec. The output of the last binary latch is counted in a two-stage counter (see count sequence in Fig. 8). If the counter comes in the last position it is automatically locked. After any word produced by a time marker that has been transferred to the memory, the two-stage counter is reset. The timing diagram and the truth table associated with it will show the significance of the produced code, where a and b are time markers. The two

bits Q_0/Q_1 contained in b will decide how to proceed in order to obtain the time interval between the previous time marker a and the time marker b (see time intervals and boundaries in Fig. 8).

It is accepted here that time intervals > 1024 nsec have no significance.

The system zero-reference or last time marker will stay in the latches and will not be transferred to the memory (see Section 4.6). This makes it possible to make an early detection of this Q_0/Q_1 code.

4.6 Memory organization (Fig. 9)

The digital word produced by a time marker is stored in a scratch-pad memory. The memory is built with three integrated circuits each one having 16 words of 4 bits. The word decoder is on the Integrated Circuit. The 16 words are divided into 4 groups of 4 words. Any one group of 4 words is associated with one TDC.

The "wire address counter" WAF_0/WAF_1 is sequentially searching (200 MHz) the "request gates" REG I/II/III/IV of the four TDC's in the unit. If a "wire information FF", WIF_N is on, REG_N when selected will lock WAF_0/WAF_1. The activated "word address counter" WOF_0/WOF_1 and the locked WAF_0/WAF_1 produce the memory address. A "memory enable pulse", MEEP is generated and the word is written in memory. A delayed pulse MUP resets the modulus counter MOF_0/MOF_1 and then WIF_N. The memory "write in time" is typically 10 nsec.

The worst-case occupation time for a TDC is thus 50 nsec and the shortest occupation time 10 nsec.

This memory is working in the "overwriting mode", e.g. the word address counter WOF_0/WOF_1 counts through zero and thus overwrites an old location. This means that only the last four time markers preceding the system zero-reference can be recuperated. The system zero-reference itself will be kept in the latches JL_1/JL_4, BL_0/BL_4, and in the counter MOF_0/MOF_1 by simply disabling MEEP.

One other memory organization is shown in Fig. 10. Here, shift registers are used to store the information. Only TTL shift registers can be considered for price reasons, and thus the max. shift frequency is limited to 20 MHz. To benefit fully from this max. shift frequency, another cycle time for the Johnson and binary clocks has been selected.

The Johnson clock has 2 bits or a cycle time of 4 (positions) × × 2.5 (resolution) = 10 nsec, and the binary clock has 3 bits or a cycle time of $2^3 \times 10 = 80$ nsec.

The technique is the same as before; the binary latches are updated by the output of the Johnson latch falling in the middle of the smallest binary bit. Only the cycles of the binary clock coming through the last binary latch BL_2 are not counted in a two-stage modulus counter but are used to shift information in these registers. The shift spacing is thus 80 nsec. With a 9-bit long shift register the max. time interval that can be measured is $9 \times 80 = 720$ nsec.

In the timing diagram (Fig. 10) an example is given for a time marker arriving just (< 25 nsec) before a shift pulse. The "wire information FF" WIF is set so that the Johnson and binary latches lock the clock position and the trailing edge of the OS locks the data in intermediate latches (L_1/L_5). Then a delayed shift pulse is generated which shifts the data into the registers and resets WIF and intermediate latches.

It should be noted that a time marker arriving just after a shift pulse will not produce a delayed shift pulse. This is because the latch BL_2 contains the same information (high level) as the data at the input of BL_2.

In fact a delayed shift will only occur if a time marker arrives < 25 nsec before a real-time shift pulse.

The memory scheme as presented here has the advantage of simplicity. Only the smallest time interval that can be measured (channel occupation time) is $\sim$ 80 nsec; that is, twice as long as the previously described memory organization. But if wire occupation time in a drift chamber is $\sim$ 80 nsec, this memory organization is sufficient.

5. USE OF THE TWO-CLOCK SYSTEM FOR DRIFT CHAMBERS

Measuring electron drift time in drift chambers is fully presented in Refs. 1-4. The final packaging of the TDC's described here for drift chambers is shown in Fig. 11.

It should be noted that the zero time reference coming from the scintillator counters or decision-making logic can arrive late for making event

selection possible. This reference signal is fed into the second stage of the wire amplifier so that differences in propagation delay between channels (cable + main part of amplifier) will not enter into the measured value.

6. CONCLUSION

A new TDC has been presented where the results are obtained by logic solutions rather than the use of very fast elements. For present-day electronics, where requirements are close to technological advances, this is very often a must. This approach would also facilitate the use of IC's and thus favourize the price/performance ratio.

A TDC such as this can be built using ECL-IC's (faster and more expensive) or TTL-IC's (slower and less expensive).

This TDC has been presented at the meeting "For future Omega detectors" (see memorandum: from Dr. A. Michelini, Ref. NP/OM 183, 1 June 1973). Since then a production prototype for a time resolution of $\sim$ 2 nsec has been started. For this prototype ECL and TTL-IC has been selected.

I would like to thank Professor E. Picasso for his confidence when he asked me to work on drift chamber electronics. I wish to acknowledge: the excellent help of Mr. A. Beer in building the electronics and all the physicists working on the future Omega detectors for their stimulating remarks and critisms.

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1) G. Charpak, F. Sauli and W. Duinker, High-accuracy drift chambers and their use in strong magnetic fields, submitted to Nuclear Instruments and Methods, 10 January 1973.

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3) C. Rubbia, The time stretcher, a device to measure the time of electron drift in proportional chambers, CERN NP Internal Report 73-1.

4) H. Verweij, Some remarks on electronics for drift chambers, submitted to the International Conference on Instrumentation for High-Energy Physics, Frascati, May, 1973.

5) E. d'Humieres, Codeur en temps par canaux de 1 nanoseconde, Centre de Recherches de la Compagnie Genérale d'electricité, Aout 1968.

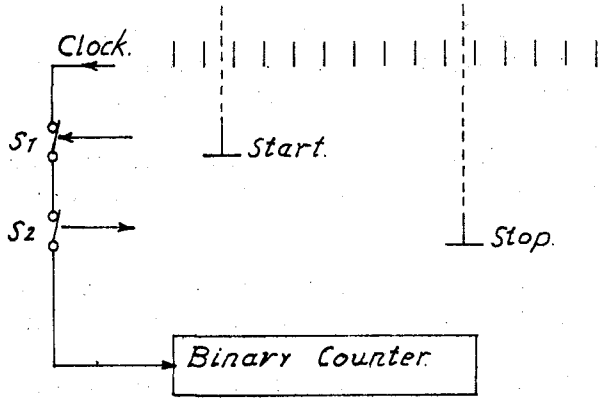


Fig. 1

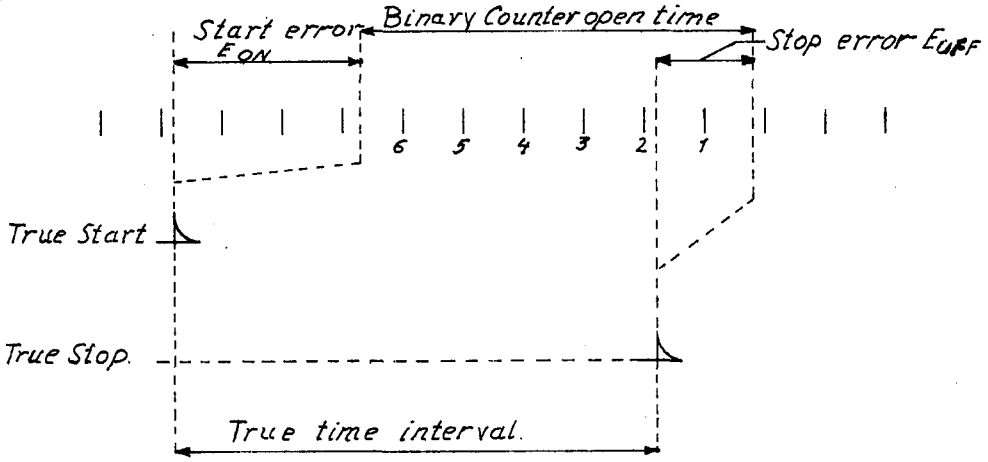


Fig. 2

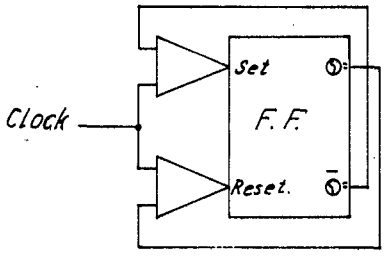


Fig. 3

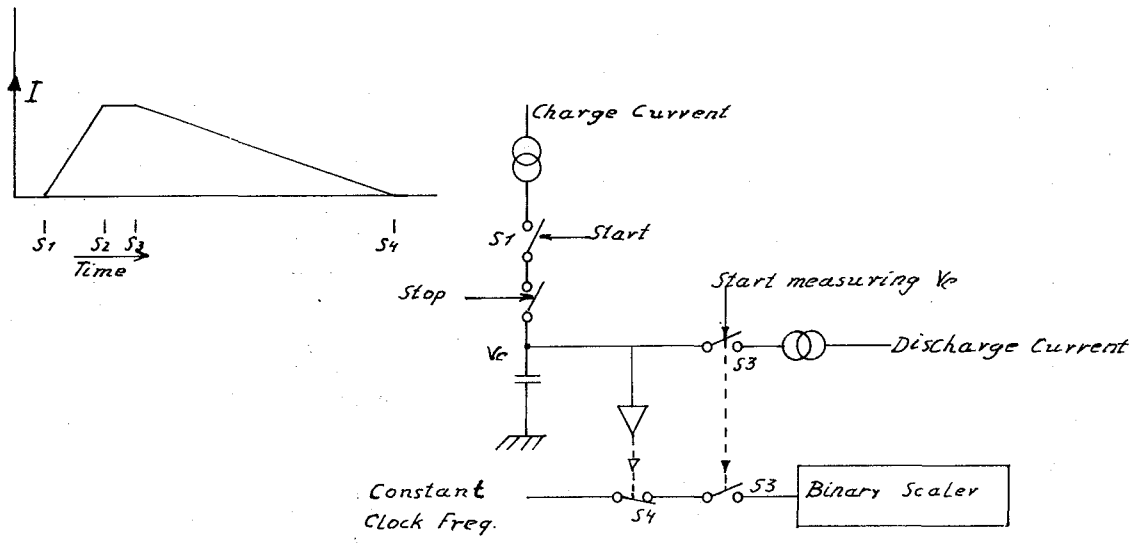

I
S1
S2
S3
Time
S4
Charge Current
S1
Start
Stop
Start measuring Vc
Vc
S3
Discharge Current
Constant
Clock Freq.
S4
S3
Binary Scaler

Fig. 4

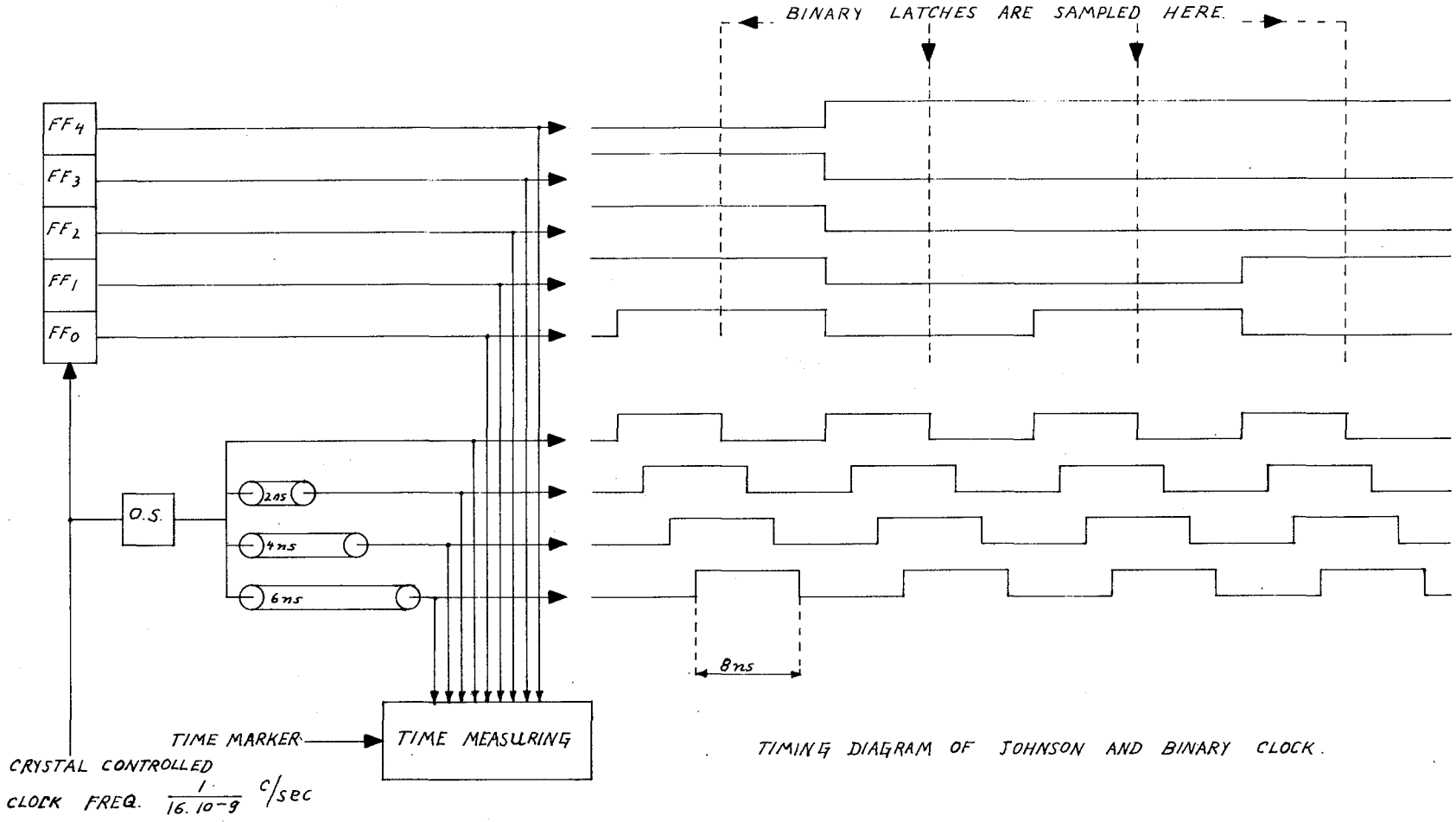

BINARY LATCHES ARE SAMPLED HERE.
FF4
FF3
FF2
FF1
FF0
O.S.
2ns
4ns
6ns
8ns
TIME MARKER
TIME MEASURING
CRYSTAL CONTROLLED
CLOCK FREQ. 1/16.10-9 c/sec
TIMING DIAGRAM OF JOHNSON AND BINARY CLOCK.

Fig. 5

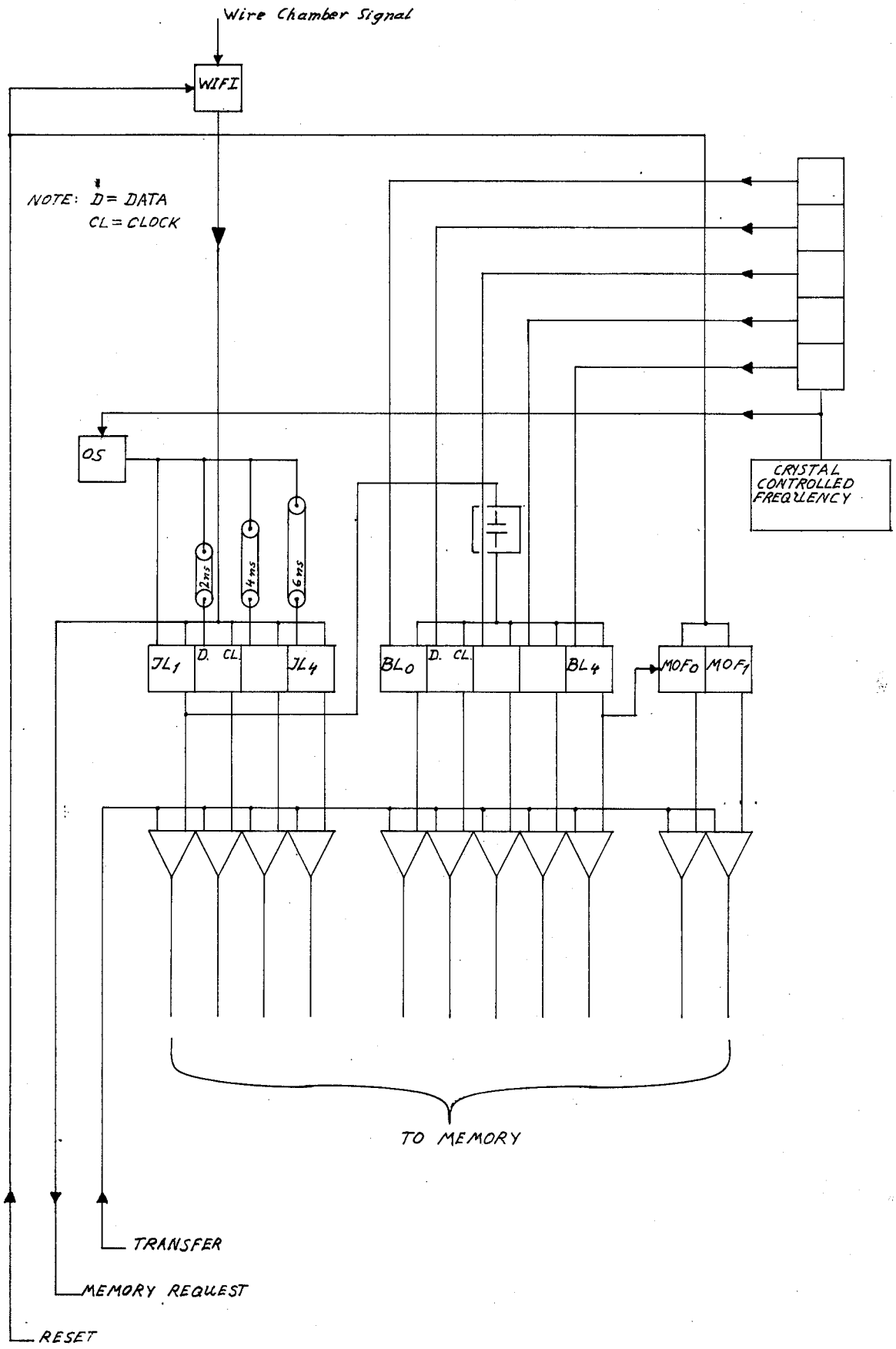
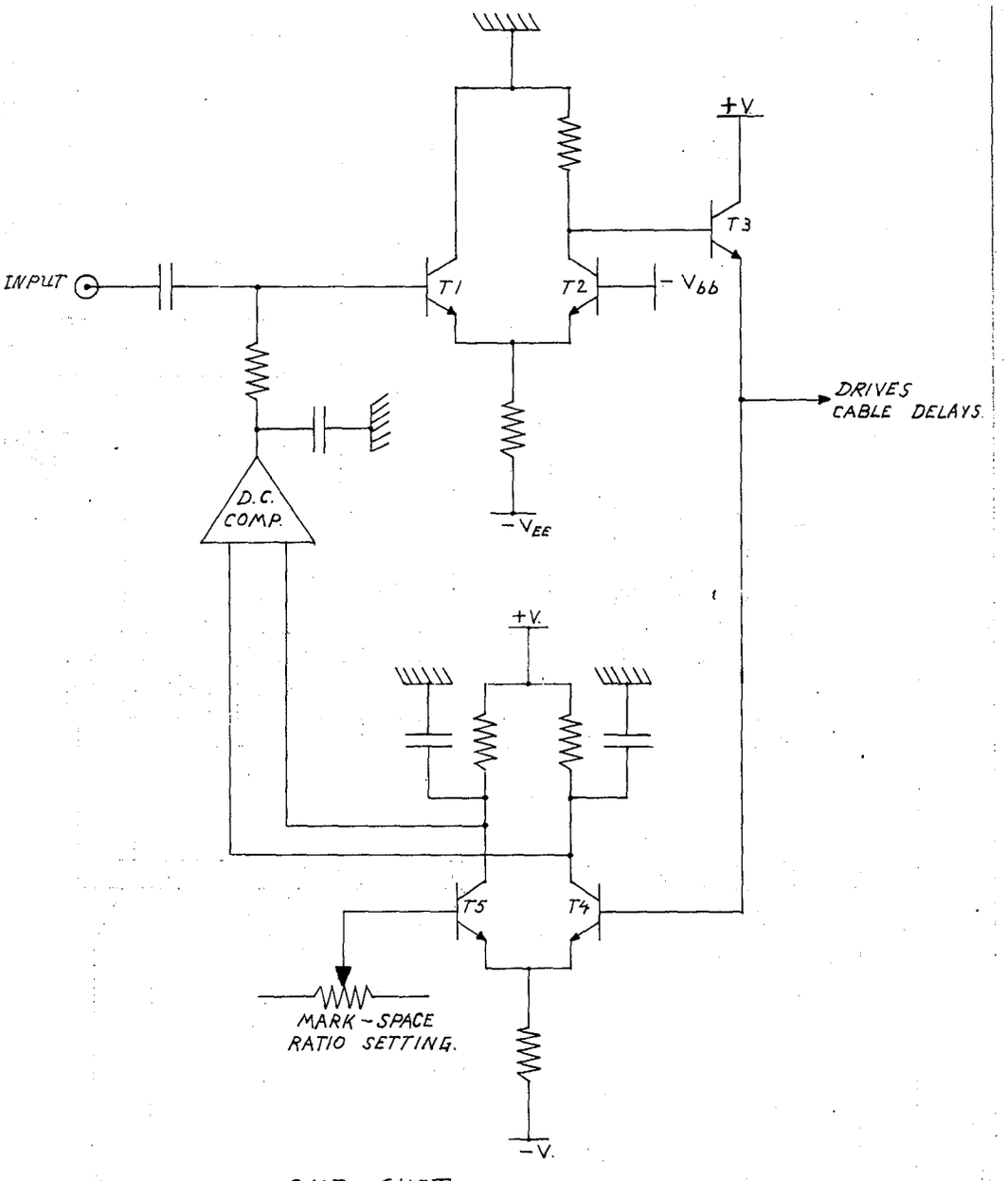

Wire Chamber Signal
WIFI
NOTE: D = DATA
CL = CLOCK
OS
CRYSTAL CONTROLLED FREQUENCY
2ms
4ms
6ms
JL1
D.
CL.
JL4
BL0
D.
CL.
BL4
MOF0
MOF1
TO MEMORY
TRANSFER
MEMORY REQUEST
RESET

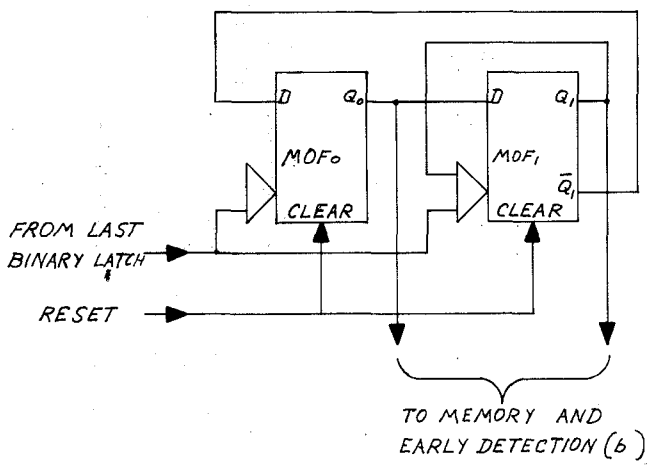
Fig. 6



ONE - SHOT.

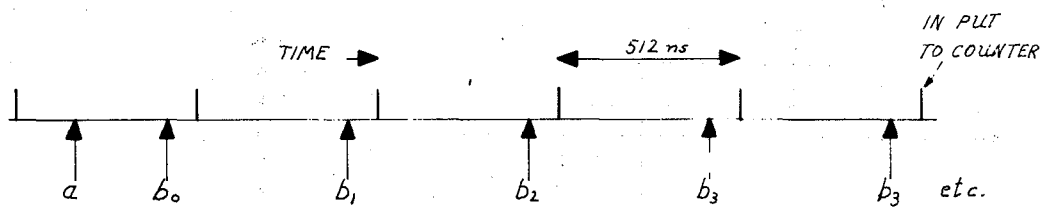
Fig. 7

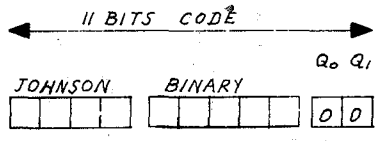
2- STAGE COUNTER



COUNT SEQUENCE

	Q_0	Q_1
RESET →	0	0
	1	0
	1	1
LOCKED →	0	1





Q_0 Q_1		TIME INTERVAL AND BOUNDARIES FOR DIFFERENT POSITION OF b WITH RESPECT TO a
0 0 $-b_0$	$b > a$	
1 0 $-b_1$	$b_1 \gtrless a$	$0 < (b_1 - a) + 512 < 1024$
1 1 $-b_2$	$b_2 \gtrless a$	$512 < (b_2 - a) + 2 \times 512 < 1536$
0 1 $-b_3$	$b \gtrless a$ $Y \geq 3$	$1024 < (b_3 - a) + Y \times 512 < (Y+1)512$

NOTE: a AND b ARE TIME MARKERS. Q_0/Q_1 CAN CONTAIN 4 POSSIBLE CODES ($b_0 - b_1 - b_2 - b_3$) IN THE 2- STAGE COUNTER.

Fig. 8

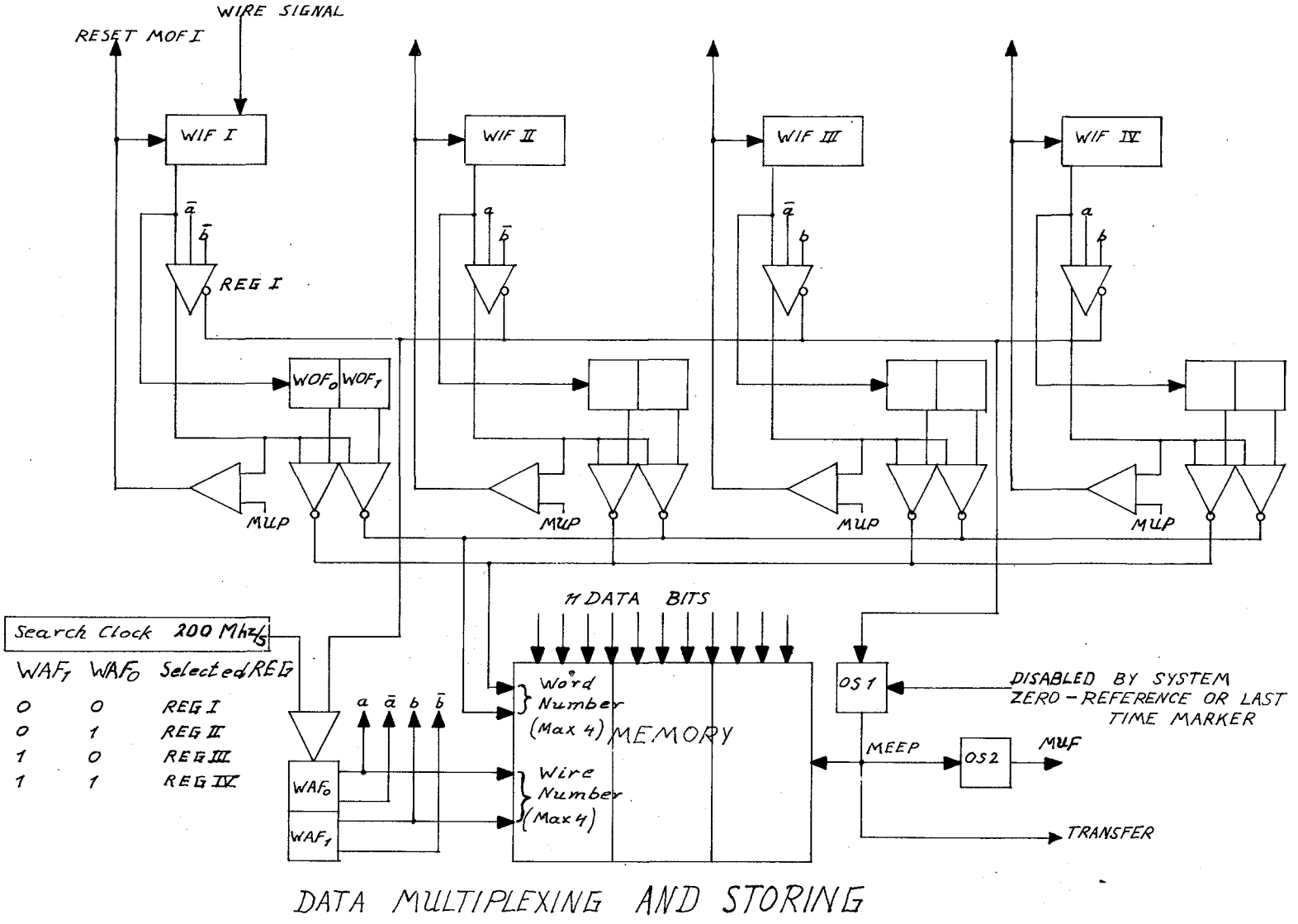

WIRE SIGNAL
RESET MOF I
WIF I
WIF II
WIF III
WIF IV
REG I
WOF0 WOF1
MUP
MUP
MUP
MUP
n DATA BITS
Search Clock 200 Mhz/5
WAF1 WAF0 Selected REG
0 0 REG I
0 1 REG II
1 0 REG III
1 1 REG IV
WAF0
WAF1
Word Number (Max 4)
MEMORY
Wire Number (Max 4)
OS1
DISABLED BY SYSTEM ZERO - REFERENCE OR LAST TIME MARKER
MEEP
OS2
MUF
TRANSFER
DATA MULTIPLEXING AND STORING

Fig. 9

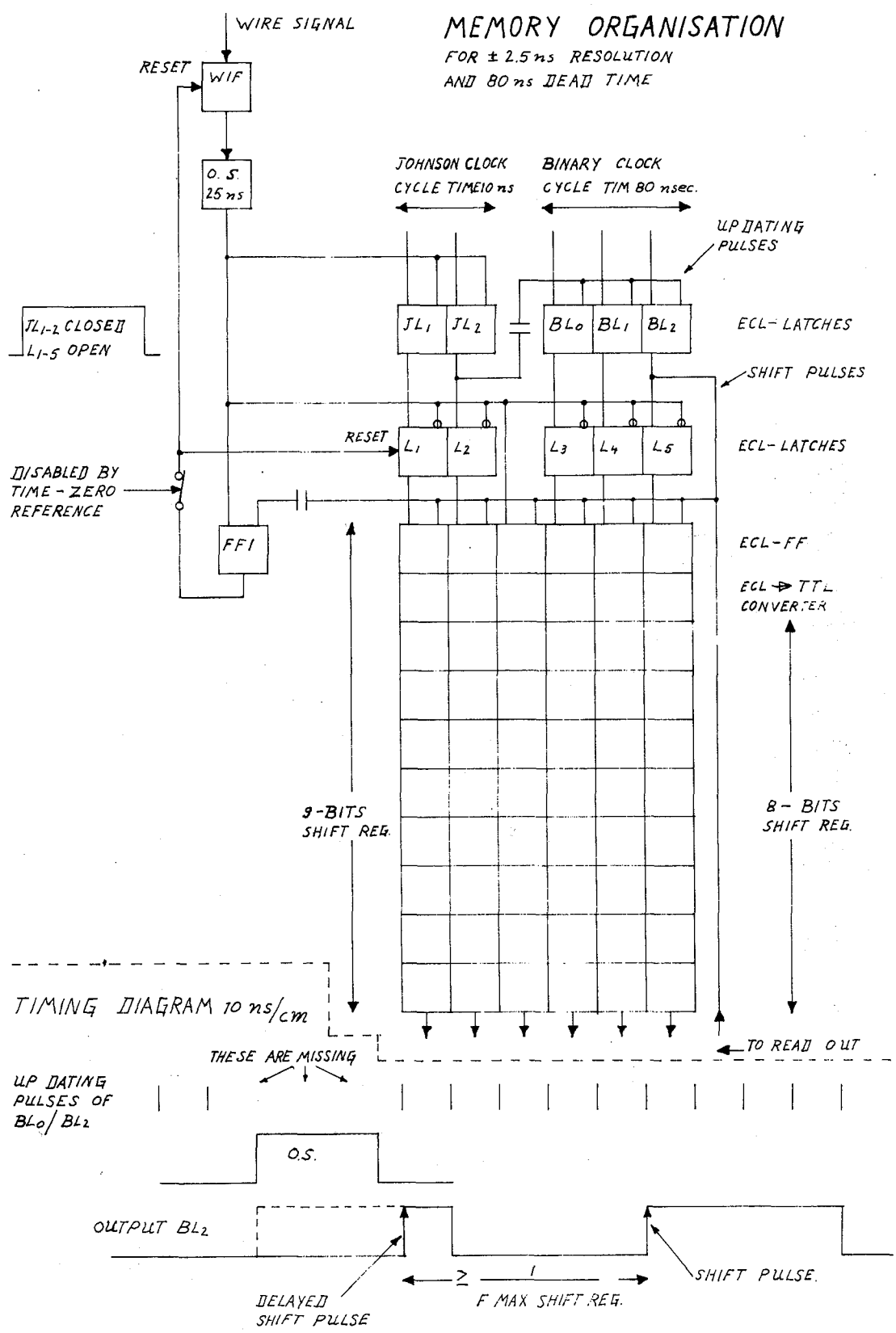

MEMORY ORGANISATION
FOR ± 2.5 ns RESOLUTION
AND 80 ns DEAD TIME
WIRE SIGNAL
RESET
WIF
O. S. 25 ns
JOHNSON CLOCK CYCLE TIME 10 ns
BINARY CLOCK CYCLE TIM 80 nsec.
UP DATING PULSES
JL1-2 CLOSED L1-5 OPEN
JL1
JL2
BL0
BL1
BL2
ECL- LATCHES
SHIFT PULSES
RESET
L1
L2
L3
L4
L5
ECL- LATCHES
DISABLED BY TIME - ZERO REFERENCE
FF1
ECL- FF
ECL → TTL CONVERTER
9-BITS SHIFT REG.
8- BITS SHIFT REG.
TIMING DIAGRAM 10 ns/cm
TO READ OUT
THESE ARE MISSING
UP DATING PULSES OF BL0/ BL2
O.S.
OUTPUT BL2
DELAYED SHIFT PULSE
≥ 1 / F MAX SHIFT REG.
SHIFT PULSE.

Fig. 10

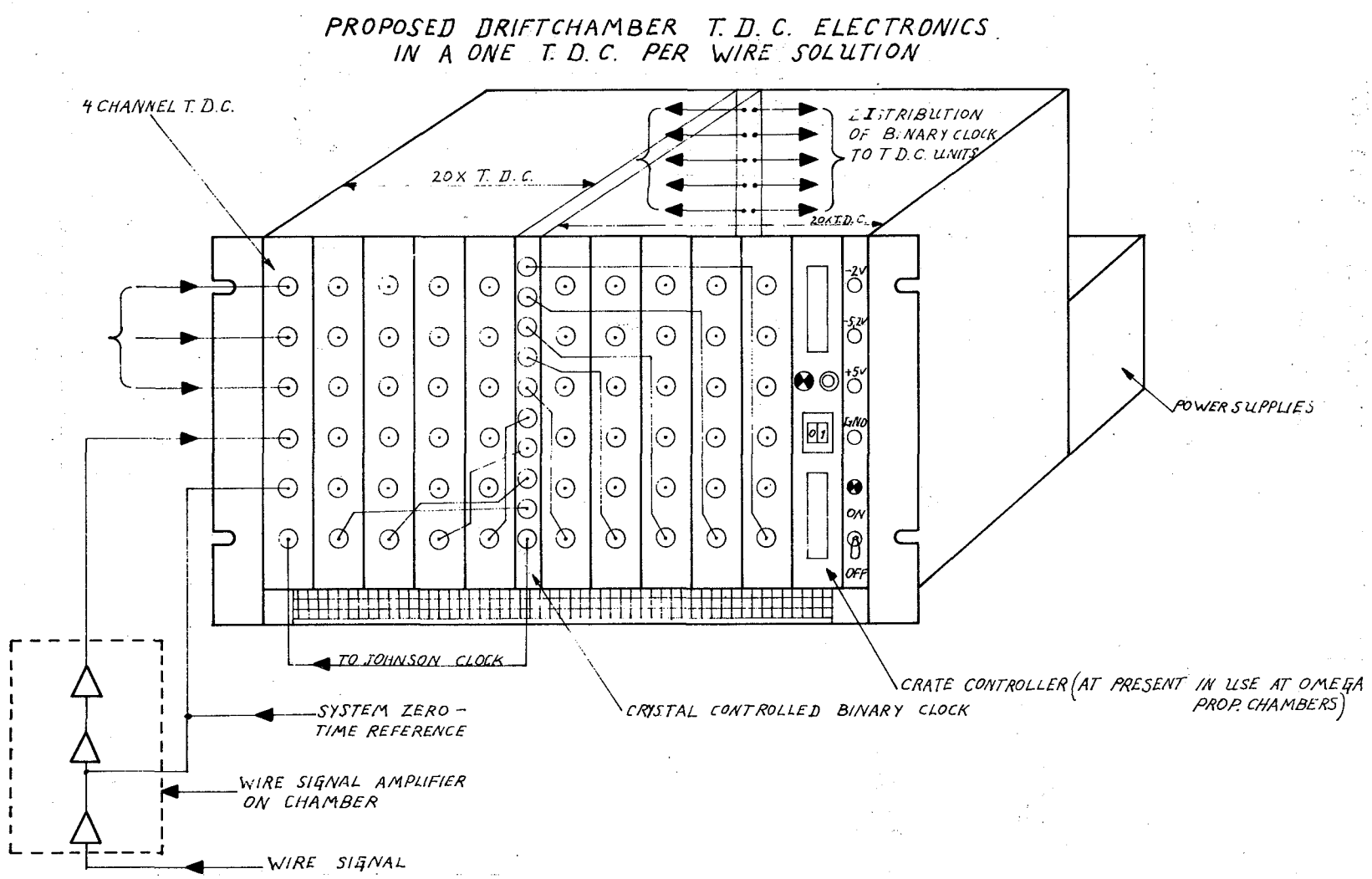

PROPOSED DRIFTCHAMBER T. D. C. ELECTRONICS
IN A ONE T. D. C. PER WIRE SOLUTION
4 CHANNEL T. D. C.
20 X T. D. C.
DISTRIBUTION OF BINARY CLOCK TO T D.C. UNITS
20 X T. D. C.
-2V
-5.2V
+5V
GND
ON
OFF
POWER SUPPLIES
TO JOHNSON CLOCK
CRYSTAL CONTROLLED BINARY CLOCK
CRATE CONTROLLER (AT PRESENT IN USE AT OMEGA PROP. CHAMBERS)
SYSTEM ZERO - TIME REFERENCE
WIRE SIGNAL AMPLIFIER ON CHAMBER
WIRE SIGNAL

Fig. 11