Design and Prototype Performance of the ATLAS Pixel Detector

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Abstract

The ATLAS experiment at the LHC will have three barrel and two times five disk layers of silicon pixel detectors as the innermost elements of the Inner Tracking Detector. The detector is built adopting the hybrid pixel technology in which 16 highly performant FE chips are connected to a silicon sensor by means of the bump and flip-chip technique. Owing to the high bunch crossing rate of 40 MHz at the LHC and the high particle fluences a sophisticated design concept is employed. The project is presently entering the pre-production phase. The various aspects of the design of the detector, the expected performance and the so far obtained prototype results are presented.

Introduction

The ATLAS pixel detector [2,3] sketched in fig.1 provides three precise space points along a track within $|\eta| \leq 2.5$ which are critical for pattern recognition near the LHC collision point and vital for the ability to determine secondary vertices of long lived particles. It is the largest of the pixel detector systems presently proposed comprising a total of 1.4×10^8 pixels and as many amplifying cells. The innermost B-layer is located as close as possible (4.1 cm) to the interaction point to provide optimal impact parameter resolution. While the building block unit, a module, is identical for the barrel layers 1 and 2 as well as for the disk system, the B-layer will have a different design to cope with the higher demands on its performance regarding radiation, band width and speed. The entire system comprises 2228 modules with 46000 pixels each covering a total area of about 2.3 m^2. It is supported by a light weight carbon composite, flat panel support structure which constitutes only 10% of the total weight of the pixel detector. Locally, the modules are fixed to barrel staves (13 modules per stave) and disk sectors (6 modules per sector), both of which

are all-carbon structures with carbon coolant channels and pipes, respectively. Using an evaporative fluorinert cooling fluid (C_4F_{10} or C_3F_8) the modules will be held below $-6°$C to assure optimal performance in the high radiation (up to 300kGy) environment. The system is hermetic down to transverse particle momenta of 1 GeV/c achieved by tilting and partially superimposing the modules. The tilt angle in the barrel is different in every layer and chosen as a compromise between the desire to counter-balance the Lorentz-angle effect occuring in a 2T magnetic field and the constraints imposed by the geometry of the arrangement.

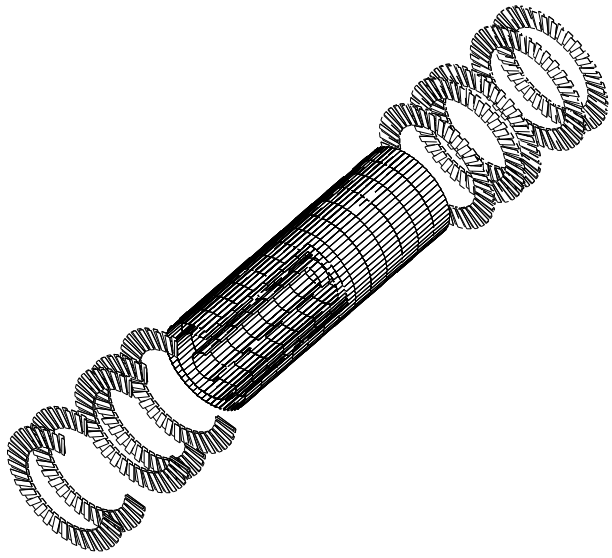

Fig. 1. Overall layout of the ATLAS Pixel detector system.

Design Features

In the "hybrid pixel technique" sensor and FE-chips are connected using the bump and flip-chip technology. In the ATLAS case the pixel area is 50μm$\times 400\mu$m (50μm $\times 300\mu$m in the B-layer) resulting in 50μm fine pitch bumping which is achieved with either PbSn (solder) or indium bumps at a failure rate of $< 10^{-4}$.

Modules

Sixteen FE-chips bump-connected to a silicon sensor (250μm thick, 200μm in the B-layer), equipped with control and clock circuitry as well as bus routing form a *module* of 2.1 cm by 6.4 cm area (fig. 2). In layers 1 and 2 as well as in the disk system FLEX-hybrid modules will be used. The FE-chip area is slightly larger than the sensor area. The I/O lines of the chips are connected via wire bonds to a kapton flex circuit glued atop the sensor. The flex houses a

module control chip (MCC) responsible for front end time/trigger control and event building as well as an optical package containing driving and receiving electronics for the optical signals via which each module is connected to the outside. The B-Layer, apart from being special in terms of higher fluence and resulting demands, will most probably also be removed and installed more frequently in order to allow access to the ATLAS beam pipe. For the B-layer modules ($\sim$ 8% of all modules) the so-called Multi-Chip-Module-Deposited (MCM-D) technology is adopted, in which a multi-layer structure is built up on the silicon sensor. This allows to bury all bus structures in four layers in the inactive area of the module thus avoiding the kapton flex layer and any wire bonding at the cost of a thickness increase of $0.1\%X_0$. Figure 3 illustrates the principle.

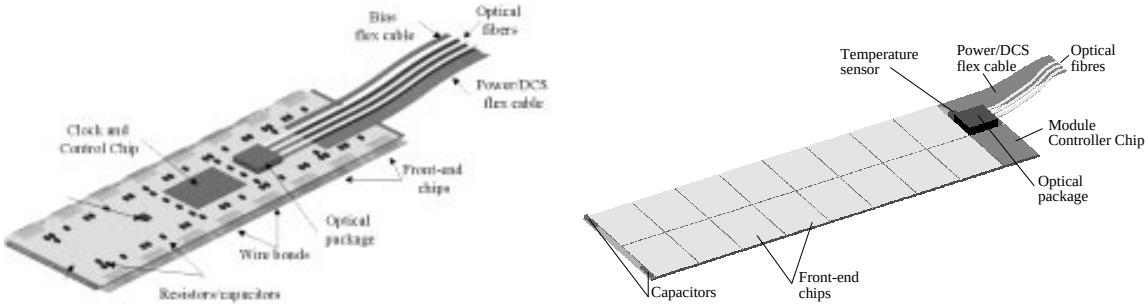

Fig. 2. The two module concepts. (left) FLEX-hybrid module (layers 1 and 2, disks), (right) MCM-D module (B-layer)

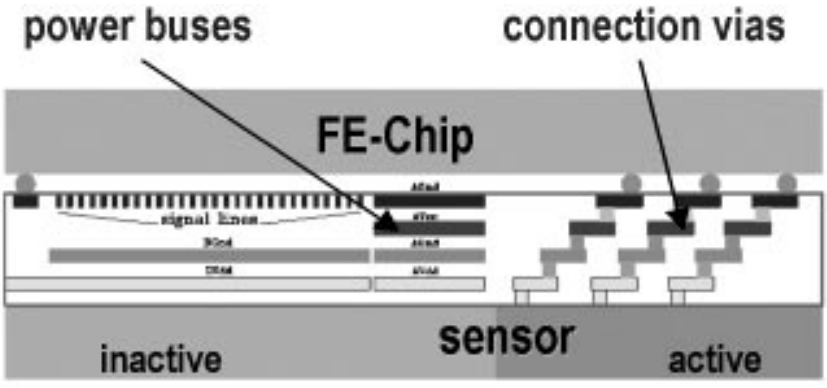

Fig. 3. Principle of the MCM-D module concept

Sensors

Radhard n^+ in n silicon pixel sensors [4] have been designed and fabricated in three prototyping iterations (see dedicated talk by F. Hügging [5] at this conference). Best performance was obtained using the p-spray isolation technique between pixel cells rather than p-stop implants, which has been commonly

used for strip detectors, providing the lowest electric field gradients at the implant boundaries after and - by employing a smoother dose at the transition regions - also before irradiation. Figure 4 shows the charge collection efficiency ($> 99\%$) obtained for this device for two adjacent pixels ($50\mu m \times 800\mu m$) which has a very homogeneous behaviour over the entire pixel area except for a region at the boundary between the pixels where a bias grid with two punch through biasing dots is located. While the efficiency is even better without this structure ATLAS has adopted this design for reasons of better testability (and hence yield insurance) of the sensors which by means of the grid is made feasible before the FE chips are connected. The sensors have been tested irradiated to 300 kGy or 10^{15} n_{eq}/cm^2 and have been shown to stand more than 600 V necessary for nearly full depletion after irradiation.

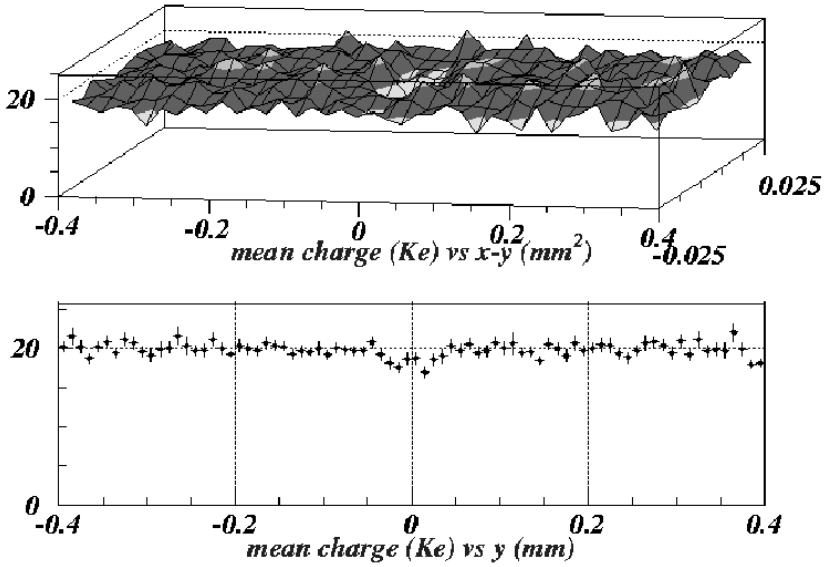

Fig. 4. Charge collection in two adjacent pixels (top) and projection onto the long pixel direction (bottom)

Electronics

Figure 5 shows an overview of the electronics components on- and off-module. The pre-assembled event (in the MCC-chip) is sent via optical link connections to the off-module Read-Out-Drivers (ROD) in which a 36 module event is formed and further processed in the Read-Out-Buffers (ROB) for a complete pixel event. The design and test of the rad-hard FE-chips, in which amplification and hit logic and storage must be done within a very limited available space is a formidable task, indeed. Several rad-soft prototype iterations have led to the so-called FE-D chip a predecessor of which is shown in fig. 6 and has been recently submitted. The architecture is characterized by a column-wise readout in which the time (7 bit) in units of the bunch crossing clock upon which an analog pulse crosses a discriminator threshold is stamped into a ram

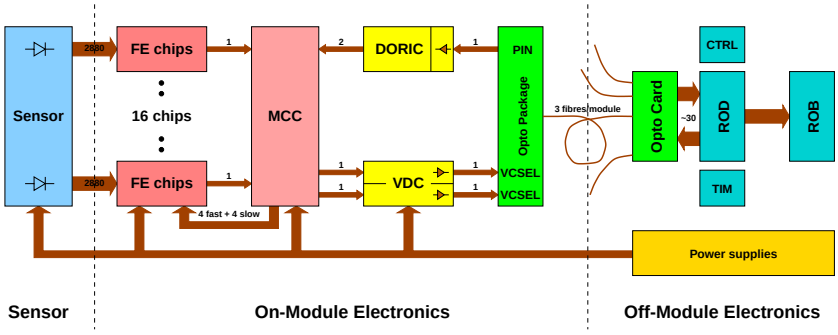

Fig. 5. Block diagram overview of the on- and off-module electronics.

present in every pixel cell. From there it is fetched by a fast scanner to be buffered at the bottom of the column until a first level trigger signal arrives. The column structure and the end-of-column logic can be recognized even in the photograph of the chip. In a little more detail the front end sticks out allowing a very fast and stable operation due to a dc-amplifier with a current source in the feed-back loop [3,6] which is able to also digest a leakage current up to about 100 nA at the input and which assures a linear decay of the amplified pulse. The latter then leads to the possibility to obtain a "poor man's" analog information (3-4 bit) by stamping the time into the column rams not only upon rising above but also upon falling below the discriminator threshold (time over threshold, ToT). Threshold fine tuning is achieved in every cell by a 3-bit DAC and a fast hit OR for tests and triggering. A mask and inject circuit is also provided. The block diagram is shown in fig. 7.

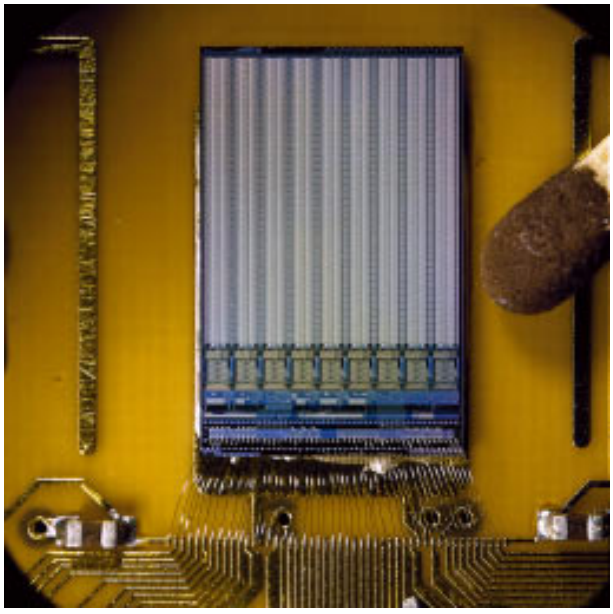

Fig. 6. Micro-Photograph of a pixel FE-chip

Prototype Performance

The performance of the critical pixel detector elements has been tested with prototype chips, sensors and modules as well as using mechanics elements. I will present here a few examples.

The challenges

The challenge imposed by the LHC physics on the pixel detector can be summarized in one sentence: in-time (i.e. 25 ns) detection of minimum ionizing particles with charges that might be as low as about 9000 e (most probable value) after several years of LHC operation due to irradiation. This in turn imposes severe requirements on the system

- low threshold operation (below $\sim$ 3000 e)
- low noise ($<$ 200 e)
- low threshold dispersion ($<$ 200 e)
- fast amplifier rise time ($\sim$ 20 ns)
- low time walk ($<$ 25 ns) and low time walk dispersion
- radiation tolerance to 10^{15} cm^{-2}
- large leakage current tolerance (up to 100 nA per pixel)
- low power consumption ($<$ 40 μW / pixel, 7.7 W per module)
- large cooling capacity (evaporative fluorinert liquid at -20°C)

An additional technical complication is added by the fact that these performance features must be maintained homogeneously in a system with 10^8 channels over a long period of time where only very limited access is possible during operation.

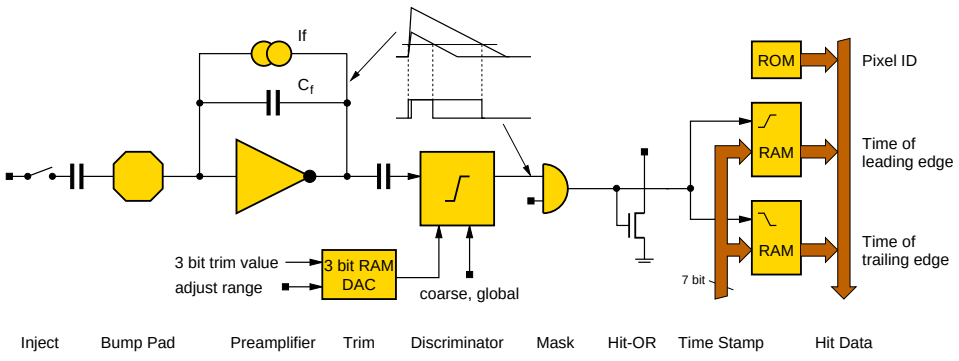

Fig. 7. Block diagram of the FE - electronics implemented in every cell

Performance of the FE-Chips

Figure 8(a) shows a preamplifier output pulse for an input charge of about 10000 e. Choosing different feedback current settings the return to the baseline can be slower or faster, depending on the needs (better ToT range or faster return) which are different for the innermost and the outer detectors. For complete modules global thresholds as low as 3000 e could be maintained in test beams with a spread of 230 e. The on-module noise was measured to be 150 e. Figure 8(b) shows the preamplifier noise as a function of the integrated radiation fluence. After a noise decrease at the radiation dose corresponding to the type inversion of the sensor bulk material, the noise then increases with fluence but stays well below 300e even for fast shaping.

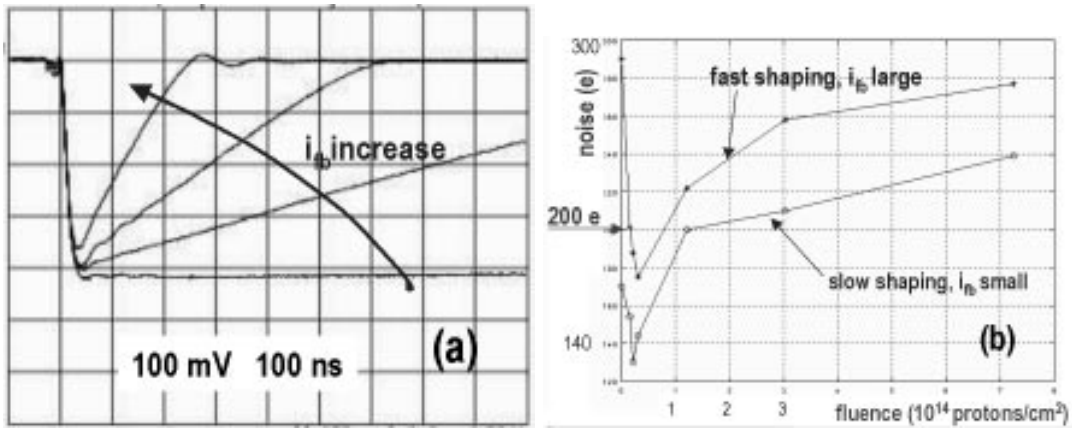

Fig. 8. (left) Preamplifier output response to a charge of about 10000e for various feedback current settings, (right) preamplifier noise as a function of the radiation dose.

Depletion depth and Lorentz angle

The depletion depth of the sensors can be nicely measured [7] operating the detectors at an angle with respect to the incident particle beam. From the projected particle trajectory inside the sensor volume the depth of the active (depleted) bulk below the pixel electrodes can be computed from the charge measured on adjacent pixels. Figure 9 shows the depletion depths determined in this way for pixel sensor assemblies before and after irradiation to the full LHC fluence of $10^{15} n_{eq}/cm^2$ and for different depletion voltages. Figure 9(b) indicates that after 10 years of LHC operation the depletion depth at the foreseen maximum operation voltage (600 V) will be shrunk to about 200μm. The Lorentz angle α_L is the angle of the drift path of the charge carriers (here electrons) in the sensor when operated in a magnetic field: $\tan \alpha_L = \mu_H B$, where μ_H is the Hall-mobility and B is the magnetic field in Tesla. It is desirable to optimize the amount of charge sharing between pixels for best spatial resolution and/or maximum charge yield after irradiation by tilting

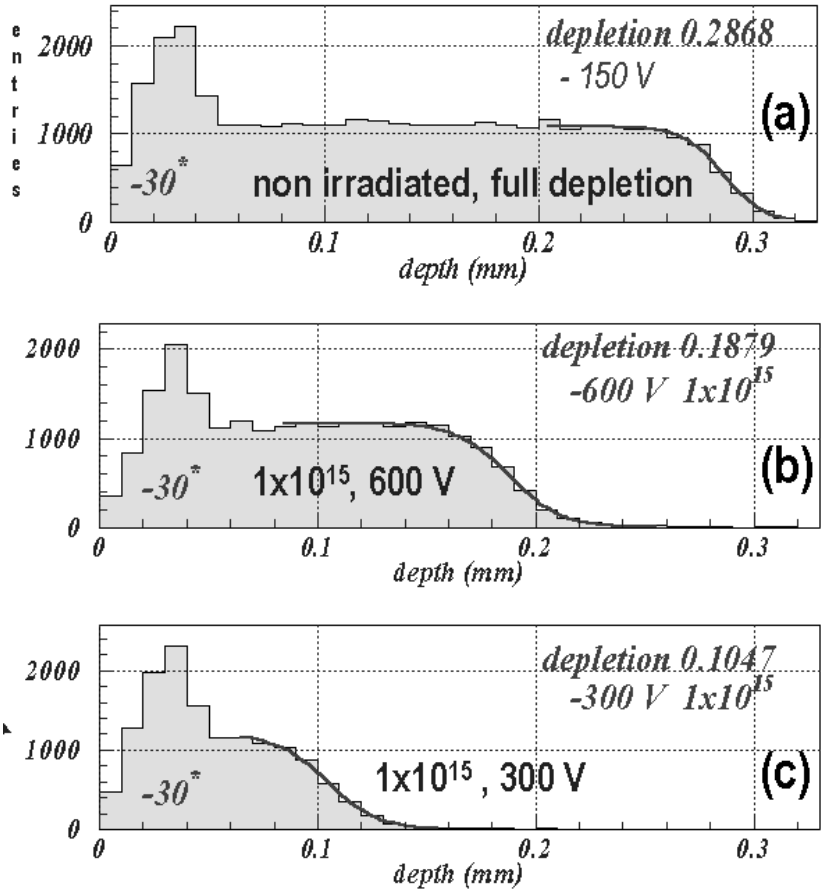

Fig. 9. Measurement of the depletion depth after irradiation for different conditions: (a) non-irradiated sensors, full depletion at 150 V, (b) irradiated to $10^{15} n_{eq}/cm^2$, 600 V, (c) same irradiation dose, but 300 V.

the detectors with respect to the beam line. In practice the geometry of the cylindrical layout in the barrel region leaves only little room for a variation of the detector's tilt. The Lorentz angle has been determined in the test beam by measuring the mean pixel cluster size as a function of incidence angle of the particle in a field of 1.4 Tesla. A decrease of α_L after irradiation by a factor of about three is observed. This behaviour is meanwhile understood [8] in terms of the change of the electric field inside the sensor due to the change in space charge and depletion depth for the applied voltage together with the functional dependence of the drift velocity $v_{drift}(E)$ on the drift field. For high E the simple relation for α_L is lost when the linearity between v_{drift} and E is no longer valid and saturation sets in. Measurements where the Lorentz angle rises after irradiation are reported by the authors of [9] for the CMS pixel detector.

Efficiency and Space Resolution

At LHC the collected charge in one pixel must be detected "in time", i.e. associated to the corresponding bunch crossing window of 25 ns. Because the discriminator's response depends on the height of the preamplifier pulse the time of a pixel hit will depend on the signal charge. The so-called time-walk is the charge above threshold necessary to observe a hit within 25 ns. Time-walk of a about 1000 e has been measured with prototype single chip assemblies with detector. The time-walk homogeneity over all pixels adds another uncertainty in this important characterization quantity. A total time-walk of the order of 2000 e is expected for ATLAS.

The "in-time" efficiency has been determined in test beams by measuring the hit efficiency relative to a track in the beam telescope as a function of the time of the track arrival (measured by a scintillation counter) with respect to the (free running) clock of the FE-chip. Using the selected ATLAS p-spray sensors with a bias grid a total in-time efficiency of 99.1% (98.4%) is measured with only 0.4% (1.2%) of all hits being lost because they are out of time. The numbers in parenthesis characterize the performance after full LHC irradiation. The number of two or more hits per particle decreases from about 15% before to $4-7\%$ after irradiation mainly due to the change in Lorentz angle.

Finally, the spatial resolution is measured as shown in fig. 10 using analog (ToT) information with the following observations: (a) the region in which charge sharing occurs extends to only $\pm 5\mu m$ between pixels, (b) the overall space resolution in the short ($50\mu m$) pixel direction combining the results for 1-hit and 2-hit events is $13(14.5)\mu$ m and in the long pixel direction it is $400/\sqrt{12}\mu$ ($300/\sqrt{12}\mu m$ in the B-layer). The numbers in parenthesis are for irradiated detectors. Using binary information only results in a space resolution which is marginally worse.

Summary

The ATLAS pixel project has now entered the pre-production phase. Radhard sensors have been produced and full radhard FE-chips with the final R/O architecture have been submitted. Full FLEX and MCM-D modules have been successfully assembled and characterized. It has been shown that the chosen design can cope with the fierce radiation and demanding detection environment expected at the LHC.

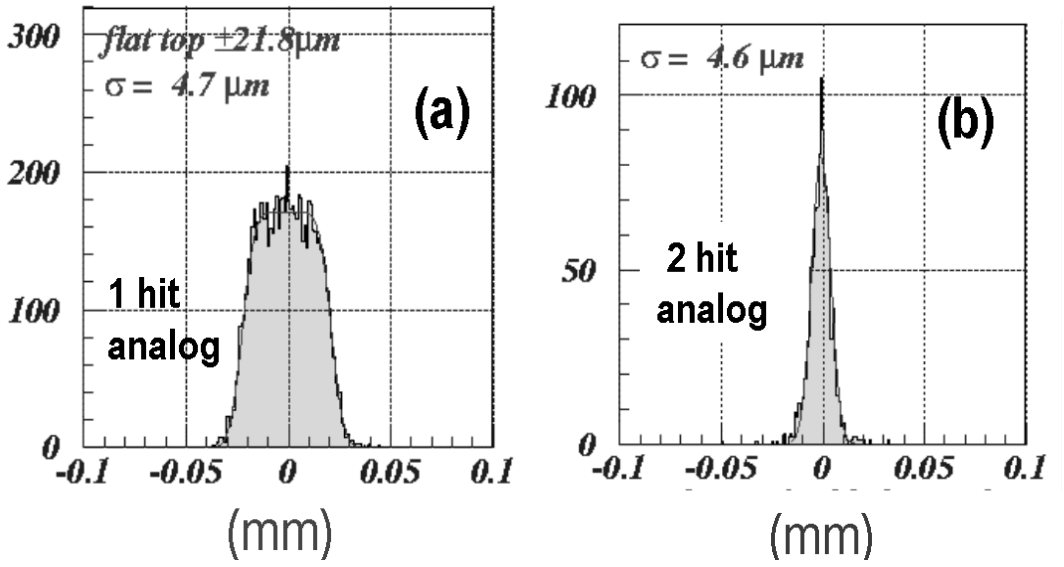

Fig. 10. Space resolution measured in testbeam conditions. Resolution using the ToT analog information (short direction of the pixel) for (a) single hit clusters, fitted with a flat top convoluted with a gaussian for the wings ($\sigma = 4.7\mu$m, (b) double hit clusters. fitted with a gaussian only.

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References

[1] Member institutes of the ATLAS pixel collaboration:
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