Development of Media Interfaces for Gbit/s Fibre-optic Links

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Abstract

An experimental 1.0625 Gbit/s fibre-optic media interface has been developed within the framework of the ALICE collaboration. First it has been used on the Destination Interface Unit (DIU) card in the ALICE Detector Data Link (DDL) project. The results of this development have also been applied in the design of the 2nd version interface cards in the Fibre Channel S-LINK project. These applications raised different constraints for the design of the PCB layout, signal routing, cross section, and power supply. The different realizations of the same media interface circuit gave us the opportunity to carry out thorough tests and measurements to compare and evaluate the different solutions used in the design of these PCBs.

Introduction

In a previous project, two media interface test boards (MI1 and MI2) were built in order to test the available electrical and optoelectronic interface components and gain experience about designing PCBs of digital circuits working at gigabit/s signaling speed. On MI1, we used Vitesse VSC7125 10-bit electrical transceiver chip and Methode MDX-19 optical transceiver module, on MI2 we used HP HDMP-1526 electrical transceiver chip. On MI1, we tried the so-called buried capacitance technology to improve the power supply decoupling.

The follwing tests and measurements were carried out on the experimental MI test boards:

Bare board measurements

- Buried capacitance evaluation
- Matched-trace impedance verification
- Impedance-limit verification

Component measurements

- Bypass capacitors
- Decoupling inductors
- Optical transceiver input impedance

Signal integrity tests

- Noise amplitude and spectrum
- waveform measurements

As the result of these tests we chose the Vitesse chip against the HP one, and decided to keep the 'buried capacitance' where other constraints on the PCB cross section allow this.

After these preliminary studies we started to design the media interface part of optical link interface cards in the ALICE DDL project. The same results were used in the S-LINK project, too, building the new version of the S-LINK interface cards.

In the DDL project, the DIU (Destination Interface Unit) has ben designed first. To help the designers of the logic parts of these cards, we chose a 20-bit wide data interface at 53.125 MHz clock speed instead of the 10-bit wide interface at 106.2 MHz. This had become possible, because Vitesse released the 20-bit version of his transceiver chip, VSC7126. Otherwise, this chip has the same characteristics as the 10-bit VSC7125.

In the S-LINK project, the first version of the Fibre Channel S-LINK cards used a standard GLM (Gigabit Link Module) daughterboard as the media interface. As this daughterbaord requires a lot of space and costs a lot, we improved the FC S-LINK cards by integrating the media interface on the board. With VSC7126 we were able to keep the original 20-bit data interface, did not have to move to 10-bit.

The DDL SIU (Source Interface Unit) card is the next link card where the same media interface will be applied.

These link cards have the following common block diagram. *Figure 1.*

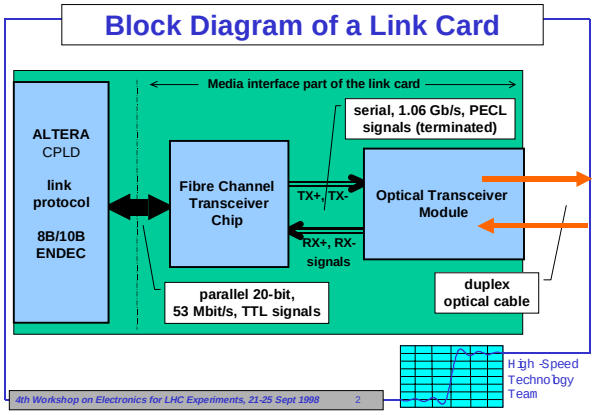

Figure 1

The media interface circuit has TTL compatible, 20-bit-wide data interface at 53.125 MHz clock speed. The Fiber Channel compatible electrical transceivers make the serialization/deserialization of the encoded data. The serial encoded data is transmitted and received at the rate of 1062.5 Mbit/s. These differential PECL signals are connected to the optical transceiver module that can be Fiber Channel or Gigabit Ethernet compatible. (FC optical transceivers are designed to work at 1062.5 Mbit/s, while Gigabit Ethernet transceivers can work up to 1250 Mb/s.) The optical interface is a duplex SC connector compatible with both Fiber Channel and Gigabit Ethernet standards. For the simplest test setup, the optical signal can loop back to the receiver.

The main features of the media interface design on the DIU card can be seen in *Figure 2*.

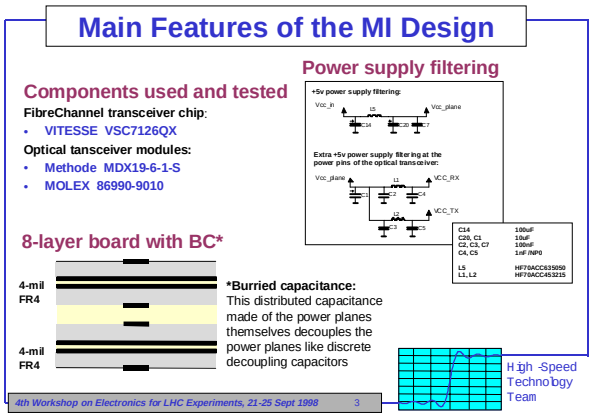

Figure 2

These applications raised different constraints on the design of the PCB layout, signal routing, cross section, and power supply. We laid emphasizes on the careful layout design keeping the general rules of high-speed board design and the instructions in the application notes of the components used. However, it was not possibe to keep every rule without compromise everywhere because of the constraints of the actual physical arrangement.

The main difficulty in the design of the FC S-LINK card has been that the same single PCB layout has to serve 4 different mounting options. These are the combinations of the following two alternatives:

- *copper media* (skipping the optical transceiver module) – *optical media*
- Media connector mounted on the *top side* – *bottom side* of the PCB.

The DIU card is a small form factor PCB populated with components very densly. This raised difficulties for the optimal routing of the signal traces. The SIU card will have an even smaller size meaning a real challenge to design and route the PCB.

The different realizations of the same media interface circuit gave us the opportunity to carry out thorough tests and measurements to compare and evaluate the different solutions used in the design of these PCBs.

We carried out a lot of measurements on the DIU and FC S-LINK boards. We mesured the followings:

- Waveforms of the critical signals.
- Jitter of the high-speed serial signals
- Power supply noise amplitude and spectrum

The following instruments were used in these measurements.

- HP 54120 oscilloscope mainframe
- HP 54121T TDR unit
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The setup for measuring the waveforms of the serial signals can be seen in *Figure 4.*

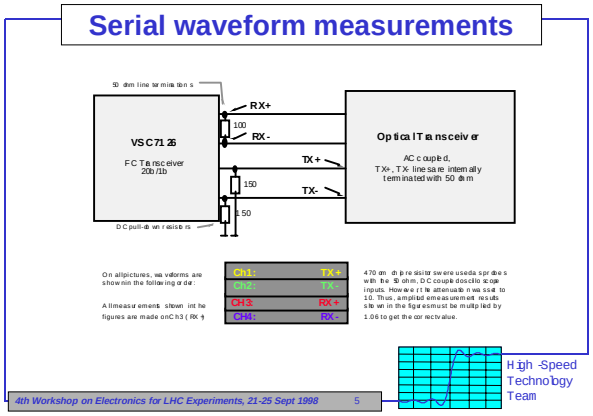


Figure 3

Test Results

The results of the test are summarized in the following points.

5. Signal-integrity tests

We have carried out a lot of signal waveform measurements at various conditions. Typical signal and noise waveforms can be shown in the following figures. (See *Figure 3-8.*) The PECL signals are nice. The reasons of the small distortions on the waveforms can be identified. On the transmit lines it happens because of the reactance of the internal input terminations of the optical module; on the receive lines on MI1 it is resulted by the not-ideal placement of the line termination resistors. We could not place them at the very end of the signal trace. This can be improved later. The reactive component of the impedance of the inputs of the optical module may also be compensated to further improve the signal quality. The power supply noise levels were measured at several places on the board. The amplitude of the noise is low, it is far below the level that can cause problems in the operation of the media interface. There is very few noise propagated back to the power supply. The SSN results are also satisfying, the transients are small enough, and are attenuated within a time window, when no sampling of the data occur. See *Figure 9.*

Conclusions

- The 3.3V VSC7125 transceiver chip has significantly lower power consumption than HDMP1526.
- Methode transceiver MDX-19 has built-in termination. It can be compensated for a better signal shape.
- Buried capacitance and careful placement of the discrete decoupling capacitors make quiet board.
- Signal integrity questions, including power supply noise, signal shape distortions, simultaneous switching noise and others, can be handled in such 100Mb/s parallel - 1Gb/s serial media interface card designs.

The results of these tests allow us to safely integrate the high-speed serial media interface directly on the DDL cards.

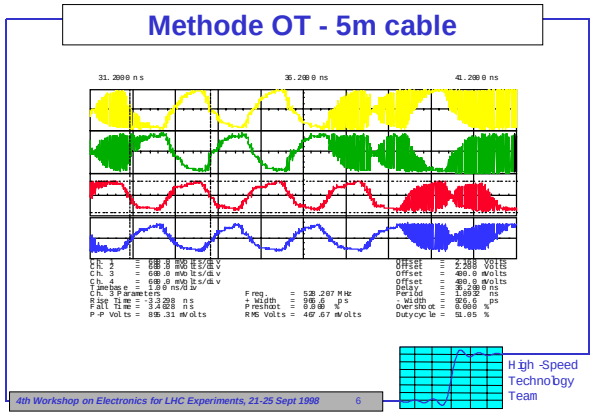


Figure 4

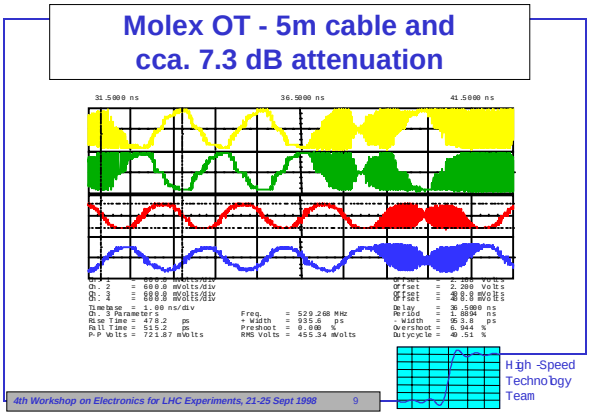


Figure 7

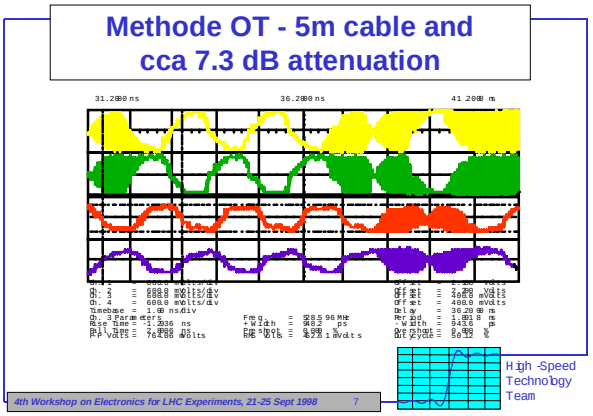


Figure 5

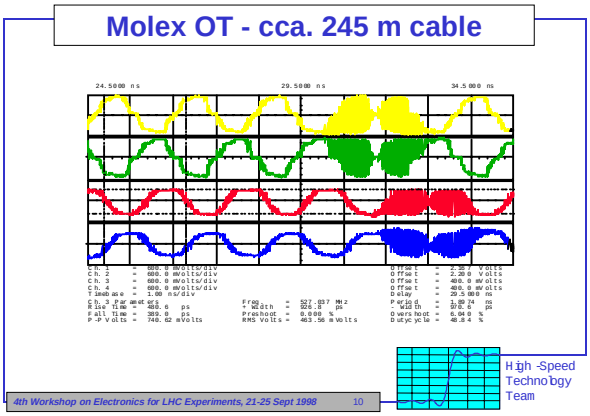


Figure 8

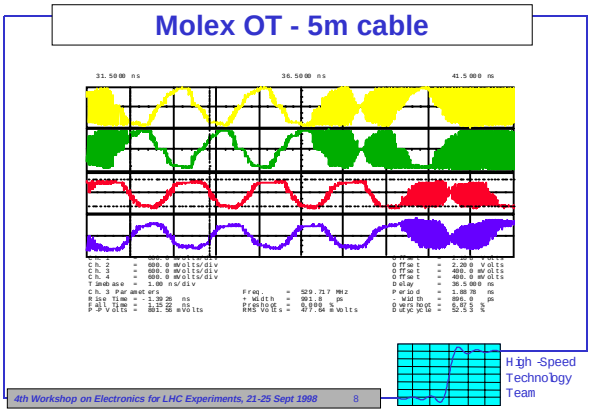


Figure 6

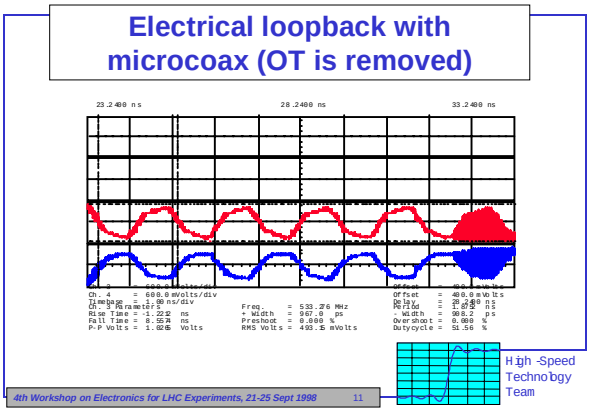


Figure 9

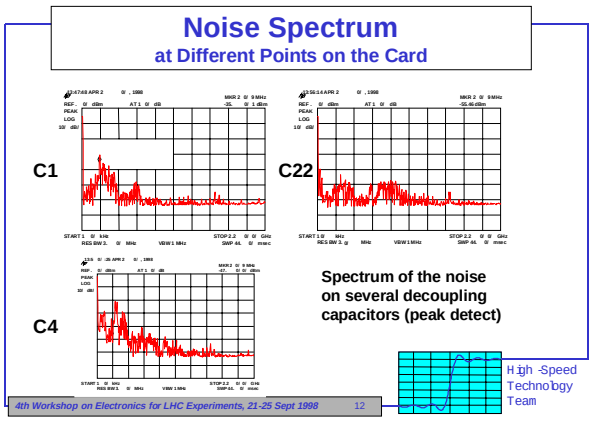


Figure 10

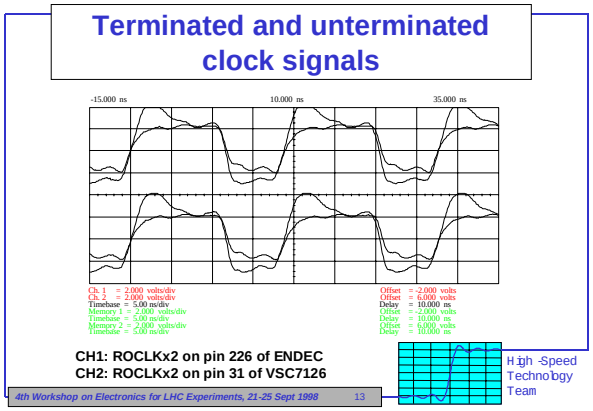


Figure 11

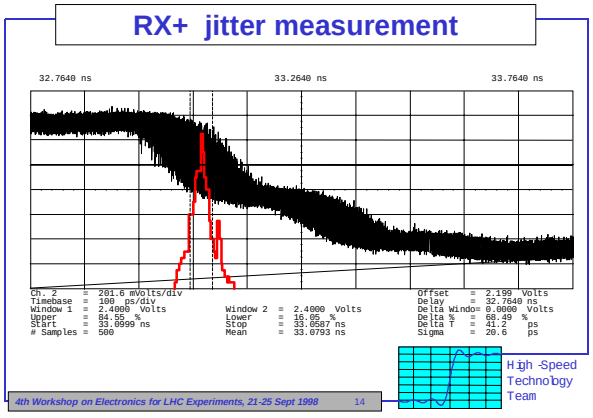
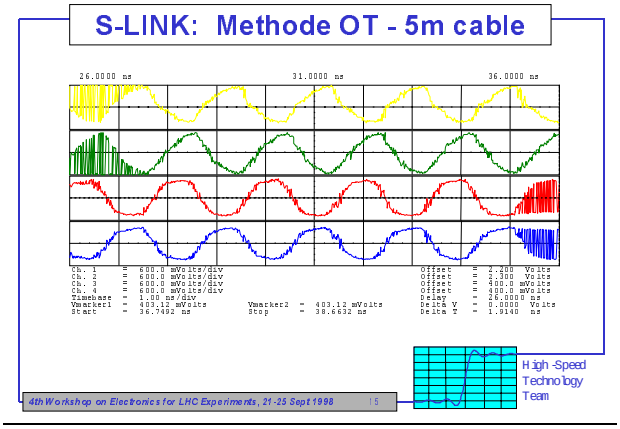


Figure 12



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