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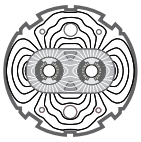

Large Hadron Collider Project

LHC Project Report 311

High Precision and High Frequency Four-Quadrant Power Converter [±600A, ±12V]

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Abstract

The LHC (Large Hadron Collider) particle accelerator makes extensive use of true bipolar power converters. All these converters will be installed in excavated caverns underground; hence the necessity for minimum volume and high efficiency for the power converters.
This paper presents the design and the realisation of a compact (19",6U) and high frequency (50 kHz) four-quadrant power converter [±600 A, ±12 V].
The obtained performance (DC stability, efficiency, EMC,…) is presented and discussed.

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1. Introduction

The Large Hadron Collider (LHC) is a 7 TeV proton-proton collider to be installed in an existing, 27 km long, accelerator tunnel by the year 2005 [1]. The LHC particle accelerator makes extensive use of true bipolar power converters [±600 A, ±12 V] to correct the multipole errors of the main superconducting magnets. These power converters will feed sextupole and decapole spool piece circuits as well as octupole magnets. Several trim magnets also require 600 A four-quadrant converters. In total there are around 500 such converters.
These four-quadrant converters will be installed in excavated caverns underground; hence the necessity for minimum volume and high efficiency.

The main requirements are:
- high precision (<50 ppm)
- galvanic isolation between mains and load
- very high reliability and operational redundancy; access to the underground areas will be difficult and time consuming.
- reparability. All converters must be designed with fast plug-in modules (6U module) to facilitate rapid replacement.

The normal industrial topologies for a four-quadrant converter are:
- converters consisting of anti-parallel thyristor bridges with a circulating current (known as dual converters). The main drawbacks of this topology are the volume and weight (50 Hz transformers and passive filters) and the low bandwidth.
- topology using a 50 Hz step-down transformer, a diode rectifier and a PWM inverter. This solution has the disadvantage to use a large and heavy transformer.

The disadvantage of these topologies is low efficiency due to the presence of two conversion stages working at low voltage and high current. In addition, the power flow is controlled by a hard-switching inverter working with high current. During the phase where the magnet is acting as a generator, the energy is dissipated in a resistance ("brake chopper").

To improve the above-described topology, this paper presents a topology where a unipolar resonant converter replaces the first conversion stage. The output stage consists of two branches: one is acting as a polarity switch and the other handles the magnet energy dissipation.

2. Four-Quadrant Topology

Unipolar resonant converter topology

The diagram of the converter (Figure 1) is composed of: a diode rectifier, an H.F. inverter (I1), an H.F. series resonant network (L2, C2, C2'), an H.F. step-down transformer (T1), an H.F. rectifier, and the output converter.
A high switching frequency (>30 kHz) is necessary to obtain a large bandwidth and also to reduce size and weight of the converter. The bandwidth enables good rejection of the mains harmonics and disturbances.

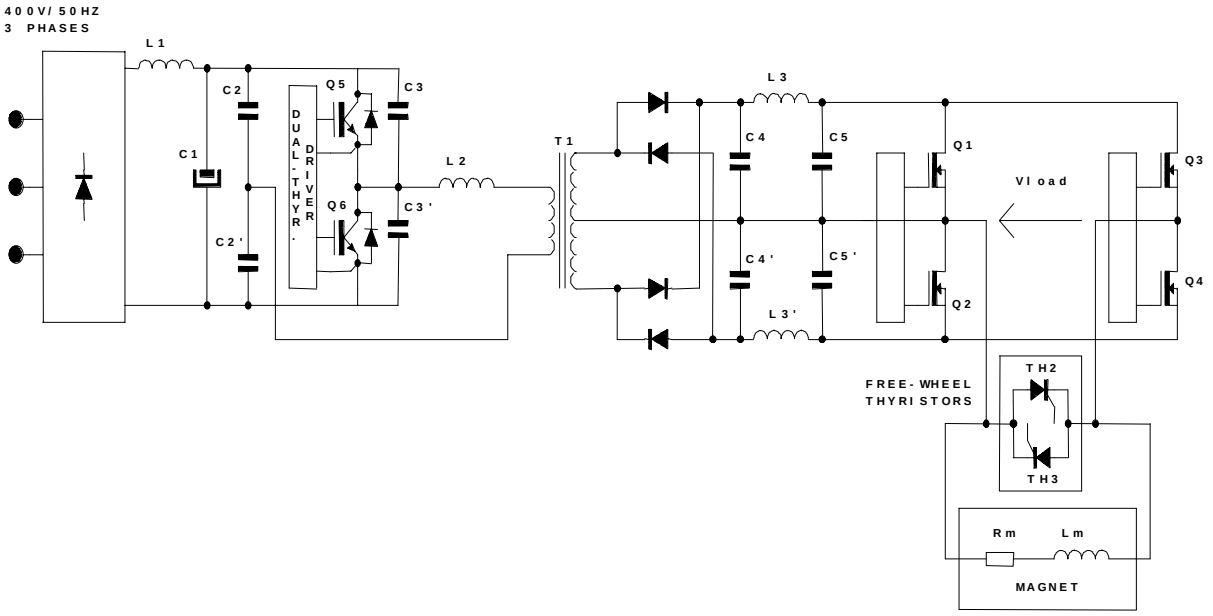


Figure 1 : Four-quadrant soft-commutation converter

The inverter uses a switching frequency of 50 kHz and a 600 V voltage source which forces the use of MOS or IGBT transistors operating in ZVS or ZCS mode. MOS transistors are not well suited for ZCS mode and have more conduction losses than IGBT for a voltage source greater than 300 V. Therefore IGBT transistors operating in Dual-Thyristor mode (ZVS) are more suitable [2]. The voltage source of I1 is the 400 V three phase distribution network rectified and filtered (L1, C1). For a low output power (7.2 kW) and voltage (12 V), a half bridge inverter is preferred since it reduces inverter losses, the transformer ratio and cost. The inverter I1 is a series-resonant inverter operating above the natural frequency (45 kHz) and the control range is between 50 kHz and 110 kHz. Turn-off losses are reduced with a lossless snubber consisting of a single capacitor placed in parallel across each IGBT.
The series-resonant inductance value is minimised by making use of the leakage inductance of the transformer. The H.F. step-down transformer T1 has a centre-tap secondary connected to the H.F. full bridge rectifier. Thanks to current rectification, PIN or Schottky diodes can be used. Capacitors C4 and C4' make the main H.F. output filter, and L3, C5 (L3', C5') an auxiliary filter to comply with EMC requirements.

Output converter topology

The output converter is a full-bridge inverter built with low voltage MOS transistors. One branch operates in linear mode (Q1, Q2) and handles the magnet energy dissipation, while the other branch is a polarity switch (Q3, Q4). Consequently, there is no H.F. switching. The dimensioning of Q1 and Q2 is imposed by the energy to be dissipated from the magnet. Q3 and Q4 are dimensioned to minimise voltage drop at full magnet current.
When the reference voltage is positive, Q3 is ON and Q4 is OFF, else Q3 is OFF and Q4 is ON. The current in Q3 or Q4 can be positive or negative depending on the power flow direction.

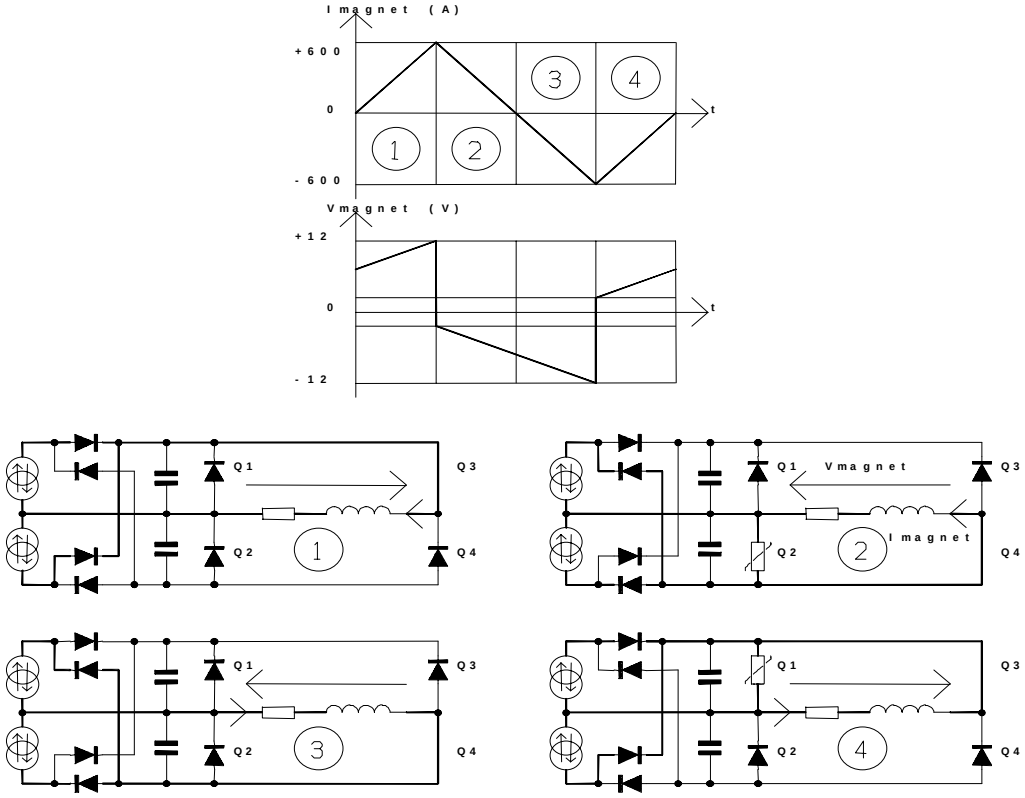


Figure 2: Working principle of output inverter I2

Transistors Q1 and Q2 have two functions. The first is to dissipate the energy of the magnet :

- If the sign of output voltage and output current is the same (quadrants 1 and 3, Figure 2), Q1 and Q2 are OFF.
- If the sign of output voltage and current are different (quadrants 2 and 4, Figure. 2), Q1 or Q2 is conducting, depending of reference voltage sign.

The second function of Q1 and Q2 is to allow ZVS operation of the inverter IGBTs even at low output current.

The working principle of the output converter can be seen in Figure 2. The current sources simulate the centre-tap secondary transformer of the series-resonant inverter. When a MOS transistor is blocked, it is symbolised by its parasitic diode. A small resistor in series with a large inductor models the magnet.

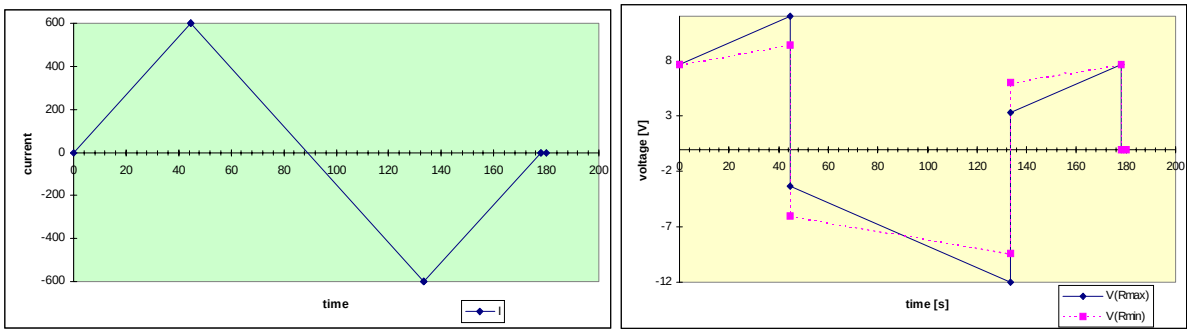
3. ELECTRICAL DESIGN

The four-quadrant converter is designed to feed superconducting magnets with an inductance L of up to 570 mH and a resistance R between 2.8 and 7.2 mΩ. The current (I) could vary from –600 A to +600 A with linear ramps of up to 13.5 A/s or stay at constant value.

Output voltage

The load voltage V is given by the V = R.I + L.dI/dt. The maximum voltage is obtained at maximum of current, inductance and ramp rate (Figure 3):

- with R_{max} the voltage reaches 12 V maximum in the first quadrant and –12 V in the third. The converter power is 7200 W in generator mode.
- with R_{min} the voltage begins at –6 V in the second quadrant and 6 V in the fourth. The converter power is –3600 W in brake mode.



a) Output Current Cycle @ 13.48A/s, 178 s period

b) Output Voltage with R_{max} = 7.2 mΩ and R_{min} = 2.8 mΩ

Figure 3: Output current and voltage waveform.

Working area

The reference voltage is produced by the digital or analogue current control loop. To prevent excessive braking power during an abnormal step-down of current reference, a limitation is implemented in the current control loop. To simplify the limits, a useful area in V(I) plan is defined. It is suitable for resistances between minimum and maximum, and it has a parallelogram shape (-12 V to +6 V at –600 A, -9 V to +9 V at 0 A, -6 V to +12 V at 600 A). The whole area is used during current transients with inductive and resistive loads, but only a part is used in static operation with resistive loads. With this limitation, the dissipation Mosfets should be designed to handle a maximum energy of 175 kJ for a cycle (cycle defined in Figure 3) instead of 205 kJ, with a maximum power of 3600 W instead of 7200 W or more.

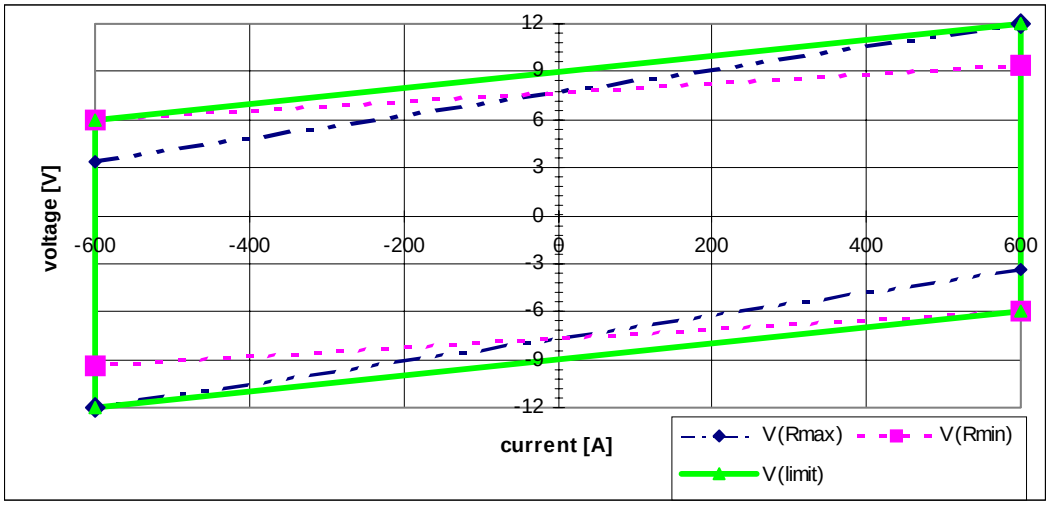


Figure 4: Useful area in output voltage and current.

Converter

The H.F. inverter uses one 1200 V half-bridge module (Q5/Q6, Figure 1). The Dual Thyristor function is synthesised by a custom driver made with discrete components. The output converter uses forty 50V MOS transistors to dissipate the magnet energy (Q1/Q2, Figure 1) and for the polarity switch (Q3/Q4, Figure 1). The H.F. inductor and transformer are made with ferrite U-I cores and Litz wires. The transformer, H.F. rectifier, output power capacitors and the forty MOS transistors are interconnected with busbars. The IGBT, H.F. rectifier, H.F. inductor and transformer are water cooled. The H.F. current loop, output voltage loop, switching control and four-quadrant control strategy, use analogue and programmable logic devices.

Converter fault and magnet quench protections

The converter output must always assure a safe path for the magnet current. An electronic device, constituted of two back-to-back thyristors (crowbar), turns on if an over-voltage appears at the converter output (>20V). The triggering of the crowbar is completely autonomous and does not need any auxiliary voltage. An extra resistor (1 Ohm) can be placed in series with the thyristors to discharge the magnet energy quickly.

4. MECHANICAL DESIGN

Figure 5: [±600A, ±12V] power converter; 6U module.

The four-quadrant converter is designed as a 6U module inserted in a 19” rack and is thus extremely compact (Figure 5). The weight of one power module is 74 kg. To allow easy insertion and extraction for an operator, it is placed on lateral slides. Two people can carry it thanks to the removable side handles.

Two complete power converters, each including a power module, an output circuit with two DCCTs, the crow-bar protection and two 6U CERN electronics chassis, are housed in one 19" rack of 1.8 m total height (Figure 6). Each power module is supplied with cooling water and mains and is thus fully independent.

Before unplugging a module, self-sealing water connectors have to be removed from the front panel for the inlet and outlet, the signal cables to the CERN electronics and the mains. The DC outputs are placed on the rear side of the module. They are quick-fit connections (Multi-contact®) and do not require manual action.

Figure 6: 19"rack with two converters.

5. PERFORMANCE

Test on resistive loads.

To verify the static performance in the generator quadrants (1 and 3), variable water-cooled resistors with a small inductor (1 mH) have been used.
Figures 7 and 8 show the output voltage ripple which is < 1 mV_{rms} in the 50 Hz - 30 kHz frequency band and < 2 mV_{rms} in the 3 MHz band (Rload = 19.5 mΩ)

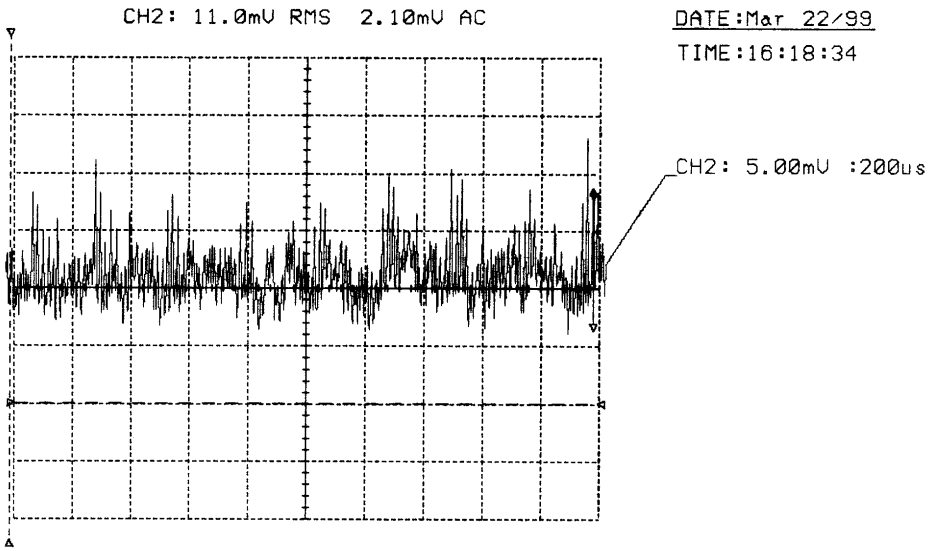


Figure7: Output voltage ripple @450 A, 8.8 V

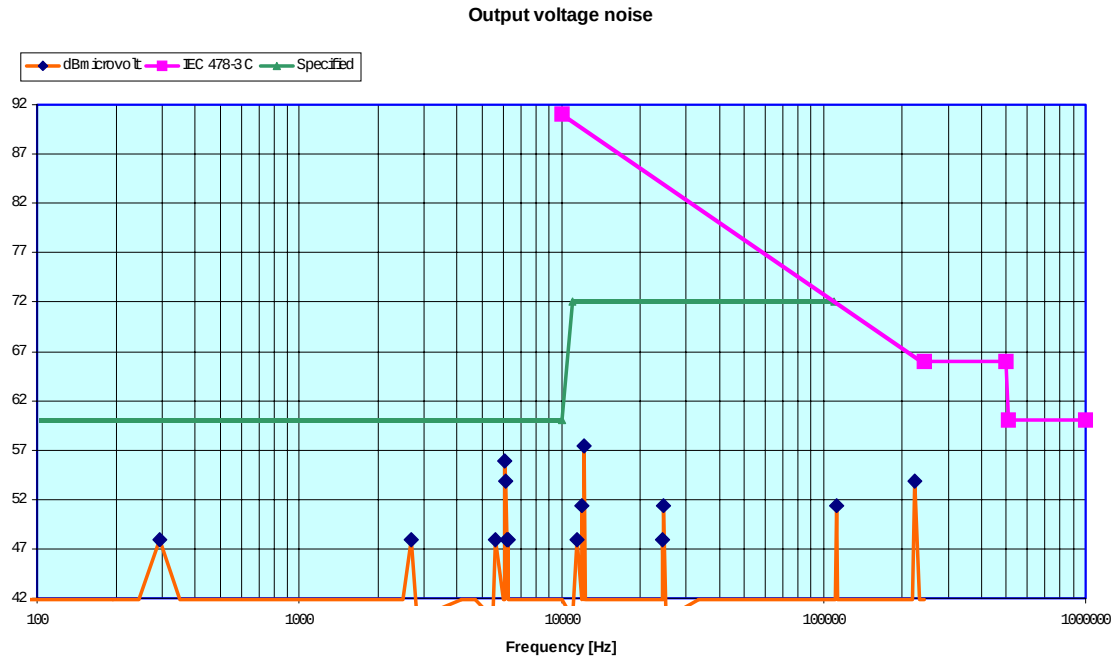


Figure 8: Frequency spectrum analysis of the output voltage ripple @450 A, 8.8 V.

Figure 9 shows the output voltage ripple for different currents at constant resistance. At zero current and zero voltage the output polarity changer commutates between two thresholds and produces a small voltage ripple of ±20 mV.

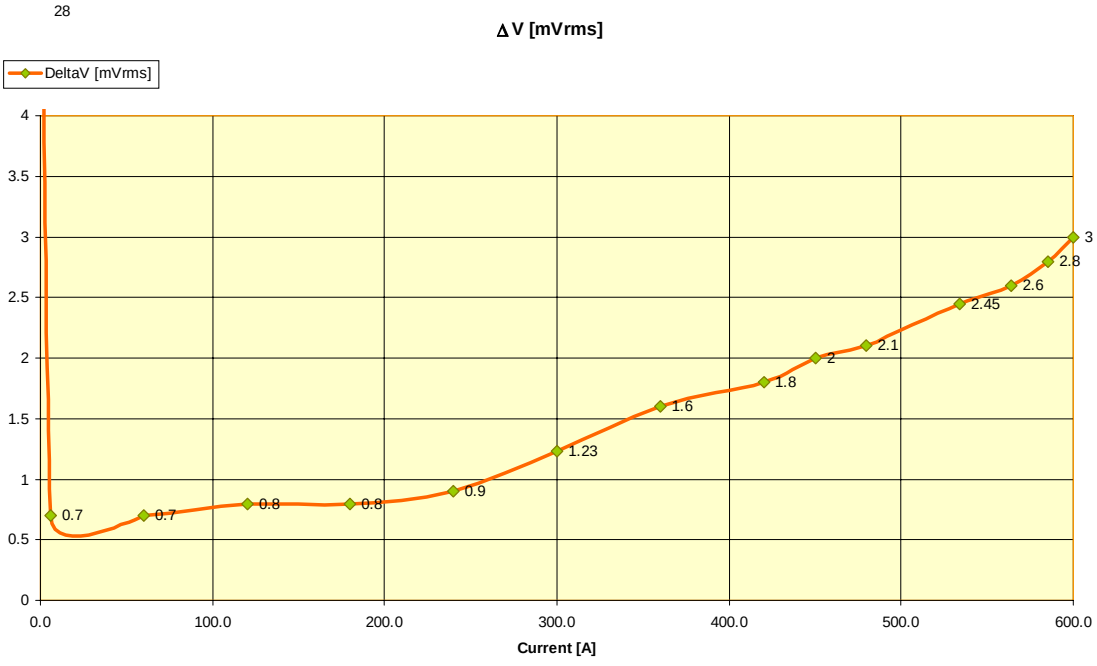


Figure 9: Output voltage ripple on 19 mΩ

A mains with unbalanced amplitudes up to 10%, does not produce output voltage ripple. As a voltage source the frequency response has a bandwidth of 3 kHz.

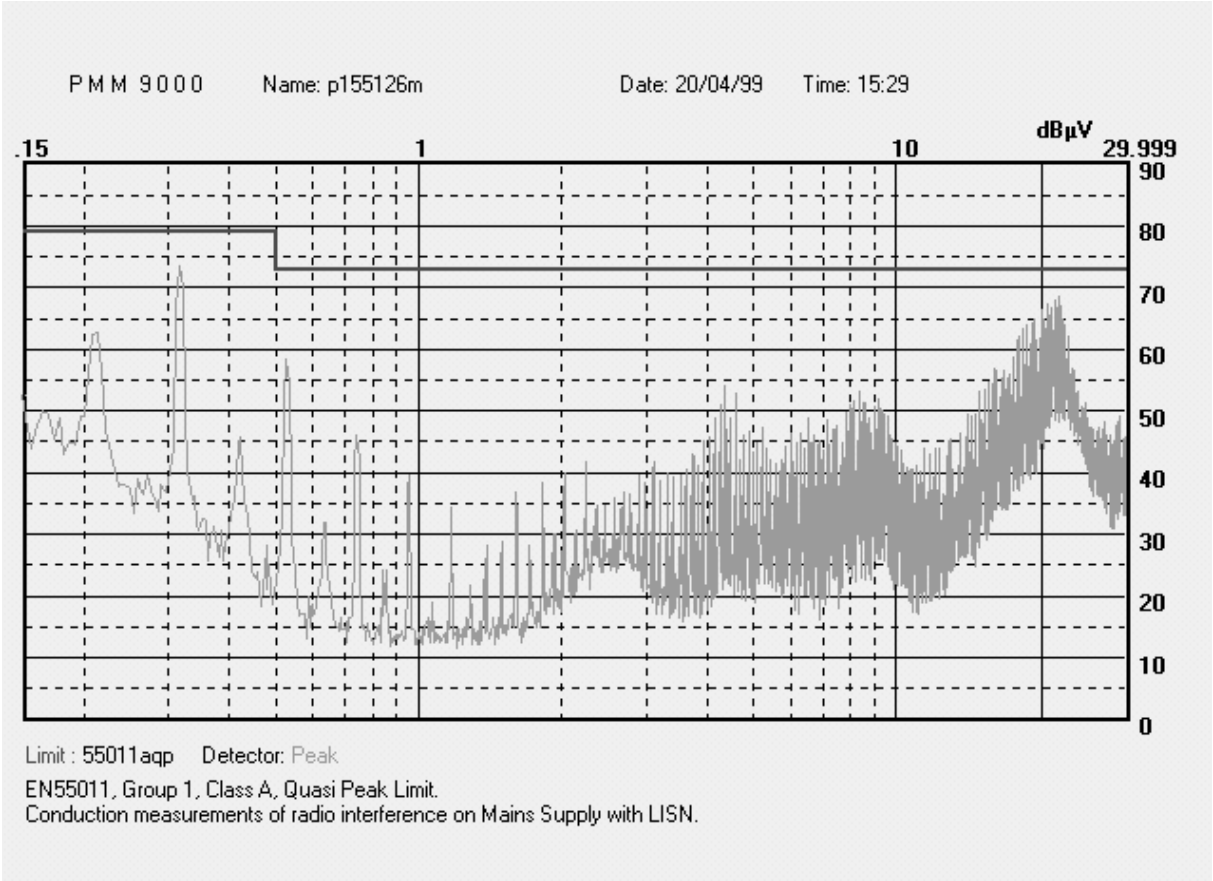


Figure 10 : E.M.I. voltage on mains supply

The Figure 10 shows the radio-interference voltage (bottom) measured with a Line Impedance Stabilising Network (LISN) on the mains supply. The EN55011 standard specifies a Quasi Peak limit (top) in the 150 kHz – 30 MHz band. Peak detection gives the worst case because the measurement is attenuated by 3-6 dB with the required standard Quasi Peak Detector. The converter is CE compliant.

The measured efficiency (included CERN electronics) is more than 75% from half to full power range (Figure 11).

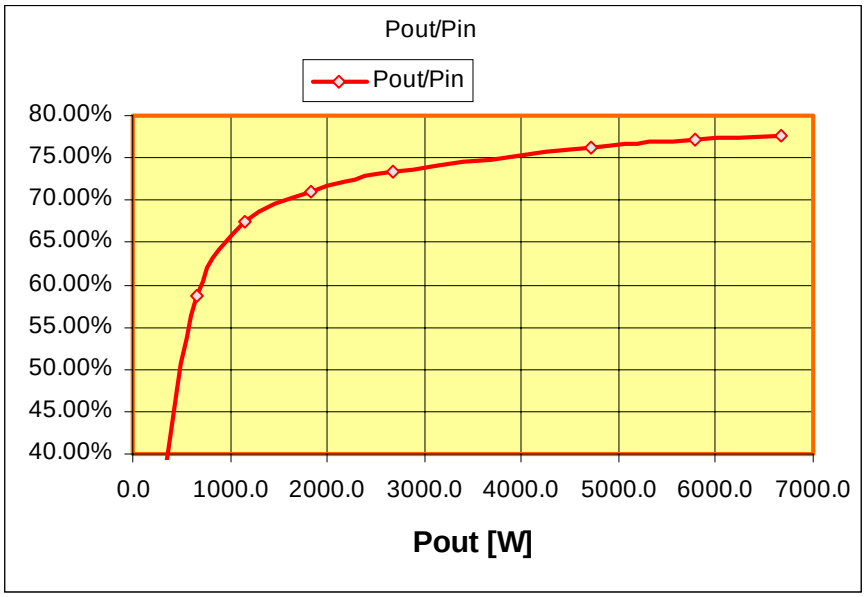


Figure 11: Efficiency with 20 mΩ load

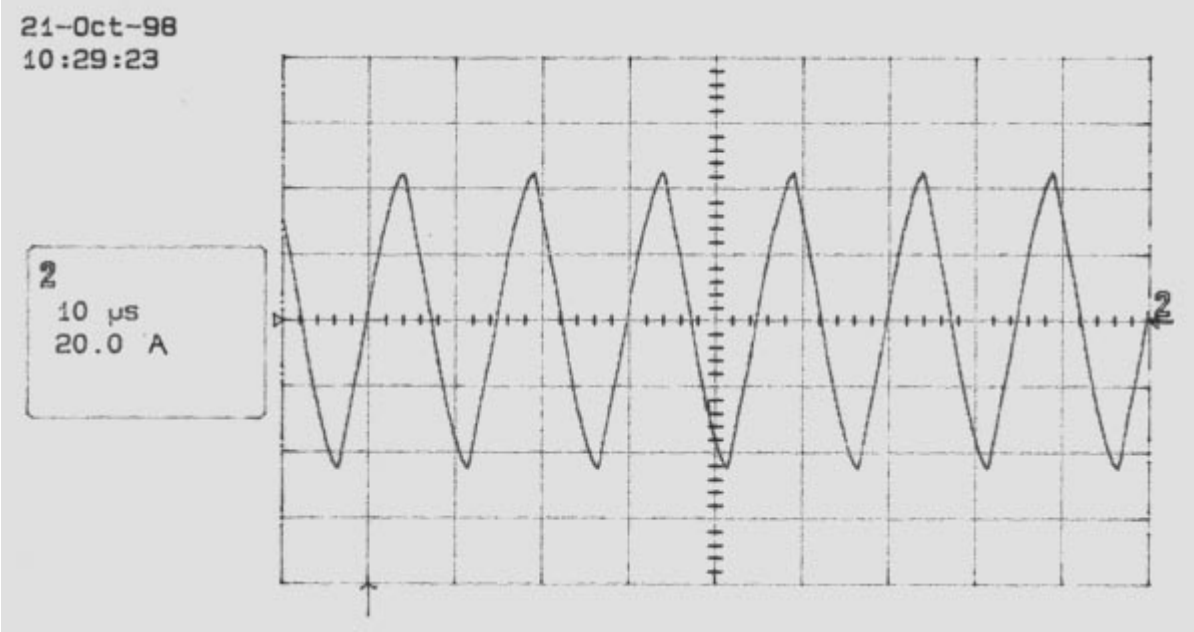


Figure 12: Inverter current @ 600 A, 0.35 V

In Figure 12, the IGBT switched current is about 45 A and the switching frequency is 67 kHz. This operating point represents the maximum of the IGBT switching losses (#200W). The inverter operates in Dual-Thyristor mode (ZVS) in the whole working area.

Test on inductive loads

With the aim to test the converter in the brake quadrants, the use of small inductors is not sufficient. Then, a dummy load, modelling inductance of up to 16 H, allows to test the zero-crossing of the output current (Figure 13) [3].
Tests on real superconducting magnets have can be carried out (±600 A on 36 mH and ±60 A on 6 H), with the current ramps (respectively ±5 A/s and 0.5 A/s). These converters are presently used intensively to evaluate the LHC corrector magnet prototype.

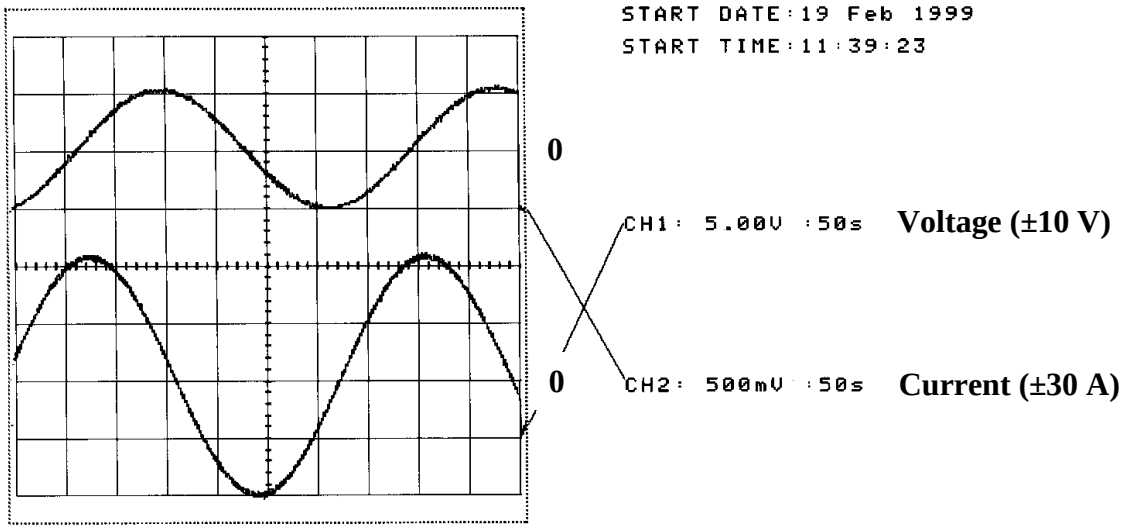


Figure 13: Zero-crossing of the output current with a dummy load of 15.8 H and 80 mΩ.

Test of the working voltage-current area.

The use of two similar converters, connected in opposite direction, was used to evaluate the performance in static or transient mode. One is controlled as a current source and the other one as a voltage source. The current and voltage references can be constant or variable to cover the whole area V(I). When one is the generator mode , the other one is the brake mode. The maximum possible power in generator mode (7200 W) is more than the maximum foreseen power in brake mode (3600W). Then, to test simultaneously the full possibilities of the both converters, a 10 mΩ resistor (6 V – 600 A) is connected between the two converters; it assures for each one a suitable working range in accordance with the useful area defined in Figure 4.

6. Conclusion

Six converters [±600 A,±12 V] were designed and built by CIRTEM according to CERN specification.
The performance requirements of the six converters have been tested and have been achieved under the severe constraint of small volume (19", 6U module).
These converters are and will be used intensively to evaluate the LHC magnet tests. They can be considered as a full-size LHC converter prototype.

7. References

1. http://www.cern.ch and http://wwwlhc01.cern.ch/lhcpub/Welcome.html
2. P. Cussac, Y. Cheron, "A reliable MOS transistor driver intended for a series resonant converter in zero voltage switching mode", EPE Firenze, Italy, 1991.
3. P.Campiche, "Proposal for a Dummy Load Configuration for Testing Converters for Superconducting Magnets", Electrical Power Technology in European Physics Research (EP2'98 forum, Grenoble ,France, Oct.98