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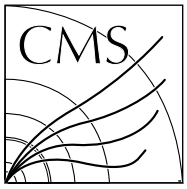

The Compact Muon Solenoid Experiment

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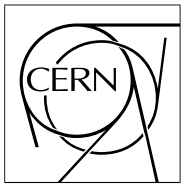

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Radiation hardened transistor characteristics- for applications at LHC and beyond

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Abstract

The high radiation environment at the LHC will require the use of radiation hardened microelectronics for the readout of inner detectors. Two such technologies are a Harris bulk CMOS process and the DMILL mixed technology process. Transistors have been fabricated in both of these and have been tested before and after irradiation to 10 Mrads, the total dose expected in the innermost silicon microstrip layers. Several processing runs of Harris transistors have been carried out and samples from one have also been irradiated to 100 Mrads. A preamplifier-shaper circuit, to be used for readout of the CMS microstrip tracker, has been tested and the noise performance is compared with individual transistors.

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1. Introduction

Future high energy physics experiments at the CERN Large Hadron Collider will operate at far higher energies and luminosities than at present. These challenging conditions necessarily lead to high particle fluences in the detectors. Simulations show that in the inner tracking regions (~20 cm from the beam pipe) these particles will generate approximately 10 Mrads of ionizing radiation dose and 10^{14} neutrons/cm^2 over the 10 year lifetime of the experiment [1,2]. Normal CMOS microelectronics processes do not tolerate doses of more than a few krads, and radiation-hardened technologies, hitherto unused for high energy physics applications, are required to construct many of the critical front end readout circuits to instrument particle detectors.

One of the few radiation hardened microelectronics processes available for ASIC construction via foundry access is the Harris [3] AVLSIRA 1.2 μm bulk CMOS process. It is a digital CMOS process adapted for analogue use by the addition of metal-dielectric layers to provide accurate capacitors. PMOS and NMOS transistors of various dimensions, laid out in the low noise finger structure [4] appropriate for the input device of a front end amplifier for silicon microstrips or microstrip gas chambers (MSGCs), have been constructed in four separate processing runs. The first three runs were carried out at Harris's Research Triangle Park (RTP) plant in North Carolina and the most recent at Harris's Melbourne, Florida foundry, where all future circuits will be fabricated.

Another accessible radiation hardened process is the DMILL mixed technology process, developed primarily for high energy physics applications by a French academic / industrial consortium [5] and which includes CMOS, bipolar and JFET structures, with an SOI substrate to reduce transient irradiation effects. This technology is currently in the stage of industrial transfer and stabilisation after acquisition by Matra MHS [6]. Transistors laid out in a similar way to those in the Harris process were designed by CEA Saclay and constructed in the DMILL Hadron run. The Hadron run was processed in November 1994, close to the end of the research phase of the project, although further optimisation has since been carried out.

As part of extensive characterisation of the transistors, measurements have been made of transconductance (g_m), threshold voltage (V_T) and noise voltage spectral density (e_n) of many transistors from each processing run. Measurements have been repeated on at least three devices from each run after several irradiation doses up to 10 Mrads, and then up to 100 Mrad with one Harris run. Various PMOS and NMOS transistors of different dimensions were measured, but results presented here will focus on the 2000 μm × 1.4 μm PMOS transistor, identical to that used for the input device to the APV3 [7], the APV5 [8] and a preamplifier-shaper test structure which was included on each Harris run. The APV3 and APV5 were prototypes of a complete front end readout chip including amplifier, pipeline memory and analogue signal processing, which is to be employed for readout of microstrip detectors in the CMS experiment [1]. The preamplifier-shaper test structure has also been measured to compare noise performance with that estimated from measurements of individual transistors. These measurements give crucial information about noise performance, which can be compared with results obtained from the APV chip which does further signal processing after amplification.

2. Transfer characteristics

Measurements of the transconductance (g_m) of the devices before and after irradiation allow evaluation of the hardness of the process, while the uniformity between runs provides valuable information about stability. The magnitude of threshold voltage variations are also an indicator of the hardness of the process and are important to digital functionality as well as analogue performance.

2.1 Measurement procedure

The transfer characteristics of the devices were measured using apparatus built at Imperial College. The resolution of the apparatus (described in [9,10]) is approximately 1% in drain current, I_{DS}. The devices were measured under the biases shown in table 1, which reflect the conditions expected in the experiment, discussed further in section 5.

	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
PMOS	-1	-0.7 → -4	0, +2
NMOS	+1	+0.7 → +4	0, -2

Table 1. Bias conditions for channel transconductance measurements

2.2 Irradiation conditions

The transistors were irradiated using a ^{60}Co source under the biases shown in table 2. The irradiation source consists of six separate rods inside a large concrete cell. Due to mechanical problems, not all of the rods have been available throughout the series of measurements, therefore the dose rate has varied between 300 krad/hr and 50 krad/hr. These dose rates are approximately a factor of 10^3 higher than predicted for the innermost silicon microstrip layers at the LHC [2].

	V_{DS}/V	V_{BS}/V	I_{DS}/µA
PMOS	-1	2	500
NMOS	1	0	500

Table 2. Bias conditions during irradiation.

Between irradiations, the devices were left unbiased (pins shorted) at room temperature for varying times of up to several weeks, so some annealing occurred between measurements.

2.3 Transconductance measurements

To compare devices of different dimensions, transconductance is commonly plotted as g_m/I_{DS} vs I_{DS}/W, thus removing the width dependence [10,11]. Length dependence is not corrected for to allow comparisons between devices which were constructed at close to the minimum length.

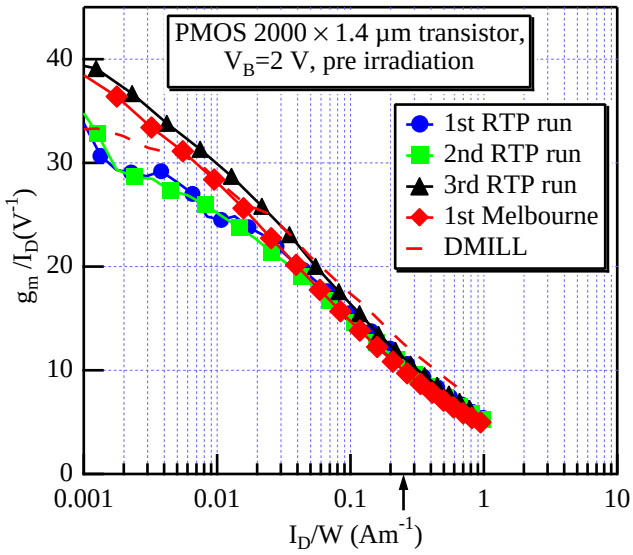

Figure 1. Transconductance of 2000 µm × 1.4 µm PMOS devices, prior to irradiation.

Fig. 1 shows the scaled transconductance of a typical 2000 µm × 1.4 µm PMOS transistors from each of the processing runs. For 500 µA drain current, the region of interest is around $I_{DS}/W = 0.25Am^{-1}$. At this value, the transconductance is stable to within 10% across Harris processing runs. The DMILL transconductance can be seen to be 20% higher.

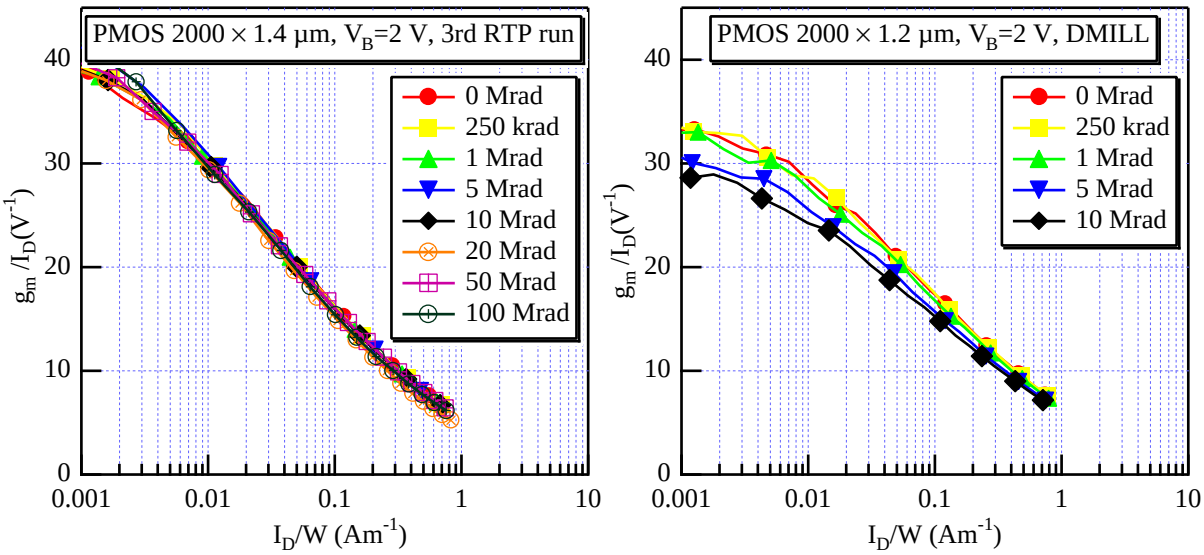

Figure 2. Scaled transconductance of a typical transistor from (a) the 3rd Harris RTP run after irradiation to 100 Mrads. (b) DMILL after irradiation to 10 Mrads.

Fig. 2 (a) shows the scaled transconductance of a typical device from the third RTP run after irradiation. In the region of interest, the changes in transconductance after the maximum dose of 100 Mrads are well below 10%, demonstrating the hardness of the process. Fig. 2 (b) shows a similar plot for a typical DMILL transistors, also decreasing by at most 10% after irradiation at $I_{DS}/W = 0.25Am^{-1}$.

2.4 Threshold voltage measurements

The threshold voltage of the transistors was calculated after each irradiation step using data taken at $V_{BS} = 0$ V [11]. Both PMOS and NMOS devices were monitored since the threshold voltage is critical to digital circuitry. The threshold voltage shifts up to 10 Mrads for the 2000 µm × 1.4 µm PMOS and 2000 µm × 1.2 µm NMOS transistors are shown in fig. 3 (a). The first RTP run is shown for the Harris process since many readings were taken at low doses for this run. The shifts exhibited by this run are typical for all Harris runs.

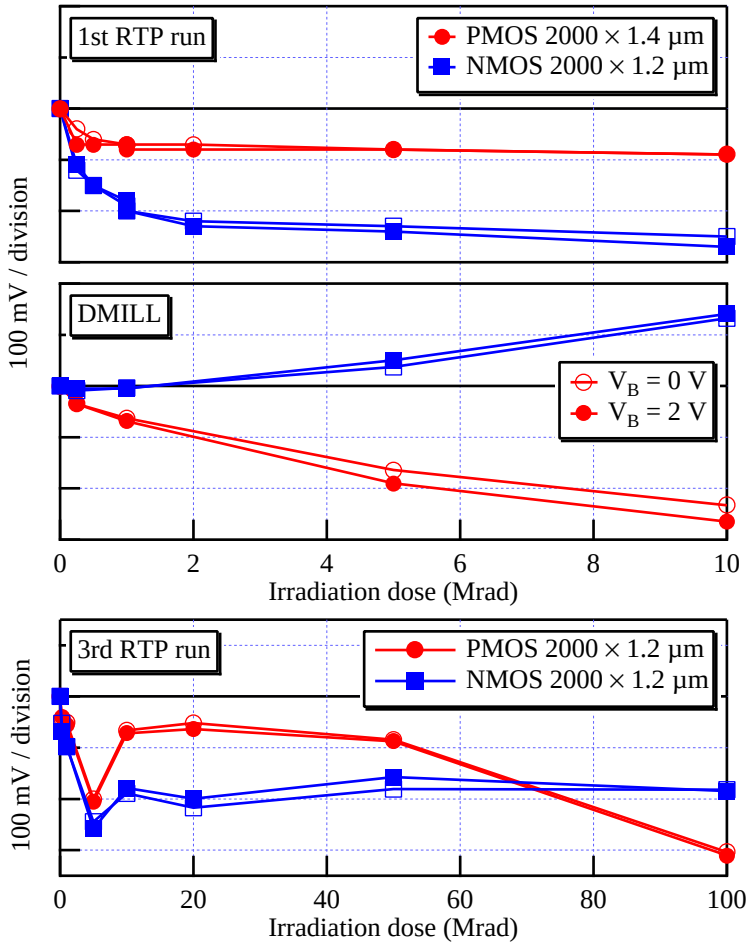

Figure 3. Threshold voltage shifts of 2000 µm × 1.4 µm PMOS and NMOS devices
(a) from the Harris and DMILL processes up to 10 Mrad. (b) from the 3rd Harris RTP run up to 100 Mrad.

Approximately 2/3 of the overall threshold voltage shifts in the Harris process occurs within the first 2 Mrads. The shifts were found to be independent of transistor dimension. The threshold voltages of the DMILL process appear to shift steadily throughout the irradiations. It was found that the shifts were less for transistors with a smaller area (500 µm × 1.2 µm) [10]. The overall shift is similar to that seen in the Harris transistors.

Fig. 3 (b) shows the change in threshold voltage of transistors from the third RTP run after 100 Mrad. The largest changes occur before 5 Mrad followed by continued recovery in the NMOS devices, and initial recovery followed by a final shift of 300 mV after 100 Mrads for the PMOS devices. The precise threshold voltage shifts are dependent on annealing conditions, which were not constant (section 5) therefore the shifts do not provide an exact comparison between the two processes, but an indication of their hardness.

3. Noise spectral density measurements

The noise spectral density of the transistors was measured from 10^4 Hz to 10^7 Hz using an HP4195A spectrum analyser and a custom built biasing device which has been described in [9]. The measurements were made under

the same bias conditions as irradiations (table 2), except for the first RTP run which was measured at I_{DS} = 300 µA, resulting in approximately 12% higher noise than at 500 µA. The bulk voltage for the DMILL transistors was applied to the top substrate, whilst the global substrate was grounded.

The noise spectral density of a typical PMOS transistors from each run is shown in fig. 4. The region of interest is around 3 MHz, the central frequency for 50 ns CR-RC shaping used in the APV chips. The noise spectral density of the Harris transistors has decreased at all measured frequencies with each processing run. This is believed to be due to improved process control at the foundry.

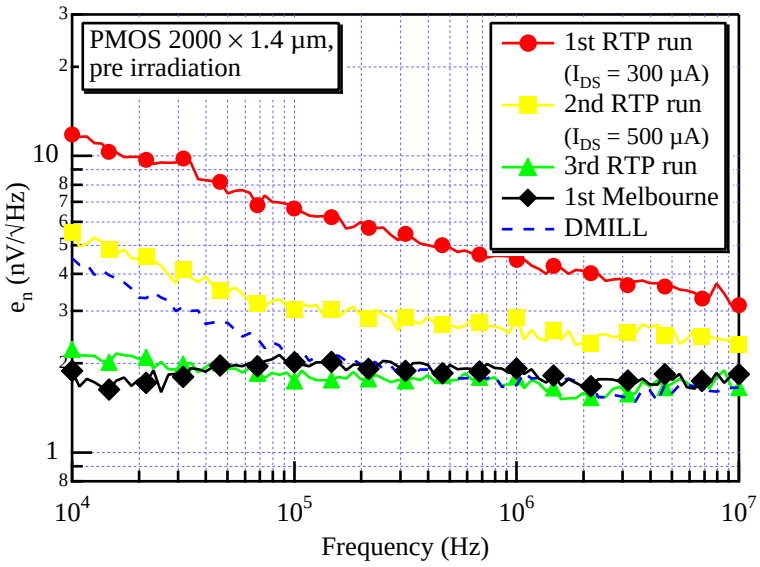

Figure 4. Noise spectral density of 2000 µm × 1.4 µm PMOS devices.

Fig. 5 (a) shows the noise spectral density of a typical transistor from the third RTP run after irradiation up to 100 Mrads. The noise in the thermal region increases by 0.5 nV/√Hz (30%) after 100 Mrads and 1/f noise becomes apparent at lower frequencies. After irradiation to 10 Mrads, the noise spectral density of DMILL 2000 µm × 1.2 µm PMOS transistors has been shown to similarly increase by approximately 50% at all frequencies (fig 5 (b)).

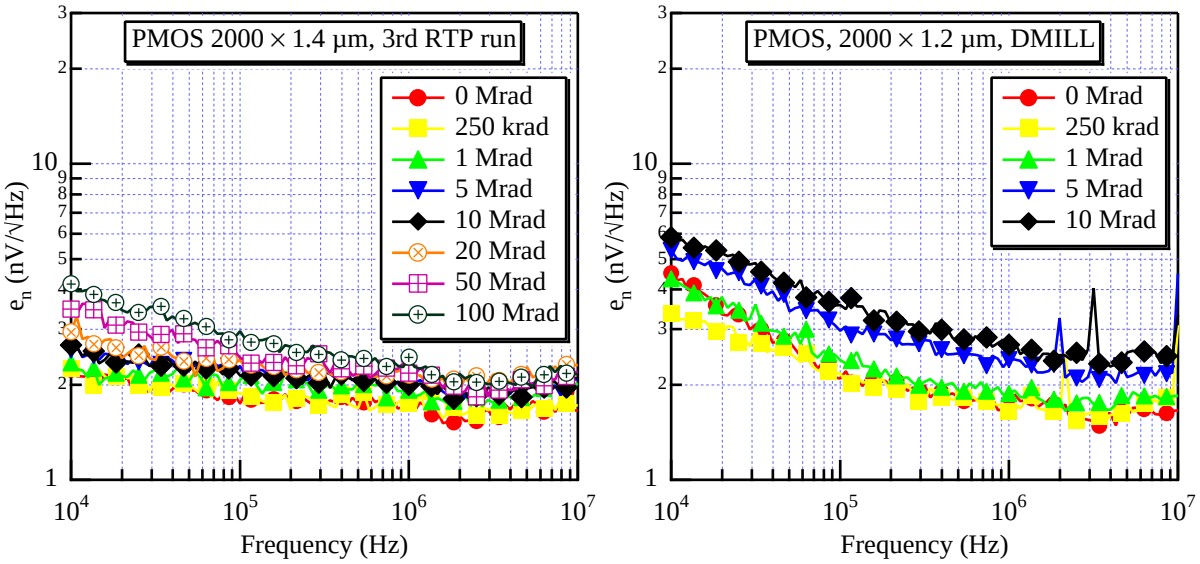

Figure 5. Post irradiation noise spectral density of a typical transistor from (a) the 3rd RTP run after 100 Mrad (b) the DMILL process after 10 Mrad.

3.1 1/f noise coefficients

In non-radiation hardened processes it is expected that at low frequencies the noise spectral density will vary approximately as 1/f (the exact corner frequency is process and dimension dependent). However, these two hardened processes seem to exhibit noise which is a function of $1/f^{\alpha}$, where α is closer to 0.3. Where 1/f noise

is seen, the coefficient α has been calculated from 10^4 Hz to the corner frequency (Table 3). For the application in CMS, the 1/f noise component of the noise makes little contribution, both before and after irradiation.

Processing run	Pre irradiation α	Post irradiation α
1st RTP	0.34	0.31
2nd RTP	0.28	0.28
3rd RTP	N/A	0.36
1st Melbourne	N/A	N/A
DMILL	0.73	0.43

Table 3. 1/f noise slope of 2000 μm × 1.4 μm PMOS transistors before and after irradiation. N/A indicates no 1/f noise measured in this frequency range.

3.2 Thermal noise coefficients

Equation 1 shows how the noise spectral density (e_n) in the thermal region is related to the transconductance (g_m) in terms of frequency (f), absolute temperature (T), Boltzmann's constant (k) and the channel thermal noise coefficient (γ), which is process dependent and has a theoretical minimum of 2/3 in the strong inversion region [11].

$$e_n^2 = \frac{4kT\gamma\Delta f}{g_m} \qquad (1)$$

The coefficient γ has been calculated for all runs except the first RTP run where no thermal noise plateau was apparent, and is shown in fig. 6. Little variation in γ is seen between each run prior to irradiation. After irradiation γ is always seen to increase. The thermal noise of the DMILL and most recent Harris processing runs are all close to the theoretical minimum of γ = 2/3.

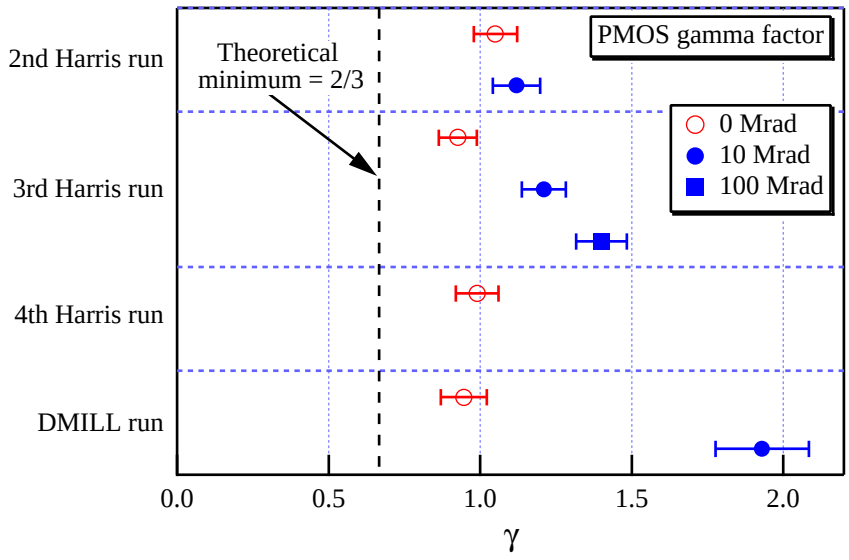

Figure 6. Noise coefficient, γ, of PMOS transistors, before and after irradiation. The dotted line indicates the theoretical minimum value of 2/3.

A graph of g_m against noise spectral density in the thermal region (3 MHz) is shown for a 2000 μm × 1.4 μm PMOS transistor from the third RTP processing run in fig. 7 (a). The open circles show measurements of g_m and e_n on an unirradiated transistor, varying I_D to alter g_m. The solid line shows the theoretical curve (equation 1) for γ = 0.93 (the best fit). The closed circles show the data for another transistor after irradiation up to 100 Mrad. It can be seen that the excess noise seen after irradiation is not due to a reduction in g_m, but to some other mechanism. Fig. 7 (b) shows the same plot for the DMILL transistors. Up to 1 Mrad, the data fit the experimental curve for γ = 1.18, but after 5 Mrad the noise is seen to increase, as with the Harris process.

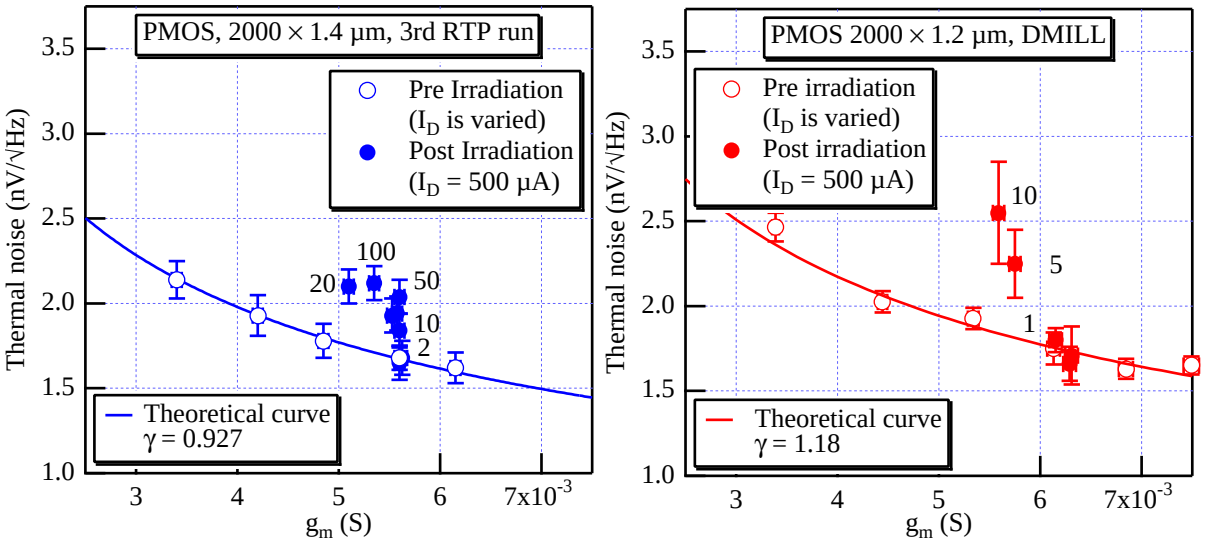

Figure 7. Noise spectral density at 3 MHz as a function of transconductance for Harris and DMILL transistors, before and after irradiation. Numbers indicate post irradiation level in Mrad.

4. Amplifier test structures

Test structures containing preamplifier-shapers identical to those in the APV3 and APV5 have been constructed in the Harris process. The noise of these circuits has been measured using the apparatus described in [9]. It was known that the shaper, which ideally should contribute no noise, did contribute. This can be calculated and subtracted by measuring the noise of the circuit with the preamplifier turned off. In the latest version of the chip, the APV6, the preamplifier and shaper have been redesigned with increased gain to eliminate this excess noise [12].

The expected noise, assuming ideal CR-RC shaping with a bandwidth above the 1/f region, may be expressed in terms of external input capacitance (C_E), capacitance of the transistor (C_T), series noise spectral density of the input transistor (e_n) and shaping time of the amplifier, τ, as described in equation 2 (e=2.718). The parallel noise is assumed to be negligible.

$$ENC^2 = \frac{e^2 C^2}{2}\frac{e_n^2}{4\tau} = \frac{e^2 (C_T + C_E)^2}{2}\frac{4kT\gamma}{g_m}\frac{1}{4\tau} \qquad (2)$$

$$ENC = \frac{e}{\sqrt{2}}\sqrt{\frac{4kT\gamma}{g_m}}\frac{1}{2\sqrt{\tau}}(C_T + C_E) \qquad (3)$$

It can be seen that this can be split into two components, one linearly dependent on C_E (the noise slope) and a constant (the noise intercept). These can be calculated by measuring the noise of the preamplifier-shaper for various values of C_E. The capacitance of the transistor must be added to other internal capacitances, estimated in table 4.

Contributor	Capacitance (pF)
2000 µm × 1.4 µm transistor	3.9 ± 1%
Feedback capacitor of preamplifier	0.6 ± 1%
Protection diode	0.5 ± 50%
Bond wire	0.5 ± 50%
Other (bond pad, feedback resistor)	0.5 ± 100%
Total	6 ± 0.6

Table 4. Fixed capacitance of preamplifier-shaper test structures.

The results of these measurements for 50 ns CR-RC shaping are shown in fig. 8. The measured noise of (350 ± 40 e^- + 37 ± 3 e^-/pF) matches the expected noise slope of 40 ± 2 e^-/pF as predicted by equation 3, but the intercept is larger than the predicted value of 240 ± 24 e^-.

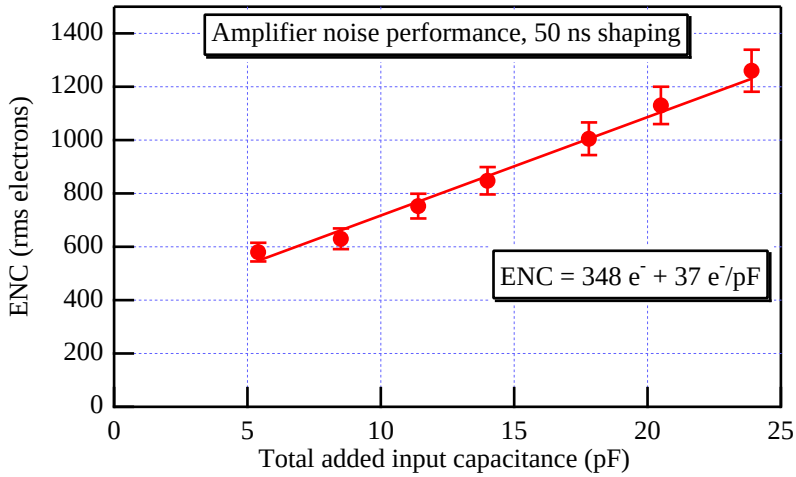

Figure 8. Noise of preamplifier-shaper as a function of external capacitances.

The noise of the preamplifier-shaper has also been measured at other shaping times. This was achieved by adjusting the input bias currents to alter the rise and fall time of the amplifier, whilst retaining correct CR-RC shaping. The noise slope matches well the predictions made in equation 3 (fig. 9), whilst the intercept is slightly higher than predicted (fig. 10).

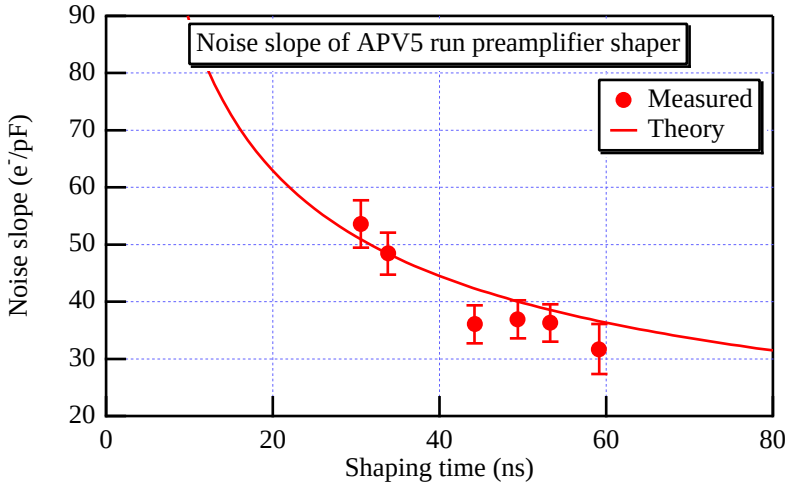

Figure 9. Theoretical and measured noise slope of preamplifier-shaper.

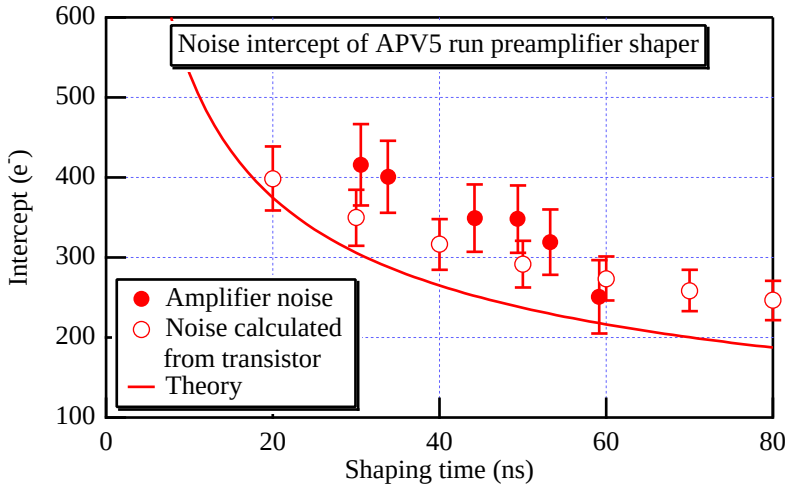

Figure 10. Theoretical and measured noise intercept of preamplifier-shaper. Noise calculated from individual transistors is also shown.

The measured noise spectral density of a discrete transistor identical to the input transistor (PMOS 2000 µm × 1.4 µm) has been integrated over the appropriate bandwidth and this noise, added to the noise due to the other capacitances (table 4) is also shown in fig. 10. It can be seen that the transistor noise is higher than the

theoretical noise at long shaping times. This is associated with the 1/f noise. At these long shaping times, the measured noise of the transistors is in agreement with the measured noise of the preamplifier-shapers.

5. Comments on measurement conditions

The bias conditions under which the devices were irradiated and measured were chosen to match those under which devices will be operated in CMS [1]. The power rails for the inner tracker are ± 2 V, therefore a transistor could never have more than 4 V across it, and the measurements were restricted to this range (section 2.1).

Since the CMS experiment will contain 10^7 channels of electronics in a small volume, it is imperative to minimise the power consumption. To achieve low noise in the circuit, the input transistor must have the highest gain possible, and the operating current is a compromise between low noise and low power. The maximum current has been set at 500 μA, and this was the level at which the transistors were irradiated and noise was measured (section 2.2).

The devices have all been measured and irradiated at room temperature. In CMS it is expected that the ambient temperature will be approximately 0°C. Irradiation at lower temperatures is expected to worsen the damage because the defects do not anneal as well [13].

The devices were irradiated at far higher dose rates than those possible at the LHC, and the devices were not all irradiated at the same dose rate (section 2.2). The time between irradiations varied from one day to over a week, giving less annealing than will be seen at the LHC.

These studies were undertaken to provide an indication of the radiation hardness of the processes and for the stated reasons are not a characterisation of the process under every set of conditions, nor even an exact indication of the levels of change that will be seen in CMS. They do however indicate that both the Harris and DMILL processes are suitable for use at the LHC. In addition every chip has been simulated with the manufacturers best and worst case SPICE parameters to verify operation in all situations.

Conclusions

To investigate the radiation hardness of transistors from the Harris and DMILL processes, measurements have been made of transconductance, threshold voltage and noise spectral density. Measurements have been repeated after 10 Mrads of ionizing radiation.

The transconductance of the Harris transistors has been shown to be stable to within 10% after 100 Mrads of irradiation, while the DMILL transistors reduce in transconductance by less than 15% after 10 Mrads.

After 10 Mrads the threshold voltage of the Harris PMOS transistors increased in magnitude (became more negative) by 100 mV, whilst the NMOS transistors reduced by 250 mV. The DMILL PMOS transistors increased in magnitude by 350 mV and the NMOS increased by 150 mV.

The thermal noise of the Harris and DMILL transistors is very similar prior to irradiation., with the Harris noise increasing by 25% after 100 Mrads and the DMILL noise increasing by 50% after 10 Mrads.

The noise of the APV preamplifier-shaper has been measured. The noise slope of the preamplifier has been found to behave as predicted, and compares well with the measurements of individual transistors.

These measurements all indicate that both the Harris and DMILL processes are suitable for use at the LHC and will be of sufficiently low noise to be used for front end microstrip readout.

Acknowledgements

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