# Measurements of radiation hardened transistors from Harris and DMILL technologies

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**Abstract**

All experiments at the LHC will require front end electronics capable of reading small signals at high speed from silicon microstrips and other types of detector, in a harsh radiation environment. The electronics adopted by the CMS collaboration for the microstrip tracking system is based on the APV CMOS front end readout chip. One possible radiation hardened technology under consideration for this chip is the Harris 1.2 μm AVLSIRA bulk CMOS process. Results are presented of measurements of transistors from this process from several processing runs, monitoring the stability of the process and testing its radiation hardness and suitability. Measurements have also been made to verify the radiation hardness of other structures in the process, in particular resistors and capacitors.

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## 1. INTRODUCTION

It is well known that experiments at the LHC will be subject to high radiation doses. For the CMS detector, simulations show radiation levels in the inner tracking regions of 10 Mrads of ionizing radiation and $10^{14}$ hadrons/cm$^2$ over the 10 year lifetime of the experiment [1,2]. Standard microelectronics processes are incapable of withstanding these doses, therefore radiation hardened processes must be used. The two main processes that have been made available to the European high energy physics community are the Harris 1.2 μm AVLSIRA bulk CMOS process [3] and the DMILL mixed technology process which includes CMOS, NPN and JFET structures[4].

Test structures have been constructed in three processing runs of the Harris process and one in DMILL, each consisting of CMOS transistors suitable for use as input transistors for a preamplifier-shaper circuit for front end readout of silicon microstrip detectors or MSGC's. All devices have been measured before and after gamma irradiation to at least 10 Mrads. The most recent Harris run also included test resistors and capacitors, and devices have been irradiated up to 100 Mrads.

At the outset of these studies, very little was known about the analogue performance of radiation hardened CMOS transistors, in particular of the AVLSIRA process which was originally developed for digital applications. Investigations concentrated on PMOS devices since in radiation hardened processes they have lower noise and greater radiation hardness. Measurements were made of the behaviour of transconductance, threshold voltage and noise spectral density after irradiation.

A complete prototype radiation hardened front-end readout chip for use with silicon microstrips was the APV5, designed in the Harris process. It has previously been tested in the lab [5] and in a beam [6] and now has been tested after irradiation to 16 Mrads.

## 2. TRANSISTOR IRRADIATIONS

The devices have been irradiated, whilst biased with 500 μA drain current, in a $^{60}$Co source. Between irradiations the devices remained unbiased, giving similar conditions to LHC where the detector system will be unpowered for half of the year. Due to external circumstances the available dose rate from the $^{60}$Co source changed over a period of time, from between 300 krad/hr for the first Harris transistors to 50 krad/hr for the DMILL transistors. The transistors received doses of 250 krad, 1 Mrad, 5 Mrad and 10 Mrad for all except the second Harris processing run which received 15 Mrad only. Devices from the third Harris processing run were irradiated further to 20 Mrad, 50 Mrad and 100 Mrad.

The time between irradiation varied by several days, allowing variable amounts of annealing to take place. These results do not therefore represent an exact comparison between transistors but are an indicator of the ability of the devices to withstand irradiation in an LHC environment. At present it is not clear that other measurement protocols developed for military or space

applications are applicable to the LHC conditions e.g. in terms of temperature range, LHC operating cycles and annealing conditions.

## 3. TRANSISTOR MEASUREMENTS

Measurements have been made of transconductance, threshold voltage and noise spectral density of the transistors using equipment described in [7,8].

Up to eighteen transistors of varying size were measured from three die from each processing run. Results are shown of a typical example of the shortest device, of size 2000 × 1.4 µm for the Harris PMOS transistors and 2000 × 1.2 µm for DMILL and Harris NMOS transistors.

### *3.1 Transconductance Measurements*

The data from the transconductance measurements are plotted as current scaled transconductance against current density ($g_m/I_D$ vs $I_D/W$) as described in [7] to remove width dependence from the plots, thus allowing comparison between devices of different dimensions. No corrections for length dependence was made since the devices were constructed with minimum length, giving a uncertainty of up to 50% in the effective length.

#### *3.1.1 Pre-irradiation measurements*

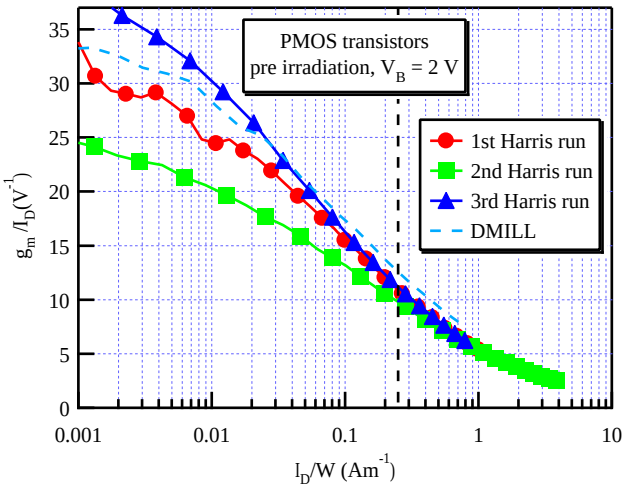


Fig. 1. PMOS scaled transconductance prior to irradiation. Line shows $I_D$ = 500 µA.

Plots of $g_m/I_D$ against $I_D/W$ for the transistors, prior to irradiation are shown in figs. 1 and 2. The dotted line indicates 500 µA, the current of interest for the preamplifier-shaper of the APV5. All Harris transistors had similar transconductance at this current, indicating the stability of the process. The DMILL transistors had very similar properties to the Harris transistors.

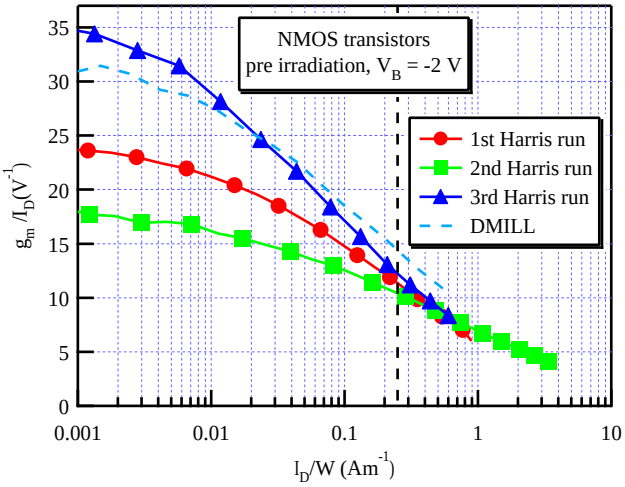


Fig. 2. NMOS scaled transconductance prior to irradiation. Line shows $I_D$ = 500 µA.

#### *3.1.2 Post irradiation measurements*

Fig. 3 shows the scaled transconductance of the PMOS transistors after irradiation changing by less than 1% in the Harris process and up to 15% after 10 Mrads in the DMILL process .

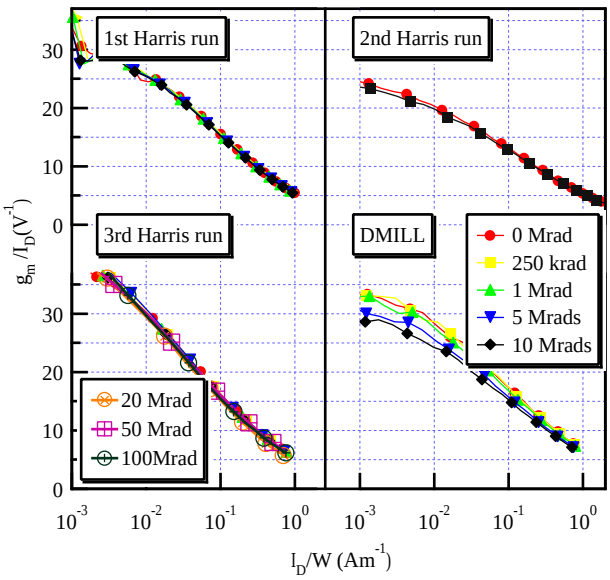


Fig.3 Scaled transconductance of PMOS transistors after irradiation ($V_B$ = 2V).

Fig. 4 shows that the NMOS devices transconductance reduced very little after irradiation at $I_D$ = 500 µA, but by

larger amounts in the weak inversion region. Whilst the changes appear to be greatest in the third processing run, this saturated after 20 Mrads with transconductance still above that of the other two processing runs.

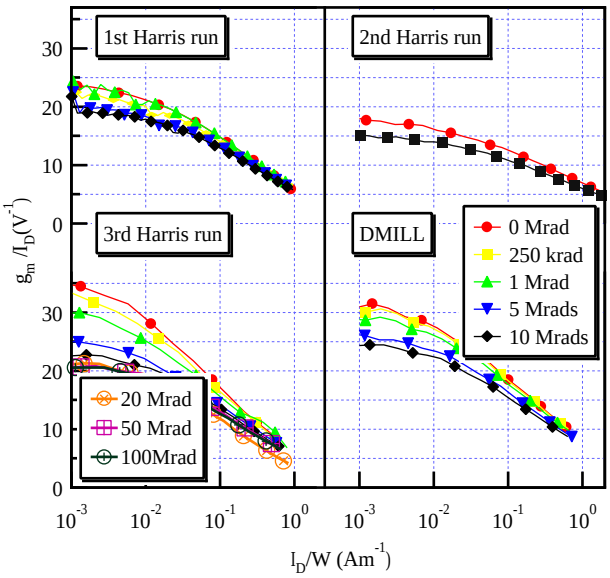


Fig. 4. Scaled transconductance of NMOS transistors after irradiation ($V_B$ = -2V).

## *3.2 Threshold Voltage Shifts*

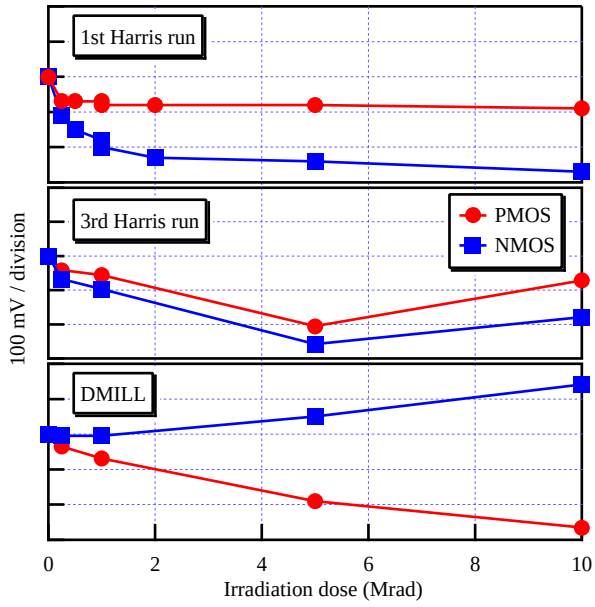


Fig. 5. Threshold voltage shifts ($V_B$ = ±2 V)

The threshold voltages of the transistors were calculated from the data which were used to calculate the transconductance. Fig. 5 shows the threshold voltage shifts of the transistors after irradiation up to 10 Mrads. The threshold voltage shifts of all of the devices is within 300 mV. Further irradiation up to 100 Mrad for the third Harris processing run showed little further change.

The threshold voltage shifts of the Harris transistors were found to be independent of dimension, whereas the shifts of the DMILL transistors were dimension dependent [7] with smaller devices (500 × 3.2 µm) having less than 100 mV shift. It is also interesting that the DMILL NMOS transistors have a positive threshold voltage shift, showing the influence of the interface trapped charge which normally only becomes dominant after annealing.

## *3.3 Noise Measurements*

The noise spectral density of the devices has been measured with a drain current of 500 µA, except for the devices from the first Harris processing run which were measured at $I_D$ = 300 µA [7]. The important frequency is 3 MHz which corresponds to the central frequency of a 50 ns CR-RC pulse, the typical shaping time of the preamplifier-shaper circuits being designed for LHC inner tracking detectors.

### *3.3.1 Pre irradiation measurements*

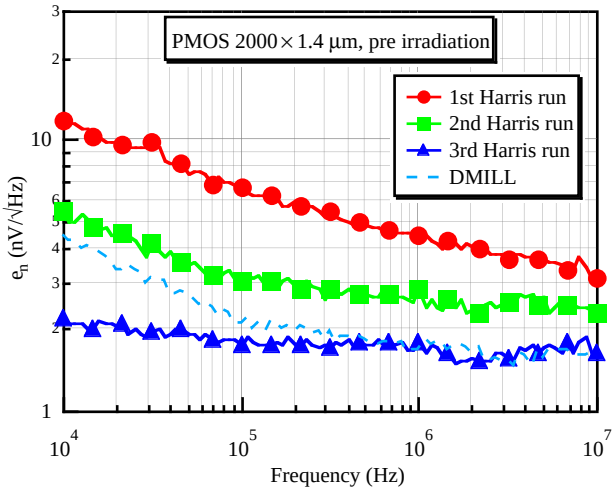


Fig. 6. Noise spectral density of PMOS transistors. $I_D$ = 500 µA (300 µA for first processing run).

Figs. 6 and 7. show that the noise spectral density prior to irradiation of the Harris transistors although consistent between devices from the same batch, has improved in each subsequent processing run. This is believed to be due to improved quality control in the foundry during the three year period over which the fabrications took place,

leading to a reduction in the 1/f noise. The noise in the 3 MHz region of the DMILL transistors and the latest Harris transistors is comparable. The noise of the NMOS transistors is larger than that of the PMOS ones.

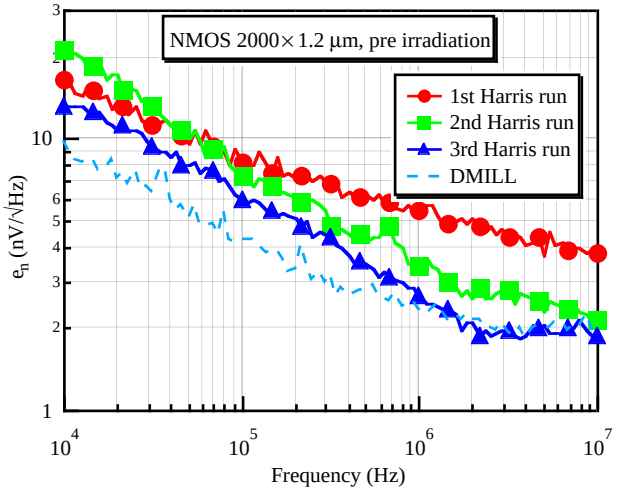


Fig. 7. Noise spectral density of NMOS transistors. $I_D$ = 500 µA (300 µA for first processing run).

### *3.3.2 Post irradiation measurements*

Figs. 8 and 9 shows the noise spectral density of the 2000 × 1.4 µm transistors after irradiation. The noise of the Harris PMOS transistors increased by 5-10% after 10 Mrad, with only a slight further increase in 1/f noise after 100 Mrad. A larger increase was evident in the DMILL PMOS transistors.

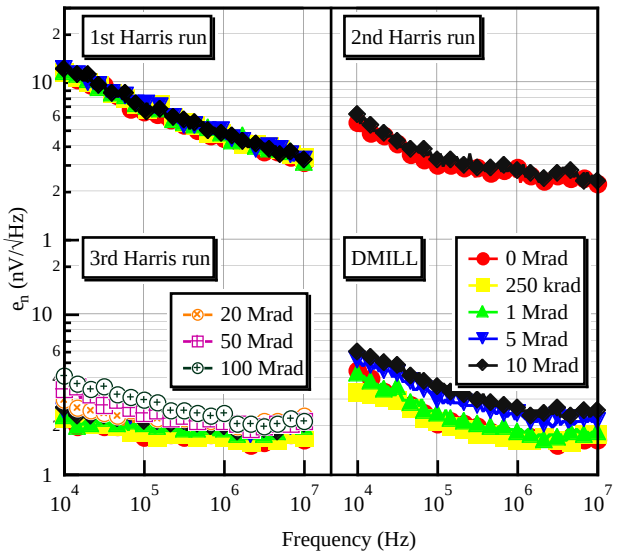


Fig. 8. Noise spectral density of PMOS transistors after irradiation. $I_D$ = 500µA (300µA for first processing run).

Fig. 9 shows an increase of up to 30% in the noise spectral density of the NMOS Harris transistors after 5 Mrads, with little further increase up to 100 Mrads. Again the increase in the noise of the DMILL transistors was larger and showed no sign of saturating after 10 Mrads.

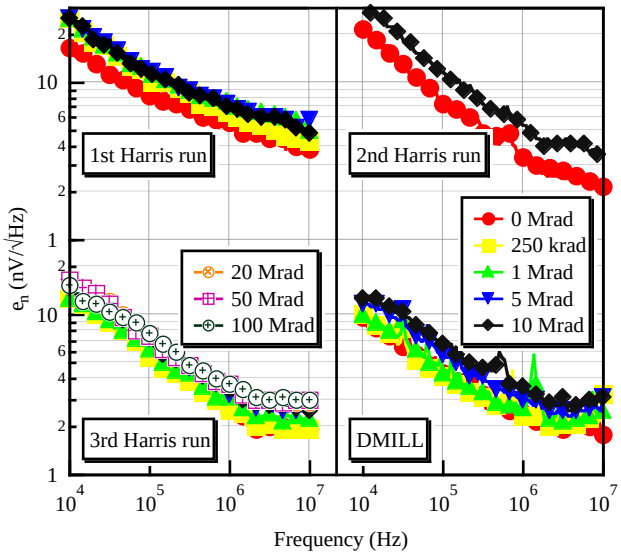


Fig. 9. Noise spectral density of NMOS transistors after irradiation. $I_D$ = 500µA (300µA for first processing run).

## 4. PASSIVE COMPONENTS

Five resistive test structures were included on the third Harris processing run. This included Metal 1, Metal 2 and Polysilicon resistors and Polysilicon / Metal 1 and Metal 1 / Metal 2 via chains of 960 contacts to verify performance. Fig. 10. shows that the structures are unaffected by irradiation.

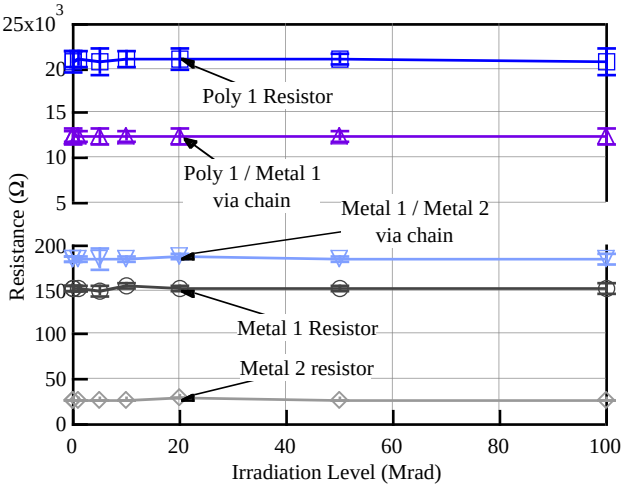


Fig. 10. Resistive structures after irradiation.

Two capacitor arrays, one of 20 1 pF capacitors and one of 500 42.7 fF capacitors were measured at 100 kHz. Negligible changes were seen in their measured values after irradiation.

## 5. APV5 IRRADIATIONS

The APV5 front-end readout chip has been irradiated up to a total dose of 16 Mrad. During irradiation, it was supplied with the nominal biases and clock and trigger signals to fully exercise the chip.

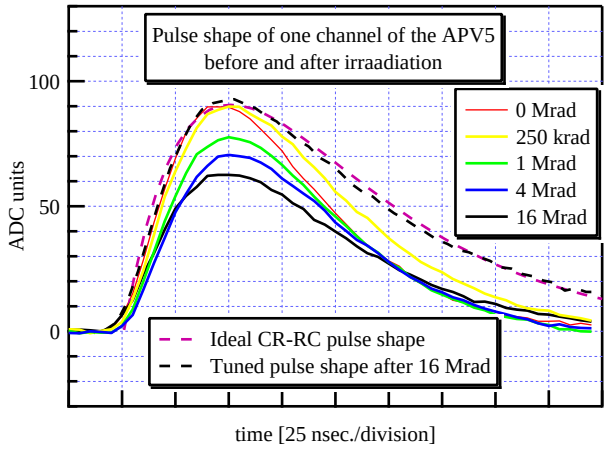


Fig. 11. APV5 pulse shape changes with irradiation.

The pulse shape of the preamplifier-shaper circuit was recorded at nominal bias after irradiation (fig. 11). No direct analogue output existed on the chip therefore the pulse shape was measured in many steps by altering the trigger time with respect to the charge injection time. Since the correct operation of the digital circuitry was required for this, it is evident that it was unaffected by irradiation. The pulse height at nominal bias reduced with irradiation due to the reduction in transconductance of an NMOS transistor in a key position in the circuit, which has been replaced with a PMOS transistor for the next chip, the APV6. Nevertheless after irradiation, by adjusting biases it was possible to achieve the ideal CR-RC pulse shape which is necessary for deconvolution. Within the limits of simple measurements, no increase in equivalent noise charge was evident after irradiation. The chip power consumption after irradiation was identical to the pre-irradiated value from a comparison between two different chips.

## 7. CONCLUSIONS

Harris and DMILL transistors have been tested to 100 Mrads and 10 Mrads respectively. They have been shown to have similar properties and to operate well after these doses, with less change seen in the PMOS transistors than the NMOS ones. Resistors and capacitors in the Harris process are also stable to 100 Mrads.

The APV5 has been irradiated to 16 Mrads. The analogue pulse height reduced with constant bias conditions, but modifications have been made on future chips to remove this effect. The correct pulse shape is always achievable by adjustment of biases. The digital circuitry was not affected by irradiation.

## ACKNOWLEDGEMENTS

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