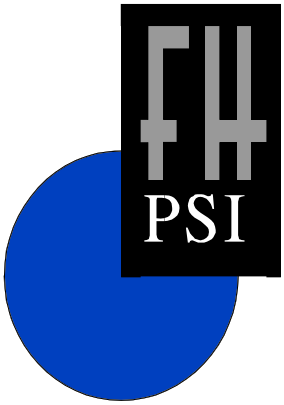

Study for a failsafe trigger generation system for the Large Hadron Collider beam dump kicker magnets

April 1999 Martin Rampl

Eidesstattliche Erklärung

Titel:

Study for a failsafe trigger generation system
for the Large Hadron Colider
beam dump kicker magnets

Diplomarbeit

Eingereicht von Martin Rampl

Vertiefung Mikro- und Feinwerktechnik

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Präzisions-, System- und Informationstechnik

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Datum Unterschrift

Kurzzusammenfassung:

Der 27 km-Teilchenbeschleuniger Large Hadron Collider (LHC) wird nach seiner Fertigstellung am Europäischen Labor für Partikelphysik (CERN) im Jahr 2005 mit noch nie zuvor dagewesenen Strahlenergien arbeiten (~334 MJ pro Strahl). Da die Anlage und vor allem die supraleitenden Magnete vor Beschädigung durch diese hochenergetischen Strahlen geschützt werden müssen, muß der Beam Dump (=Strahlabsorber) jederzeit und in jeder Arbeitsphase in der Lage sein, die gesamte Strahlenergie zu absorbieren. Die Kickermagnete extrahieren die Partikel vom Beschleuniger und werden vom Triggergenerationssystem mit dem Teilchenstrahl synchronisiert.

Diese Diplomarbeit ist eine erste Studie für dieses Elektronikmodul und seine Funktionen. Eine spezielle Synchronisationsschaltung und ein sehr zuverlässiger elektronischer Schalter wurden entwickelt. Die meisten Funktionen wurden in ein Gate-Array implementiert, um die Zuverlässigkeit zu verbessern und Modifikationen während der Testphase zu erleichtern. Diese Studie enthält weiters das komplette Konzept für den Prototypen des Triggergenerationssystems. In allen Projektphasen war Zuverlässigkeit immer der Hauptbestimmungsfaktor für das gewählte Schaltungsdesign.

Schlagworte: Teilchenbeschleuniger, Synchronisation, Zuverlässigkeit, Gate-Array

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Abstract:

The 27 km-particle accelerator Large Hadron Collider (LHC), which will be completed at the European Laboratory for Particle Physics (CERN) in 2005, will work with extremely high beam energies (~334 MJ per beam). Since the equipment and in particular the superconducting magnets must be protected from damage caused by these high energy beams the beam dump must be able to absorb this energy very reliable at every stage of operation. The kicker magnets that extract the particles from the accelerator are synchronised with the beam by the trigger generation system.

This thesis is a first study for this electronic module and its functions. A special synchronisation circuit and a very reliable electronic switch were developed. Most functions were implemented in a Gate-Array to improve the reliability and to facilitate modifications during the test stage. This study also comprises the complete concept for the prototype of the trigger generation system.

During all project stages reliability was always the main determinant for the chosen circuit design.

Keywords: Particle accelerator, Synchronisation, Reliability, Gate-Array

To my parents Alfred and Maria,
who made it possible to get such an education.
Thank you !

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A.Introduction

1. Project overview

In the field of electronics the reliability aspect is gaining more and more importance. In particular in critical applications, where faults can cause damage to the equipment and risk for human life, failure rates determine the structure of the electronic design.
The new particle accelerator Large Hadron Collider (LHC) at CERN will deal with beam energies of about 334 MJ for a proton beam [1]. This fact includes a high demand for failsafe operation and functional safety for certain systems.
One of these critical systems is the LHC beam dump, which has to absorb the beam energy as fast as possible in case of an emergency or at the end of a physics run. A fault in this system would cause serious damage to the machine, which would lead to high costs for repair and a long downtime.
This paper is a first study for a part of the control electronics for this system, namely the “Failsafe trigger generation system for the LHC beam dump kicker magnets”. The aim is the construction of a Trigger Generator prototype (one trigger generation system consists of two parallel redundant Trigger Generators) to investigate further appearing problems and the necessary requirements for the final installation. This paper provides the base for the design of the circuit schematics and the PC-board. Further it contains the complete programming for the used Gate-Array-chip.
The main task of this device, along with a lot of additional functions, is the synchronisation of the beam dumping action with the circulating proton beams.
During the entire design process great attention was paid to reliability and accuracy properties:

- A combination of redundancy and continuous surveillance was used to reach the required low overall failure rate of $1/10^6$ hours, which equals to one fault per 114 years.
- A special digital synchronisation algorithm was developed to maintain the precise timing requirements.

The following chapters will give an introduction into the project, explain the detailed structure, provide the mathematical proofs and describe the functions of all subunits included in the Trigger Generator.

2. CERN – The European Laboratory for Particle Physics

The CERN laboratories that are located directly on the Franco-Swiss border west of Geneva provide the world-leading facilities for particle physics.

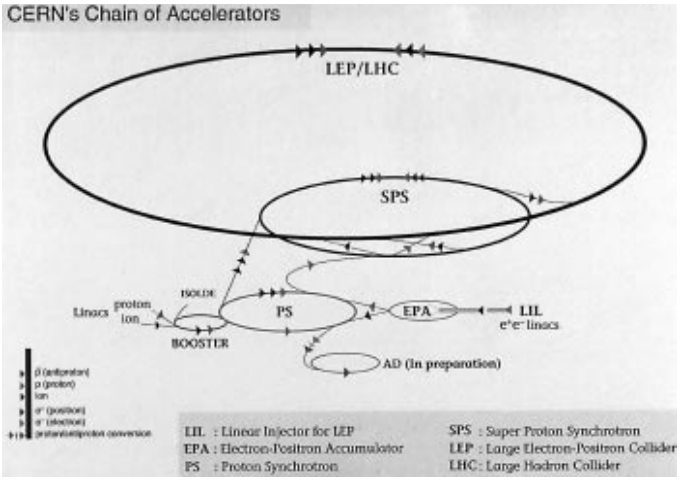

Figure 1: The CERN accelerator chain (CERN Photo)

Since CERN was founded in 1954 several particle accelerators have been built to explore the deeper layers of matter. Particles are accelerated nearly to the speed of light and examined through colliding with fixed targets or with themselves inside of huge particle detectors.

Scientists analyse the data that is obtained there to get further knowledge about the structure of matter.

3. LHC- The Large Hadron Collider

In 2005 the new 27 km-proton accelerator LHC, which will be installed into the existing LEP (Large Electron - Positron Collider)-tunnel, will go into operation (see Figure 2).

Figure 2: LHC tunnel (CERN photo)

At the final stage it will provide proton-proton collisions with an energy of 14 TeV and lead-ion collisions with 1150 TeV [1]. Superconducting radio-frequency cavities accelerate both counter-rotating proton beams within 25 min from 450 GeV to 7000 GeV. Superconducting dipole magnets

steer the particles along the 27 km circumference. The high particle energies require dipole magnet flux densities of at least 8.4 T at maximum energy [1]. Superfluid helium cools the magnets to 1.9 K to maintain the superconductivity of the magnet material (NbTi) [1]. The whole CERN accelerator chain (Figure 1) will be involved into the injection process for LHC.

Scientists expect to get a deeper view into the processes immediately after the Big Bang and in particular to obtain information about the Higgs-Boson, which is assumed to be responsible for the mass of matter.

3.1. LHC beam dump

The beam dumping system has the purpose to extract the proton beam safely from the accelerator at the end of a physics run, when the beam quality becomes insufficient and a refill is necessary (~after 10 h [1]). Also during machine studies and setting-up operations the dump system must always be ready to remove the beam from the collider. Since the LHC works almost only with superconducting magnets and the beam energy is 334 MJ per ring [1], the proton beams must be extracted as fast as possible in case of an emergency or if a serious system malfunction occurs.

If the beam strikes the beam pipe within the superconducting magnets the lost energy is dissipated in the magnet which will quench due to the increasing temperature. Magnet quenching means that the superconducting property is lost by exceeding the critical temperature of the superconductor and the material gets immediately into normal resistive operation. As a result the magnetic field strength is modified which will bring the beam in dangerous oscillations.

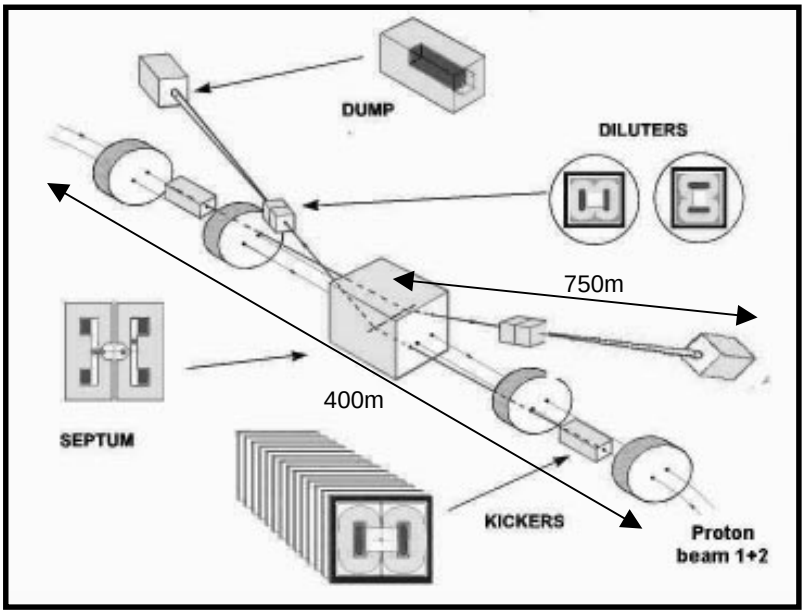

Figure 3: LHC beam dump

Therefore the beam dump systems must always work

correctly and never be the origin of such an event.

Figure 3 shows the LHC beam dump insertion, which will be installed at IP6 (so-called insertion point within Octant 6 of the LHC tunnel). Both counter-rotating beams have their own and independent beam dumping system. Since both installations are completely identical only one system will be treated in the following parts of this paper.

A beam dump system consists of the septum magnets, the kicker magnets, the diluter magnets, the transfer tunnel and the dump block. In case of a dump request the kicker magnets kick the circulating beam into the iron septum magnet, which deflects it vertically. The following diluters distribute the particles horizontally and vertically over the surface of the dump block to avoid damage caused by too high energy concentrations during the absorption process. The dump block measures 14 m x 3 m x 3 m (l x w x h) and consists of a graphite core surrounded by iron and aluminium [1]. Both blocks for the two counter-rotating beams will be installed at the end of two 750 m long, tangentially emerging transfer tunnels. All beam dump magnets are normal conducting, so-called warm magnets. Table 1 shows the main parameters of the septum, kicker and diluter (horizontal and vertical) magnets.

	Septum	Kicker	Diluter hor.	Diluter vert.
Nom. Field (T)	1.00	0.51	1.20	1.20
Overall length (m)	70	25	8	10
Nr. of modules	25	14	4	5

Table 1: Main parameters of the beam dump magnets [1]

3.2. The kicker magnets and their control

As mentioned above the kicker magnets have to extract on request the proton beam from the collider. This action must be synchronised with the 3.17 µs particle–free gap of the circulating LHC beam. One beam revolution cycle lasts 88.924 µs that equals to the travelling time the particles need, nearly at the speed of light, for one turn around the 26659 m circumference [1].

The beam itself consists of 2835 bunches of 10^{11} protons each separated by 25 ns. The gap in the beam is obtained by eliminating 127 bunches in the last batch transfer from the SPS (Super Proton Synchrotron) to the LHC [1]. Fitting the 3 µs rise time of the kicker magnets exactly in the particle free gap avoids damage to the septum by partially deflected bunches. The magnetic field in the kicker magnets must have a

flat-top of at least one turn of the beam (89 µs) to ensure that the whole beam is extracted. Absorbers are installed at both sides of the septum for its protection in case of a bad synchronisation of the beam dumping action or a system fault.

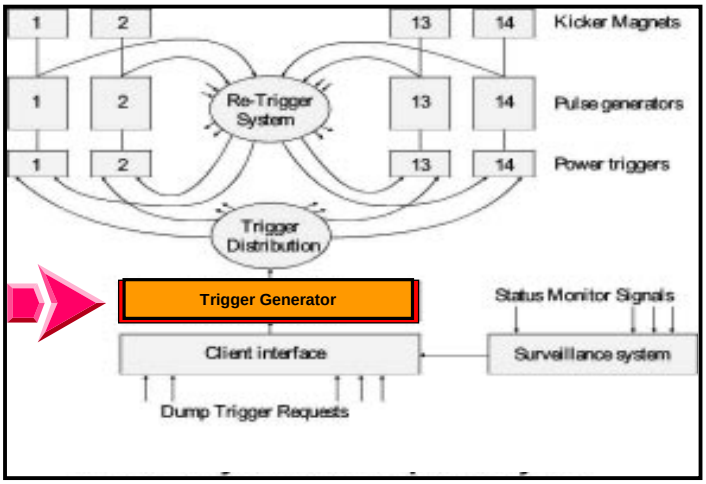

Figure 4: Functional layout of the dump-kicker system

Figure 4 shows that each of the 14 kicker magnets has its own Pulse Generator, which gets its trigger signal from a Power Trigger. The dumping action can safely be executed even if only 13 subsystems are working. Each of the 14 kicker magnet controls is further divided into two parallel redundant branches A and B that can fully take over the task of each other [2].

All 14 Power Triggers are triggered by only one trigger generation system, which delivers the synchronised pulse via the Trigger Distribution device. Thus every malfunction of the trigger generation system causes a faulty dumping action and must be avoided. A Surveillance System supervises all important subelements and components and issues a trigger request if the correct functioning of the system is not more maintained. The purpose of the Re-Trigger System is the detection of spontaneously triggering of one of the Pulse Generators and distributing this information, as fast as possible, to the other ones. It prevents damage to the machine by partially deflected beams. Finally the Client Interface collects the dump trigger requests and forwards them to the Trigger Generator [2].

Further details about the LHC beam dump kicker system can be found in the *CERN-report "Design aspects related to the reliability of the LHC beam dump kicker systems"* [2].

All electronic and power systems will be installed in the equipment gallery at IP6, which runs parallel to the LHC tunnel. The shielding between both tunnels protects the electronics from radiation damage.

4. Detailed problem definition

The following chapters contain the detailed project description and the requirements for the Trigger Generator.

4.1. Main requirements for the Trigger Generator

The main task of the Trigger Generator is to respond to a beam dump request exactly at the moment the 3 µs-particle-free gap in the LHC proton beam passes through the kicker magnets. Since this system controls all 14 kicker magnet modules the functionality must always be maintained even if other systems are failing. This fact includes a very low inherent failure rate of the trigger generation system.

4.2. General structure

Figure 5 shows the scheme of the trigger generation system for one beam. It consists of two parallel redundant, completely independent and identical Trigger Generator for branch A and B. Both can take over the function of each other if a serious fault occurs. In this case a dumping action must immediately be triggered by the correct working channel, because further operation without redundancy is risky.

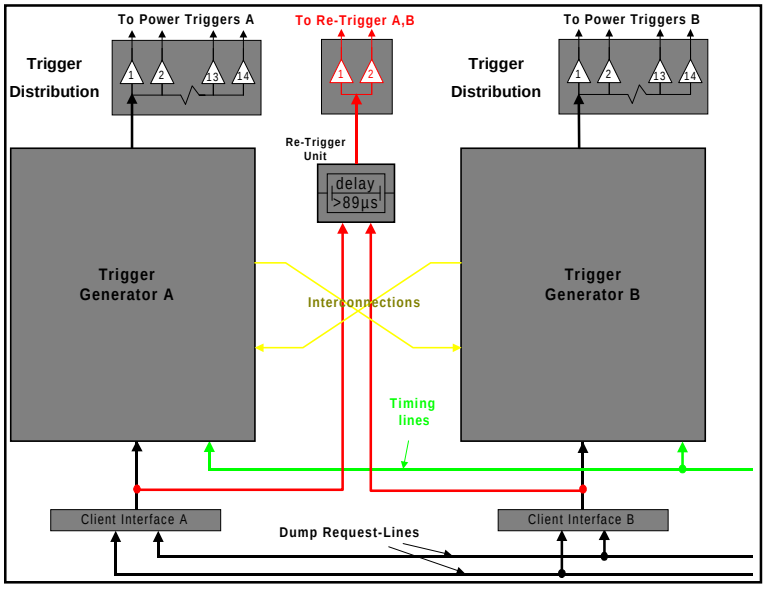

Figure 5: Trigger generation system

Both redundant systems receive their trigger request signals from their own Client Interface and issue the synchronised trigger to their own Trigger Distribution system, i.e. starting with the Client Interface both branches are completely independent.

If both Trigger Generator A and B are faulty at the same time the Re-Trigger system works like a third redundant path by issuing an asynchronous trigger pulse. Since both Trigger Generators are completely identical only one will be described in the further chapters of this paper.

4.3. Input/Output-signals

The main input/output-signals of the Trigger Generator are determined by the surrounding devices and will be described in the following part:

Input signals:

- Timing lines:

  This signal provides the exact revolution frequency of the LHC proton beam, from which the appearance of the particle-free gap at the kicker magnets can exactly be derived by a constant delay. Possible sources for this signal are the Radio-Frequency (RF)-timing and/or beam monitors at the kicker magnets at IP6.

  Since this has not been defined in detail yet, it is assumed that this signal is coincident with the particle free gap and provides the base information about the required dump trigger instant.

- Dump request lines:

  If a dump request command is sent to the Client Interface it issues a signal to the Trigger Generator, which must result in a dumping action at the next possible opportunity [2].

- Interconnections between Trigger Generator A and B:

  A severe fault occurring in one of the Trigger Generators has to result in a dumping action issued by the correctly operating redundant device.

  Fast reaction can only be obtained by continuous mutual surveillance of both circuits. For that reason certain interconnections must be foreseen.

Output signals:

- Trigger output:

  The Trigger output signal must trigger the kicker magnets in the way that the rising edge of the magnetic field, seen by the circulating beam, starts exactly at the beginning of the particle-free gap. Therefore the leading edge of the Trigger output signal must be premature to compensate all following system delays.

4.4. Tolerances and beam-dependent values

Since there is the possibility that the input timing signal fails, an internal oscillator must continue to generate the synchronisation signal for a certain period or number of cycles until the decision is made by the Surveillance System to request a beam

dump. Since this free-running period is not yet defined it was assumed to be 5 beam turns. During these 5 turns an accumulated timing error of +100 ns can be tolerated. It contains the oscillator drift and inaccuracies of other fixed, but unadjusted delay offsets. Adjusted fixed delays do not contribute to this tolerance, but should be as low as possible that the overall propagation delay from the timing input to the trigger output does not exceed 100 ns.

The LHC proton beams are injected at 450 GeV and accelerated within 25 min to 7000 GeV, which means, that the speed or revolution frequency respectively will increase.

Table 2 shows the exact values of this, so-called, acceleration ramp. In particular for the design of the internal oscillator, which has to follow the revolution frequency very precisely, these values are essential (Circumference of the LHC ring is 26659 m [1]).

Calculated values	Beam Energy (GeV)	Particle Velocity (m/s) *)	Revolution frequency **) (Hz)	Revolution time period **) (µs)
Injection	450	299791800	11245.42556	88.92504732
Top Energy	7000	299792450	11245.44994	88.92485451
Difference	6550	650	-24 mHz	~0.2 ns

from equations *) $v = c\sqrt{1 - \frac{m_p^2 c^4}{E_p^2}}$ [3] **) $f_{\text{Revolution}} = \frac{\text{ParticleVelocity}}{\text{CircumferenceLHC}}$ **Table 2: Beam-dependent values**

4.5. Reliability aspects

Every beam dump request must be safely executed, as fast as possible, at every stage of operation, i.e. from the injection at 450 GeV to the maximum energy of 7 TeV. A faulty or incorrect working beam dump system would lead to serious damage to the accelerator.

The following reliability performance is required [2]:

- The failure rate λ for the execution of a beam dump request should not exceed 1 failure per 10^6 hours (=114 years) for the whole beam dump system.
- A redundant Trigger Generator is necessary to maintain a safe beam dumping action even if one device is failing. A dump trigger is always asynchronously

issued via the Re-Trigger system even when both circuits are not working. Thus it works as a third redundant system.

- Due to two parallel redundant branches one failure per year can be tolerated for each branch. Nevertheless the failure rate should be as low as possible.
- The failure behaviour of the trigger generation system must be fault-tolerant, i.e. a fault shall lead to unavailability and not to an asynchronous dumping action. Therefore the redundant device must take over the task of the faulty Trigger Generator.
- The availability for physics must not be significantly impaired by the trigger generation system due to internal dump requests.

4.6. System surveillance

Two different procedures are foreseen to get information about the status of the equipment:

- Continuous surveillance:

  Certain parameters are supervised continuously or e.g. every beam cycle. This makes it possible to take immediately counter-measures, if a failure occurs.
- Post-mortem analysis:

  At least every 10 hours, when a regular refill is necessary, a beam dump has to be executed. The data about the system status obtained during this action provides valuable information about the current condition of the trigger generation equipment.

The Surveillance System evaluates the information, forwards data about the current system status to a higher-level system and decides about necessary measures, if a failure occurs.

4.7. Results

This paper concludes with the complete preparation for the Trigger Generator prototype. As already mentioned in chapter A.1. only the final circuit schematics and the design of the PC-board remains to be done for finishing the test device. This circuit fulfils already all functions of the final Trigger Generator, which will be installed in 2004. It will serve as a test module for investigating unexpected problems and as a trigger generation device for the kicker magnet test chain. The work on the prototype will be completed until end of July 1999.

B.Technical Execution

1. General scheme

The functional requirements lead to a structure, which is easy to realise and where every subunit can be treated separately. A choice has been made for implementing the most important functions in a FPGA (Field Programmable Gate-Array). This maintains an easy structure with a flexible programming facility for experimental purposes. Although the chip contains thousands of logic blocks it has a failure rate similar to a simple logic IC. The expected reliability is thus significantly increased. Further it saves much space on the PC-board.

Figure 6 shows the structural block diagram including all input/output signals of the Trigger Generator. The **Oscillator Unit** generates continuously the beam-synchronised trigger pulses and continues for a certain time even if the timing lines are faulty. The synchronisation signal for the Oscillator Unit is derived from the Timing input by a fixed delay, which is implemented in the **Timing Unit**. The delay time is adjusted in such a way that the rising magnetic field of the kicker magnets starts exactly at the beginning of the particle-free gap.

The Client Interface receives the dump requests and issues a simple pulse to the dump request input of the Trigger Generator. The **Dump Request Preparation** stores this information. If the request path is not locked caused by an internal or an external detected synchronisation or system fault the **Output Trigger Gate** is closed and the following beam-synchronised trigger pulse is amplified, shaped and issued to the Trigger Distribution system.

The **Synchronisation Surveillance Unit** supervises the position in time of the Oscillator Unit signal compared to the delayed timing signal generated by the Timing Unit. If a certain time difference is exceeded certain measures are taken dependent on the current status of the parallel redundant Trigger Generator.

The **Surveillance System** supervises all vital internal functions like phase deviations and detects the origin of all important actions within Trigger Generator.

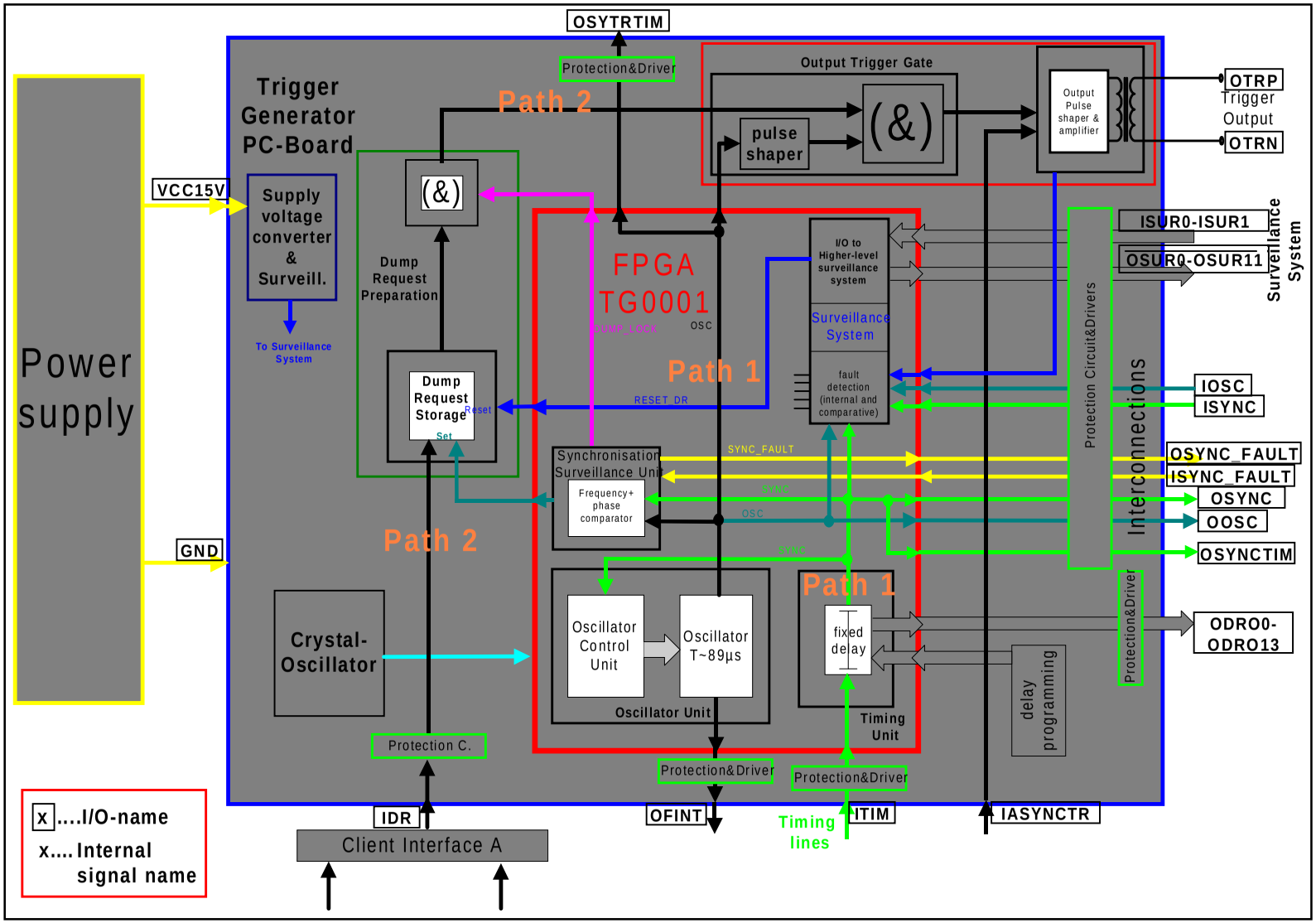

Figure 6: Structural block diagram of the Trigger Generator

The prepared information is then forwarded to the higher-level surveillance system via a number of status bit lines.
A beam dump can also be directly requested by the higher-level surveillance system in case a severe failure occurs in the beam dump system.
Further specifications can be found in Appendix A, which contains the detailed input/output-specifications for the Trigger Generator.

As can be seen from Figure 6, the Trigger Generator consists of two independent signal paths:

- Path 1 is responsible for the generation of the synchronisation signal and consists of the Timing Unit and the Oscillator Unit.
- Path 2 is responsible for the preparation of the dump requests (Dump Request Preparation unit).

Both paths are only connected in the Output Trigger Gate, which issues solely a signal, if both paths 1 and 2 are active. In the worst case a failure in the Dump Request path can cause a synchronous beam dump generated by the Trigger Generator itself.
An error in the synchronisation path can early be detected by the supervising units (Synchronisation Surveillance Unit and of course the Surveillance System) which follows in a beam dump triggered by the parallel redundant device. An asynchronous beam dumping action caused by the trigger generation system can only occur, if a failure exists in path 1and a beam dump is requested, but this case is very unlikely.
The reliability of the whole device is increased by separating both paths also spatially on the circuit board. Thus no internal error of the FPGA-chip can cause a disastrous system malfunction.

During the whole implementation process the principle of simplicity was always one of the determinants for the way of realisation.

Why simple realisation ?

- The fewer components are used and less complex operations have to be executed the higher is the reliability of the whole module.

- Due to less complexity fewer problems will arise during practical realisation of the prototype.

Further all parts responsible for timing and supervising are realised completely digital.

Advantages of digital realisation:

- *Component tolerances do not influence the overall stability and accuracy, thus there are no problems with time or temperature drift.*
- *The long-term stability of the whole device is then only determined by the properties of the internal reference oscillator, which is very stable (e.g. crystal oscillator).*
- *Digital circuits can be supervised much easier than analogue ones by reading-out of typical values.*

The further implementation process is divided in three parts:

1. The implementation of the most complex functions into the FPGA, which will be treated in chapter B.2.
2. The design of the circuits realised with discrete components described in chapter B.3.
3. The structure of the peripheral units, like the internal reference oscillator, the power supply, the FPGA-configuration circuits and the protection circuits is the main part of chapter B.3.3.

All described circuit designs are results of extensive investigation and selection procedures where the most adequate solutions were chosen. Since the description of these procedures would be beyond the scope of this paper they are not treated here.

2. FPGA-Implementation

Figure 7 shows the internal and the input/output-structure of the Trigger Generator-FPGA-chip TG0001. The detailed pin description can be found in Appendix B that contains the complete data sheet of this chip.

In the chapters B.2.1 until B.2.4 the different subunits are treated separately including modelling, designing and implementation. Chapter B.2.5 contains the insertion of the individual modules into the overall chip and B.2.6 the final power dissipation calculation, which is necessary to determine the method of cooling.

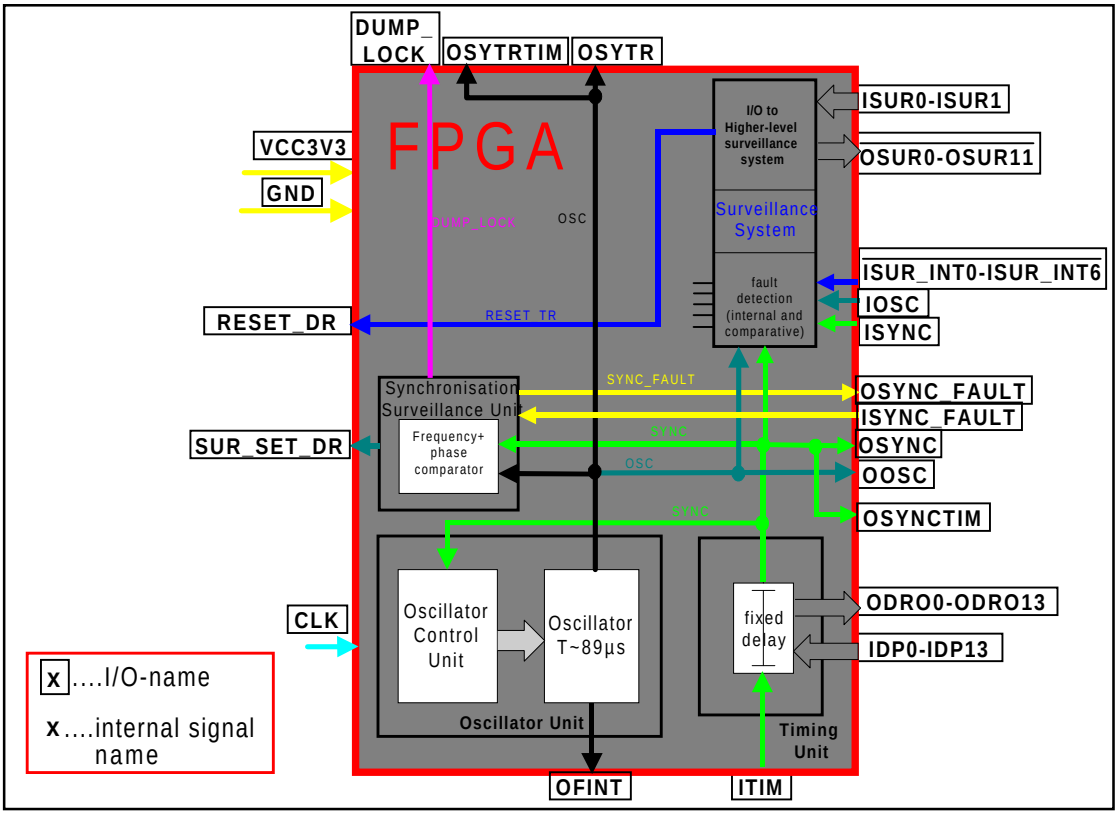

Figure 7: Trigger Generator FPGA-chip TG0001: Internal and input/output-structure

The insertion of the subunits into the XILINX®-FPGA was executed with the XILINX® Foundation Series 1.5i software package. All functional simulations and the data about the timing and delays after implementation are based on the included simulator. The design entry was executed with the Schematic Editor, because of the possibility of easy modification and the clearer arrangement compared with the state diagram and HDL-based programming. A XILINX®-FPGA XC4044XLA - speed grade 08 chip was used for this application. A first estimation revealed that only 20% of the 3800 logic cells will be used, but only this measure makes it possible to fulfil the speed requirements. All statements concerning time deviation and the position of the signals in time refer to the leading edges of the pulses.

2.1. Oscillator Unit

This unit represents the most complex structure within the Gate-Array. It generates the beam-gap synchronised OSC-signal (issued at OSYTR). OSC always has to be in synchronisation with the internal SYNC-signal, which is derived from ITIM by the Timing Unit delay. The maximal timing deviation between SYNC and OSC was

defined with +40ns, i.e. OSC must not be later than 40ns compared to SYNC and never earlier. In case SYNC fails, OSC must be further generated with the last known time period of SYNC for a time of 5 beam cycles (~445 µs). After that period the maximal time deviation must not be exceeded. The combination of an easy and precise working revolution frequency measurement on the base of a second-order Phase-Locked-Loop (PLL) with an independent output oscillator (see Figure 8) is used for this application.

Why a PLL ?

- *A PLL adapts continuously its output frequency to the input frequency, therefore long-term deviations of the internal reference clock have no influence.*
- *The damping properties of the PLL prevent considerable oscillations of the output frequency due to noise and jitter of the input signals.*

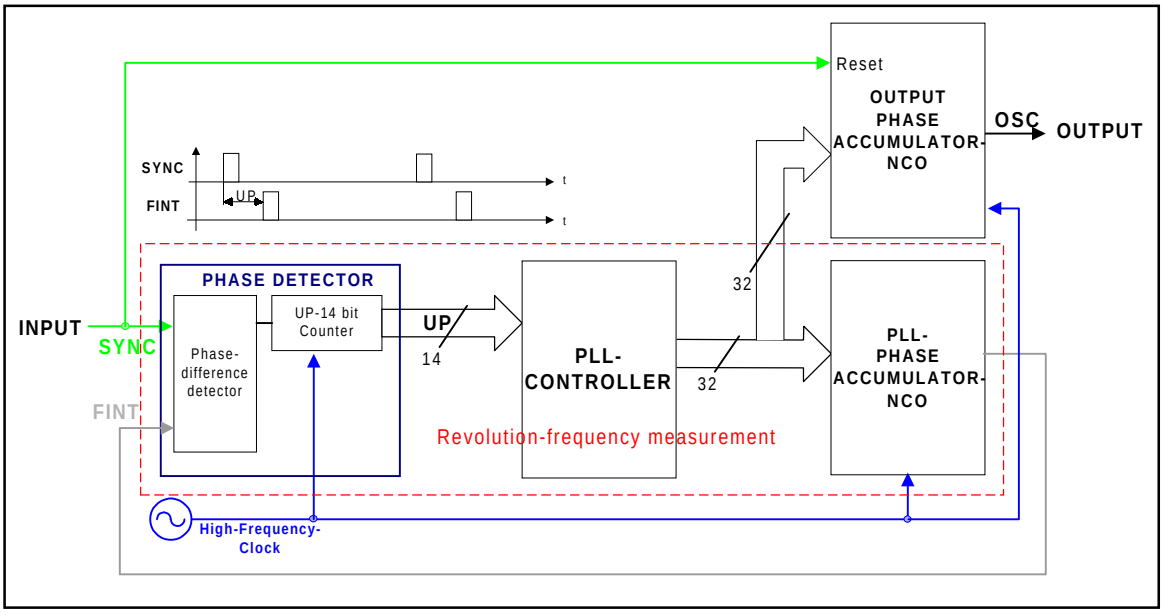

Figure 8: Structure of the Oscillator Unit

The measurement and output parts are only connected through a 32-bit data line; which transfers continuously the last measured value of the beam revolution frequency to the output Numerical Controlled Oscillator (NCO). Reseting the output oscillator every beam cycle through SYNC ensures that OSC is resynchronised with the input every 89 µs. If SYNC fails then the data line is disabled and the output oscillator continues with the last measured revolution frequency. All synchronisation faults caused by frequency fluctuations of either the high-frequency clock or SYNC are immediately detected by the Synchronisation Surveillance System.

2.1.1. Revolution Frequency Measurement (RFM)

The following part provides the mathematical proofs and shows the technical realisation of each module of the Revolution Frequency Measurement. The RFM uses a special digital second-order PLL (for further reading and literature about digital PLL's please refer to the paper of *Lindsey* [4]) to follow very precisely and stable the revolution frequency of the LHC.

This scheme was especially developed for this project, but can surely be used to fulfil similar tasks in other applications.

Figure 9 shows the structure of the used circuit. The main determinant for the properties of a PLL is the chosen controller algorithm. Simulations and mathematical calculations (the methods are described later in this chapter) revealed that for this application an controller algorithm of the form

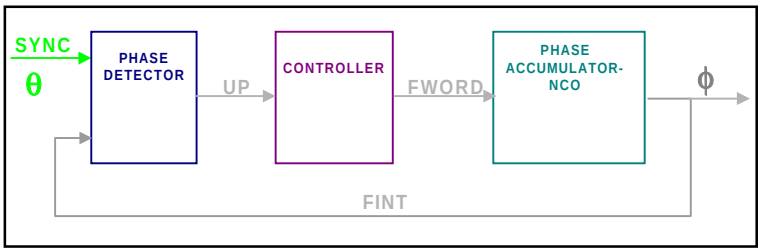

Figure 9: RFM-Phase-Locked-Loop

$$C(z) = k_C \cdot \frac{z-1}{z-1} \qquad (1)$$

provides the best results. Further it is very simple to realise (see Figure 10). The boundaries within the controller are necessary to maintain that it always works in the same range as the PLL-NCO.

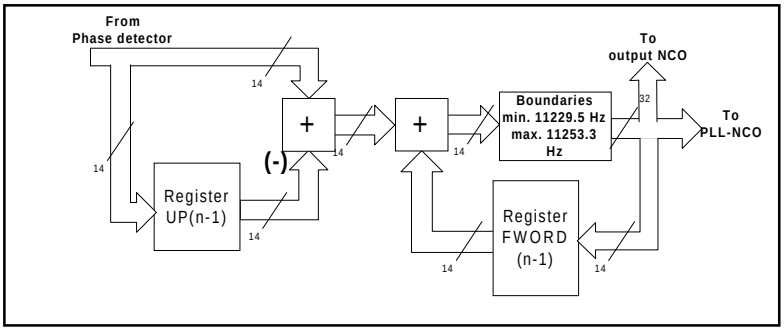

Figure 10: Controller realisation

The mathematical form (1) shows that the fraction can be reduced to 1, which means that this circuit has certain properties of a First-Order PLL, e.g. it synchronises only the frequencies not the phases of both SYNC and FINT (RFM output), thus it is actually a Frequency-Locked-Loop. The following mathematical treatment will reveal these properties and will explain the reasons for the choice of such an algorithm.

As Figure 8 shows, the Phase detector employs a counter that is enabled by the phase difference detector. The phase difference detector works like a RS-Flip-Flop that is continuously set and reset by SYNC and FINT. It issues pulses with a length exactly corresponding to the time difference between both signals.

The following counter issues the phase difference from SYNC to FINT as the number of high-frequency-clock cycles passed during this time (=UP). Since both input signals are already synchronised with the internal reference clock no additional timing jitter is generated by this measurement. The transfer function of the whole phase detector contains only a constant and equals to

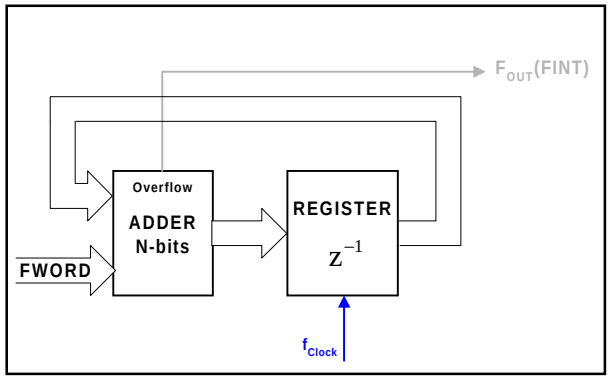

Figure 11: Phase Accumulator

$$PD(z) = k_{PD} \tag{2}$$

For the NCO a phase accumulator consisting of an adder and a register (Figure 11) was used. This is a special and very precise technique for digital frequency generation with high resolution. The operation is based on continuous adding of the "frequency word" (FWORD) to the content of the phase accumulator (N bits) with every clock cycle of the internal reference clock. Every time it overflows an output pulse is issued, the Most Significant Bit (MSB) is truncated and the addition continues (Figure 12).

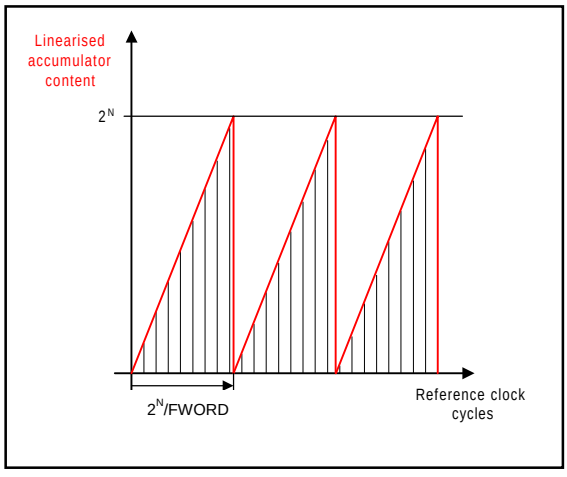

Figure 12: Phase Accumulator operation

The output frequency f_{OUT} is given with

$$f_{OUT} = \frac{FWORD}{2^N} \cdot f_{Clock} \tag{3}$$

where f_{Clock} is the frequency of the internal reference clock. f_{OUT} is only the average frequency, if every cycle is observed there will be a worst case jitter of $T_{Clock} / 2$ due to the truncation of the MSB. But since this jitter influences only the cycle to cycle time period and is not accumulated over time the accuracy properties of the Trigger Generator are not impaired.

The resolution of the phase accumulator NCO equals to

$$f_{Re\ solution} = \frac{f_{Clock}}{2^N} \tag{4}$$

and the transfer function can be derived from Figure 10 as

$$NCO(z) = k_{NCO}\frac{1}{z-1} \tag{5}$$

The reference clock frequency was chosen to be at 100 MHz.

Why 100 MHz ?

- *Every digital time counting and signal generation causes a certain amount of jitter due to the discrete intervals determined by the internal reference clock. The phase accumulator contributes $T_{Clock}/2$ and the Timing Unit has an uncertainty of $1xT_{Clock}$ and a maximal resolution error of $T_{Clock}/2$. Thus the overall jitter is $2xT_{Clock}$ (=20 ns).*
- *To maintain a sufficient long free-running time a time range of at least 40 ns (± 20 ns) must be foreseen. The lower the reference frequency the worse the oscillator resolution, which entails a larger drift range. This fact will be explained in detail in chapter B.2.1.2.*
- *Further the output part and the internal oscillators have also time delay tolerances, which were assumed to contribute with 50 ns to the total tolerance.*

At a frequency of 100 MHz the time period is 10 ns, i.e. if all above mentioned errors are summarised it can easily be seen that 100 MHz is nearly the lowest possible reference clock frequency.

Based on the above obtained results the PLL-constant k_{PLL} can be calculated with

$$k_{PLL} = k_{PD} \cdot k_C \cdot k_{NCO} \tag{6}$$

Since the time period of one beam cycle (T_{SYNC}) is ~88.92 µs and the counting frequency of the phase detector is 100 MHz, k_{PD} equals to [5]

$$k_{PD} = \frac{UP(2\pi)}{2\pi} = \frac{8892}{2\pi} = 1415.21 \tag{7}$$

Due to simpler possibility of realisation k_C=1.

k_{NCO} from equation (5) is calculated with [5]

$$k_{NCO} = \frac{(\omega_{OUT\,max} - \omega_{OUT\,min}) \cdot T_{SYNC}}{FWORD_{max} - FWORD_{min}} \qquad (8)$$

The NCO width was determined with 32 bits. Hence the frequency resolution equals to 23.28 mHz (4) and the time period resolution to 0.1841 ns.

Due to simple realisation only the least significant 10 bits of the NCO are programmable, the remaining bits are hardwired (FWORD= $111010111XXXXXXXXXX_{bin} \Rightarrow 482304\text{-}483327_{dez}$). This fact entails that the possible frequency range reaches only from 11229.5 Hz to 11253.3 Hz (3) compared to the working point of ~11245.5 Hz (see Figure 13).

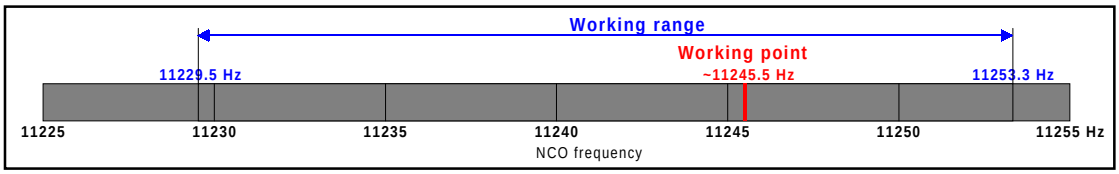

Figure 13: Phase accumulator working ranges

Why such a narrow working range ?

- *If an NCO malfunction occurs it can either fail completely (no pulse is issued) or it oscillates only in this small range, i.e. in the worst case the time signal drifts slowly away, which gives the Synchronisation Surveillance Unit the necessary time to react in the right way on the failure. Thus this system is fault-tolerant.*
- *All calculations are simpler, which increases the reliabilty and decreases the complexity of the circuit.*
- *The range is large enough to avoid running-out of range due to changes of properties of the internal reference oscillator (aging, temperature fluctuations,….). First investigations revealed that an ordinary temperature compensated crystal oscillator would be sufficient for an theoretical lifetime of nearly 100 years (proof follows in chapter B.3.3.1.)*

Substituting all values in (8) gives yields to $k_{NCO}=12.9920 \cdot 10^{-6}$ and with (6) to $k_{PLL}=18.3877 \cdot 10^{-3}$.

Figure 14 shows the phase advance of both SYNC (input θ) and FINT (output ϕ), from which the difference equation can be derived.

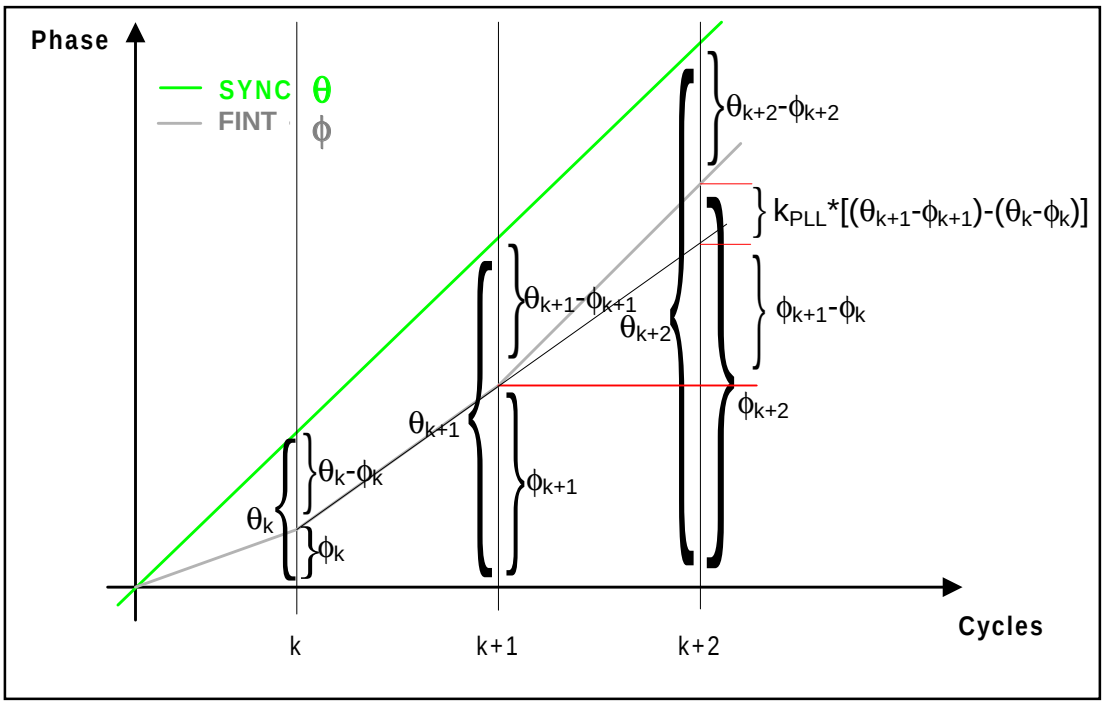

Figure 14: Phase advance of SYNC and FINT

The difference equation for the RFM equals to

$$\phi_{k+2} = \phi_{k+1} + (\phi_{k+1} - \phi_k) + k_{PLL} \cdot [(\Theta_{k+1} - \phi_{k+1}) - (\Theta_k - \phi_k)] \qquad (9)$$

Introducing the z-Transform with $z = e^{Ts}$ [6] (9) can be simplified to the transfer function

$$\frac{\phi}{\Theta} = \frac{k_{PLL} \cdot (z-1)}{z^2 + (k_{PLL} - 2) \cdot z - k_{PLL} + 1} \qquad (10)$$

Formula (10) is the base for the following calculations concerning the stability and behaviour of the RFM-loop.

Mathematical proofs

With the above gained results the properties of this circuit can be investigated. Of interest are the ramp response and the parabolic response, that correspond to a frequency offset and a frequency ramp (=acceleration ramp) applied to the SYNC input.

Figure 15 shows the response of the RFM on a frequency offset, which corresponds to the lock-in process, when SYNC is enabled and the PLL-NCO adapts its output frequency from f_0 (11229.5 Hz) to the frequency of injection (at 450 GeV) of 11245.43 Hz. Since the phase error is

$$\mathrm{UP}(k) = \varphi_{\mathrm{SYNC}} - \varphi_{\mathrm{FINT}} \qquad (11)$$

it follows that (taken from App. C1)

$$\lim_{k\to\infty} \mathrm{UP}(k) = 6.865\,\mu s \qquad (12)$$

and

$$\lim_{k\to\infty} \mathrm{UP}'(k) = 0 \qquad (13)$$

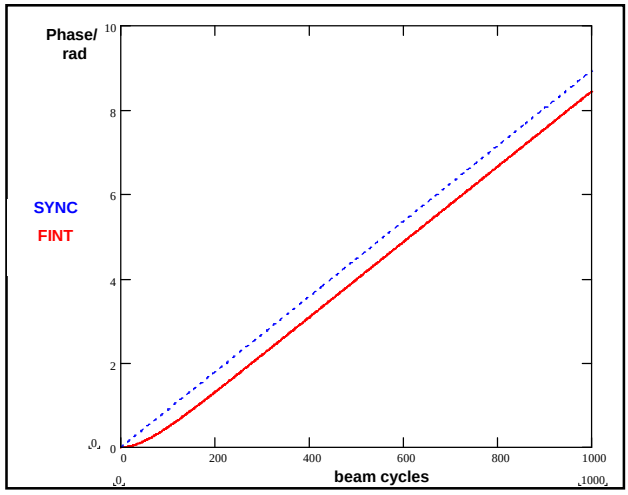

Figure 15: PLL frequency offset response

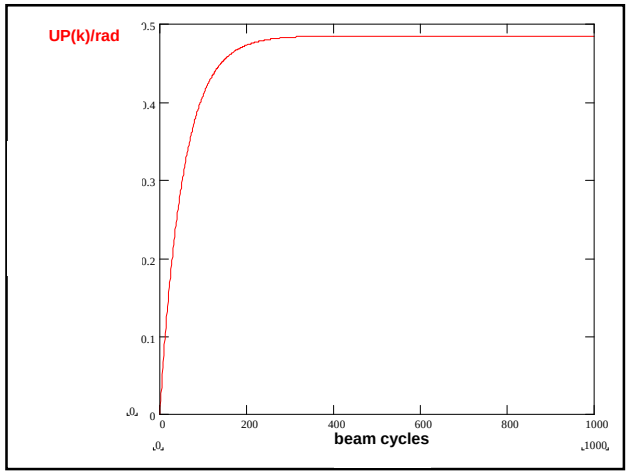

Figure 16: Phase difference after frequency offset

Figure 16 and equations (11)-(13) show that this circuits regulates precisely the frequency (13), but the phase difference is not compensated (12), i.e. the lock-in process causes a phase drift of 6.865 µs.

Why only frequency-lock ?

- *Investigations revealed that exactly phase-synchronous signals would cause problems at the phase detector (wrong measurements due to overlapping). With the used loop it is possible to lock at any phase difference.*
- *Since the RFM-loop can lock on any phase difference the frequency-lock can be checked by subtracting the last UP-value from the current one. Thus the phase*

difference must only be measured in one direction (UP), which simplifies the realisation significantly.

The definition of certain operating ranges maintains safe frequency lock and avoids problems caused by overlapping. The different ranges are shown in Figure 17.

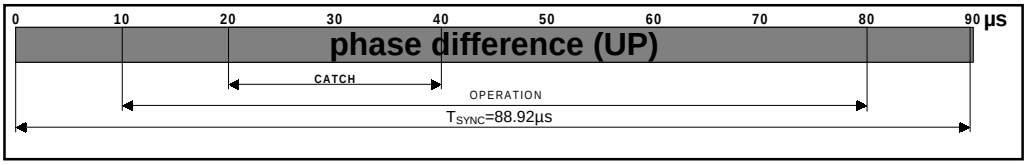

Figure 17: RFM operating ranges

If at the beginning of the initial lock-in process the phase difference UP is outside of the CATCH-range the oscillator frequency is set to the lower boundary (11229.5 Hz) and remains there until CATCH is reached, i.e. FINT locks on the next cycle of SYNC. This operation needs maximal ~550 cycles or 50 ms (=time for drifting from the end of CATCH at UP=40 µs to the beginning of CATCH of the next cycle at 20 µs).

After that the OPERATION-range is enabled, which is then the normal working range. Subsequently f_{FINT} is locked to f_{SYNC}, which will cause an accumulated time drift of +6.865 µs (12), i.e. UP drifts from the beginning of CATCH at ~20 µs to 26.685 µs. When the lock-in process is finished (drift of UP/cycle≤10 ns) the data connection to the output NCO (Figure 8) is enabled and the current FWORD is loaded into its input register. Only at this instant the output NCO starts its operation. Each time the time drift of UP exceeds 10 ns/cycle or it is out of the OPERATION-range (UP<10 µs or UP>80 µs) then the data connection is disabled and the output NCO continues with the last correct FWORD value until the RFM is locked again.

If the acceleration ramp of LHC is applied (i.e. SYNC increases by 24 mHz within 25 min [see table 2]) UP will drift by further +0.012 µs. But since this phase drift has never an influence on the frequency-lock it can be tolerated and the output NCO will always issue the correct OSC-signal.

The limits of all ranges were determined on the base of simplicity, i.e. an exceeding of the limit at 10 µs is detected, when bit 10 of the UP-counter is set (equals exactly to 10.24 µs), bit 11 is responsible for the 20 µs boundary and so on.

For the proof of all these statements, please refer to Appendix C.1, which contains the complete Mathcad 6.0 calculation.

Stability check

An important question is always the stability of a feedback loop. The calculation of the position of the transfer-function poles (Figure 18) provides a good proof. The poles of the closed loop are located at p_1=0.982 and p_2=1, i.e. one pole lies really inside of the z-unity circle and the second one is directly placed on it. Additionally in accordance with [7] a discrete PLL-controller must have a pole at z=1 to compensate a frequency offset. Thus the used PLL-algorithm is stable.

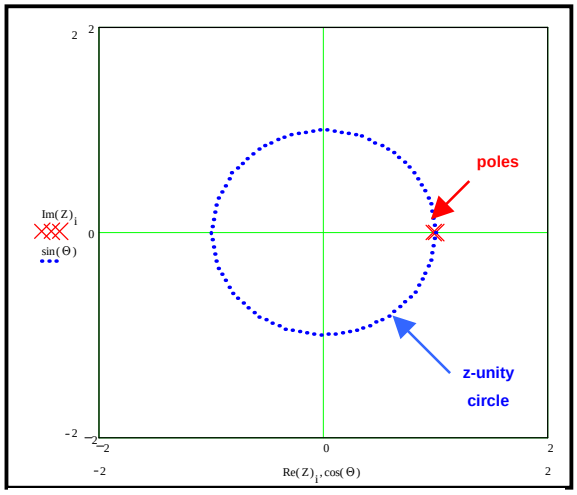

Figure 18: poles in the z-plane

Cycle-by-cycle simulation

All results and figures that were obtained until now are based on mathematical calculations with the z-Transform. The following cycle-by-cycle simulation shows that the mathematical treatment is correct and that the circuit works in the required way.

Different attempts were made and finally Microsoft® Excel 97 was chosen as platform of the simulation. The reasons for this extraordinary choice for a mathematical simulation were the possibilities of easy step-by-step display, the graphic tools and the simple obvious style of programming.

All values are computed step-by-step like in the real circuit, all boundaries were implemented and even disturbance factors like jitter were reproduced. It was assumed that the PLL-NCO oscillates at the lower frequency boundary (11229.5 Hz) and UP is zero, when the SYNC-signal (beam revolution frequency at 450 GeV ⇒ 11245.4826 Hz) was enabled and the lock-in process started.

Figure 19 shows that the frequency locks without overshoot and follows the acceleration ramp very stable. The simulated phase drift due to frequency lock-in and the acceleration ramp (see Figure 20) equals to $\Delta UP_{Simulation}$=6.865 µs, which corresponds nearly exactly to the figure obtained from the mathematical calculation with z-Transform (6.877 µs).

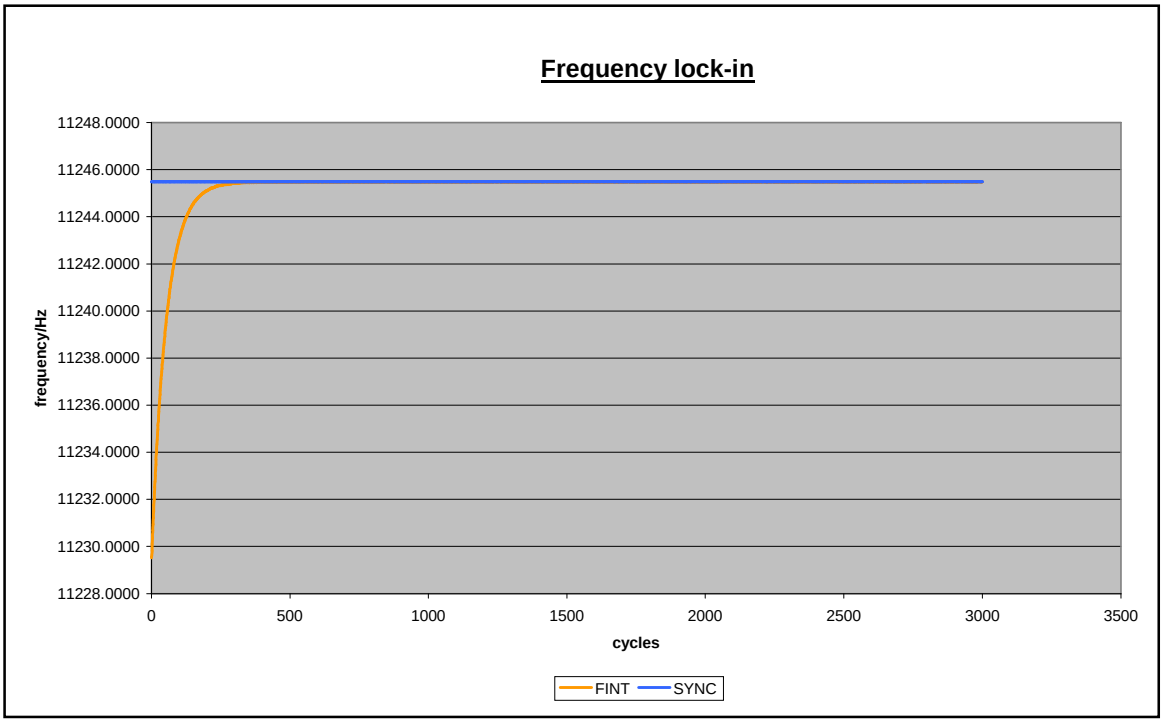

Figure 19: Excel-Simulation Frequency lock-in

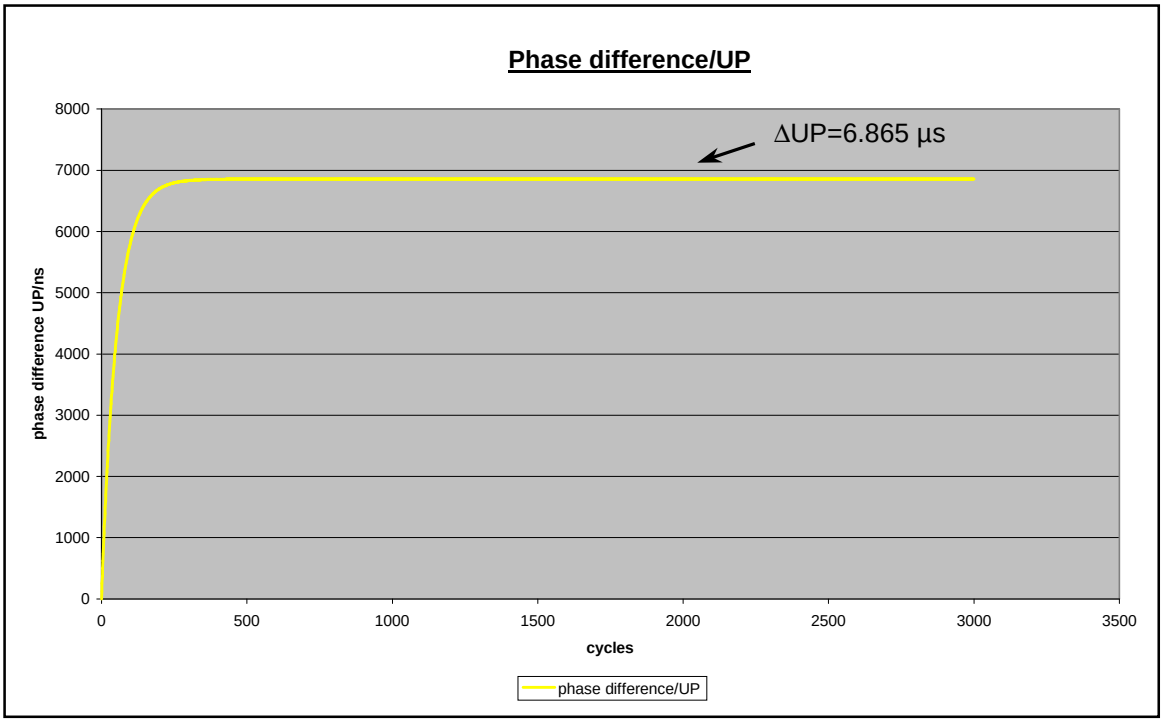

Figure 20: Excel-Simulation Phase drift

A detailed description of the Excel 97-simulation can be found in Appendix C.2.

Conclusion

Since both calculation and simulation provide nearly the same result the correct function of the algorithm is proven. The RFM fulfils all requirements and further entails the advantage of easy realisation due to its particular properties.

2.1.2. Output Oscillator

The output NCO (see Figure 8) works independently from the RFM, i.e. it can be resynchronised at any moment to another part of the LHC beam. This might be necessary if the normally particle-free 3 µs-gap will accidentally be filled caused by a faulty injection from SPS.

The RFM issues every beam cycle the current value of FWORD. This value is only transferred to the output oscillator, if the RFM is locked (ΔUP/cycle < $\pm$10 ns) and no other FWORD is currently loaded, which lasts N (=32) cycles.

The SYNC signal, which provides the information about the gap position resets the oscillator every beam cycle. If SYNC fails or the beam timing signal ITIM is not more available respectively, the output oscillator continues the generation of OSC with the last loaded beam cycle frequency. Both PLL-NCO and output-NCO are completely identical.

Why identical oscillators ?

- *All delays, reference oscillator fluctuations and other disturbance factors are compensated by the RFM-feedback-loop. Further the output oscillator is clocked by the same reference. Therefore all FWORD-values are automatically error compensated and component deviations must only be considered in view of the operation ranges.*
- *The output oscillator is loaded with the same FWORD as the PLL-NCO, which simplifies operation because no additional translation logic is needed.*

Due to the fact that the PLL-NCO has only a certain time period resolution (0.1841 ns from equation 4) it oscillates either on the step above the real beam revolution time period (SYNC) or below. That means in case the timing signal fails the output NCO drifts away during free-running operation. Thus the time tolerance range was defined

with ±20 ns around the working point (Figure 21). Therefore the Oscillator Unit maintains a minimum free running time of ~8.9 ms (~100 beam cycles).

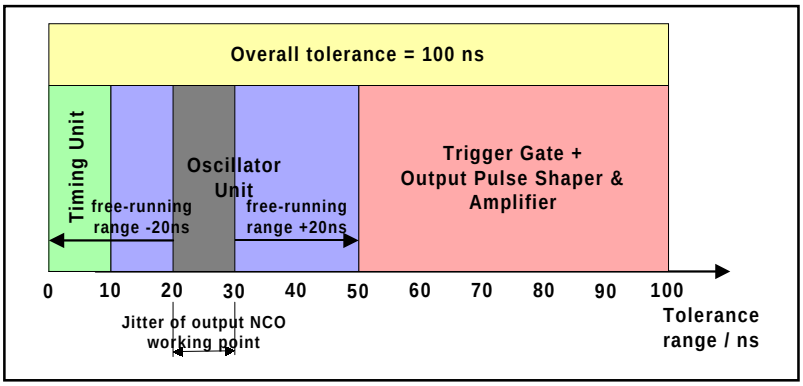

Figure 21: Time tolerance distribution

The time tolerance range around the working point of ±20 ns must always be maintained, i.e. the output oscillator must have its working point always 20 ns later than SYNC. The reset operation triggered by SYNC automatically provides this delay. This measure maintains that OSC comes never earlier than SYNC.

The Timing Unit produces a time uncertainty of 10 ns, which has the reason that the input timing signal can have any position relating to the internal reference clock. Due to this fact the working point of the output NCO fluctuates within 10 ns.

The problem of the output NCO-reset every beam cycle is that due to the clearing and loading operations the phase accumulator is set to zero before an OSC-pulse is issued. But for the system surveillance it is necessary to check the position of the output oscillator signal OSC compared to the SYNC signal every beam cycle.

The clearing operation delays the start of accumulating by 2 clock cycles and the loading operation of FWORD into the accumulator registers needs 19 clock cycles for the 19 necessary bits (FWORD width). The summed delay of 21 clock cycles was compensated in the following way:

1. SYNC is delayed by 21 clock cycles (210 ns) before it resets the oscillator. Combined with the normal loading operation bit 21 and bit 23 are set (=10.485.576$_{dez}$). The average FWORD is ~483000, i.e. by this operation the missing 21 (exactly 21.7) clock cycles are added into the phase accumulator and the delay is compensated.
2. The time difference between SYNC and OSC is then always +20 ns.
3. The timing of this operation is not critical because bit 21 is only needed again after 4 clock cycles (=40 ns).

2.1.3. Implementation of the Oscillator Unit

The most critical parts in this subunit are both NCO's. For realisation of a 32-bit phase accumulator, which works at 100 MHz within a XILINX®-FPGA, certain techniques were necessary. The design is based on a XILINX®-Application Note [8], which was modified and adapted. A pipelined (ripple-carry logic) adder design with a delay equaliser for the loading operation is applied to meet the requirements.

Another important part is the LOADCTRL-unit, which enables and disables the data connection between both oscillators. It ensures that only correct values are loaded and synchronises the FWORD data flow with the operation of the output-NCO.

The OSCTIMING-unit controls the timing of all operations within the Oscillator Unit so that no errors can occur due to non-synchronised logic operations.

The implementation details and the schematics for the Oscillator Unit can be found in Appendix D.1.

2.2. Timing Unit

The Timing Unit delays the ITIM signal, which provides in fact the beam revolution and position information, in the way that the rise of the magnetic field of the kicker magnets is coincident with the appearance of the particle-free gap at the kicker magnets. The delay must be stable and failsafe, i.e. either the correct signal is issued or no pulse is generated. It is additionally assumed that in case a resynchronisation onto another beam gap is necessary ITIM provides the necessary information. Therefore a preceding circuit must be foreseen, which links the available signals of the RF-timing and the beam monitors in a certain way and generates the ITIM signal. Figure 22 shows the implemented Timing Unit. The longest possible delay requirement is one beam cycle (~88.92 µs).

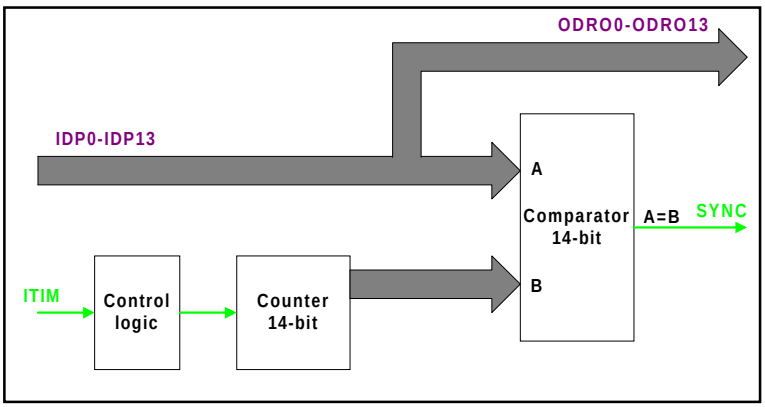

Figure 22: Implementation Timing Unit

The maximal attainable delay of this circuit equals to

$$\Delta T_{\text{Delay max}} = 2^{N_{\text{Timing}}} \cdot T_{\text{Clock}} \qquad (14)$$

That means a 14-bit counter with N_{timing}=14 would have a maximal delay of 163.84 µs, which is sufficient for this application. The delay length is programmed by DIP-Switches, that are directly connected to the IDP0-IDP13 input of the Timing Unit. The DIP-Switches will be placed on the PC-Board, for adjustments the board has to be removed from the rack.

Why programming through DIP-Switches ?

- *Every change of the delay length can cause an asynchronous beam dumping action and subsequently severe damage to the accelerator. The experience shows that remote programming would represent a possible failure source. For that reason the more difficult way of adjustment increases the reliability of the overall system.*
- *The frequency drift of the internal reference oscillator (refer to chapter B.3.3.1) is so low that a readjustment of the delay value IDP is in principle not needed. The comparison of the SYNC signals of both devices will detect large drifts outside of the specifications.*

With the rising edge of ITIM the counter is started and increments with every reference clock cycle. The comparator issues a SYNC-pulse when the counter content and the IDP value are equal. Thus the delay length is calculated with

$$\Delta T_{\text{Delay}} = \text{IDP} \cdot T_{\text{Clock}} \qquad (15)$$

[IDP..programmed delay value]

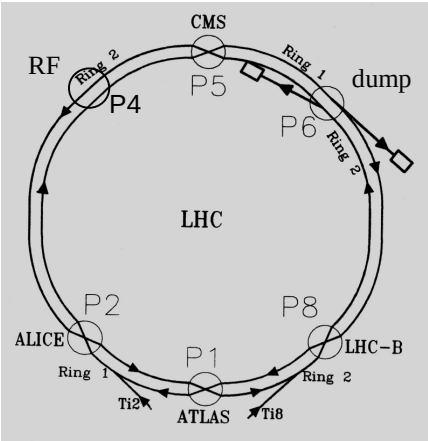

Figure 23: Spatial distribution of the LHC systems and detectors

The necessary time delay is adjusted such that the rising edge of the kicker magnet field fits always into the particle-free gap. Figure 23 shows the spatial distribution of the LHC systems and detectors. It gives an idea about the beam and signal runtimes around the accelerator and is the base for a first estimation of the delay adjustment.

Due to the necessary counter clear the delay range goes from 10 ns to (T_{SYNC}-20ns). As an alternative a DOWN-Counter with preceding preset of the IDP-value was

considered but it has the disadvantage that the loading action needs time, which means not the full range can be covered. Further the necessity of a loading circuit with all the timing requirements would offend against the guideline of simple realisation.

A failure of one of the Timing Units can only be detected by the TIM_FAULT time difference detector of the Surveillance System, which compares the SYNC-signals of both parallel devices. Thus it is very essential for the whole system that this subunit works always correctly. Further details and schematics can be found in Appendix D.2.

2.3. Synchronisation Surveillance Unit

The main task of this subunit is the continuous surveillance of the phase relation between OSC, which is issued by the Oscillator Unit, and SYNC, the delayed beam timing signal ITIM. If malfunctioning occurs in the Oscillator Unit, the phase difference exceeds the maximum tolerated value of 40 ns (see Figure 21) and the SYNC_FAULT signal is issued. Thus it detects mainly failures of the Oscillator Unit. Figure 24 shows the circuit scheme of the Synchronisation Surveillance Unit.

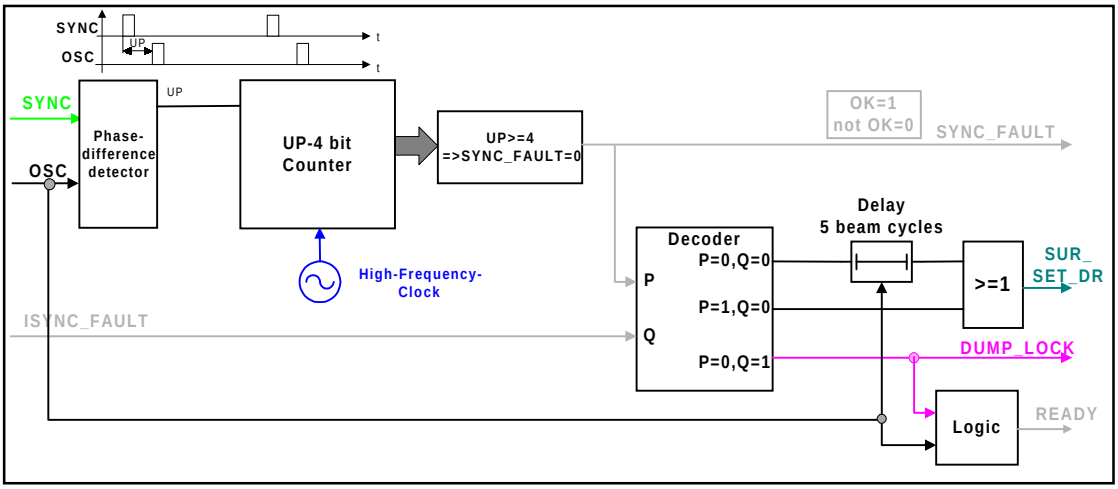

Figure 24: Circuit scheme of the Synchronisation Surveillance Unit

It applies the same phase difference detector as the RFM-loop of the Oscillator Unit. During UP is high the 4-bit counter, which is clocked with 100 MHz (T_{Clock}=10 ns) by the internal reference, increments. If the counter content reaches 4 (bit 2 set) the SYNC_FAULT bit goes to 0, i.e. the duration of UP was longer than 40 ns and OSC either precedes SYNC or is more than 40 ns later.

For the surveillance of the overall trigger generation system the status of the redundant circuit must also taken into account. Therefore the own SYNC_FAULT bit is linked in a certain way with the SYNC_FAULT bit of the parallel device, which is delivered via a cross-connection between both circuits. Different actions are necessary dependent on the system status (see Table 3). The mentioned actions refer to the detecting device.

P	Q	Status	Action
0	0	Timing is failing	Dump after 5 cycles
0	1	own oscillator fails	Lock dump request
1	0	parallel device fails	Dump immediately
1	1	all OK	nothing

Table 3: Surveillance System reaction on different faults

The most severe fault, that can occur, is a complete malfunction of the timing distribution system (P=0, Q=0; ITIM not more available). In that case the Oscillator Unit has to provide the beam synchronised timing signal for at least 5 beam cycles (~445 µs) before a beam dump will be requested by the Synchronisation Surveillance System. The delay avoids a decrease of the availability of the LHC due to short malfunctions of the timing distribution, e.g. short-term connection faults. If the timing signal is not back after 5 cycles, a serious fault of the timing distribution system must be assumed and it is necessary to dump the beam immediately.

A failure of the own Oscillator Unit (P=0, Q=1) must result immediately in locking of the dump request path (DUMP_LOCK=0, negative logic to prevent fail-dangerous operation, when the FPGA-chip itself fails). If the redundant Trigger Generator fails (P=1, Q=0), the beam must be dumped without preceding delay (SUR_SET_DR=1).

READY goes to 1 if the Trigger Generator is able to trigger a proper beam dumping action, i.e. output NCO of the Oscillator Unit provides the correct synchronisation signal. This bit has no connection to another unit but can be later used to indicate the READY-status of the Trigger Generator.

Appendix D.3 contains further details about the implementation and the schematics of the Synchronisation Surveillance Unit.

2.4. Surveillance system

The Surveillance System supervises all subunits of the Trigger Generator. Characteristic status bits are collected and forwarded to the higher-level system.

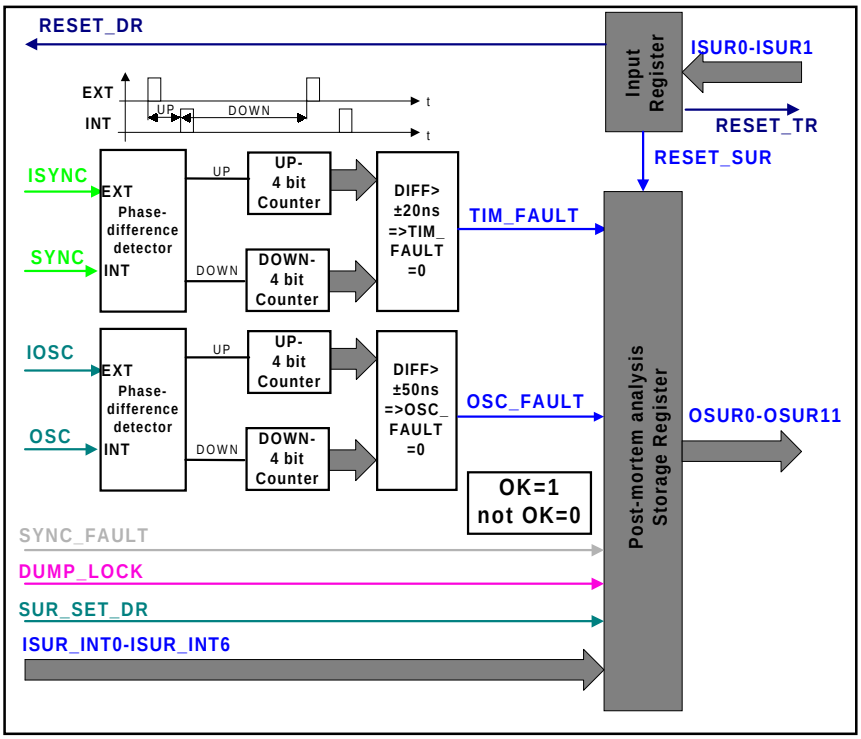

Figure 25: Principle of the Surveillance System

They are stored in registers and read out for post-mortem analysis. That makes it possible to identify failures in the system and investigate their origin.

Figure 25 shows the principle of the Surveillance System. This unit has no control function. It provides only information about the current condition of the Trigger Generator and is part of the surveillance and diagnostic facilities of the LHC beam dump kicker magnet system.

Generally there are three different categories of status bits:

a. Bits, that are issued if certain time difference limits are exceeded (1=OK, 0=NOK). If the power fails, or if the FPGA is severely damaged or if the cables have no proper contact a failure is automatically indicated. The necessary signals of the parallel Trigger Generator are transmitted via direct cross-connections.

b. Bits, that indicate, which signal triggered or inhibited a dumping action (1=set, 0=not set).

c. Bits, that provide information about analogue values, like the power supply voltage and the functionality of the Output circuit.

Category a. contains the following status bits:

♦ TIM_FAULT: Checks the correct function of both Timing Units by comparing the SYNC-signals mutually. If the difference exceeds ±20 ns, TIM_FAULT goes from 1 to 0. This function is directly implemented in the Surveillance System. It applies the same technique as the Synchronisation Surveillance Unit (Phase

difference detector, Counter, Threshold), but is able to detect deviations in both directions.

- OSC_FAULT: This signal goes to zero, if the Oscillator Unit output signals OSC have a time deviation of more than ±50 ns. A failure of one unit immediately leads to the indication of a synchronisation error. The time difference detection is done in the same way as for the TIM_FAULT bit.
- SYNC_FAULT: The SYNC_FAULT bit goes to 0 if the time difference between the internal SYNC and the own OSC-signal exceeds +40 ns. The Synchronisation Surveillance Unit provides already this bit.

The time difference limits represent the ideal case that is assumed for the prototype. For the final system the cable delays of the cross-connections and the different delay properties between branch A and B must be taken into account, when the time difference limits are defined.

Category b. bits provide information about the origin of an action:

- DUMP_LOCK: This bit is set, when the own dump request path is locked due to an internal synchronisation fault and therefore a dumping action is triggered by the redundant Trigger Generator.
- SUR_SET_DR: If the Synchronisation Surveillance Unit triggers a dumping action this bit goes to 1.
- ISUR_INT0 (DUMP_REQU): A dump request, which is received from the Client Interface sets DUMP_REQU to 1.

Category c. bits are responsible for the surveillance of analogue parameters:

- ISUR_INT1 (SUR_TRGATE): This bit is only set, when a trigger pulse is issued via OTRP and OTRN.
- ISUR_INT2 (SUR_PS3V3): The maximum tolerance for the power supply voltages is defined with ±10 %. That means for the 3.3 V line a lower alarm limit of 3 V. Below this voltage the SUR_PS3V3 bit goes to 0.
- ISUR_INT3 (SUR_PS5V): If the 5 V supply voltage falls below 4.5 V this bit goes from 1 to 0.

- ISUR_INT4 (SUR_PS15V): A value of the 15 V-supply voltage below 13.5 V triggers a 1 to 0 transition of SUR_PS15V.

The internal surveillance bits ISUR_INT5 and ISUR_INT6 are reserved for additional surveillance functions for the prototype during the test stage.

All bits are forwarded directly and without synchronisation via the OSUR0-OSUR11 line to the higher-level system, i.e. any change of the status is immediately transmitted. For the detailed assignment of the surveillance status bits to OSUR0-OSUR11 please refer to Appendix B.

The surveillance input (ISUR0-ISUR1) consists of the following signals:

- ISUR0 (RESET_DR): After detection of a successful dumping action the higher-level surveillance system sends this signal (ISUR0=1) to clear the dump request storage.
- ISUR1 (RESET_SUR): After the post-mortem analysis is finished and the status information is not more needed the RESET_SUR bit is set to clear all surveillance registers.

Only if both ISUR0 and ISUR1 are 1 at the same time all FPGA internal units are reset and restarted (RESET_TR, which is connected to the CLR-inputs of all units, goes to 1). This logic combination avoids a system restart without preceding clear of the Dump Request Storage and the Surveillance System Flip-Flops.

Since the Surveillance System will be subject to change during the final implementation and is very similar to the Synchronisation Surveillance Unit the preliminary schematic was not enclosed.

2.5. Insertion of the subunits

The final insertion of the circuits described in B.2.1-B.2.4 with the XILINX® Foundation Series 1.5i software package is divided in 5 steps (see Figure 26):

1. The design entry was done with the Schematics Editor, which represents an excellent tool for clear programming and offers an easy possibility for fast modifications during the test stage of the prototype.
2. After that the functionality of the circuit was checked with the included functional simulation facility of the software package.

3. The implementation into the XILINX® XC4044XLA-08-FPGA (package HQ-160) covers the translation of the programming data, the mapping on the chip, the placing and routing, the timing and delay calculations and the configuration of the final binary stream.

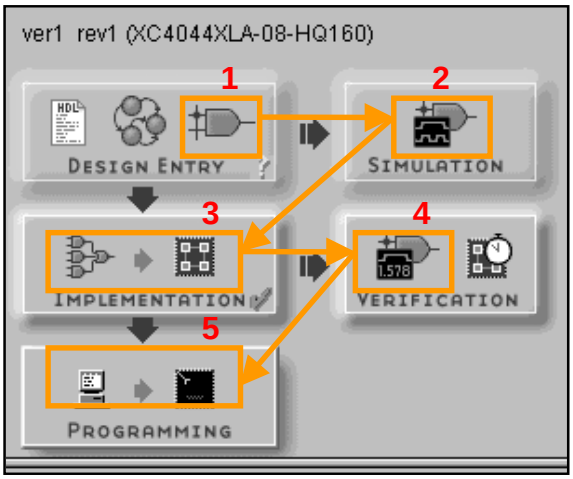

Figure 26: FPGA insertion stages (cut from XILINX® Foundation Project Manager)

4. The timing and delay data is then used to simulate the circuits including all appearing delays and to check finally the correct function and behaviour.

5. After step 1-4 had been finished for each subunit all systems were combined and step 1-4 executed again for the complete circuit. The generated binary stream was then programmed into the configuration PROM (see chapter 3.3.2).

Modifications that are possibly necessary during the test stage of the prototype can easily be executed by repeating these five steps.

The schematics for the complete FPGA-chip TG0001 can be found in Appendix D.4.

2.6. FPGA power dissipation

As mentioned above the implementation of the complex digital part of the Trigger Generator in a FPGA entails a significant improvement in reliability. A necessary forced cooling would diminish this advantage. The ventilation can fail, which leads to overheating and finally destruction of the entire Trigger Generator chip in case the failure is not detected early enough. Therefore only natural cooling maybe in combination with a heat sink should be foreseen. The level of power dissipation within the FPGA-chip determines the way of cooling. The following calculation was taken from [9]:

The total power consumption P_T of the FPGA is

$$P_T = P_{Static} + P_{INT} + P_{OUT} \tag{16}$$

where P_{Static} is the power dissipated by the inactive device, P_{INT} the power consumption due to the internal switching and P_{OUT} the power needed for output

operations.

With I_{CC0}=10 mA and V_{CC}=3.3 V [10], $P_{Static}=I_{CC0}\cdot V_{CC}$ results in a static power consumption of 33 mW.

The internal power dissipation equals to

$$P_{INT} = V_{CC} \cdot K_P \cdot F_{max} \cdot N_{LC} \cdot Tog_{LC} \quad (17)$$

The power factor K_P for XC4000XL-devices is $17\cdot10^{-12}$[10], the maximum frequency F_{max} equals to 100 MHz, the number of used logic cells N_{LC} was estimated with 20 % of 3800 (=the total number of logic cells for the XC4044XLA-chip), where 20 % of them are toggling every cycle (=Tog_{LC}). These estimations were made considering a certain security factor. The internal power dissipation is then calculated to P_{INT}=0.85W. The power consumption due to output operations is expressed through

$$P_{OUT} = \sum_{n=1}^{N} \left(C_n \cdot V_n^2 \cdot F_n \right) \quad (18)$$

N is the number of outputs, C_n the capacitance and V_n the voltage swing of the N^{th} output, and F_n the output frequency. 32 outputs each with a load of 100 pF with 3.3 V output swing and an output frequency of 11245 Hz (=beam cycle frequency, which is the maximum toggling frequency of the outputs) were assumed.

This assumption leads to a maximum P_{OUT} of 0.2 mW. Thus the total power consumption P_T amounts to 0.88 W.

The maximal allowed thermal resistance $\Theta_{J\text{-}Amax}$ of the FPGA is then [11]

$$\Theta_{J-A\,max} = \frac{T_J - T_A}{P_T} \quad (19)$$

T_J is the maximum junction temperature (125°C) and T_A the highest possible ambient temperature, which was assumed with 75°C in the worst-case.

Since $\Theta_{J\text{-}Amax}$ is 56 °C/W and for all XILINX®-packages lower thermal resistances are specified at still air, no forced cooling is necessary.

Nevertheless a heat sink should be foreseen, because at a junction temperature of 125°C, which is still in the specified operating range, all internal delays are already 14% longer and the overall speed decreases then by 12 % than the guaranteed values [11]. Since a lot of critical timing operations are necessary for the correct function of the Trigger Generator, the temperature stress for the chip should be kept as low as possible.

3. Discrete implemented functions

Peripheral functions like the crystal oscillator, the power supply surveillance and the FPGA-configuration electronic are implemented with discrete components. Furthermore some of the Trigger Generator subunits provide better properties in view of reliability if they are installed outside of the FPGA-chip. Also the Output Trigger Gate where a lot of power is switched must be realised with discrete components.

In chapter B.1 was already mentioned that due to reliability the Trigger Generator circuit is divided in two paths. Path 1 is responsible for the time synchronisation and Path 2 prepares the dump requests. Reliability is significantly increased if both paths are additionally separated spatially, i.e. the components have no direct connection. The more sophisticated Path 1 is implemented into the FPGA and Path 2, due to its simplicity, is realised with discrete components.

3.1. Dump Request Preparation

This subunit covers two main tasks. The first function maintains that every incoming dump request is stored until the beam dump is executed. A beam dump can be requested through two different channels:

- Regular beam dump requests that are received by the Client Interface. Possible sources are e.g. one of the 4000 quench protection systems for the superconducting magnets or scheduled beam dumps at the end of a physics run.
- Internal surveillance beam dump requests that occur, when an internal failure of the redundant Trigger Generator has been detected.

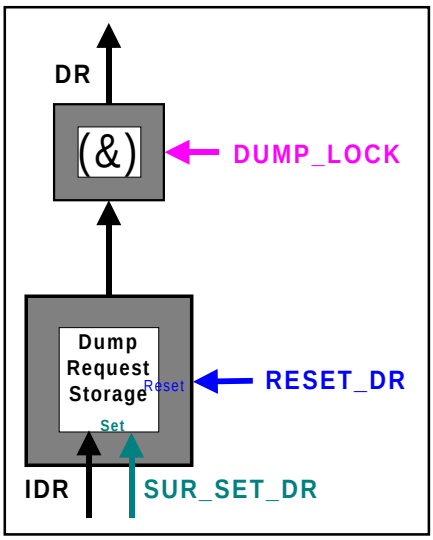

Figure 27: Dump Request Preparation

The second part locks the own dump request path if an internal failure of the own circuit has been discovered.

Figure 27 shows the block diagram and the signals. If IDR or SUR_SET_DR go from 0 to 1 the Trigger Request Storage is set until the Surveillance System resets the Flip-Flop (RESET_DR goes to 1) after a successful beam dumping action.

The dump request path is locked if DUMP_LOCK goes from 1 to 0. Even if the power supply of the FPGA-chip breaks down a failure is indicated and no faulty dump trigger can be issued.

This subfunction is realised with a simple D-Flip-Flop and an AND-Gate that work with the normal 5V-FAST-TTL (74F….-components) standard. The FAST-TTL chips additionally maintain the short rise times and propagation delays that are necessary for this application. Furthermore they are compatible to the 3.3V-LVTTL standard used by the FPGA. The execution with integrated circuits provides a sufficient failure rate, because every malfunction of the Dump Request Preparation unit can only cause a synchronous beam dump.

3.2. Output Trigger Gate

The Output Trigger Gate has the task to issue a 15V and ~1µs long pulse starting with the rising edge of OSYTR solely if DR is 1 (+5V). This pulse is transmitted via OTRP and OTRN to the Trigger Distribution system. The input resistance of this device was assumed with 150 Ω.

The required behaviour is reached by a kind of AND-function that admits an output pulse only if both OSYTR and DR are high. The maximum time tolerance range for this unit is +50ns (see Figure 21).

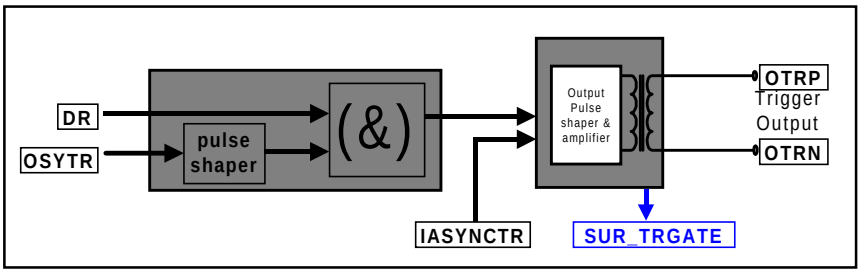

Figure 28: Functional block diagram Output Trigger Gate

Figure 28 shows the functional block diagram of the Output Trigger Gate.

If IASYNCTR gets high an asynchronous beam dump is triggered directly and without delay. Since no driver circuit is foreseen for this channel the IASYNCTR signal must have sufficient power to trigger the output gate, which makes this input insensitive to disturbances like noise and electromagnetic coupling. This additional input is available for possible future needs.

SUR_TRGATE is set when a trigger pulse is issued via OTRP and OTRN. This status bit records the correct function of the Output Trigger Gate and its connections to the Trigger Distribution device.

The Output Trigger Gate is one of the most critical parts within the Trigger Generator, because only at this point the synchronisation part (Path 1) and the dump request part (Path 2) are interconnected, i.e. almost every single failure that occurs in an unit preceding the Trigger Gate cannot cause an asynchronous beam dump. On the other hand every malfunction of this subunit will lead to a faulty dump trigger and must be avoided by the use of particular simple circuit design *(The golden rule of reliable design: Use as less components as possible !!!)*.

The Output Trigger Gate circuit is derived from a Blocking Oscillator, which can produce output pulses with a fast rise time and with high power. It has the advantage of simple circuitry using only a transistor and a transformer to generate a pulse with determined length and output voltage.

Why a Blocking Oscillator ?

- *Integrated circuits contain complex structures consisting of thousands of components, i.e. their behaviour in case of a failure is difficult to predict. Whereas the Blocking Oscillator mainly consists of a transistor and a transformer determining the properties.*
- *As galvanic isolation of the output is needed a transformer is necessary in any case. An additional third winding is sufficient to get a Blocking Oscillator.*
- *A Blocking Oscillator can supply high-power pulses and entails thus a high fan-out capability. It also has the advantage that the driver inputs of the following Trigger Distribution device can have low input impedance and are therefore less noise-sensitive.*
- *Due to regenerative feedback through the transformer a very short rise time (~10ns) for a 0 to 15V transition can be obtained.*

Basically eighteen different ways of realisation of a Blocking Oscillator are possible by combining three properties:

1. Way of feedback (collector to base, collector to emitter, emitter to base)
2. Placement of the timing resistor (emitter line, collector line, base line)
3. Operation mode of the transistor (saturated, non-saturated)

All possibilities were analysed to attain the best switching properties and the highest fault-tolerance.

Finally the principle with

1. Collector to emitter feedback,
2. the timing resistor in the emitter line and
3. non-saturated operation

was used.

Why this principle ?

The following enumeration specifies the advantages of the chosen principle compared with the others referring to the different properties:

ad 1.: Transistor parameters and the load have only a small influence on the pulse width and amplitude. Additionally there is no coupling between input and output, thus no signals are fed back to the input.

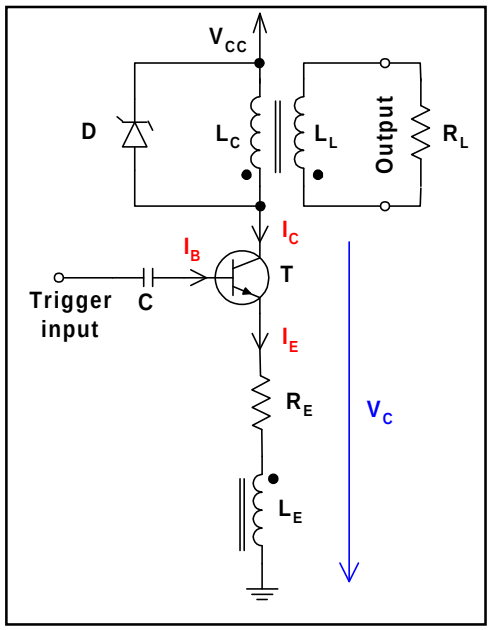

Figure 29: Blocking Oscillator principle

ad 2.: Transistor parameters have only a small influence on the output pulse width.

ad 3.: This behaviour is reached by inserting a Zener-Diode (with low capacitance) in parallel to the collector winding. This measure maintains a proper flat-top and the amplitude of the output is exactly defined.

The trigger for the output pulse is applied to the base, otherwise (trigger applied to the collector) the short 20-30ns trigger pulse would prematurely terminate the output pulse. Additionally this has the advantage of complete input/output-decoupling.

The function of this circuit is explained on the

chosen principle in Figure 29:

- A positive trigger pulse with sufficient amplitude is applied to the base.
- The transistor conducts ⇒ I_B flows ⇒ I_C flows ⇒ U_C decreases.
- The change of V_C is transformed to the emitter and contributes to I_E ⇒ regenerative feedback ⇒ the transistor current rises very fast (t_r=10ns).
- The magnetising current in the collector windings increases proportional to V_{CC}/L_C (L_C….inductance of the collector winding)
- The transistor turns off, when the current sum (Rising magnetising current + Load current) equals to the collector current I_C.
- The change of V_C is transformed to the emitter ⇒ fast fall-time (t_f=40ns).

The feedback must always be regenerative (i.e. right polarity of the transformer) and the load should always be galvanic isolated through a third winding.

Figure 30 shows the adaptation of the Blocking Oscillator to get the final design of the Output Trigger Gate. The modifications that were made are divided in five parts:

a. AND-function:

The Output Trigger Gate must work like an AND-Gate, i.e. an output pulse is solely issued if both OSYTR and DR are high. Through the introduction of a second transistor T2 in series with T1 this requirement is fulfilled. T1 can only conduct in the 20-30 ns time window (see modification b.) after the rising edge of OSYTR and T2 solely if DR is high. Since both T1 and T2 are in series the Blocking Oscillator can only start its operation if both transistors have a positive base to emitter voltage at the same time.

b. Trigger window:

The maximum allowed time tolerance for the Output Trigger Gate is divided in two parts; the first part is a time window of 20-30ns after the rising edge of OSYTR, where the output pulse is allowed to be triggered; the second part, which equals to 20 ns covers delay inaccuracies of the Output Trigger Gate.

For the time window a 20-30 ns pulse has to be generated which is then applied to the base of T1. On the prototype PC-board there are two possibilities foreseen for the generation of this pulse:

- The OSYTR pulse has a length of 20 ns, which means that due to switching delays and the inductance of TX2 the time window for triggering the dumping

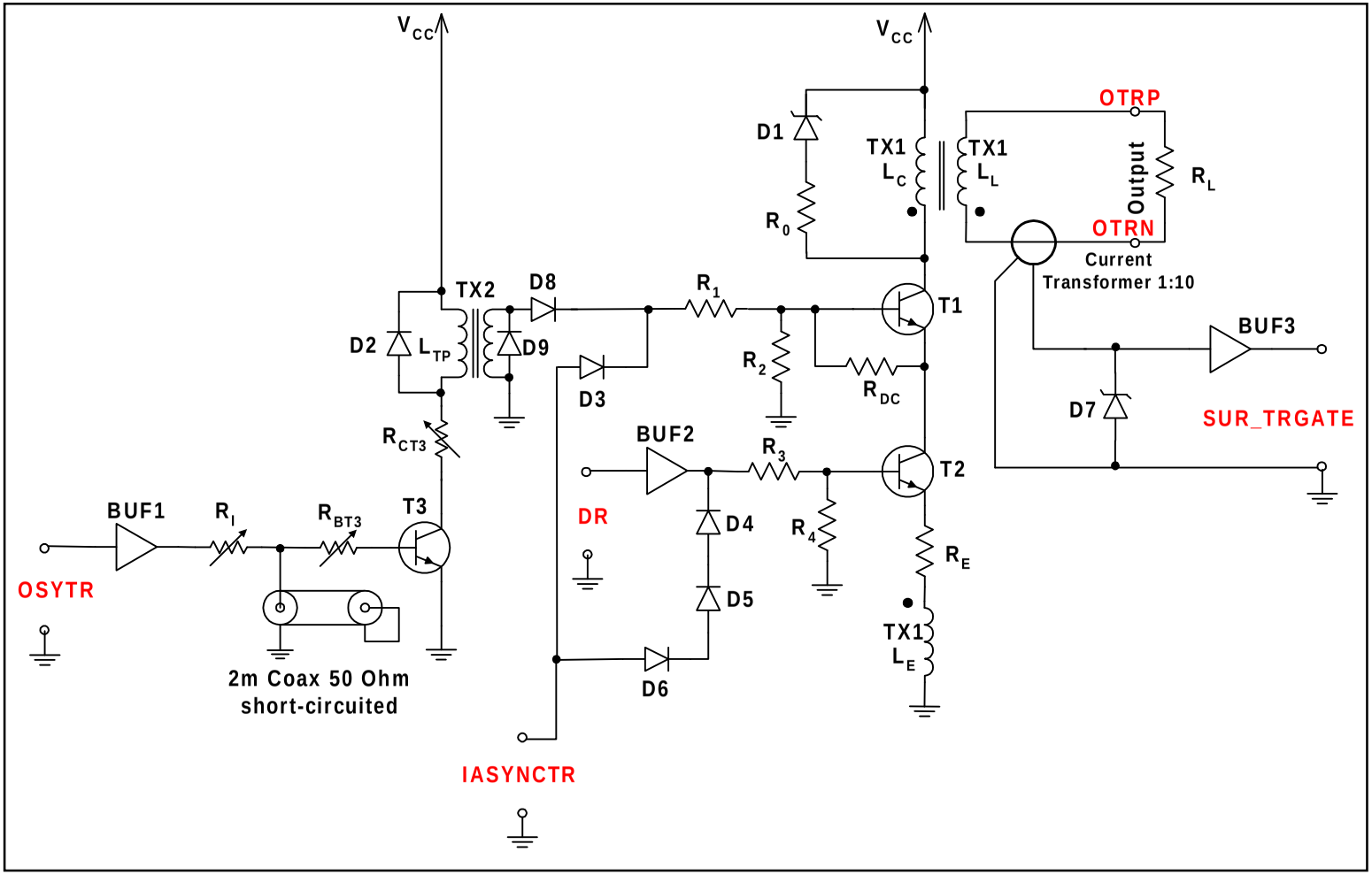

Figure 30: Schematic Output Trigger Gate

action is ~30 ns. In this case the length of the window is determined by the FPGA-chip, thus an internal chip failure would cause a faulty time window.

- The more reliable solution is the connection of a short-circuited 50Ω-Coaxial cable with a length of 2m to the base of T3. The OSYTR pulse is then reflected at the short-circuited end with the opposite polarity, i.e. after 20 ns (the speed of propagation of an electromagnetic wave in a Coaxial-cable is approximately 1 m per 5 ns) the base is short-circuited and T3 switches off.

a. Prevention of an asynchronous beam dump caused by a failure of T3:

TX2 has two main functions. The first task is providing sufficient base to emitter voltage in the right polarity for T1 to get it into conduction within the 20-30 ns time window. The second purpose is the galvanic decoupling of T3 from the real output part. In case this transistor fails (short-circuit) only a short pulse is transmitted, which length is dependent on the time constant $\tau_T=L_{TP}/R_{CT3}$. Only if a dump is requested by chance during this time period an asynchronous dumping action is triggered. Since the length of the pulse is estimated with ~1 µs the likelihood that this occurs can be neglected. For that reason and also for a proper pulse shape the inductance of TX2 should be kept as low as possible.

b. Trigger Gate Surveillance:

The SUR_TRGATE status bit is set if a trigger pulse is issued via OTRP and OTRN. A very reliable way to pick up this signal is a bobbin around one of the output cables, which works then as a current transformer. Thus the SUR_TRGATE bit records failures of the Output Trigger Gate and also of the connections to the following Trigger Distribution device. This signal is limited by a Zener-diode and buffered before it is applied to the input of the FPGA-chip.

c. Direct beam dump trigger via IASYNCTR:

This signal triggers T1 and T2 directly. The diodes D3-D6 are necessary for decoupling of both transistors and to maintain the voltage difference between the base of T1 and the base of T2. This voltage difference is necessary that T1 can conduct while T2 is switched on.

All inputs of the Output Trigger Gate except IASYNCTR are buffered to provide the currents (~50 mA) that are necessary for correct operation. The buffers must maintain rise times ≤5 ns and an output voltage of 5 V.

OSYTR and DR are not synchronised and have finite rise and fall times. That means in the case when both edges are overlapping a certain risk exists that the Blocking Oscillator is not triggered properly and a distorted output pulse is issued. This uncertain time slot was assumed with 20 ns in the worst-case. Since the likelihood for that incidence amounts to $2 \cdot 10^{-4}$ (=0.020 µs/89 µs) this fact is neglected for the prototype. The final device must issue a proper pulse at every time and condition. Therefore certain thresholds must be foreseen to avoid such faults due to overlapping.

The reliability properties of this circuit are excellent, galvanic decoupling and series transistors maintain failsafe operation in all conditions. A spontaneous asynchronous beam dump is only possible if either T1 is short-circuited and T2 switches on or T3 gets a short-circuit while T2 is conducting. Both possibilities are very unlikely because for such a failure within a transistor both the base-emitter and the collector-base-diode must be short-circuited at the same time.

The functionality of the Output Trigger Gate was proven by a simulation with MicroSim® Pspice. The detailed calculations and the component values for this unit can be found in Appendix E.

3.3. Peripheral functions

The peripheral circuits comprise the internal reference oscillator, the configuration electronics for the FPGA, the power supply, the protection circuits, the driver and buffer circuits and the power supply voltage surveillance.

All these functions are only roughly explained because all parts are commercial available and often used. For details please refer to the specific datasheets.

3.3.1. Internal Reference Oscillator

Since all critical timing systems are implemented digitally the only determinative factor for the accuracy of the Trigger Generator is the internal reference oscillator. In particular the operation of two subunits is affected:

- Oscillator Unit
- Timing Unit

The oscillator principle was chosen in view of meeting the requirements for both units. Only quartz crystal oscillators were taken into account, Rubidium and Caesium-standards would be too expensive and additionally not necessary, and RC- or LC-oscillators contain too many components and are not stable and precise enough.

Since the oscillation frequency of a crystal oscillator is only determined by the cut, size and shape of the resonator, it is very insensitive to disturbance factors like temperature changes, supply voltage deviations and maintains an excellent long-term stability. Additionally it is a relatively inexpensive method of obtaining accurate frequency references.

Three main factors affect the oscillation frequency of a crystal oscillator, other influences like short-term fluctuations are so small that they were neglected:

1. The major disturbance parameter influencing the crystal frequency is a **change in temperature.**
2. The second largest source of frequency deviations is **aging**, which is caused by the change of the physical properties of the crystal mounting or of the quartz itself.
3. **Fluctuations of the line voltage** of the crystal power supply also affect the oscillation frequency.

All time errors due to these main disturbance factors were calculated for both Oscillator Unit and Timing Unit. This was then the base for the choice of the suitable oscillator. The data for the following analysis were taken from the application note *"Fundamentals of Quartz Oscillators"* from *Hewlett-Packard* [12].

There are three different crystal oscillator configurations that are used for reference sources:

a. **RTXO** (Room Temperature Crystal Oscillator): Special crystal cuts are used to maintain a minimum frequency change over temperature.
b. **TCXO** (Temperature Compensated Crystal Oscillator): Special components outside of the crystal are used to compensate temperature effects.
c. **OCXO** (Oven Controlled Crystal Oscillator): The crystal and temperature sensitive elements are placed within a temperature-controlled oven. Since the OCXO entails the risk that the heating fails and as a result the oscillator looses its stability, it should not be considered for this application.

Table 4 contains the typical specifications for each of the three oscillator types that are the base values for the calculation of the time errors. These figures represent the fractional change of frequency (Δf/f) relating to the given base.

Fractional change of frequency F	Base	RTXO	TCXO	OCXO
Temperature	0°C-50°C	$<2.5 \cdot 10^{-6}$	$<5 \cdot 10^{-7}$	$<7 \cdot 10^{-9}$
Aging	per month	$<3 \cdot 10^{-7}$	$<1 \cdot 10^{-7}$	$<1.5 \cdot 10^{-8}$
Line Voltage	10% change	$<1 \cdot 10^{-7}$	$<5 \cdot 10^{-8}$	$<1 \cdot 10^{-10}$

Table 4: Typical specifications of the three crystal configurations [12]

For the calculation of the frequency drift due to aging the minimum lifetime of the Trigger Generator was assumed with 10 years.

Oscillator Unit

This unit contains a Frequency-Locked loop, which phase detector and NCO's are clocked by the reference oscillator. Since the loop continuously adapts itself to maintain frequency lock, changes of the reference oscillator frequency are automatically compensated.

The only problem, which can arise, is running-out of the narrow working range (see Figure 13). If it is assumed that the oscillator oscillates exactly at 100 MHz the distance to the upper boundary is 7.8 Hz, to the lower one 16 Hz. With the working point frequency of 11245.5 Hz the corresponding fractional frequency errors (F=Δf/f) equal to +694 ppm and to –1422 ppm.

Table 5 shows the drift of the working point due to the three main disturbance factors.

Change of working point	Base	RTXO	TCXO	OCXO
Temperature	0°C-50°C	<28 mHz	<5.6 mHz	<0.78 mHz
Aging	10 years	<404 mHz	<134 mHz	<20 mHz
Line Voltage	10% change	<1 mHz	<0.56 mHz	<0.001 mHz
Worst-case-sum		<433 mHz	<140 mHz	<20.8 mHz
Worst-case-sum	ppm	+38	+12.5	+1.8

Table 5: Drift of the Oscillator Unit-NCO's

It follows that each of the three crystal configurations would provide sufficient stability.

Another important point for correct function of the Oscillator Unit is the initial oscillation frequency of the crystal. The borders for the maximal deviation were stated at ±100 ppm (that means ±10 kHz for the 100 MHz oscillator). Nearly every commercial crystal oscillator maintains a lower initial accuracy.

Timing Unit

This unit generates a delay of a certain length by counting of reference clock cycles. Therefore every change of the reference oscillator frequency causes a delay time error. Table 6 shows the delay time deviation caused by the different disturbance factors for each of the three oscillator configurations. The calculated time deviation equals to

$$\Delta T = T_{Delay\ max} \cdot \left(\frac{-F}{F+1} \right) \tag{20}$$

The base for the calculation was the longest necessary delay $T_{delaymax}$=88.92 µs.

Delay time deviation ΔT	Base	RTXO	TCXO	OCXO
Temperature	0°C-50°C	-222 ps	-44ps	-0.6ps
Aging	10 years	-3.2 ns	-1.1 ns	-160 ps
Line Voltage	10% change	-8.9 ps	-4.45 ps	-0.008 ps
orst-case-sum		-3.43 ns	-1.15 ns	-160.6 ps

Table 6: Delay time error of the Timing Unit

Referring to the tolerance distribution between the subunits (Figure 21) the negative drift of the delay due to temperature fluctuations, aging and supply voltage changes can be tolerated. The only effect is in the worst-case the abridgement of the free-running-time of the Oscillator Unit by

$$\frac{\Delta T}{20ns} \cdot 100\%$$

If a RXCO is used this would be a reduction from 100 cycles to 83 cycles after 10 years. Since the maximal necessary free-running-cycles are defined with 5 this reduction is accepted. Additionally the Timing Unit entails the possibility to readjust the delay by increasing of the programmed IDP-value.

Conclusion

The analysis of the influence of internal oscillator instabilities on the overall behaviour of the Trigger Generator revealed that in view of timing and frequency requirements a

RTXO is sufficient for this application.

Nevertheless also the reliability aspect must be considered. The failure rate λ_p of a quartz oscillator equals to

$$\lambda_P = \lambda_b \cdot \pi_Q \cdot \pi_E \tag{21}$$

where $\lambda_b = 0.013 \cdot (f)^{0.23}$ (f…frequency in MHz), π_Q=2.1 for commercial components and π_E=2.6 for installations in permanent racks [13]. Thus the failure rate for the used 100 MHz oscillator is 205 FIT's (failures in time per 10^9 hours), which is more than sufficient for this application.

3.3.2. Configuration electronic for the FPGA

Configuration is the process of loading the programming data into the FPGA to define the functional operation of the internal blocks and their interconnections. Every time the power supply is switched on the data is serially loaded from the Configuration PROM (in this case the XQ1701L from XILINX®) into the FPGA-chip. This loading process needs its own clock frequency of 10 MHz, which is generated by dividing the 100 MHz internal reference clock by 10. For more details about the configuration electronic please refer to the XILINX®Application Notes and Data Sheets [10], [14] and [15].

3.3.3. Power supply

Three different voltages are needed on the Trigger Generator PC-board:

- 3.3V for the power supply of the XILINX®-chip
- 5V for the drivers and
- 15V for the output power part

Due to simplicity the prototype has only two terminals for +15V and GND, fixed voltage regulators derive all other voltages directly on the PC-board. During the choice of the regulators and the heat sinks attention must be paid to the quite high current consumption of the different circuits.

3.3.4. Protection circuits

The Trigger Generator contains a lot of electronic that is sensitive to excess voltage. Electrostatic discharge or a wrong connected cable can cause the total destruction of

the entire PC-board.

For that reason clamping diodes to 5 V and GND, like in CMOS-IC's, are installed at each input and output that is connected to a logic device.

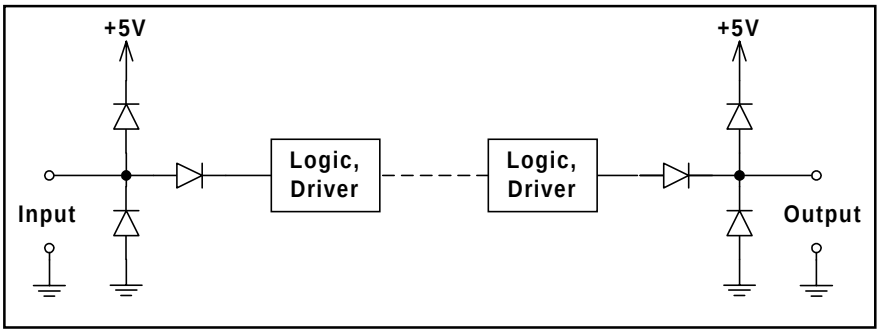

Figure 31: Input/Output-Protection circuits

Figure 31 shows the input / output-protection circuit. If the voltage at one pin exceeds 5.7 V or falls below –0.7 V these diodes get into conduction and drain away the hazardous voltage. Additionally series diodes (Schottky-diodes U_f=0.3 V) prevent damage caused by input signals with wrong polarity.

Fast diodes that are capable of conducting the current should be used to block the hazardous signals from the logic circuits.

3.3.5. Driver circuits

Although the FPGA is capable to drive currents up to 24 mA most of the measuring and signal outputs are additionally buffered. This has as purpose to avoid damage to the expensive FPGA-chip caused by faults during the measuring and test phase of the prototype. Drivers are necessary for the following signals:

OSYTRTIM, OFINT, OSUR0-OSUR11, ISUR0-ISUR1, IOSC, ISYNC, OSYNCTIM, ISYNC_FAULT, OSYNC_FAULT, OSYNC, OOSC, ODRO0-ODRO13, ITIM.

Each driver that drives a measuring output for an oscilloscope (OFINT, OSYTRTIM, OSYNCTIM) has a 450 Ω-resistor in series to get a divide by 10 output at 50 Ω. All inputs have a resistor of 1 kΩ in parallel to GND.

Further drivers are necessary for the signals of the Output Trigger Gate, in particular for the amplification of OSYTR to provide enough current for the delay line at T3, for the buffering of DR to maintain the base current for T2 and for the pick-up of SUR_TRGATE.

Thus 41 drivers and buffers are necessary. A recommendation for the driver circuits is either the 74F757, which is an open-collector octal buffer with a maximal low-level

current of 64mA, or the 74F832, which is a Hex 2-input OR-driver with a maximum output current of ±64mA. Both are compatible to the 3.3 V logic levels of the FPGA-chip, but the '832 has a better propagation delay of 3.5ns compared to 9ns of the '757 (values for PHILIPS components).

3.3.6. Supply voltage surveillance

Supply voltage deviations can cause unforeseen circuit failures that must be avoided. For that reason each power supply line is supervised by a voltage watchdog. It issues a signal to the Surveillance System if a voltage falls below the nominal value minus 10%, i.e. 3 V for the 3.3 V-line, 4.5 V for the 5 V-supply and 13.5 V in case of 15 V. The supply surveillance status bits (SUR_PS3V3, SUR_PS5V and SUR_PS15V) go to 0 if any of these voltages falls under one of these limits.

For the detection of the voltage deviations, the µP-Supervisory circuit MAX707 from MAXIM is used. Its $\overline{\text{RESET}}$-output goes to 0 if the supply voltage drops below 4.65 V and its $\overline{\text{PFO}}$-output goes to 0 if the PFI-input falls below 1.25 V. That means one MAX707 can supervise the 5 V-line and by adding a potential divider simultaneously also the 3.3 V. A second MAX707 combined with a potential divider supervises the 15 V-line voltage.

4. Technical conclusion

The Oscillator Unit, which represents the most critical part within the Trigger Generator module, is realised very simple compared to its properties. Using only a small part of the overall tolerance range of the Trigger Generator (only 40 ns) it provides a very good maximal free-running time of 8.9 ms (~100 beam cycles). Although only 5 cycles necessary free-running time were assumed a comparison of all possible digital principles revealed that no other method can fulfil this requirement within the defined tolerance range. That means additionally for all other parts a wider tolerance range, which makes the operation of the Trigger Generator safer and more reliable. A first estimation revealed that the proposed circuit fulfils the reliability requirements and maintains a sufficient failure rate.

The surveillance functions were chosen in the way that almost every failure is early detectable to prevent disastrous consequences.

C. Conclusion

1. Final remarks

The design steps in this paper followed a preceding investigation and selection process, where in each case the most adequate principle had been chosen. The final concept for the prototype of the Trigger Generator fulfils all requirements and specifications made for this project. The PC-board design based on this concept is relatively uncritical. Except for the internal reference oscillator, no high-frequency signals are used, only the rise time specifications must be maintained.

Before the final PC-board will be designed the actual components availability must be checked to include circuit modifications for the use of more recent components.

In the test stage the Trigger Generator prototype will provide valuable information about requirements, problems and for sure solutions for the final installation of the trigger generation system for the LHC beam dump kicker magnets in 2004.

The techniques and principles described in this paper are based on the current state-of-the-art in electronics. The fast developing electronic sector will maybe provide better opportunities in the future for the realisation of the Trigger Generator. Additionally the dynamic design process of the Large Hadron Collider necessitates continuous adaptations of the requirements, which significantly influences the circuit design of the Trigger Generator.

The prototype will serve as a base for the final design and will help to understand the critical processes within this system.

2. Acknowledgments

I would like to thank Johan Dieperink for his valuable help and advice during the preparation of this project. His big experience and repertoire of ideas was always an important support for my work.

3. List of abbreviations

The following list contains the abbreviations used in the text of this paper in order of appearance. Abbreviations that are used in formulas are explained there.

LHC	Large Hadron Collider
CERN	Organisation Européenne pour la Recherche Nucléaire European Organisation for Nuclear Research
PC-board	Printed Circuit-board
LEP	Large Electron-Positron Collider
SPS	Super Proton Synchrotron
RF	Radio-Frequency
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
PLL	Phase-Locked-Loop
RFM	Revolution Frequency Measurement
NCO	Numerical Controlled Oscillator
MSB	Most Significant Bit
FRC	Free-Running-Cycles
DIP	Dual-In-line-Package
RTXO	Room Temperature Crystal Oscillator
TCXO	Temperature Compensated Crystal Oscillator
OXCO	Oven Controlled Crystal Oscillator
ppm	part per million ($x10^{-6}$)
FIT	Failures In Time (failures per 10^9 hours)
IC	Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor

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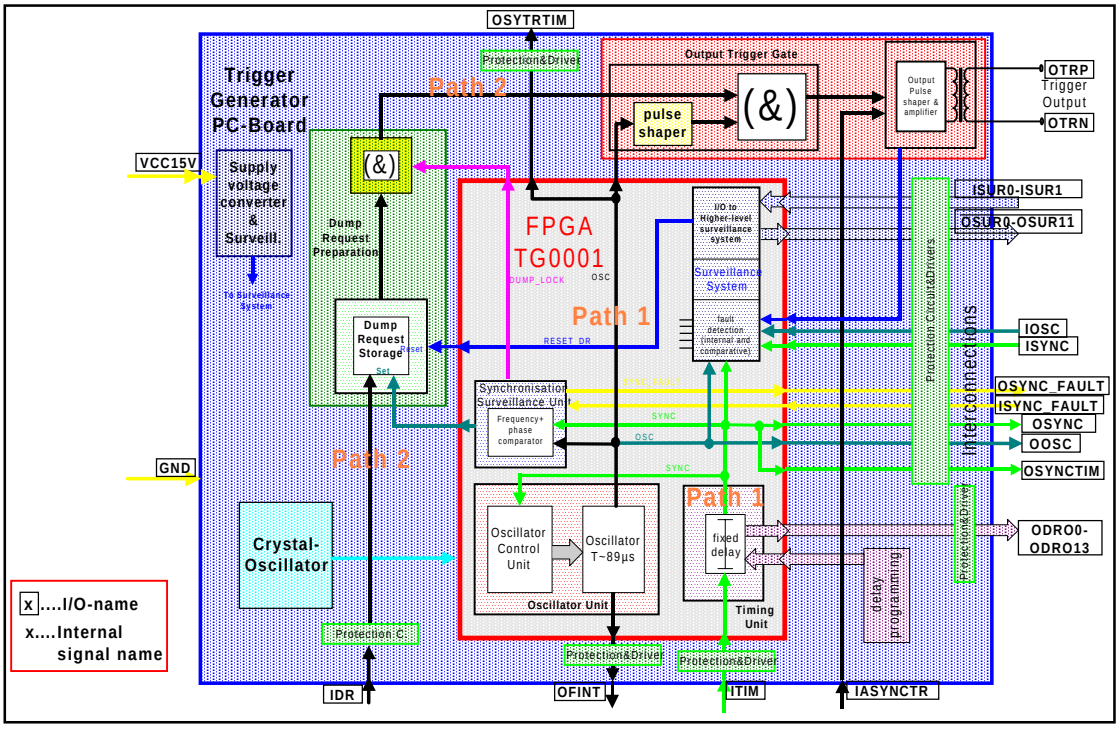
Appendix A: Data sheet Trigger Generator module

1. General Description

The Trigger Generator module contains all functions that are described in this paper. This part provides the exact input/output-specifications to connect this module to the environment.

- ♦ Environment temperature: 0°-75°C
- ♦ Mounting: Rack in the equipment tunnel of LHC at IP6 (Prototype in laboratory rack)
- ♦ Supply voltage: +15 V
- ♦ Supply current: max. ~1 A
- ♦ Rise time of the inputs: <10 ns

2. Pin configuration



Since the size and type of the Trigger Generator PC-board has not been specified yet, the pins are only assigned functionally, but not geometrically.

3. Pin specifications

The following part describes mainly the electrical characteristics of the inputs and outputs, the function of each pin is only outlined. For a detailed description refer to the specific parts of this paper.

Input pins: (Naming convention: All input pin names start with an I)
The following signal inputs are TTL(LVTTL)-compatible.

Symbol	Parameter	limits
V_{IH}	High-level input voltage	min. 2.0 V
V_{IL}	Low-level input voltage	max. 0.8V
V_{OH}	High-level output voltage	min. 2.4 V
V_{OL}	Low-level output voltage	max. 0.4 V

The drivers maintain a maximal input current of ±20 µA. The protection circuits decrease the input voltage by 0.3 V.

ITIM — Input Timing
Connected via the Protection and driver circuit with the ITIM input of the TG0001 chip. A 1kΩ-resistor is connected in parallel to GND.

ISYNC_FAULT — Synchronisation fault input
Connected via the Protection and driver circuit with ISYNC_FAULT of the TG0001 chip. A 1kΩ-resistor is connected in parallel to GND.

ISYNC — Synchronisation input
Connected via the Protection and driver circuit with ISYNC of the TG0001 chip. A 1kΩ-resistor is connected in parallel to GND.

IOSC — Oscillator Unit input
Connected via the Protection and driver circuit with IOSC of the TG0001 chip. A 1kΩ-resistor is connected in parallel to GND.

ISUR0-ISUR1 — Surveillance input

Connected via the Protection and driver circuit with ISUR0-ISUR1 of the TG0001 chip. 1kΩ-resistors are connected in parallel to GND.

IDR — Dump request input

Connected via the Protection circuit to the set input of the Dump Request Storage. A 1kΩ-resistor is connected in parallel to GND.

IASYNCTR — Asynchronous dump trigger input

A signal V>5 V (max. 15 V) and I~50 mA triggers directly an asynchronous beam dump. This input is not protected.

VCC15V — Supply input +15 V

GND — Ground connection

0 V reference for all signals

Output pins: (Naming convention: All output pin names start with an O)

OTRP, OTRN — Dump Trigger output

This output delivers nominally 15 V and 100 mA pulses on a 150 Ω-termination. This output is galvanic decoupled and floating. The maximal deviation from the load specifications without significant influence on the pulse properties is ±25 %.

OTRP is the positive and OTRN the negative terminal.

The following outputs (OSYNC_FAULT, OSYNC, OOSC) are surveillance interconnections to the parallel redundant Trigger Generator. The TTL-outputs can drive ±64 mA.

OSYNC_FAULT — Synchronisation fault output

OSYNC_FAULT of the TG0001 chip controls this output via the Protection and driver circuit.

OSYNC — Synchronisation output

OSYNC of the TG0001 chip controls this output via the Protection and driver circuit.

OOSC — Oscillator Unit output

OOSC of the TG0001 chip controls this output via the Protection and driver circuit.

The following outputs (OSYTRTIM, OFINT, OSYNCTIM) make it possible to investigate internal signals for test purposes. The TTL-outputs of the drivers have a 450 Ω-resistor in series, i.e. the potential is divided by 10 on 50 Ω. The maximal current of these outputs is ±64 mA.

OSYTRTIM — Synchronised Trigger Timing output

Connected via the Protection and driver circuit to the OSYTRTIM pin of the TG0001 chip.

OFINT — Revolution Frequency measurement output

Connected via the Protection and driver circuit to the OFINT pin of the TG0001 chip.

OSYNCTIM — Synchronisation Timing output

Connected via the Protection and driver circuit to the OSYNCTIM pin of the TG0001 chip.

The following bit lines (OSUR0-OSUR11, ODRO0-ODRO13) provide information about the current status of the Trigger Generator module to the higher-level Surveillance System. The TTL-outputs of the drivers can provide ±64 mA.

OSUR0-OSUR11 — Surveillance System output

Connected via the Protection and driver circuit to OSUR0-OSUR11 of the TG0001 chip.

ODRO0-ODRO13 — Delay Read Out output

Connected via the Protection and driver circuit to ODRO0-ODRO13 of the TG0001 chip.

Appendix B: Data sheet Trigger Generator FPGA-chip TG0001

1. General Description

For the TG0001-FPGA chip a XILINX® XC4044XLA-speed grade 08 is used. Since the chip works at its maximum speed, maximal 20% of the 3800 logic cells are used. The package can be chosen dependent on the availability of the chip but should be as small as possible. For the simulations and first implementation a HQ160 package was assumed.

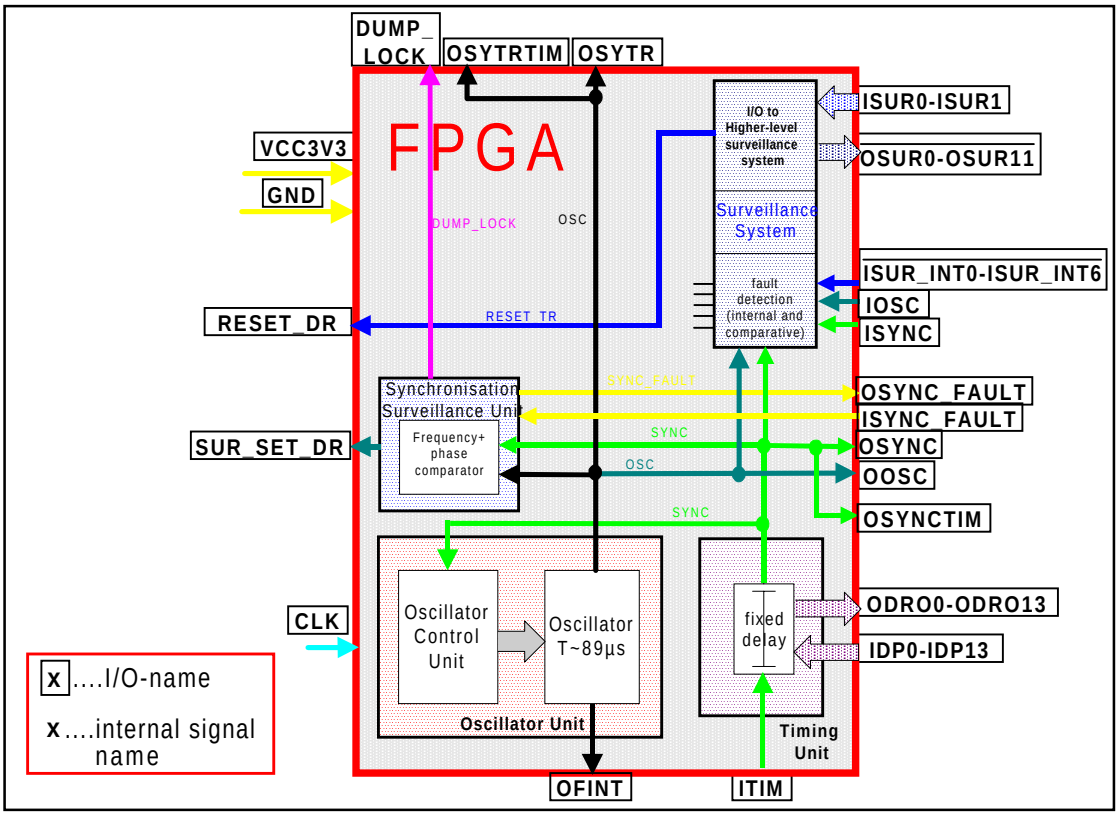
The TG0001 comprises all important timing and surveillance functions of the Trigger Generator (for further details please refer to chapter B.2), but maintains a failure rate similar to a single gate.

- Clock frequency: 100 MHz ±100 ppm
- Rise times at Inputs: < 10 ns
- Rise times at the outputs: < 5 ns (at C=50 pF)
- Environment temperature: 0°C-75°C
- Cooling: convection cooling with heatsink
- Supply voltage V_{CC}: 3.3 V ±10%
- Estimated supply current at full operation: ~250 mA
- All inputs and outputs are TTL(LVTTL)-compatible:

Symbol	Parameter	limits
V_{IH}	High-level input voltage	min. 2.0 V
V_{IL}	Low-level input voltage	max. 0.8V
V_{OH}	High-level output voltage	min. 2.4 V
V_{OL}	Low-level output voltage	max. 0.4 V

- Maximum output current: ±24 mA
- All FPGA-pins can only withstand voltages from –2.0 V until +7.0 V, i.e. hazardous voltages must be blocked before.

2. Pin configuration TG0001



The functional pins are not geometrically assigned to the pins of the FPGA chip (=pin-lock), because changes of the package and the circuit design or speed improvements during the design of the schematics will influence the pin assignment significantly. All mentioned signals are digital TTL-square pulses.

3. Pin description

Input pins: (Naming convention: All input pin names start with an I)

ITIM — Input Timing

This input delivers the base information about the current beam revolution frequency and the position of the beam gap. Each rising edges triggers the delay cycle of the Timing Unit. The time position of ITIM plus this delay results to the nominal time position of OSYTR. The allowed frequency range reaches from 11229.5 Hz to 11253.3 Hz.

IDP0-IDP13 — Delay programming input

The value of this 14-bit word multiplied with the time period of the clock CLK equals to the Timing Unit delay. IDP0-IDP13 are not registered, i.e. it is not allowed to change the value, when the device is in operation.

ISYNC_FAULT — Synchronisation fault input

This input reads the synchronisation fault output bit of the parallel Trigger Generator and issues together with the SYNC_FAULT bit internally the following actions:

SYNC_ FAULT	ISYNC_ FAULT	Status	Action
0	0	Timing is failing	SUR_SET_DR=1 after 5 cycles
0	1	own oscillator fails	DUMP_LOCK=0
1	0	parallel device fails	SUR_SET_DR=1 immediately
1	1	all OK	nothing

ISYNC — Synchronisation input

If the time difference between ISYNC and the internal Timing Unit signal SYNC exceeds ±20 ns then TIM_FAULT (=OSUR0) goes from 1 to 0. ISYNC must be connected to the OSYNC output of the parallel Trigger Generator.

IOSC — Oscillator Unit input

If the time difference between IOSC and the internal Oscillator Unit signal OSC exceeds ±50 ns then OSC_FAULT (=OSUR1) goes from 1 to 0. IOSC must be connected to OOSC of the parallel Trigger Generator.

ISUR_INT0-ISUR_INT6 — Internal Surveillance bits

ISUR_INT0: If this bit goes to 1 a normal dump request (Trigger Request Storage is set) is indicated to the surveillance system (OSUR5 goes to 1).

ISUR_INT1: If this bit goes to 1 a successful dump trigger via the OTRP, OTRN output of the Trigger Generator is indicated to the Surveillance system (OSUR6 goes to 1).

ISUR_INT2: If this bit goes from 1 to 0 a voltage deviation of the 3.3 V power supply of more than ±10 % is indicated to the Surveillance system (OSUR7 goes to 0).

ISUR_INT3: If this bit goes from 1 to 0 a voltage deviation of the 5 V power supply of more than ±10 % is indicated to the Surveillance system (OSUR8 goes to 0).

ISUR_INT4: If this bit goes from 1 to 0 a voltage deviation of the 15 V power supply of more than ±10 % is indicated to the Surveillance system (OSUR9 goes to 0).

ISUR_INT5: Reserved for additional surveillance function during the prototype test stage (connected via a storage Flip-Flop to OSUR10).

ISUR_INT6: Reserved for additional surveillance function during the prototype test stage (connected via a storage Flip-Flop to OSUR11).

ISUR0-ISUR1 Surveillance input (level-dependent input)

ISUR0: If ISUR0 goes to 1 (beam dump was successfully executed) RESET_DR is immediately set to clear the Dump Request Storage.

ISUR1: If ISUR1 goes to 1 (all surveillance status bits were read out and are not more needed) all surveillance storage Flip-Flops are cleared immediately.

If both ISUR0 and ISUR1 are active at the same time all Trigger Generator systems are reset and restarted.

CLK Clock input

This pin is connected to the Global Clock Buffer of the FPGA-chip and drives all logic operations. Must be 100 MHz ± 100ppm.

VCC3V3 Supply input +3.3 V

GND Ground connection

0 V reference for all signal

Output pins: (Naming convention: All output pin names start with an O)

OSYTR — Synchronised Trigger output

This signal is always generated (even if ITIM fails) and is synchronous with the ITIM signal delayed by the programmed Timing Unit delay. This signal is the base for the synchronisation of the beam dumping action with the gap in the LHC beam.

The possible frequency range where the Oscillator Unit is able to lock reaches from 11229.5 Hz to 11253.3Hz.

OSYTRTIM — Synchronised Trigger Timing output

Same signal as OSYTR but for measuring purposes.

DUMP_LOCK — Internal Dump request lock output

If the Synchronisation Surveillance detects an internal system failure then DUMP_LOCK goes from 1 to 0, which locks the dump request path. This signal must be connected to the Dump Request Preparation unit.

RESET_DR — Reset Dump Request

If ISUR0 goes to 1 RESET_DR goes immediately to 1. This output must be connected to the reset-pin of the Dump Request Storage.

SUR_SET_DR — Surveillance Set Dump Request

This output gets 1 the Synchronisation Surveillance Unit requests a beam dump. SUR_SET_DR must be connected to the set-pin of the Dump Request Storage.

OFINT — Revolution Frequency Measurement output

The output signal of the RFM-Phase-Locked Loop is issued via OFINT for measurement purposes.

ODRO0-ODRO13 — Delay Read Out output

The programmed IDP-value is directly issued via this bus.

OSYNC — Synchronisation output

ITIM delayed by the Timing Unit (internal SYNC signal) is issued for surveillance purposes. OSYNC must be connected to ISYNC of the parallel Trigger Generator via a driver circuit.

OSYNCTIM — Synchronisation Timing output

The same signal as OSYNC but for measuring purposes.

OOSC — Oscillator Unit output

The internal Oscillator Unit signal OSC is issued for surveillance purposes. OOSC must be connected to IOSC of the parallel Trigger Generator via a driver circuit.

OSYNC_FAULT — Synchronisation Fault output

If the Synchronisation Surveillance Unit detects an internal timing fault OSYNC_FAULT goes from 1 to 0. This output must be connected to ISYNC_FAULT of the parallel Trigger Generator via a driver circuit and is part of the mutual surveillance of both Trigger Generators.

OSUR0-OSUR11 — Surveillance System output

This output is connected via driver circuits to the higher-level Surveillance System and provides information about the current status of the Trigger Generator device to the environment.

OSUR0: If the Surveillance System detects a time deviation between SYNC and ISYNC of more than ±20 ns then OSUR0 (=TIM_FAULT) goes from 1 to 0.

OSUR1: If the Surveillance System detects a time deviation between OSC and IOSC of more than ±50 ns then OSUR1 (=OSC_FAULT) goes from 1 to 0.

OSUR2: If the Synchronisation Surveillance Unit detects an internal synchronisation fault then OSUR2 (=SYNC_FAULT) goes from 1 to 0.

OSUR3: OSUR3 is set, when the dump request path is locked due to an internal synchronisation fault (=DUMP_LOCK).

OSUR4: If the Synchronisation Surveillance Unit triggers a dumping action then this output goes to 1. (=SUR_SET_DR).

OSUR5: see ISUR_INT0

OSUR6: see ISUR_INT1

OSUR7: see ISUR_INT2

OSUR8: see ISUR_INT3

OSUR9: see ISUR_INT4

OSUR10: see ISUR_INT5

OSUR11: see ISUR_INT6

Appendix C1: Mathematical treatment of the Oscillator Unit

Appendix C refers mostly to chapter B.2.1.1 Oscillator Unit, Revolution frequency measurement. All calculations were made with Mathcad 6.0 on the base of the designed Trigger Generator circuit. These calculations are part of the proof for the correctness and feasibility of the intended realisation.

1. Stability check with z-unity circle

$kPLL := 18.43\,10^{-3}$ PLL-constant (see B 2.1.1)

$CL(z) := \frac{kPLL \cdot (z - 1)}{z^2 + z \cdot (kPLL - 2) - kPLL + 1}$ Transfer function of the PLL (see B 2.1.1)

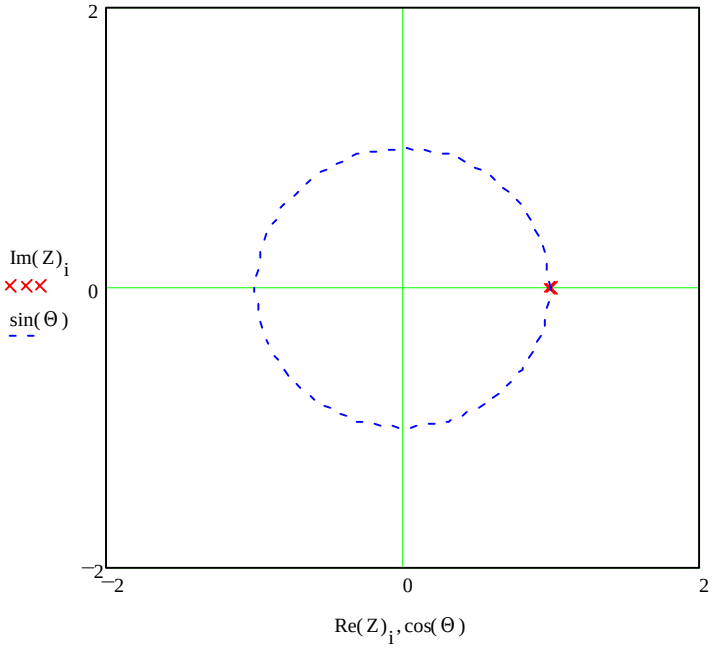
$z^2 + z \cdot (kPLL - 2) - kPLL + 1 = 0$ Characteristic equation

$Z := \begin{pmatrix} 1 \\ -kPLL + 1 \end{pmatrix}$ Roots of the characteristic equation

$Z = \begin{pmatrix} 1 \\ 0.982 \end{pmatrix}$

$i := 0 .. length(Z) - 1$

$\Theta := 0, 0.1 \cdot \pi .. 2 \cdot \pi$



Poles within the z-unit circle:

Both poles are either within or directly on the z-unit circle

=> PLL-loop is stable

2. Root-Locus diagram

The Root-Locus diagram provides the allowed range of the system constant k_{PLL} where the feedback-loop is stable. The calculation method was taken from the Mathcad Electronic Book “Theory and Selected Problems of Feedback and Control Systems”, 2nd edition, Schaum’s Outlined Series.

$z^2 + z\cdot(K-2) - K + 1 = 0$ Characteristic equation

$n := 2$ Order of the equation

$j := 0..n-2$

$C_{j+1,j} := 1$ Subdiagonal identity matrix C

$coeff(K) := \begin{pmatrix} 1-K \\ K-2 \end{pmatrix}$ Definition of coefficients

$k := 0..n-1$

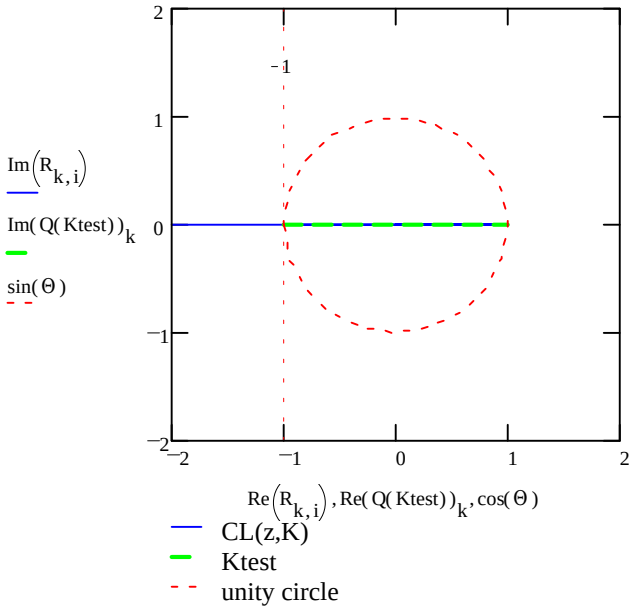
$A := 1$ Coefficient of the highest-order term

$imax := 600$ $Kmax := 3$ Vector of K

$i := 0..imax$ $K_i := \frac{i}{imax}\cdot Kmax$

$R^{<i>} := eigenvals\left(augment\left(C, \frac{-coeff(K_i)}{A}\right)\right)$ Numerical solution for the roots

$Q(K) := eigenvals\left(augment\left(C, \frac{-coeff(K)}{A}\right)\right)$ Definition of test function



$\Theta := -\pi, -.9\cdot\pi .. \pi$ $Ktest := 2$

The maximum allowed PLL-constant k_{PLLmax}=2.

3. Impulse Response

The impulse response shows the behaviour of the PLL-feedback loop, when a phase step is applied to the SYNC-input.

$$CL(z) = \frac{kPLL \cdot (z-1)}{z^2 + z\cdot(kPLL-2) - kPLL + 1}$$ Transfer function of the PLL

$$X(z) := \frac{z}{z-1} \qquad Y(z) := CL(z)\cdot X(z)$$ Phase step

$$Y(z) = \frac{kPLL \cdot (z-1)}{z^2 + z\cdot(kPLL-2) - kPLL + 1} \cdot \frac{z}{z-1}$$

$$Y(z) = z\cdot\frac{kPLL}{((z-1)\cdot(z+kPLL-1))}$$

$$Y(z) = z\cdot\frac{kPLL}{\left(z^2 + z\cdot kPLL - 2\cdot z - kPLL + 1\right)}$$

$$\frac{Y(z)}{z} = \frac{kPLL}{((z-1)\cdot(z+kPLL-1))}$$

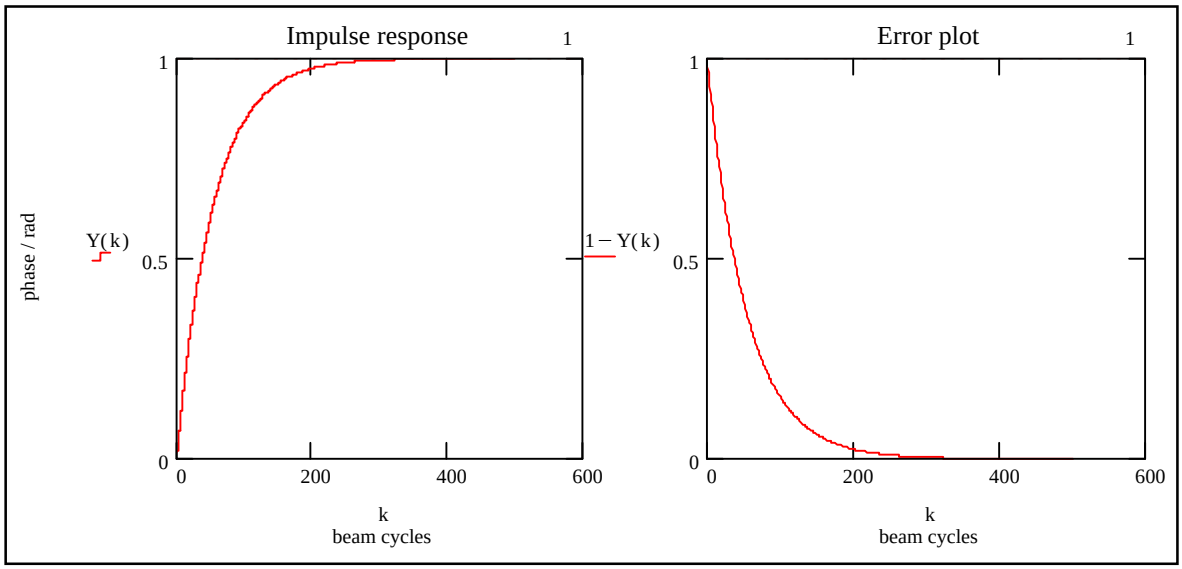
$$\frac{Y(z)}{z} = \frac{1}{(z-1)} - \frac{1}{(z+kPLL-1)}$$ Partial fraction

$$Y1(z) = \frac{z}{z-1} \qquad Y2(z) = \frac{z}{(z+kPLL-1)}$$

$$invztrans(Y1(z), z, n) = 1 \qquad invztrans(Y2(z), z, n) = (-kPLL+1)^n$$ Inverse z-Transform

$$Y(k) := 1 - (1-kPLL)^k$$ Impulse response in the time-domain

$$k := 1..500$$



4. Ramp Response

The Ramp Response shows the reaction of the PLL in case a frequency-step is applied to SYNC. In the calculation the maximum possible

$$\Delta\omega_{SYNC}=100.54\ \frac{1}{s}$$

was assumed, which equals to the step from the lower boundary of the RFM-NCO to the highest possible beam revolution frequency. This frequency step has to be compensated when the RFM-PLL locks onto the SYNC signal.

$T := 88.92\cdot10^{-6}$ $\Delta\omega\ max := 100.54$ Max. frequency-step during lock-in

$$X(z)=\frac{T\cdot\Delta\omega\ max\cdot z}{(z-1)^2}$$ Frequency offset

$$CL(z)=\frac{kPLL\cdot(z-1)}{z^2+z\cdot(kPLL-2)-kPLL+1}$$ $Y(z) := CL(z)\cdot X(z)$ Transfer function of the PLL

$$Y(z)=\left[\frac{kPLL\cdot(z-1)}{z^2+z\cdot(kPLL-2)-kPLL+1}\right]\cdot\frac{T\cdot\Delta\omega\ max\cdot z}{(z-1)^2}$$

$$Y(z)=kPLL\cdot T\cdot\Delta\omega\ max\cdot\frac{z}{\left[(z-1)^2\cdot(z+kPLL-1)\right]}$$

$$\frac{Y(z)}{z}=kPLL\cdot T\cdot\Delta\omega\ max\cdot\frac{1}{\left[(z-1)^2\cdot(z+kPLL-1)\right]}$$

$$\frac{Y(z)}{z}=\frac{-1}{kPLL}\cdot T\cdot\frac{\Delta\omega\ max}{(z-1)}+\Delta\omega\ max\cdot\frac{T}{(z-1)^2}+\frac{1}{kPLL}\cdot T\cdot\frac{\Delta\omega\ max}{(z+kPLL-1)}$$

$$Y1(z)=\frac{-1}{kPLL}\cdot T\cdot\frac{\Delta\omega\ max\cdot z}{(z-1)}$$ $$Y2(z)=\Delta\omega\ max\cdot\frac{T\cdot z}{(z-1)^2}$$

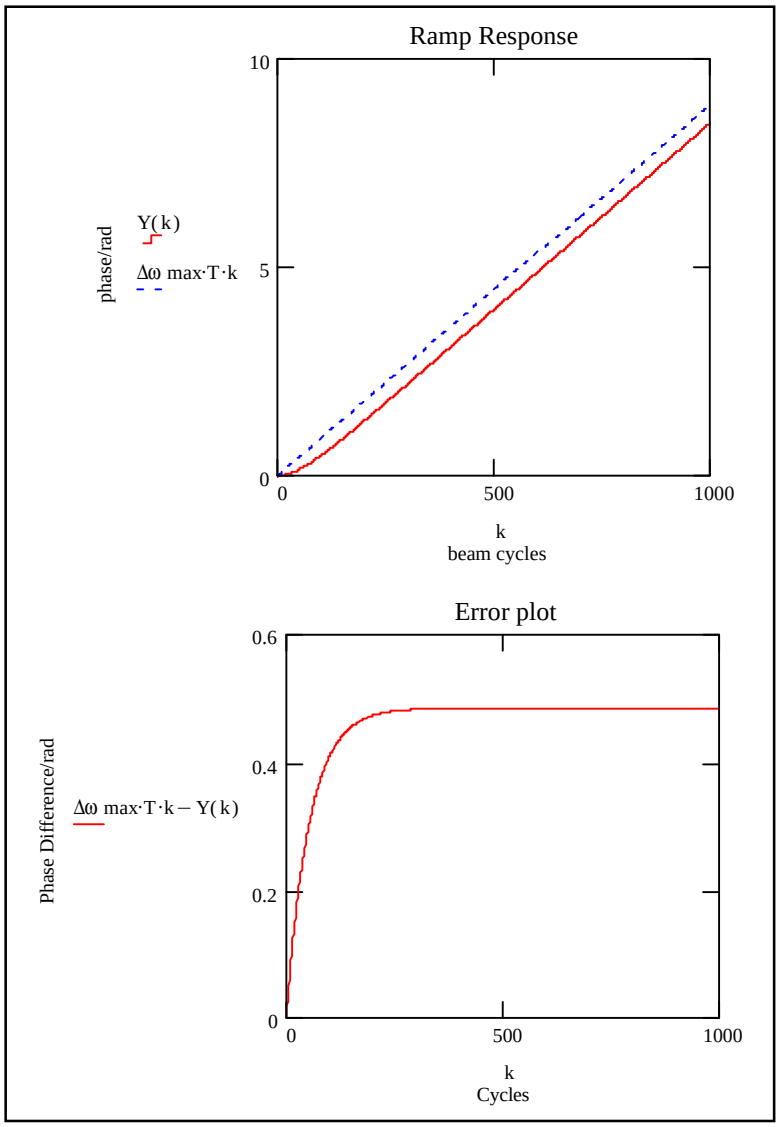
$$invztrans(Y1(z),z,n)=\frac{-1}{kPLL}\cdot T\cdot\Delta\omega\ max$$ $$invztrans(Y2(z),z,n)=\Delta\omega\ max\cdot T\cdot n$$

$$Y3(z)=\frac{1}{kPLL}\cdot T\cdot\frac{\Delta\omega\ max\cdot z}{(z+kPLL-1)}$$ Inverse z-Transform

$$invztrans(Y3(z),z,n)=\frac{1}{kPLL}\cdot T\cdot\Delta\omega\ max\cdot(-kPLL+1)^n$$

$k := 0..1000$

$$Y(k) := \Delta\omega\ max\cdot T\cdot k+\left[\frac{1}{kPLL}\cdot T\cdot\Delta\omega\ max\cdot(1-kPLL)^k-\frac{T}{kPLL}\cdot\Delta\omega\ max\right]$$ Ramp response in the time-domain



The PLL locks exactly on the frequency, the phase difference is not compensated.

During the lock-in process the phase error grows until the input frequency is reached.

$$E(k) := \Delta\omega_{max} \cdot k \cdot T - \left[\Delta\omega_{max} \cdot T \cdot k + \left[\frac{1}{kPLL} \cdot T \cdot \Delta\omega_{max} \cdot (1 - kPLL)^k - \frac{T}{kPLL} \cdot \Delta\omega_{max} \right] \right]$$

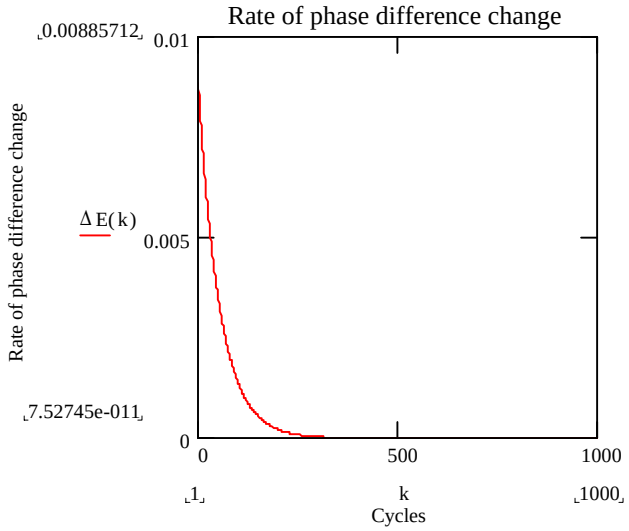
Phase difference SYNC=>FINT

$$\Delta E(k) := \frac{-1}{kPLL} \cdot T \cdot \Delta\omega_{max} \cdot (-kPLL + 1)^k \cdot \ln(-kPLL + 1)$$

First derivation: Rate of change

Final phase difference change rate: $\lim_{k \to \infty} \Delta E(k)$

$\Delta E(\infty) = 0$ => Frequency exactly locked



⇒Phase difference change converges to 0

Cycles needed to maintain frequency lock in the case of the maximum possibly frequency step ω_{minosc}=>ω_{symax}: (Assumption: Δt/cycle = Δtmaxcycle < 1ps)

$\Delta tmaxcycle := 1 \cdot 10^{-12} \cdot sec$ Max. time drift/cycle when locked

$$\Delta Elock := \frac{\Delta tmaxcycle}{T \cdot sec} \cdot 2 \cdot \pi$$

$\Delta Elock = 7.066 \cdot 10^{-8} \cdot rad$

$$\frac{-1}{kPLL} \cdot T \cdot \Delta\omega max \cdot (-kPLL + 1)^{k} \cdot \ln(-kPLL + 1) = \Delta Elock$$

$$kphaselock := floor\left[\frac{\ln\left[-\Delta Elock \cdot \frac{kPLL}{(T \cdot (\Delta\omega max \cdot \ln(-kPLL + 1)))}\right]}{\ln(-kPLL + 1)}\right]$$

$kphaselock = 632$ ⇨ after ~630 cycles the loop shifts only by 1 ps/cycle compared to the input phase

$E(1000) = 0.485$ => phase difference after 1000 cycles

$$\Delta tfstep := \frac{E(1000)}{2 \cdot \pi} \cdot T \cdot sec$$

$\Delta tfstep = 6.865 \cdot 10^{-6} \cdot sec$ => **<u>phase shift due to frequency lock-in</u>** equals to **<u>6.87 µs</u>**

5. Parabolic Response

The parabolic response represents the behaviour of the PLL, when the acceleration ramp (=frequency ramp) of the LHC revolution frequency is applied.

With the acceleration constant of the LHC [1]

$$\tau LHC := 25 \cdot min$$

and the maximal beam revolution frequency change of

$$\Delta fSYNC := 28.06 \cdot 10^{-3} \cdot Hz \qquad \Delta\omega SYNC := 2 \cdot \pi \cdot \Delta fSYNC$$

$$\Delta\omega SYNC = 0.176 \cdot sec^{-1}$$

the applied angular acceleration equals to

$$\alpha := \frac{\Delta\omega SYNC}{\tau LHC} \qquad \alpha = 1.175 \cdot 10^{-4} \cdot sec^{-1}$$

The sampling interval of the PLL is $T := 88.92 \cdot 10^{-6}$.

$$X(z) = \frac{\alpha \cdot T^2 \cdot z \cdot (z+1)}{2 \cdot (z-1)^3}$$ Frequency parabola

$$CL(z) = \frac{kPLL \cdot (z-1)}{z^2 + z \cdot (kPLL - 2) - kPLL + 1} \qquad Y(z) := CL(z) \cdot X(z)$$ Transfer function of the PLL

$$Y(z) = \left[\frac{kPLL \cdot (z-1)}{z^2 + z \cdot (kPLL - 2) - kPLL + 1}\right] \cdot \left[\frac{\alpha \cdot T^2 \cdot z \cdot (z+1)}{2 \cdot (z-1)^3}\right]$$

$$Y(z) = \frac{1}{2} \cdot kPLL \cdot \alpha \cdot T^2 \cdot z \cdot \frac{(z+1)}{\left[(z-1)^3 \cdot (z + kPLL - 1)\right]}$$

$$\frac{Y(z)}{z} = \frac{1}{2} \cdot kPLL \cdot \alpha \cdot T^2 \cdot \frac{(z+1)}{\left[(z-1)^3 \cdot (z + kPLL - 1)\right]}$$

$$\frac{Y(z)}{z} = \frac{-1}{2} \cdot T^2 \cdot \frac{\alpha}{kPLL^2} \cdot \frac{(kPLL - 2)}{(z-1)} + \frac{1}{2} \cdot T^2 \cdot \frac{\alpha}{kPLL} \cdot \frac{(kPLL - 2)}{(z-1)^2} + T^2 \cdot \frac{\alpha}{(z-1)^3} + \frac{1}{2} \cdot T^2 \cdot \frac{\alpha}{kPLL^2} \cdot \frac{(kPLL - 2)}{(z + kPLL - 1)}$$

=>Partial fraction

$$Y1(z) = \frac{-1}{2} \cdot T^2 \cdot \frac{\alpha}{kPLL^2} \cdot z \cdot \frac{(kPLL - 2)}{(z-1)} \qquad Y2(z) = \frac{1}{2} \cdot T^2 \cdot \frac{\alpha}{kPLL} \cdot z \cdot \frac{(kPLL - 2)}{(z-1)^2}$$

$$invztrans(Y1(z), z, n) = \frac{1}{2} \cdot \frac{\left(-T^2 \cdot \alpha \cdot kPLL + 2 \cdot T^2 \cdot \alpha\right)}{kPLL^2} \qquad invztrans(Y2(z), z, n) = \frac{1}{2} \cdot \frac{\left(T^2 \cdot \alpha \cdot kPLL \cdot n - 2 \cdot T^2 \cdot \alpha \cdot n\right)}{kPLL}$$

$$Y3(z) = T^2 \cdot \frac{\alpha \cdot z}{(z-1)^3}$$

$$invztrans(Y3(z), z, n) = \frac{-1}{2} \cdot T^2 \cdot \alpha \cdot n + \frac{1}{2} \cdot T^2 \cdot \alpha \cdot n^2$$

$$Y4(z) = \frac{1}{2}\cdot T^2 \cdot \frac{\alpha}{kPLL^2}\cdot\frac{z\cdot(kPLL-2)}{(z+kPLL-1)}$$

$$invztrans(Y4(z),z,n) = \frac{1}{2}\cdot\frac{\left[T^2\cdot\alpha\cdot(-kPLL+1)^n\cdot kPLL - 2\cdot T^2\cdot\alpha\cdot(-kPLL+1)^n\right]}{kPLL^2}$$

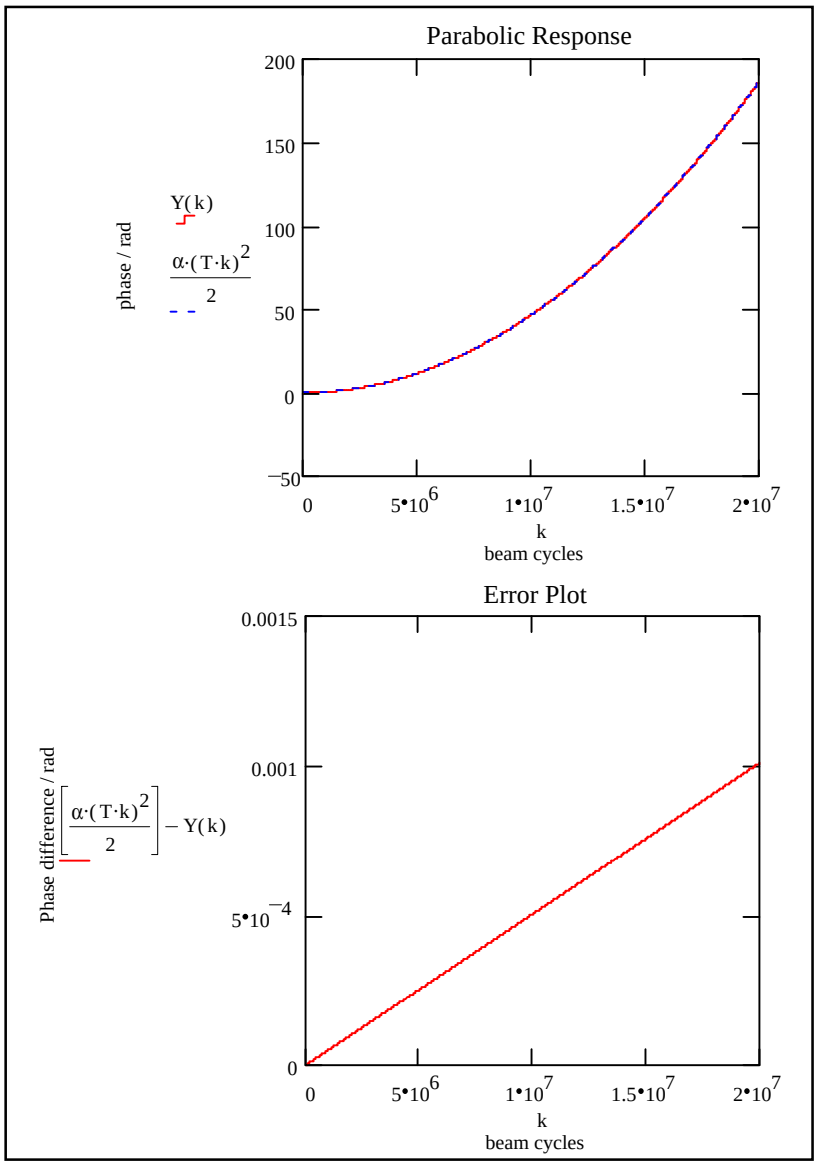
=> Inverse z-Transform

$k := 1, 1000 .. 20000000$

$$Y(k) = \left|\frac{1}{2}\cdot\frac{\left(-T^2\cdot\alpha\cdot kPLL + 2\cdot T^2\cdot\alpha\right)}{kPLL^2}\right| + \left|\frac{1}{2}\cdot\frac{\left(T^2\cdot\alpha\cdot kPLL\cdot k - 2\cdot T^2\cdot\alpha\cdot k\right)}{kPLL}\right| +$$

$$+\left(\frac{-1}{2}\cdot T^2\cdot\alpha\cdot k + \frac{1}{2}\cdot T^2\cdot\alpha\cdot k^2\right) + \left|\frac{1}{2}\cdot\frac{\left[T^2\cdot\alpha\cdot(1-kPLL)^k\cdot kPLL - 2\cdot T^2\cdot\alpha\cdot(1-kPLL)^k\right]}{kPLL^2}\right|$$

=> parabolic response in the time-domain



⇒ The PLL follows the frequency ramp with a very small and slowly growing error

$\tau LHC := 25 \cdot min$

$Ncycles := \tau LHC \cdot \frac{60}{1 \cdot min} \cdot \frac{1}{T}$

$Ncycles = 1.687 \cdot 10^{7}$ The acceleration ramp is finished after $1.687*10^7$ cycles

$k := Ncycles$

$\Delta\phi\ framp := \left[\left[\frac{\alpha \cdot (T \cdot k)^2}{2} \right] - Y(Ncycles) \right] \cdot sec^2$

$\Delta\phi\ framp = 8.506 \cdot 10^{-4} \cdot rad$ Phase drift in rad due to acceleration ramp

$\Delta tframp := T \cdot \frac{\Delta\phi\ framp}{2 \cdot \pi} \cdot sec$

$\Delta tframp = 1.204 \cdot 10^{-8} \cdot sec$ => the calculated final **time error due to the frequency ramp** of LHC (shift by 28 mHz in 25 min) equals to **12 ns**

6. Total time drift during lock-in and acceleration

Due to the special properties the lock-in and acceleration process will always result in a certain time drift. The total time drift equals to

$$\Delta ttotal := \Delta tfstep + \Delta tframp$$

$$\Delta ttotal = 6.877 \cdot 10^{-6} \cdot sec$$

A time drift of 6.877 µs is tolerated, because the operation ranges are much wider than this time drift can influence operation. On the other hand this circuit has many advantages like simple realisation and insensitiveness to disturbance factors.

Appendix C2: Revolution Frequency measurement (RFM) simulation

The cycle-by-cycle simulation made with Microsoft® Excel 97 provides the confirmation of the correctness of the mathematical calculations from Appendix C1. This simulation represents an excellent model of the real circuit because it also calculates each value step-by-step.

Both the working range from 11229.5 Hz to 11253.3 Hz and even the jitter of the digital input signals SYNC and FINT were considered.

For the simulation it was assumed that the RFM-NCO oscillates at the lower boundary (=11229.5 Hz) and UP is zero in the instant, when SYNC is enabled and the lock-in process starts.

1 2 3 4 5 6 7

cycle nr.	ΔT / ns	Tosc	fosc	Tsynchr.	fsynchr.	ΔT	m	ΔT	R	ΔT	a1*z+a0	k	add F(n-1)
-1	0	89.05104034	11229.5151	88.924655180000	11245.4751	0		0.000		0		1	482304
0	0	89.05104034	11229.5151	88.924655180000	11245.4751	0		0.000		0	0	1	482304
1	126.3852	89.05104034	11229.5151	88.924655179989	11245.4751	13		-0.361		12	12	1	482316
2	252.7703	89.04882475	11229.7945	88.924655179977	11245.4751	25		0.277		25	13	1	482329
3	376.9648	89.04642466	11230.0972	88.924655179966	11245.4751	38		-0.304		38	13	1	482342
4	498.7613	89.04402470	11230.3998	88.924655179954	11245.4751	50		-0.124		50	12	1	482354
5	618.1578	89.04180946	11230.6792	88.924655179943	11245.4751	62		-0.184		62	12	1	482366
6	735.337	89.03959433	11230.9586	88.924655179932	11245.4751	74		-0.466		74	12	1	482378
7	850.301	89.03737932	11231.2380	88.924655179920	11245.4751	85		0.030		85	11	1	482389
8	963.0501	89.03534898	11231.4941	88.924655179909	11245.4751	96		0.305		96	11	1	482400
9	1073.767	89.03331874	11231.7502	88.924655179897	11245.4751	107		0.377		108	12	1	482412
10	1182.453	89.03110404	11232.0296	88.924655179886	11245.4751	118		0.245		118	10	1	482422
11	1288.927	89.02925853	11232.2625	88.924655179875	11245.4751	129		-0.107		129	11	1	482433
12	1393.551	89.02722857	11232.5186	88.924655179863	11245.4751	139		0.355		140	11	1	482444
13	1496.147	89.02519870	11232.7747	88.924655179852	11245.4751	150		-0.385		150	10	1	482454
14	1596.714	89.02335344	11233.0075	88.924655179840	11245.4751	160		-0.329		160	10	1	482464
15	1695.433	89.02150826	11233.2404	88.924655179829	11245.4751	170		-0.457		169	9	1	482473
16	1792.306	89.01984766	11233.4499	88.924655179817	11245.4751	179		0.231		179	10	1	482483
17	1887.518	89.01800262	11233.6827	88.924655179806	11245.4751	189		-0.248		188	9	1	482492
18	1980.886	89.01634216	11233.8923	88.924655179795	11245.4751	198		0.089		198	10	1	482502
19	2072.591	89.01449727	11234.1251	88.924655179783	11245.4751	207		0.259		208	10	1	482512
20	2162.454	89.01265245	11234.3580	88.924655179772	11245.4751	216		0.245		216	8	1	482520
21	2250.472	89.01117666	11234.5442	88.924655179760	11245.4751	225		0.047		225	9	1	482529
22	2337.01	89.00951644	11234.7538	88.924655179749	11245.4751	234		-0.299		233	8	1	482537
23	2421.89	89.00804075	11234.9400	88.924655179738	11245.4751	242		0.189		242	9	1	482546
24	2505.292	89.00638066	11235.1496	88.924655179726	11245.4751	251		-0.471		251	9	1	482555
25	2587.037	89.00472062	11235.3591	88.924655179715	11245.4751	259		-0.296		259	8	1	482563
26	2667.121	89.00324509	11235.5454	88.924655179703	11245.4751	267		-0.288		267	8	1	482571
27	2745.727	89.00176960	11235.7317	88.924655179692	11245.4751	275		-0.427		275	8	1	482579
28	2822.858	89.00029417	11235.9179	88.924655179681	11245.4751	282		0.286		283	8	1	482587
29	2898.514	88.99881878	11236.1042	88.924655179669	11245.4751	290		-0.149		290	7	1	482594
30	2972.694	88.99752786	11236.2672	88.924655179658	11245.4751	297		0.269		297	7	1	482601
31	3045.581	88.99623697	11236.4301	88.924655179646	11245.4751	305		-0.442		305	8	1	482609
32	3117.177	88.99476172	11236.6164	88.924655179635	11245.4751	312		-0.282		312	7	1	482616
33	3187.301	88.99347092	11236.7794	88.924655179623	11245.4751	319		-0.270		319	7	1	482623
34	3256.131	88.99218015	11236.9424	88.924655179612	11245.4751	326		-0.387		326	7	1	482630
35	3323.67	88.99088942	11237.1054	88.924655179601	11245.4751	332		0.367		333	7	1	482637
36	3389.919	88.98959873	11237.2683	88.924655179589	11245.4751	339		-0.008		339	6	1	482643
37	3454.877	88.98849245	11237.4080	88.924655179578	11245.4751	345		0.488		346	7	1	482650
38	3518.727	88.98720182	11237.5710	88.924655179566	11245.4751	352		-0.127		352	6	1	482656
39	3581.288	88.98609560	11237.7107	88.924655179555	11245.4751	358		0.129		359	7	1	482663
40	3642.741	88.98480505	11237.8737	88.924655179544	11245.4751	364		0.274		364	5	1	482668
41	3702.905	88.98388325	11237.9901	88.924655179532	11245.4751	370		0.291		371	7	1	482675
42	3762.144	88.98259276	11238.1531	88.924655179521	11245.4751	376		0.214		376	5	1	482680
43	3820.096	88.98167100	11238.2695	88.924655179509	11245.4751	382		0.010		382	6	1	482686
44	3877.122	88.98056492	11238.4092	88.924655179498	11245.4751	388		-0.288		388	6	1	482692
45	3933.044	88.97945887	11238.5489	88.924655179487	11245.4751	393		0.304		393	5	1	482697
46	3987.86	88.97853718	11238.6653	88.924655179475	11245.4751	399		-0.214		399	6	1	482703
47	4041.753	88.97743117	11238.8050	88.924655179464	11245.4751	404		0.175		404	5	1	482708
48	4094.541	88.97650953	11238.9214	88.924655179452	11245.4751	409		0.454		409	5	1	482713
49	4146.406	88.97558790	11239.0378	88.924655179441	11245.4751	415		-0.359		415	6	1	482719
50	4197.349	88.97448197	11239.1775	88.924655179429	11245.4751	420		-0.265		420	5	1	482724

Jitter Simulation

Start values:		
ΔT / ns		0
fosc/Hz		11229.5151
Tosc/µs		89.05104034
Tsynchr./µs		88.92465518

Constants:		
Sample every	1	cycles
New value after/µs	1	
f clock/MHz	100	
T clock/ns	10	
min. f word	482304	482304
max. fword	483327	483327
N Accumulator 2^	32	

Controller:

a1= 1
k= 1

$$C(z) = k \cdot \left(\frac{a_1 \cdot z - 1}{z - 1}\right)$$

Ramp constants:		
Start	Tsynchr./µs	88.92465518
End	Tsynchr./µs	88.92446267
Ramp duration/min		25
ΔT / fs	per cycle	0.011412635

RFM-simulation with Microsoft Excel 97

The picture shows a cut from the desktop of the simulation. Column 1 represents the number of the current beam cycle after SYNC was enabled. 2 equals to the current time difference between SYNC and FINT in Nanoseconds (=UP). The time period and frequency displayed within 3 refer to the current RFM-PLL output frequency (=FINT), the values shown in 4 are the current values of the input beam revolution frequency and time period (=SYNC).

The first column of 5 represents the count of the phase detector counter UP in multiples of the internal reference clock time period (=10 ns), the third one contains already the jitter simulation and the second one is the difference between both values.

The values in column 6 are the current output values of the RFM-controller. The figures in field 7 are the base and start values for the simulation.

Due to simplicity the detailed formulas that are contained in the cells are not described. The results of this simulation and the output graphics can be found in chapter B.2.1.1 of this paper.

Appendix D: Schematics of the FPGA-Implementation

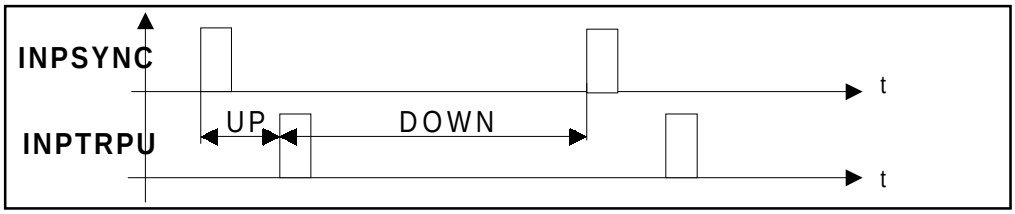
The following schematics were made with the Schematic Editor of the XILINX® Foundation Series 1.5i software package. All implemented parts were designed as simple as possible to avoid complex operations and calculations.

1. Oscillator Unit (OSCUNIT)

The Oscillator Unit is the most complex part within the Trigger Generator FPGA-chip TG0001. It contains different macros that will be described separately.

1.1. Phase difference detector (PHCOMPSY)

This macro issues the time difference between the two input signals INPFINT and INPSYNC in the form of the two output signals UP and DOWN. The length of the square pulse at UP and DOWN equals to the time differences (see figure below).



It works like a RS-Flip-Flop which is continuously set and reset by the two input signals. If one time difference is below ~8 ns the according output signal stays at 0. This macro is part of the phase detector for the Revolution Frequency Measurement (RFM) loop.

1.2. Phase detector counter (UPCOUNT)

The phase detector counter counts the rising edges at its clock input CNTCLK during INP is 1. In the case of the Oscillator Unit it issues the time difference between the rising edges of INPSYNC and INPFINT in multiples of the internal reference clock (10 ns) via its registered CNT_OUT[13:0] bus. The remaining inputs are connected to OSCTIMING, which controls the timing of the phase detector counter. Together with the phase difference detector it is part of the phase detector for the RFM-loop.

1.3. Oscillator Unit timing controller (OSCTIMING)

This circuit is responsible for the correct timing of all operations within the RFM-loop, in particular for the calculation timing of the RFM-controller.
The CALCLOCK part locks all calculations and keeps the previous values in case SYNC (derived from ITIM) is failing.

1.4. Setup controller (SETUP)

If the FPGA-chip configuration was successful, it is necessary for the start of operation to load initially the base frequency value (482304 = 11229.5 Hz) into the RFM-NCO (phase accumulator). If the chip is powered an the programming has been loaded it issues first a global clear via SETUP_CLR and gives OSCTIMING the command to issue the initial load pulse via its LD_INACC output.
If STR_SETUP goes to 1 the setup procedure is repeated. PERM_START goes to 1 when the setup is finished. This pin has no connection to another module but can be used to permit the end of the setup process.

1.5. RFM-controller (OSCCALCU)

This macro executes the mathematical (see chapter B.2.1.1, in particular Figure 10) operations that are necessary to control the RFM-loop.
The time difference word UP is applied to UPINP[13:0] and the measured 10-bit FWORD for the phase accumulator is issued via FWORD[9:0]. The RFM-operation ranges (Figure 17), the inherent boundaries and the lock detector were realised with simple logic gates. The LOCK-output is responsible for enabling the data connection to the output NCO, if the RFM-loop has locked on the SYNC frequency (drift of UP/cycle ≤ 10 ns), i.e. the correct 10 bit-FWORD value is available.

1.6. Offset (OFFSET)

Since the RFM-controller issues only a 10-bit word the remaining hardwired 22 bits are added by the OFFSET macro (see chapter B.2.1.1, page 26).

1.7. RFM-NCO phase accumulator (PHASEACC)

The detailed operation principle of this macro is described in chapter B.2.1.1. As already mentioned in chapter B.2.1.3 the design is based on the XILINX®-Application Note *"Harmonic Frequency Synthesizer and FSK Modulator"* [8], which was modified and adapted to the requirements of the Trigger Generator.

The following modifications were necessary:

- The frequency synthesiser suggested in the Application Note only worked with 26 bits. For the Oscillator Unit 32 bits are required. The missing 6 bits were completed by adding further BIT-macros.
- For the maximum clock frequency of 67 MHz the application of a slower XC3000/ 4000A FPGA-chip was recommended. To attain the required operating frequency of 100 MHz for the Oscillator Unit the faster 3.3V FPGA XC4044XLA is used.
- Although the possibility of a phase accumulator reset with coincident hold of the current FWORD word in the load register is only necessary for the output NCO it must be implemented. This measure maintains that both the output and the RFM-NCO are identical and have the same inherent delays. Therefore they oscillate at exact the same frequency when the same FWORD is applied.

If LD_IN gets 1 the current value at FWORD[31:0] is loaded into the load register, each time a rising edge is applied to CLK this value is added to the accumulator content.

If REGCLR goes to 1 all internal Flip-Flops are cleared whereas a positive pulse at CLR resets all Flip-Flops except of the load register.

The output signal is issued via FOUT and a pulse at LD_OUT indicates that the loading operation has been finished.

1.8. FWORD connection control (LOADCTRL)

The LOADCTRL unit enables and disables the datastream from the RFM-controller (OSCCALCU) to the output NCO phase accumulator (PHASEACCOUT).

The data connection is only enabled (the 32 bit register is strobed) if

a. LOCK is 1 (RFM locked)
b. STRBOUND is 0 (the OSCCALCU output value FWORD is not changing at that instant) and

c. the internal macro signal LD_ACTION is 0 (no loading operation of the output NCO, which needs 32 clock cycles, is under way).

This conditions guarantee that no incorrect FWORD value is transmitted to LDFWOUTACC[31:0] or the loading action disturbs the current operation.

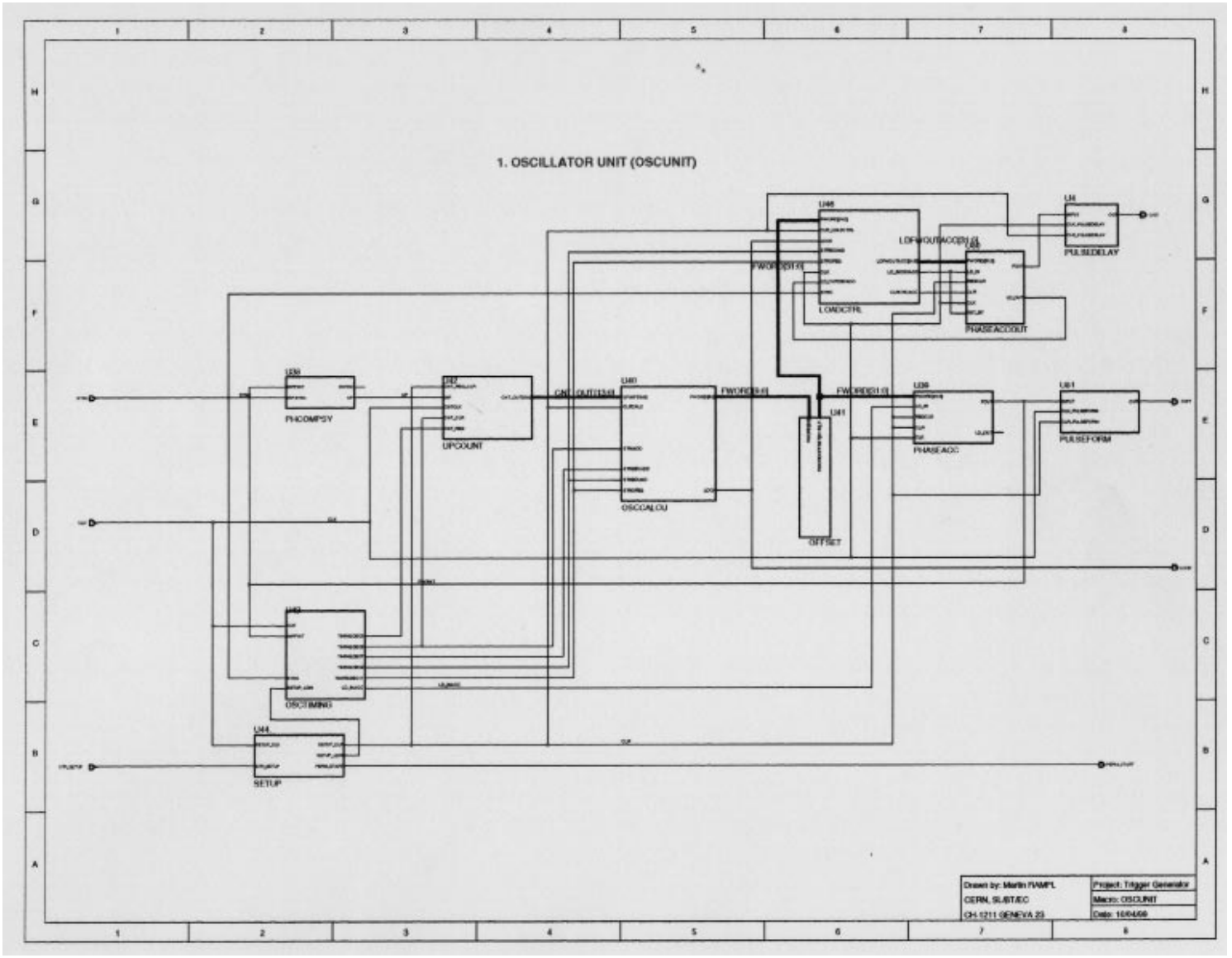
If CLR_LOADCTRL goes to one all Flip-Flops are cleared. CLROSCACC is delayed by 5 clock cycles compared to SYNC and clears the calculation registers of the phase accumulator. The following clock cycle LD_INOSCACC gets 1 to load the current output word LDFWOUTACC[31:0] into the load registers of the output NCO.

1.9. Output phase accumulator (PHASEACCOUT)

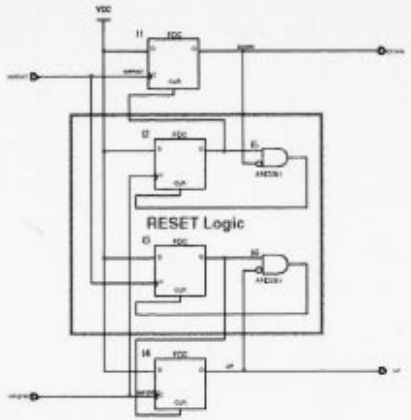
This macro is similar to the RFM-NCO phase accumulator described in 1.7 of Appendix D. The only difference is that bit 21 and bit 23 are set at the rising edge of SET_BIT. For that reason bit 21 and bit 23 were realised with the modified BIT21-macro. This operation makes it possible to add 21 cycles to the accumulator content to compensate loading delays after a clear (CLR high) triggered by SYNC. For further details please refer to B.2.1.2.

1.10. Conclusion

On the following pages you can find the schematic drawings of all macros of the Oscillator Unit. These circuit designs may change during the test phase of the prototype.

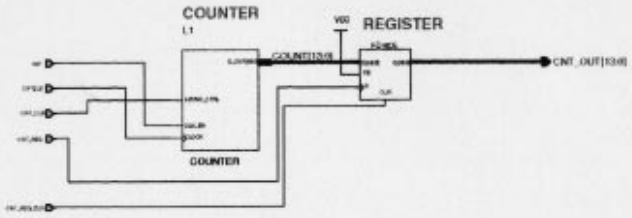

1. OSCILLATOR UNIT (OSCUNIT)
PHCOMPSY
UPCOUNT
OSCCALCU
OFFSET
LOADCTRL
PHASEACCOUT
PULSEDELAY
PHASEACC
PULSEFORM
OSCTIMING
SETUP
Drawn by: Martin RAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: OSCUNIT
Date: 16/04/08

1.1 PHASE DIFFERENCE DETECTOR (PHCOMPSY)



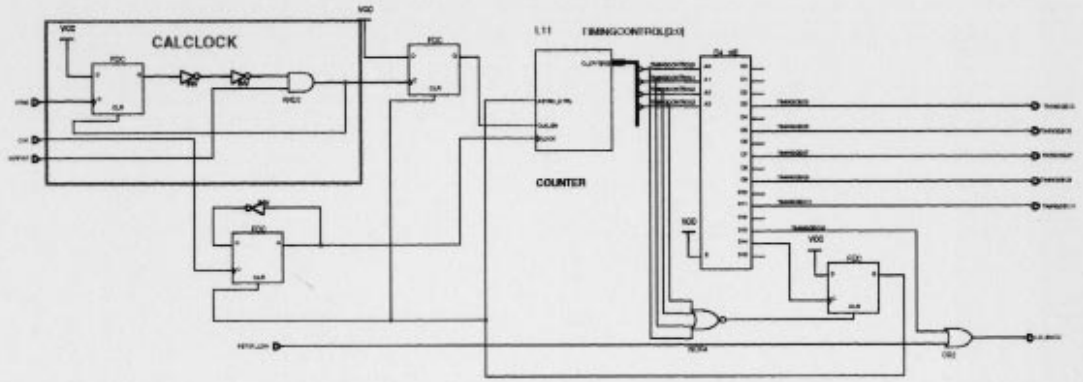
Drawn by: Martin PAMPL	Project: Trigger Generator
CERN, SL/BT/EC	Macro: PHCOMPSY
CH-1211 GENEVA 23	Date: 10/04/99

1.2 PHASE DETECTOR COUNTER (UPCOUNT)



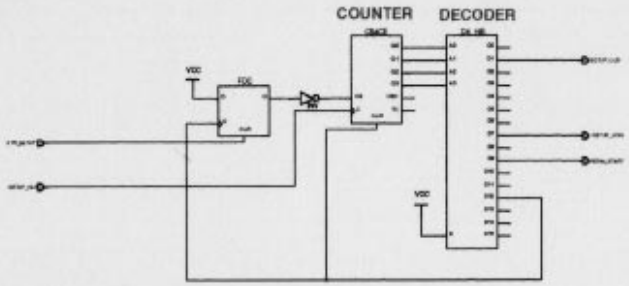
Drawn by: Martin HAMPL	Project: Trigger Generator
CERN, SL/BT/EC	Macro: UPCOUNT
CH-1211 GENEVA 23	Date: 99/04/99

1.3 OSCILLATOR UNIT TIMING CONTROLLER (OSCTIMING)

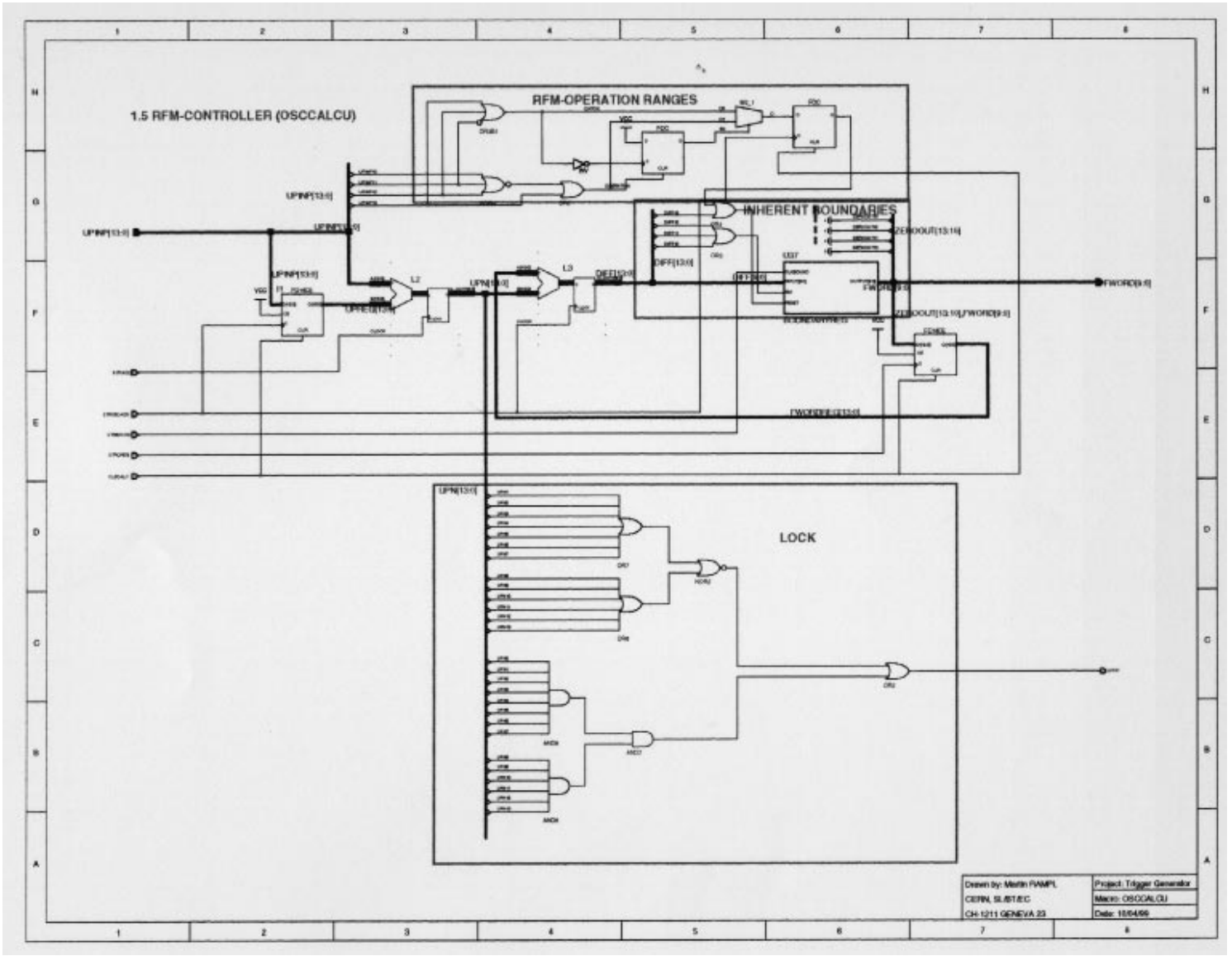


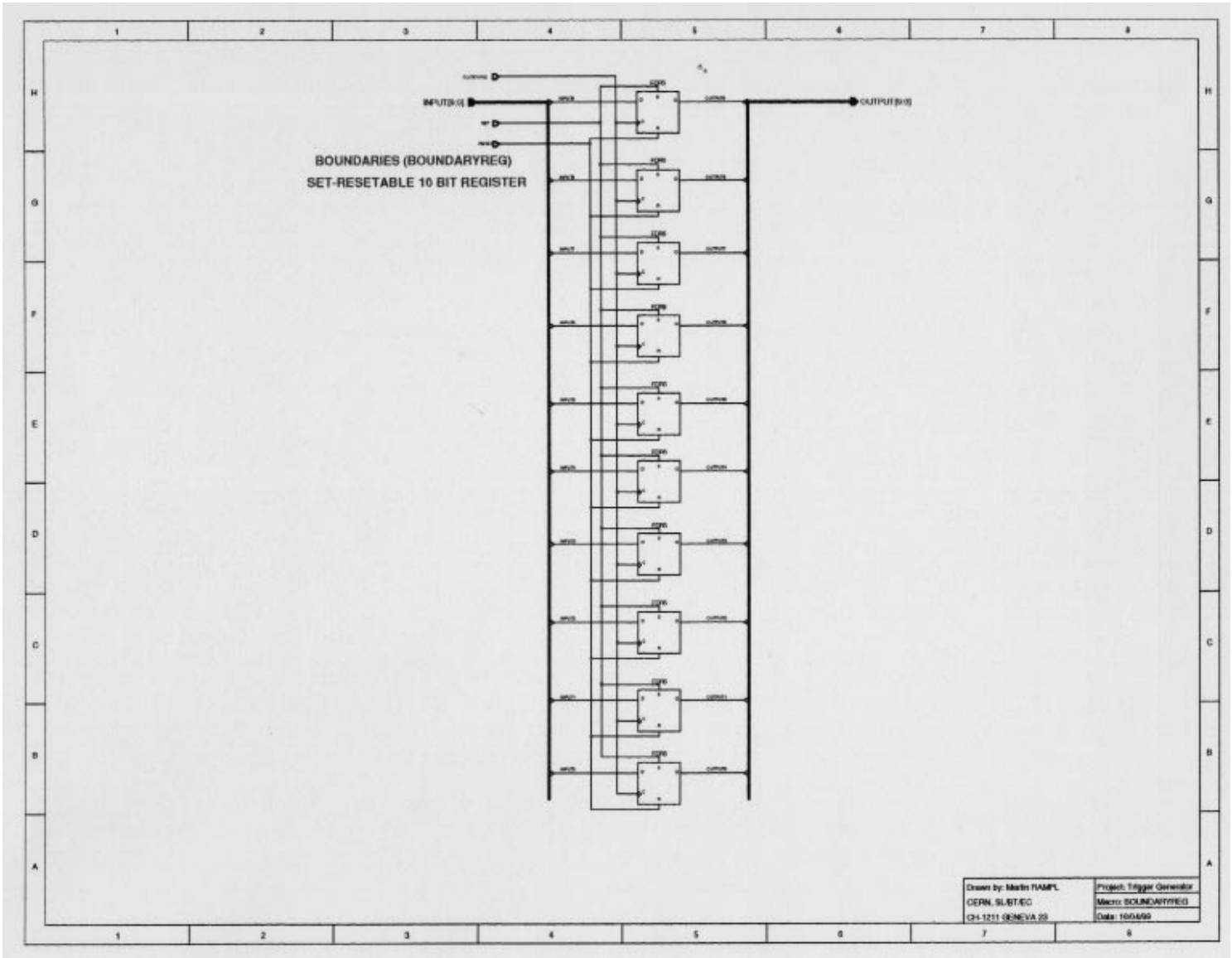
Drawn by: Martin RAMPL CERN, SL/BT/EC CH-1211 GENEVA 23	Project: Trigger Generator Macro: OSCTIMING Date: 18/04/99

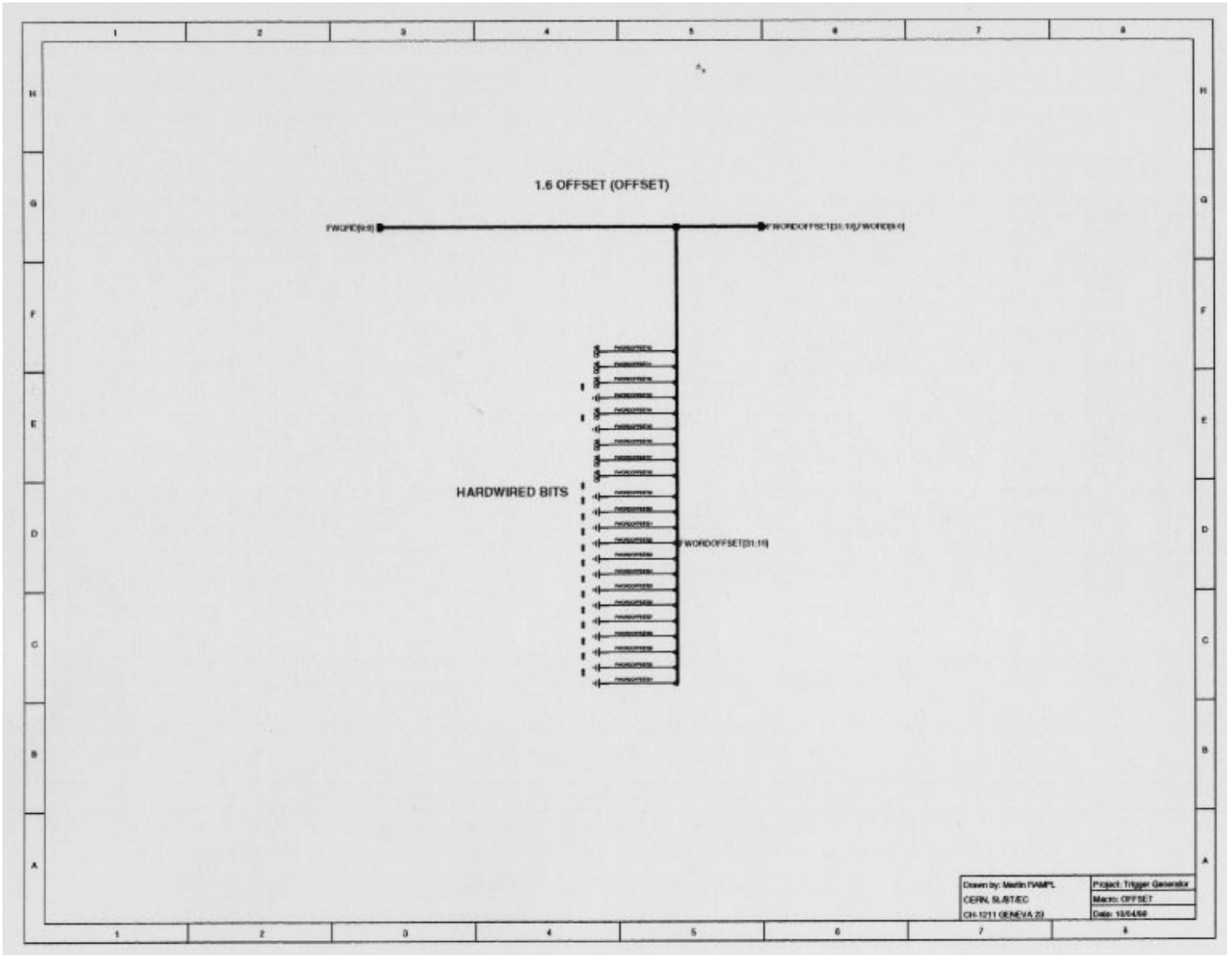
1.4 SETUP CONTROLLER (SETUP)

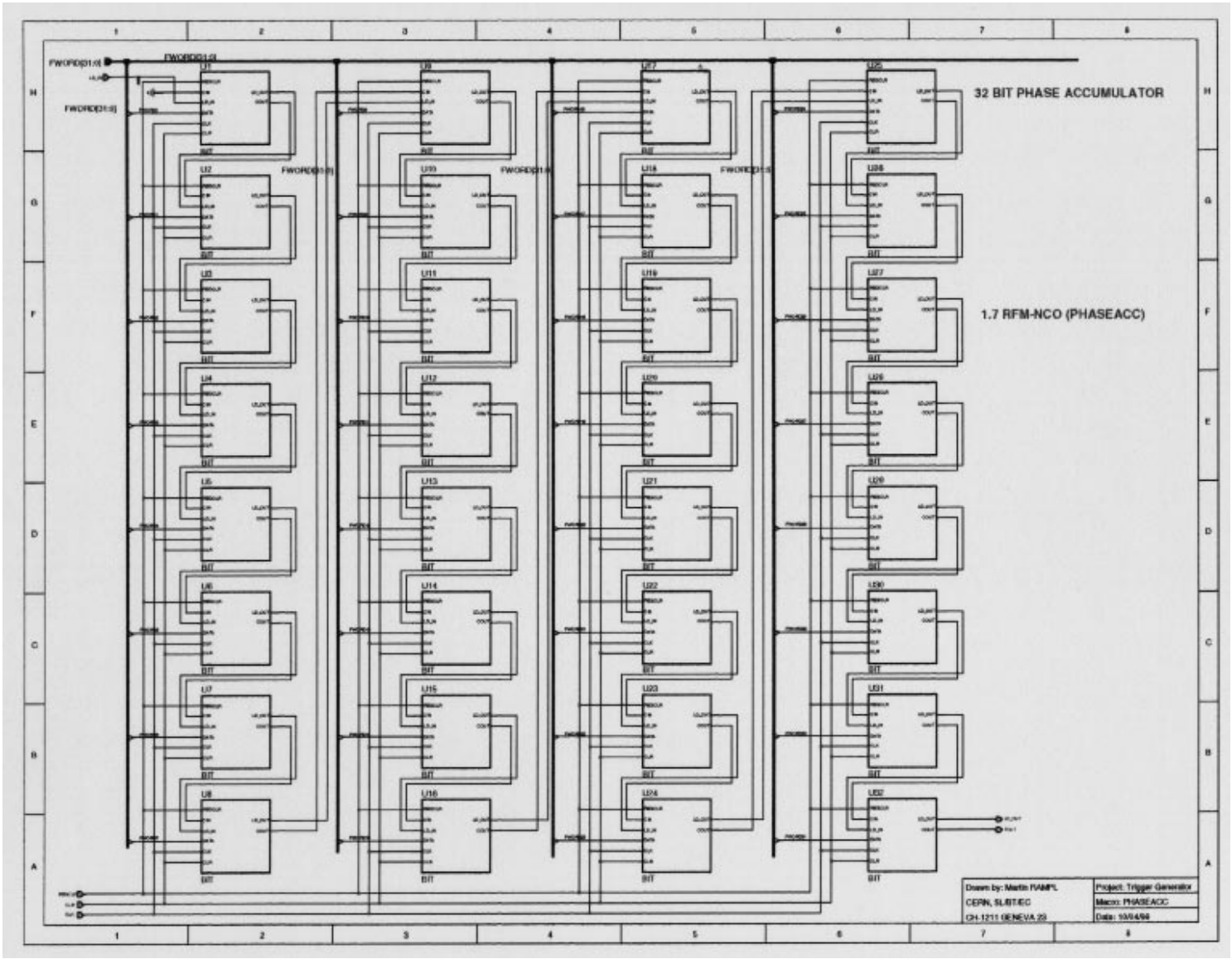


Drawn by: Martin FIAMPI	Project: Trigger Generator
CERN, SL/ST/EC	Macro: SETUP
CH-1211 GENEVA 23	Date: 18/04/96


1.5 RFM-CONTROLLER (OSCCALCU)
RFM-OPERATION RANGES
INHERENT BOUNDARIES
LOCK
Drawn by: Martin PAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: OSCCALCU
Date: 10/04/99

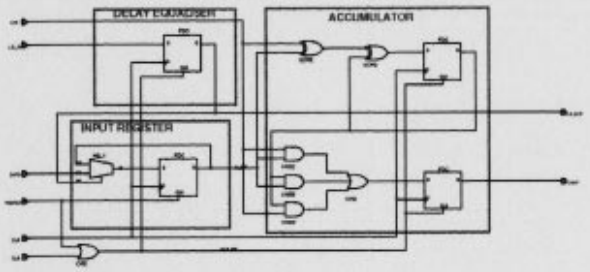

INPUT[9:0]
OUTPUT[9:0]
BOUNDARIES (BOUNDARYREG)
SET-RESETABLE 10 BIT REGISTER
Drawn by: Martin RAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: BOUNDARYREG
Date: 16/04/99

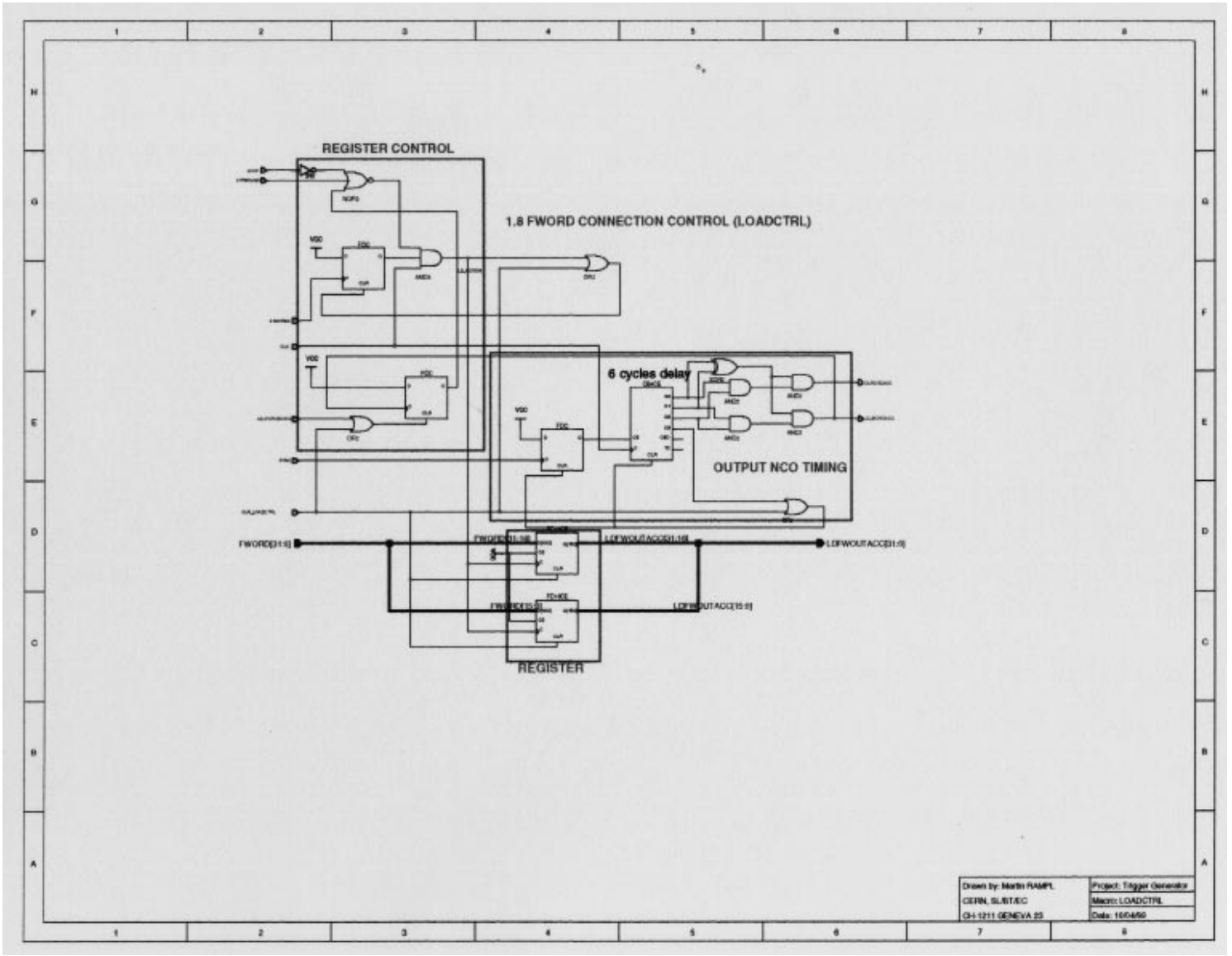

1.6 OFFSET (OFFSET)
HARDWIRED BITS
WORDOFFSET[31:16]
Drawn by: Martin FVAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: OFFSET

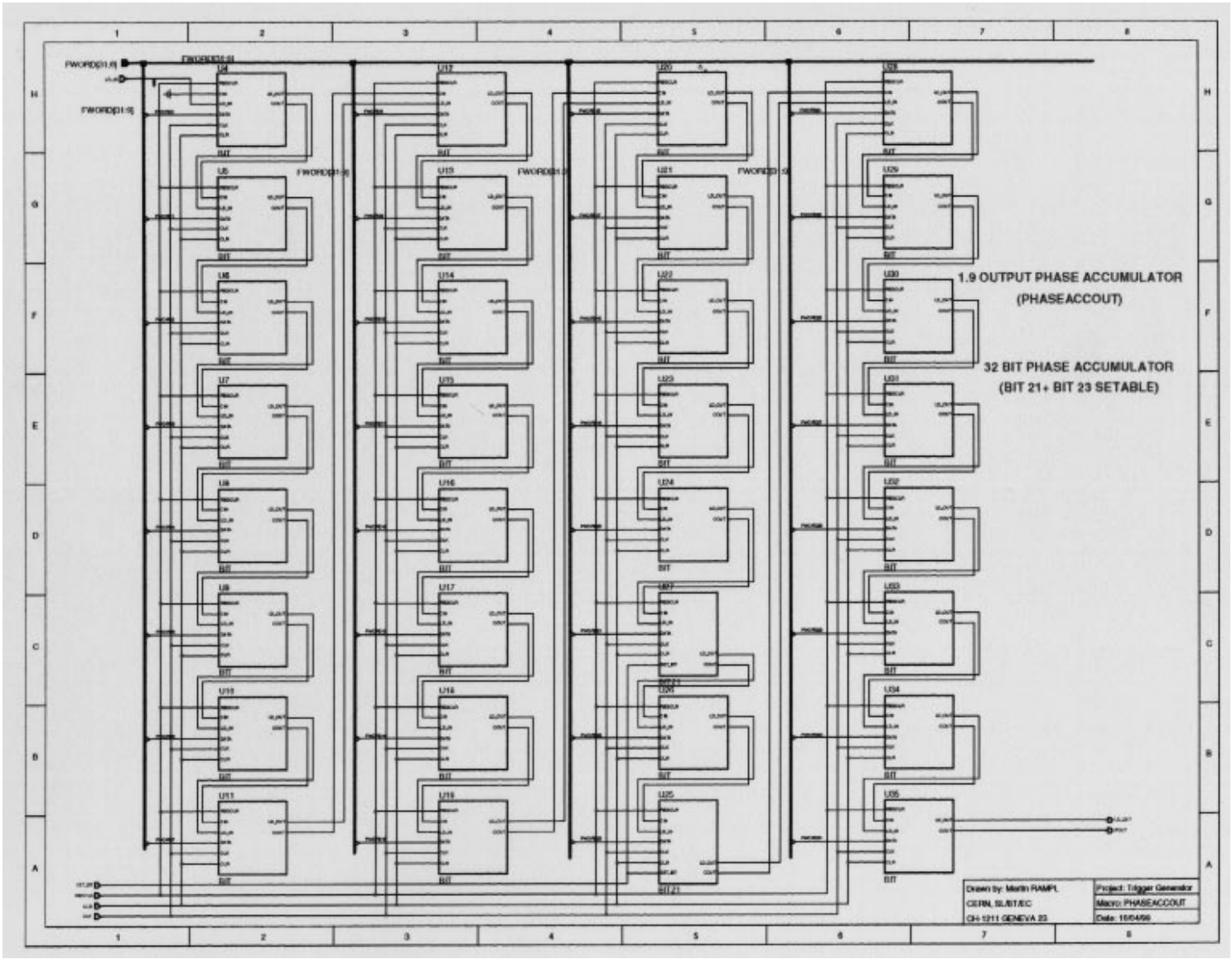

32 BIT PHASE ACCUMULATOR
1.7 RFM-NCO (PHASEACC)
Drawn by: Martin RAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: PHASEACC
Data: 10/04/98

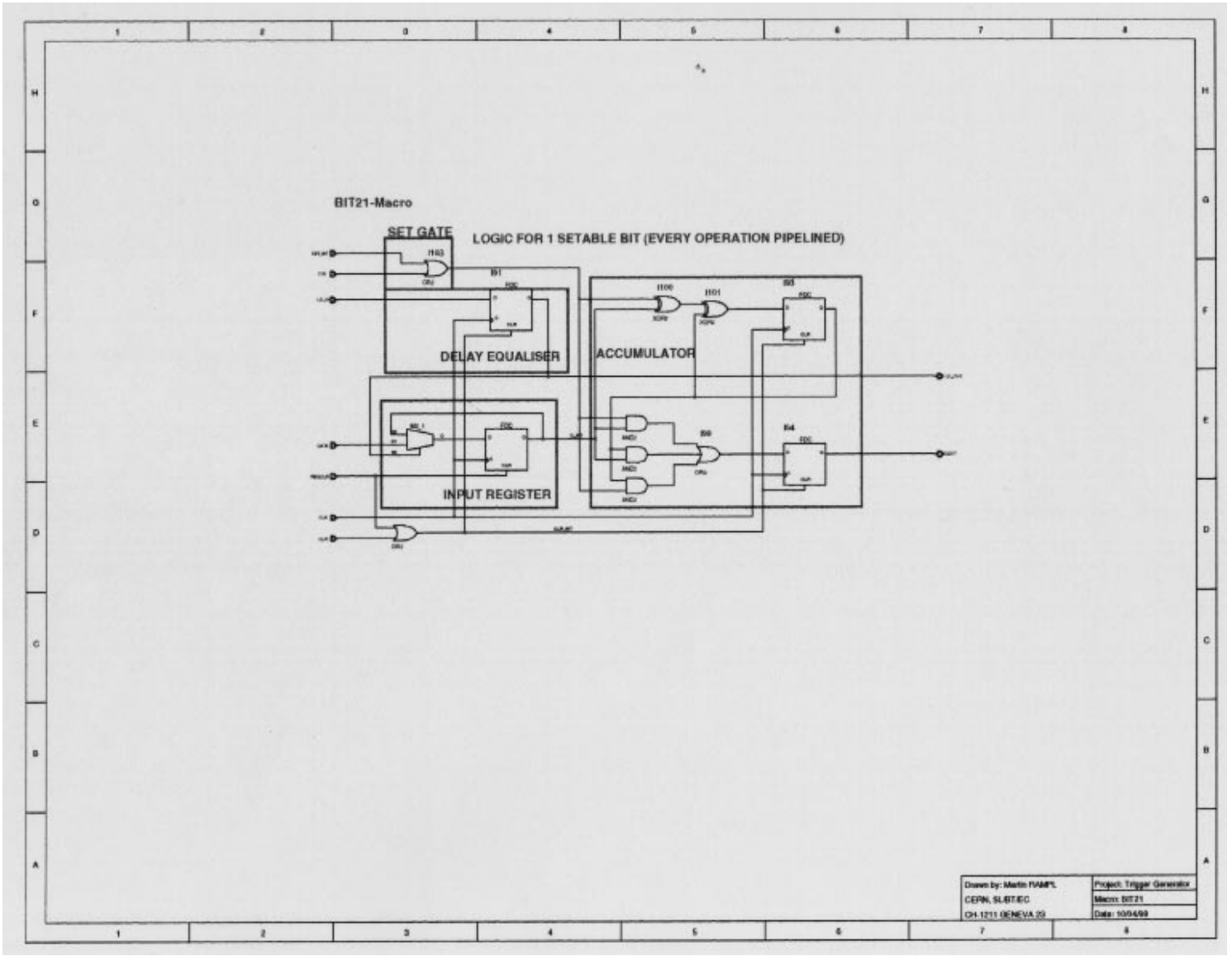
BIT-Macro

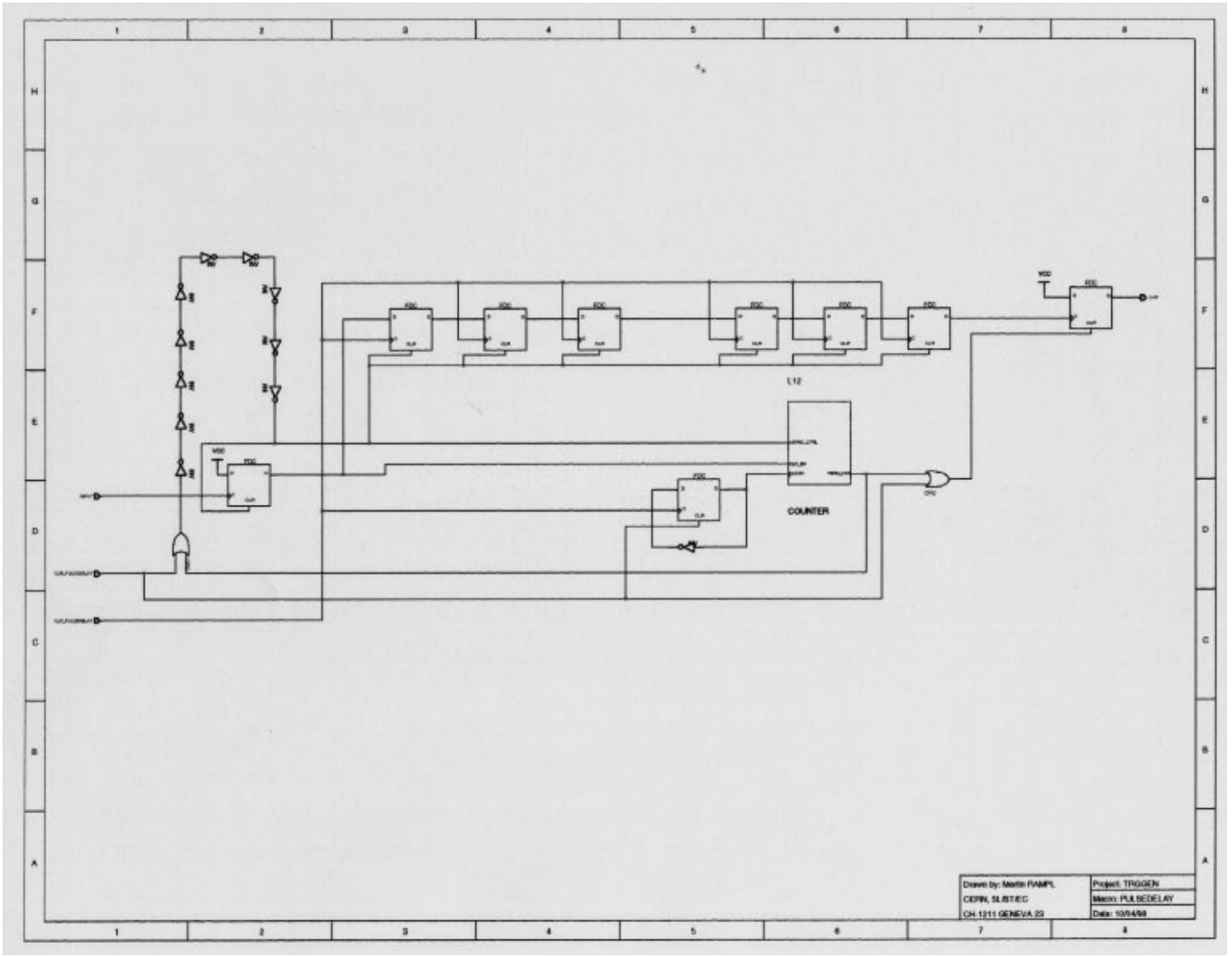
LOGIC FOR 1 BIT (EVERY OPERATION PIPELINED)

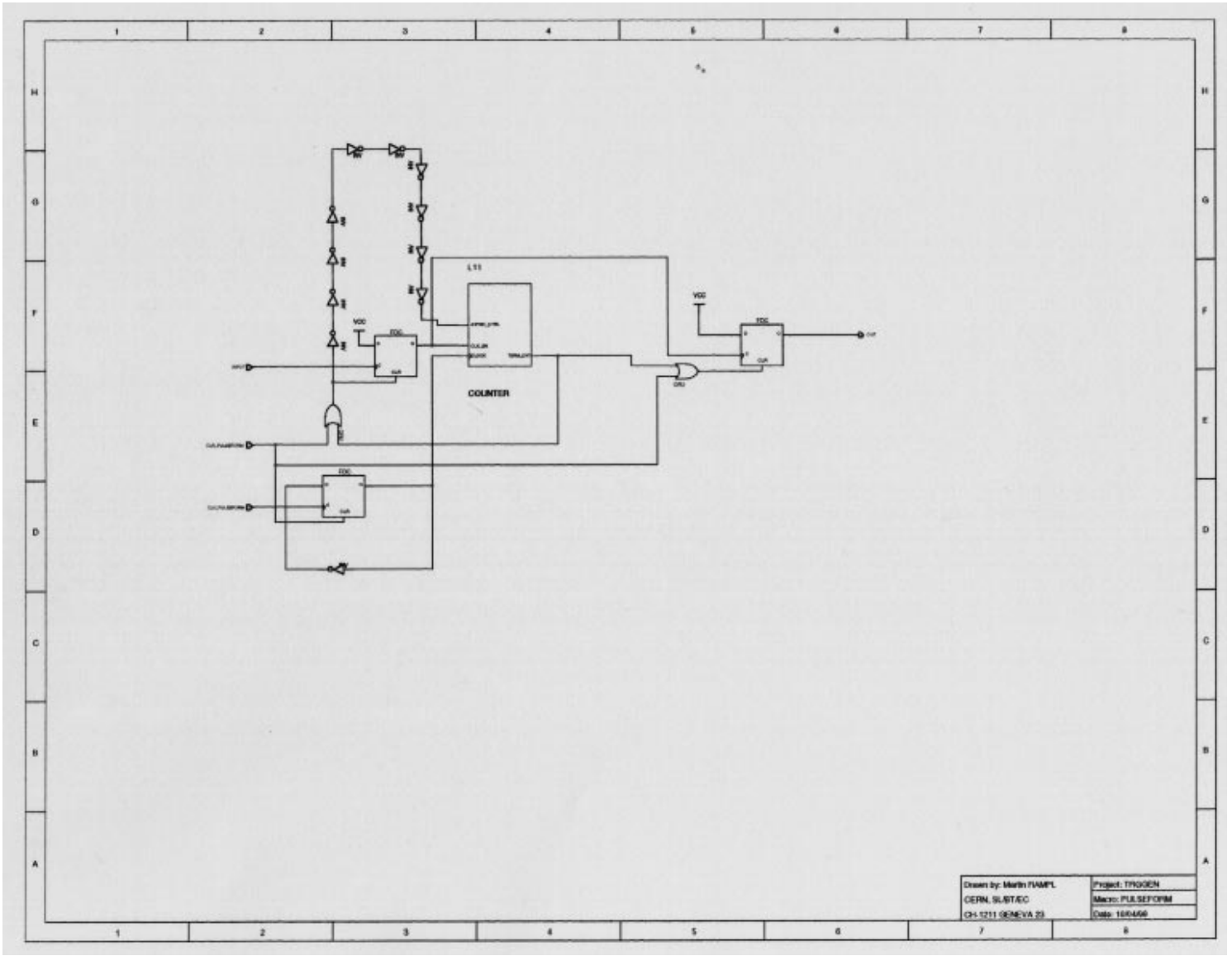



REGISTER CONTROL
1.8 FWORD CONNECTION CONTROL (LOADCTRL)
6 cycles delay
OUTPUT NCO TIMING
FWORD[31:0]
LDFWOUTACC[31:0]
REGISTER
Drawn by: Martin RAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: LOADCTRL
Date: 16/04/99


1.9 OUTPUT PHASE ACCUMULATOR
(PHASEACCOUT)
32 BIT PHASE ACCUMULATOR
(BIT 21+ BIT 23 SETABLE)
Drawn by: Martin RAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: PHASEACCOUT
Date: 16/04/99


BIT21-Macro
SET GATE
LOGIC FOR 1 SETABLE BIT (EVERY OPERATION PIPELINED)
DELAY EQUALISER
ACCUMULATOR
INPUT REGISTER
Drawn by: Martin HAMM
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: BIT21
Date: 30/04/99


COUNTER
Drawn by: Martin PAMPE
CERN, SLIS/TIEC
CH-1211 GENEVA 23
Project: TRIGGEN
Macro: PULSEDELAY


COUNTER
Drawn by: Martin FAMPL
CERN, SL/ST/EC
CH-1211 GENEVA 23
Project: TRIGGEN
Macro: PULSEFORM
Date: 16/04/96

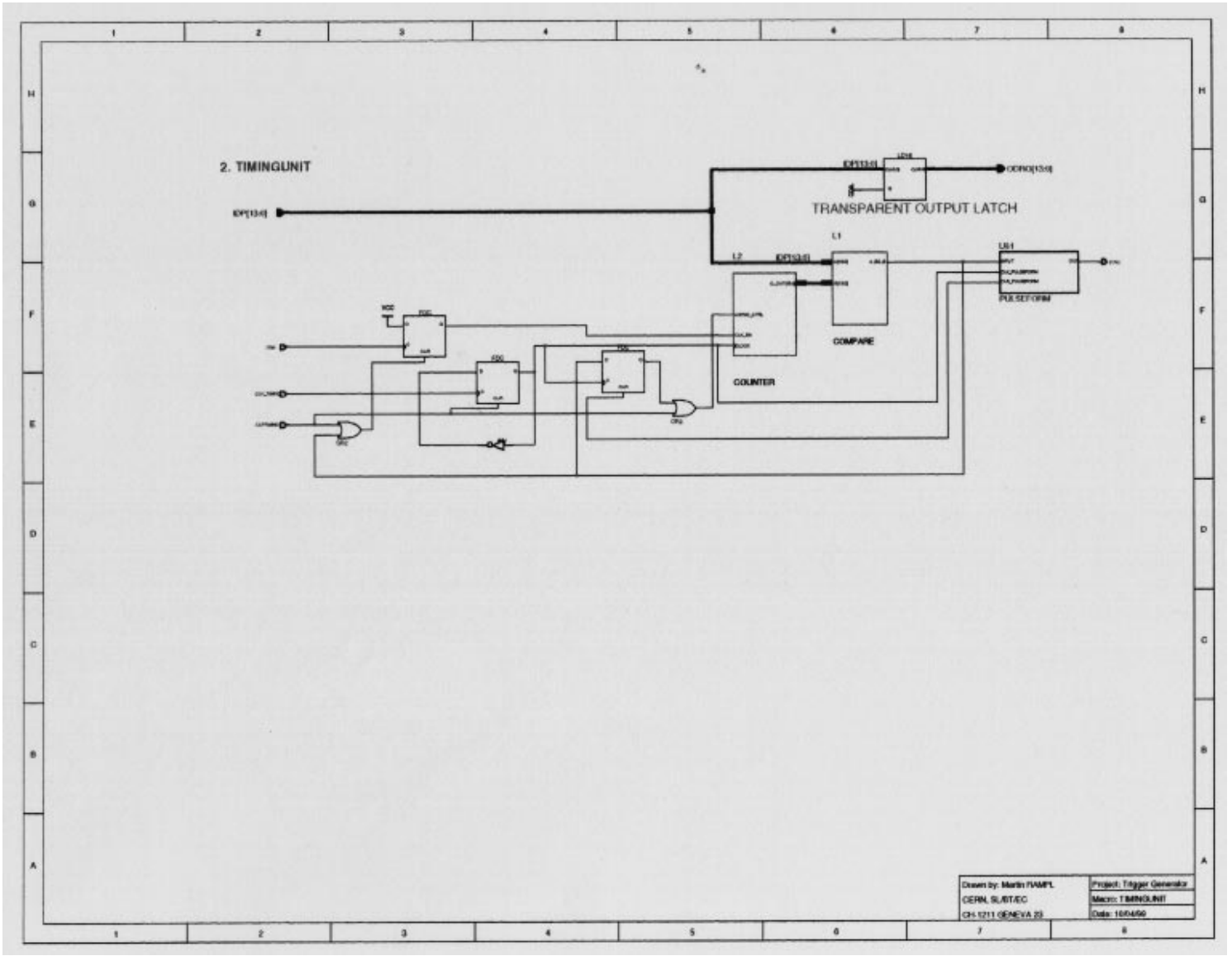
2. Timing Unit (TIMINGUNIT)

The main components of the Timing Unit are the counter and the comparator. The 14 bit counter starts to increment at the rising edge of ITIM. If the counter content equals to the value of IDP[13:0] a 10 ns pulse is issued via the SYNC output. Then the counter is cleared and ready for the next trigger through ITIM.

If the programmed delay time is longer than the beam revolution time period then the counter ignores the ITIM pulses that are applied when it is incrementing.

The CLK_TIMING input must be connected to the internal reference clock line. For surveillance purposes the IDP value can be read out via the ODRO[13:0] bus.

All Flip-Flops and the counter are cleared if CLRTIMING goes to 1 (system reset). The function of the Timing Unit is described in chapter B.2.2.


2. TIMINGUNIT
TRANSPARENT OUTPUT LATCH
COMPARE
COUNTER
PULSEFORM
Drawn by: Martin FAMPL
CERN, SUST/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: TIMINGUNIT

3. Synchronisation Surveillance Unit (INTSYSU)

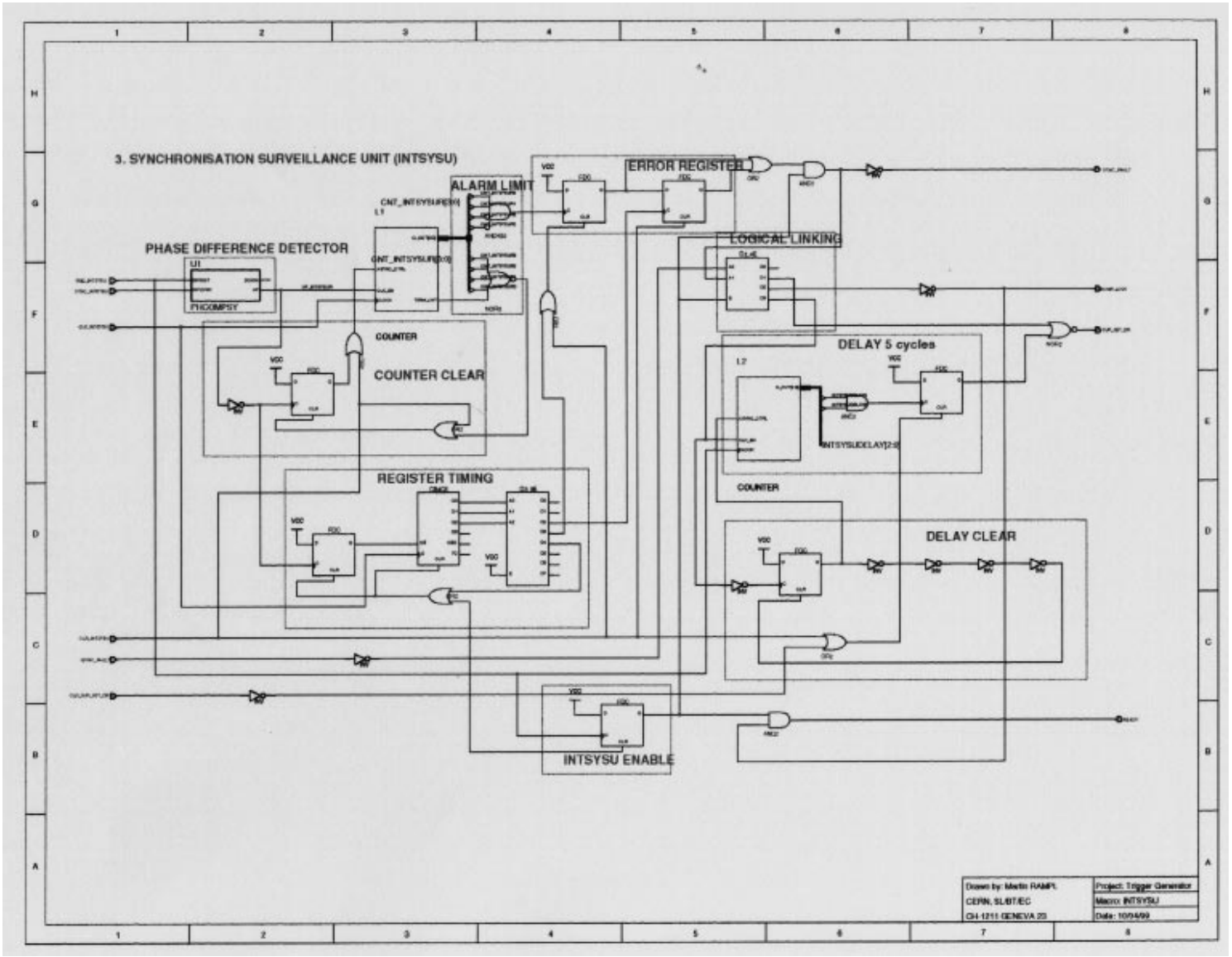
The main parts of this macro are a phase difference detector (PHCOMPSY), which was already used in the RFM-loop of the Oscillator Unit, a 4 bit counter, the logical linking and the timing part.

During UP (time difference between SYNC and OSC) the counter increments. If the content is more than four SYNC_FAULT goes to 0. This signal is directly issued to the Surveillance System. Further it is logically linked with ISYNC_FAULT in the following way:

SYNC_ FAULT	ISYNC_ FAULT	Status	Action
0	0	Timing is failing	SUR_SET_DR=1 after 5 cycles
0	1	own oscillator fails	DUMP_LOCK=0
1	0	parallel device fails	SUR_SET_DR=1 immediately
1	1	all OK	nothing

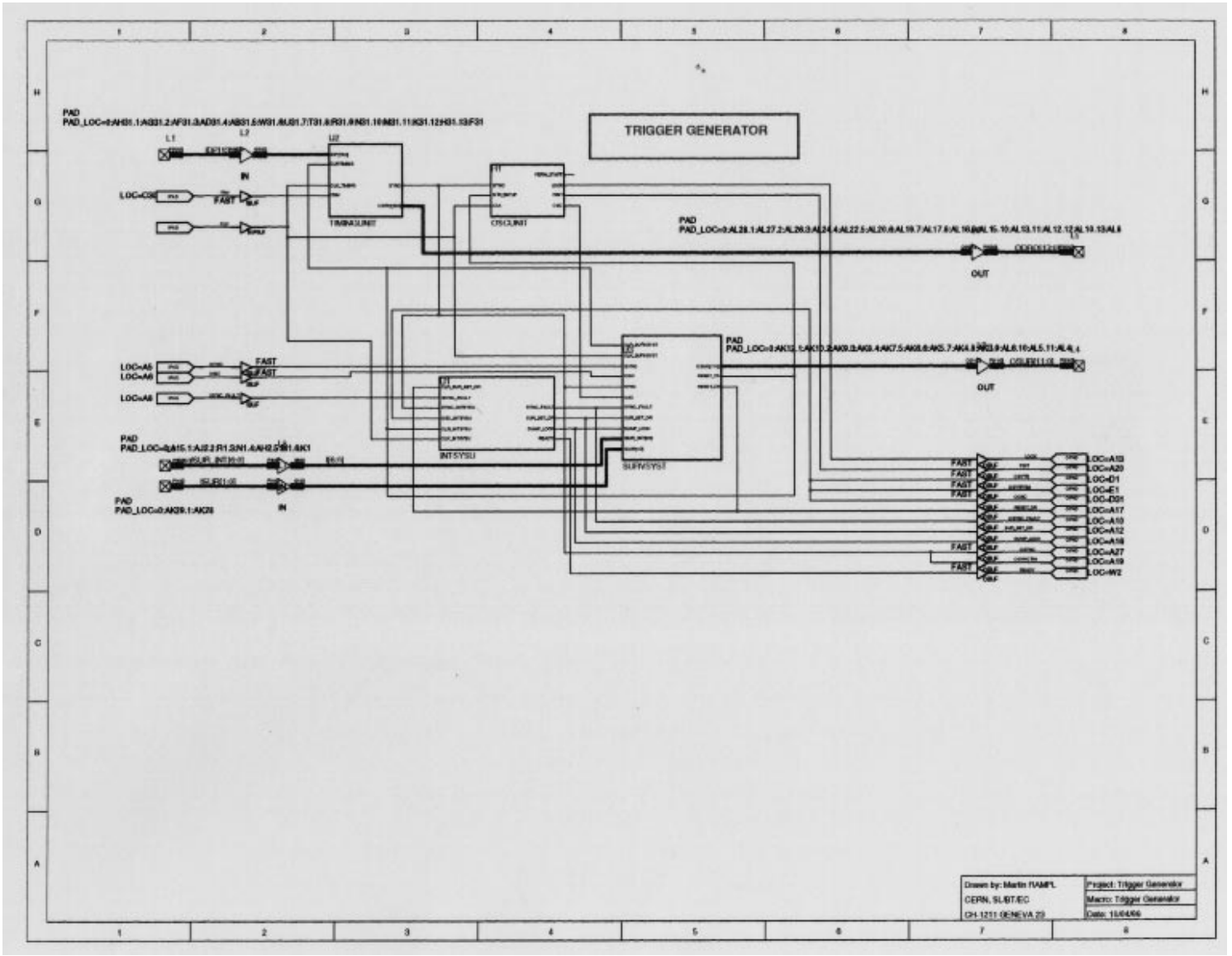
The Synchronisation Surveillance Unit is disabled (SYNC_FAULT stays at 1) until the correct OSC-signal is issued.

The READY-output goes to 1 if the Oscillator Unit has properly locked on the current beam revolution frequency and thus the Trigger Generator is able to trigger a correct beam dumping action. For the detailed functional description please refer to chapter B.2.3.


3. SYNCHRONISATION SURVEILLANCE UNIT (INTSYSU)
ALARM LIMIT
ERROR REGISTER
PHASE DIFFERENCE DETECTOR
LOGICAL LINKING
COUNTER
COUNTER CLEAR
DELAY 5 cycles
REGISTER TIMING
DELAY CLEAR
INTSYSU ENABLE
Drawn by: Martin RAMPL
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: INTSYSU
Date: 10/04/99

4. Complete schematics Trigger Generator FPGA TG0001

The macro modules were designed and tested separately. The final step is the assembling of all macros and assigning their pins to the I/O-pads of the FPGA-chip.


TRIGGER GENERATOR
IN
OUT
FAST
TIMINGUNIT
CSCUNIT
INTSYSU
SUPVSYST
Drawn by: Martin ?AMP?
CERN, SL/BT/EC
CH-1211 GENEVA 23
Project: Trigger Generator
Macro: Trigger Generator
Date: 10/04/06

Appendix E: Detailed calculations for the Output Trigger Gate

1. Introduction

The following part treats the calculation of the component values for the Blocking Oscillator part of the Output Trigger Gate. All made calculations refer to the circuit described in chapter B.3.2 of this paper. The method was taken from [16].

2. Calculation

The calculations were executed with Mathcad 6.0.

2.1. Specification

$tp := 1.5 \cdot 10^{-6} \cdot sec$ Output pulse width

$Vout := 15 \cdot volt$ Output voltage

$Rl := 150 \cdot \Omega$ Input impedance of the following unit (Trigger Distribution system)

$Iout := \frac{Vout}{Rl}$ $Iout = 100 \cdot mA$ Output current

$t0 := 89 \cdot 10^{-6} \cdot sec$ Maximal required output frequency

$Vsupply := 15 \cdot volt$ Supply voltage

$V := Vsupply$

ChosenTransistor: 2N2222A Values taken from SGS-Thomson Data sheet

$Icmax := 800 \cdot mA$ $Cbc := 8 \cdot pF$

$Icmaxpulse := 800 \cdot mA$ $Vcbmax := 75 \cdot volt$ $Vcemax := 40 \cdot volt$

$\beta := 75$ $\alpha := \frac{\beta}{\beta + 1}$ $\alpha = 0.986842$ $fT := 300 \cdot MHz$ $f\alpha := fT$

$f\alpha = 300 \cdot MHz$

$\omega\alpha := 2 \cdot \pi \cdot f\alpha$ $\omega\alpha = 1.885 \cdot 10^{9} \cdot sec^{-1}$ $rB := 60 \cdot \Omega$ $(=r_{be},....)$

$gB := \frac{1}{rB}$ $gB = 0.017 \cdot siemens$

2.2. Calculation of L_p and R_E

$N2 := \frac{Vsupply}{Vout}$ $N2 = 1$ Turns ratio from L_C to L_L

$GL := \frac{1}{Rl}$ $GL = 6.667 \cdot 10^{-3} \cdot siemens$ Load conductance

Approximation of the optimal turns ratio from L_C to L_E (N1)

$X^3 + X^2 - \frac{gB^2}{4 \cdot Cbc \cdot \omega\alpha \cdot (gB + GL)} = 0$ $X := 0.377$ ++estimate X until F=minimum++

$X1 := root\left[X^3 + X^2 - \frac{gB^2}{4 \cdot Cbc \cdot \omega\alpha \cdot (gB + GL)}, X\right]$ $X1 = 0.37839954$ Root of X

$F := X1^3 + X1^2 - \frac{gB^2}{4 \cdot Cbc \cdot \omega\alpha \cdot (gB + GL)}$ $F = 3.05220510^{-6}$ Error of approximation

$N1opt := 1 + \frac{gB}{2 \cdot Cbc \cdot \omega\alpha \cdot \left(X1^2 + X1\right)}$ $N1opt = 2.06$ $N1 := 2$ Optimal ratio and chosen value

Limits of R_E (only thorough estimation)

$Remax := \frac{Vsupply}{\left(\frac{Iout}{N2}\right)}$ $Remax = 150 \cdot \Omega$ Maximal R_E

$Remin := \frac{Vsupply}{Icmaxpulse}$ $Redc := \frac{Vsupply}{Icmax}$

$Remin = 18.75 \cdot \Omega$ $Redc = 18.75 \cdot \Omega$ Minimum R_E

=> Re smaller = shorter rise time => Re larger = flat-top more constant

$Re := 22 \cdot \Omega$ Chosen R_E

$tp = Lp \cdot \left(\frac{\alpha}{Re \cdot N1} - \frac{1}{Re \cdot N1^2} - \frac{1}{Rl \cdot N2^2}\right)$

$Lp := \frac{-tp}{\left[\frac{-\alpha}{(Re \cdot N1)} + \frac{1}{\left(Re \cdot N1^2\right)} + \frac{1}{\left(Rl \cdot N2^2\right)}\right]}$

$Lp = 341.07 \cdot \mu H$ First calculation of L_P

$$Ic := \frac{V}{N1^2 \cdot Re} + \frac{V}{N2^2 \cdot Rl} + \frac{V}{Lp} \cdot tp$$

$Ie := Ic$ $\quad Ie = 336.423 \cdot mA$ First calculation of the transistor-current

$Reroot := 10 \cdot \Omega$

$$Remin := root\left[\left(\frac{V}{N1^2 \cdot Reroot} + \frac{V}{N2^2 \cdot Rl} + \frac{V}{Lp} \cdot tp\right) - Icmax, Reroot\right]$$ Accurate calculation of R_{Emin}

$Remin = 5.917 \cdot \Omega$ $\quad Re = 22 \cdot \Omega$ $R_E < R_{Emin}$ => value OK

Correction (under consideration of the transistor resistances):

$\beta b := 75$ $\quad \alpha b := \frac{\beta b}{\beta b + 1}$ $\quad \alpha b = 0.987$

Amplification factors in common base configuration

$re := \frac{26 \cdot mV}{Ie}$ $\quad re = 0.077 \cdot \Omega$ $\quad ri := re + rB \cdot (1 - \alpha b)$ Input resistance of the transistor

$ri = 0.867 \cdot \Omega$

$$tp = \frac{Lp}{N1^2} \cdot \left(\frac{\alpha b \cdot N1 - 1}{Re + ri}\right) - \frac{Lp}{N2^2 \cdot Rl}$$

$$Lp := \frac{-tp}{\left[\frac{-1}{(N1 \cdot (Re + ri))} \cdot \alpha b + \frac{1}{\left[N1^2 \cdot (Re + ri)\right]} + \frac{1}{\left(Rl \cdot N2^2\right)}\right]}$$ Corrected calculation of L_P

$Lp = 377.024 \cdot \mu H$

$$Ic := \frac{V}{N1^2 \cdot (Re + ri)} + \frac{V}{N2^2 \cdot Rl} + \frac{V}{Lp} \cdot tp \qquad Ie := Ic$$

$Ie = 323.671 \cdot mA$ Corrected calculation of the transistor current

$I_C < I_{Cmax}$ => OK

2.3. Zenerdiode D_1 and R_0

Series resistance R_0:

Damping:

$Cwiring := 20 \cdot pF$ $\quad Ctransformer := 100 \cdot pF$ $\quad Cdiode := 70 \cdot pF$ Estimated values

$Cg := Cbc + Cwiring + Ctransformer + Cdiode$ $\quad Cg = 198 \cdot pF$

$R0max := \frac{1}{2}\cdot\sqrt{\frac{Lp}{Cg}}$ $R0max = 689.957\,\Omega$ For critical damping

$R0 \le R0max$ This condition must be fulfilled for correct damping

Protection:

$Ilp := \frac{V}{Lp}\cdot tp$ $Ilp = 59.678\,mA$ Current through L_P at the moment of switch-off

$IR0 := 0.01\cdot Ilp$ $IR0 = 0.597\,mA$ Assumed current through R_0 (and D_1)

$R0max := \frac{Vcemax\cdot Lp}{V\cdot tp}$ $R0max = 670.265\,\Omega$ Maximal value for R_0

$t0 = \frac{Lp}{R0}\cdot\ln\left(\frac{Ilp}{IR0}\right)$

$R0min := Lp\cdot\frac{\ln\left(\frac{Ilp}{IR0}\right)}{t0}$ $R0min = 19.509\,\Omega$ Minimal value for R_0

++ The smaller R_0 the longer t_0 **! ! !** ++ Chosen value for R_0: $R0 := 33\,\Omega$

++ $R_{0max} > R_0 > R_{0min}$) ++

Zenerdiode D_1:

Type: BZX55 Values from PHILIPS Data sheet

$Ifmax := 250\,mA$

$Cdiode := 70\,pF$

$Vforward := 1\,volt$

$Vindmax := \frac{V\cdot R0}{Lp}\cdot tp + Vforward$

$Vindmax = 2.969\,volt$ Maximum collector voltage at the instant of turn-off

$Ifmaxind := \frac{Vindmax - Vforward}{R0}$

$Ifmaxind = 59.678\,mA$ Maximum current through the Zenerdiode D_1

$t0calc := \frac{Lp}{R0}\cdot\ln\left(\frac{Ilp}{IR0}\right)$ $t0calc = 5.261\cdot10^{-5}\,sec$

Calculated recovery time of the Blocking Oscillator t_{0calc} <<< t_0 => OK

$Iz := \frac{1}{8} \cdot Ifmax$ $\quad Iz = 31.25 \cdot mA$

The working point was determined with 1/8 of the maximal current

$Vdiode := V - Iz \cdot R0$ $\quad Vdiode = 13.969 \cdot volt$ => Choice: BZX55C15 (15 V)

2.4. Pulse Transformer

The pulse transformer consists of 4 windings wound on a ferrite core. The collector and emitter windings L_C, L_E are necessary for the regenerative feedback of the Blocking Oscillator, the output winding L_L maintains the galvanic decoupling of the output and the surveillance winding L_{SUR} issues the trigger signal to the Surveillance System.

$VSUR := 5 \cdot volt$ Voltage of surveillance pulse

$N1 \equiv \frac{nC}{nE}$ $\quad N2 \equiv \frac{nC}{nL}$ $\quad N3 \equiv \frac{nC}{nSUR}$ $\quad N3 := \frac{V}{VSUR}$

$N1 = 2$ $\quad N2 = 1$ $\quad N3 = 3$ Required turns ratios of the transformer

$Lc = 377.024 \cdot \mu H$ Calculation of the inductances

$Le := \frac{Lc}{N1^2}$ $\quad Ll := \frac{Lc}{N2^2}$ $\quad Lsur := \frac{Lc}{N3^2}$

$Le = 94.256 \cdot \mu H$ $\quad Ll = 377.024 \cdot \mu H$ $\quad Lsur = 41.892 \cdot \mu H$

Core: (Values from PHILIPS Data sheet)

Size:23x7x14 Material: 3H2 MnZn

$AL := 2.000 \mu H$ $\quad Bsat := 0.4 \cdot tesla$ $\quad \mu i := 2000 \frac{amp}{m}$ $\quad AFe := 30.9 mm^2$

$L \equiv n^2 \cdot AL$ Base for the calculation of the number of windings

$nC := \sqrt{\frac{Lc}{AL}}$ $\quad nC = 13.73$ Chosen: nC=14

$nE := \sqrt{\frac{Le}{AL}}$ $\quad nE = 6.865$ Chosen: nE=7

$nL := \sqrt{\frac{Ll}{AL}}$ $\quad nL = 13.73$ Chosen: nL=14

$nSUR := \sqrt{\frac{Lsur}{AL}}$ $nSUR = 4.577$ Chosen: nSUR=5

Wire: Cu insulated

Flux Density: (Core must not get into saturation)

$B = \frac{V \cdot tp}{n \cdot Afe} \leq Bsat$

$B1 := \frac{V \cdot tp}{nC \cdot AFe}$ $B1 = 0.053 \cdot tesla$ B < B sat => OK

2.5. Conclusion

All component values calculated in Appendix E refer to a simple Blocking Oscillator with only one transistor. Since the behaviour of the Blocking Oscillator with two transistors in series is approximately the same the calculations are valid for the Output Trigger Gate.