TUNE MEASUREMENT FOR THE CERN PROTON SYNCHROTRON BOOSTER RINGS USING DSP IN VME

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Abstract

The CERN PS Booster (PSB) consists of 4 superposed rings supplied with protons from a 50 MeV Linac. The proton beam is then accelerated to 1 GeV and sent either to the 26 GeV Proton Synchrotron (PS) or to the ISOLDE facility. This is carried out in a multi-cycle mode every 1.2 s. For high-intensity beams, the working-point in the tune diagram needs to be changed considerably during acceleration from 50 MeV to 1 GeV and the repeated measurement of the tunes throughout the cycle is an important requirement. Up to now, tune values were obtained through calculations based on quadrupole currents. However, practical experience has shown the need for a direct tune measurement system. For this purpose, a classical kick technique is used. A fixed amplitude kick of duration equal to one revolution period excites coherent betatron oscillations. For fast treatment, a Digital Signal Processing (DSP) module in a VME-standard crate was selected. It carries out the Fast Fourier Transform (FFT) analyses of signals from position-sensitive pickups in both planes and evaluates the tunes. These measurements are carried out every 10 ms during the 450 ms acceleration ramp. The paper presents the novel features of this system, particularly the beam-offset signal suppression as well as the peak-search algorithm which yields the tune values.

1 INTRODUCTION

The PSB was constructed as an injector for the 26 GeV PS and started running in 1972. In the early days, the PSB had a very elaborate measurement system to measure the tune values [1],[2],[3] in both planes for all 4 Rings. The system was based on inducing coherent betatron oscillations by the excitation of a 'Q-kicker' for a fraction of the revolution period. However, around 1976, it was proposed to calculate the tune values based on the measurement of various magnet currents in the rings [4],[5],[6]. This meant that the Q-kicker method was progressively disused and finally abandoned in the eighties. In parallel, the current acquisition approach has been considerably refined over several generations of the control systems, to become the principal method of evaluating the tunes in PSB rings to date.   In recent years, particularly in the light of LHC beam requirements, it was decided that a tune measurement system using a Q-kicker was again necessary for the PSB. With DSP possibilities in a modern VME environment,

such measurements every 10 ms during acceleration seemed feasible. This approach was adopted, as in the PS [7], and forms the basis of the system described here.

2 SYSTEM DESCRIPTION

The PS control system is based on the VME standard. DBV96 modules, which use the Motorola 96001 DSP chip, were purchased for the PSB Q measurement System. The VME system provides the interface to the rest of the control system and permits the   down-loading of the DSP software. To perform a measurement, one needs to excite betatron oscillations, at the requested times in the machine cycle. Timing pulses are generated at these times, gated with the revolution frequency. To ensure coherence, the revolution frequency is obtained from another VME crate which generates the radio frequency signals for the PSB. The gated signal is sent to the pulser, which generates a one-turn pulse to drive the kicker. The same pulses are used to trigger the ADC, starting the process of putting the 1024 data points into memory, ready for the DSP. When the data has been acquired, the DSP commences the   processing. Fig. 1 shows the main units of the system.
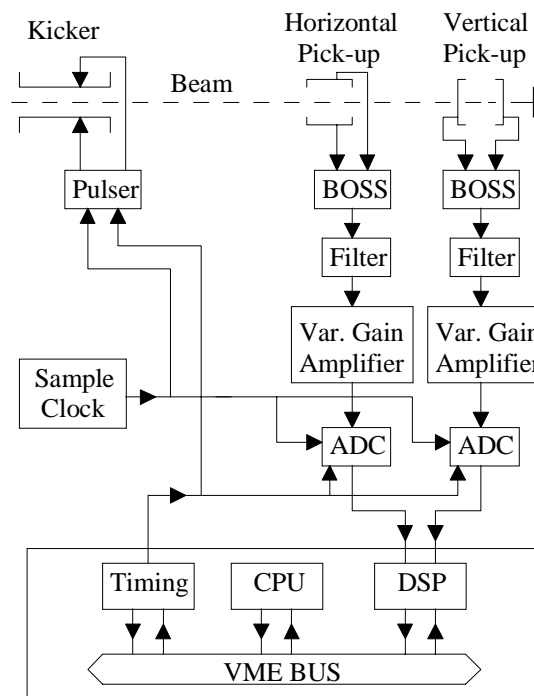

Figure 1 : System block diagram

3 HARDWARE

The layout of one acquisition channel is illustrated in Fig. 1. The PSB type-A electrostatic pick-up (PU) has 4 identical electrodes. The voltage induced on each electrode is proportional to the beam intensity and to the distance of the beam from the PU centre. The electrodes are transformer-matched to 50 Ω coaxial cables, which bring the signal from the ring up to the BOSS units. Opposite pairs of electrodes are used for the horizontal and vertical measurements, which are then processed in identical analogue signal channels.

3.1 Beam Offset Signal Suppressor(BOSS)

During the acceleration cycle the beam position can move significantly away from the centre of the vacuum chamber. Typically this can be between 5 to 10 mm. The amplifiers in front of the Analogue to Digital Converter (ADC) must have their gain set so that they do not saturate, at any point in the machine cycle. The Q measurement pulser applies a 500 V pulse to the kicker which gives an oscillation amplitude of ~0.1 mm. Therefore, the measured signal is typically of the order of one hundredth of the ADC's input range. To improve the signal-to-noise ratio, one could augment the amplitude of the pulse but this has two undesirable consequences. The pulser becomes costly and difficult to maintain and kicking many times along the cycle causes beam blow-up.

The BOSS unit has an input amplifier for each electrode of a plane. The internal feedback system acts on the gain of the two input amplifiers, to give identical output voltages. These two voltages are then subtracted to obtain the betatron signal. The frequency response of the feedback loop is chosen so that it is fast enough to act on the relatively slow changes of the closed orbit position. The betatron frequencies are higher and therefore, are not attenuated.

3.2 Filter

The PSB revolution period is 1.67 μs at injection and 0.54 μs at extraction. There are fixed cable delays between the sample clock generator and the pickup signal of the order of 1 μs. This makes it difficult to control the phase between the bunch signal and the sample clock. At present, the sample clock is at twice the revolution frequency. The beam can have a bunching factor of down to 0.4. These conditions can result in the ADC taking a block of data, sampled between the bunch signals. This effect can be clearly seen on the trace of the raw signal without BOSS, as short "drop-outs" of the signal. In an ideal case, the filter cut-off frequency should follow the revolution frequency. However, by choosing a filter with a cut-off frequency sufficiently low to stretch the bunch signal at injection, but high enough not to attenuate the betatron frequencies too much at extraction, one can use a

fixed cut-off frequency filter. In the future, these filter trade-off effects will be minimised by sampling at four times the revolution frequency.
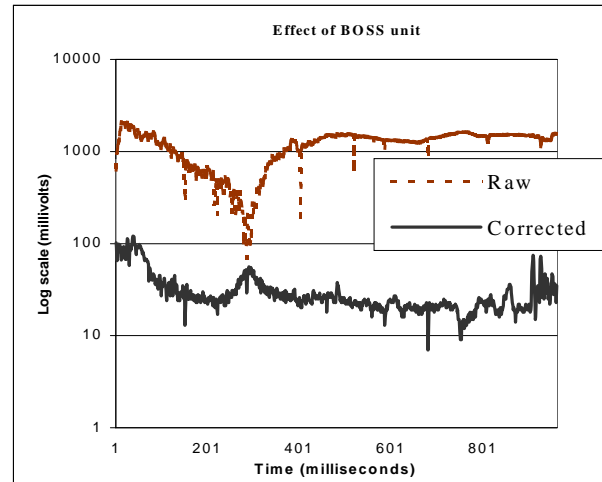

Figure 2 : Effect of the BOSS unit on the pickup signal

3.3 Variable Gain Amplifier & ADC

This uses a voltage programmable amplifier followed by a fixed gain buffer. Its gain range is –20 dB to +60 dB. At present, the gain is set by a front panel potentiometer but, this could be controlled by a DAC. For routine operation, the gain is set so that there is no saturation with the highest beam intensity. The system then measures over a range of 1×10^{12} to 3×10^{13} protons per pulse. A 12-bit resolution, 1×10^{6} samples/s ADC is used, giving a 80 dB dynamic range in the power spectrum.

3.4 Pulser

To carry out a tune measurement, betatron oscillations are excited by pulsing a kicker in each ring. The amplitude of the kick had to be chosen based on the criteria that it must be large enough to produce reliable measurements, but small enough to avoid blowing up the beam [4]. The present pulser is a device of the utmost simplicity. It is driven by a 5 V logic signal which is gated to equal one revolution period. The pulse is isolated by an opto-coupler and further gated by two monostable multivibrators. These limit the maximum pulse length to 2 μs, and the maximum repetition frequency to 200 Hz. The pulse is then amplified to 15 V to drive the output stage. This consists of two power MOSFETS wired as 10 A current sources. These are connected in parallel to an isolating transformer, which drives the kicker. The transformer permits ground isolation between the pulser and the kicker. It also permits an output pulse of either polarity, without recourse to floating power supplies.

4 SIGNAL PROCESSING & SOFTWARE

The filtered PU signal is digitised by an ADC sampling at twice the revolution frequency in a synchronised manner. The time series obtained consists of 1024 samples. This time series is manipulated by DSP programs in order to extract the information needed, i.e. the machine fractional tune. The first tasks (applying a 72 dB Blackman-Harris window [8], FFT transforms, power spectrum computation and peak search) are coded in assembler language to achieve the required speed. A peak search algorithm was developed to find all the frequencies corresponding to the first peaks in the power spectrum which are above a given noise level. It consists of two phases : the coarse search and the fine tuning. The former is based on first order differences which generate a three-levels function : 0 if at least one of the values is below the noise level, -1 if the first order difference is negative and +1 if it is positive.

The required frequencies $f^{(1)}$ are those at which the value of this auxiliary function jumps from +1 to –1. A simple algorithm sorts the obtained maxima in descending order. It is well known that the effect of the finite duration of the time series is to convolute the spectral estimate with a kernel which depends on the chosen window. This "leakage effect" introduces a small error (less than the frequency sampling interval Δf) in the computation of the frequency of the maximum. One may assume that the square root of the power spectrum $z(f)$ is well approximated by a parabola in the neighbourhood of the maximum for most types of windows by :

$$z(f) \approx z_{max} [1 - a (f - f_{max})^2]$$

where z_{max}, f_{max} and a are the square root of the power spectrum maximum, the corresponding frequency and the frequency spread respectively. If z_0, z_{-1}, z_1 are the values $z(f^{(1)})$, $z(f^{(1)}-\Delta f)$ and $z(f^{(1)}+\Delta f)$, simple algebra gives the following second estimate of f_{max} :

$$f^{(2)} = f^{(1)} - \frac{z_{-1} - z_1}{2(z_{-1} - 2z_0 + z_1)} \Delta f$$

The program checks if the fraction in this expression is less than 1 in absolute value to ensure the validity of the second estimate. It is not usually the case when z_{-1} and z_1 are below the noise level.

A program written in C language computes the machine fractional tunes in the DSP board and subsequently delivers them in the correct format to the control system. Display programs at the console provide the operator with the complete behaviour of the fractional tune along the machine cycle (Fig. 3). Facilities are available to observe

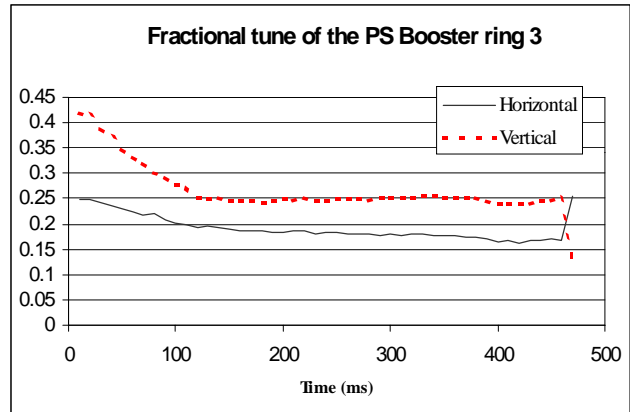all the data including the raw ADC samples and the FFT Spectra.

Figure 3. Display of the measured horizontal and vertical fractional tune in the PS Booster ring 3.

5 CONCLUSIONS

The PSB tune measurement system is evolving rapidly; considerable modifications are underway to permit measurements in all 4 rings by mutiplexing the treated source signals to the ADC and DSP chain. A new ADC board and a timing burst generator are also to be added together with a more powerful, controllable pulser to augment the kick strength. With the rapid evolution in DSP technologies, a more modern DSP Board in VME will also have to be considered in the near future; this would permit identical hardware configurations for the PSB and PS Rings.

6 ACKNOWLEDGEMENTS

7 REFERENCES

[1] H.Koziol, "Q Measurement for the PS Booster", MPS/Int.BR/74-14, (1974)
[2] H.Koziol," Beam Observation For the Booster", SI/Int.DL/68-4,rev1, (1968)
[3] C. Carter, "A Tunable BandPass Filter", CERN/SI/Int.DL/70-7, (1970)
[4] G.Baribaud, J.Donnat, M.Lelaizant, K.Schindl, "Calcul de Q a partir des Courants , Specifications du materiel et du logiciel", , PS/BR Note 76-6, (1976)
[5] C.Metzger, " Calcul de Q: Description du Programme en Fortran",PS/BR/Note/79/18, (1979)
[6] G.Baribaud, J.Donnat, H.Schönauer, "Specifications du Systeme pour le calcul de Q du PSB", PS/BR Note/80-2, (1980)
[7] J. González, S. Johnston, E. Schulte," Fast Q Measurement for the PS by FFT analysis", CERN/PS 94-12 (BD), & Proc. 4th EPAC, London, pp. 1734 (1994)
[8] F. J. Harris, "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Proc. IEEE , vol. 66, no. 1, (1978)