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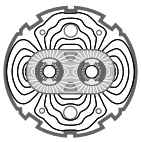

Large Hadron Collider Project

LHC Project Report 257

Full Range ZVS Phase Shifted Power Converter with "Poles"

F. Bordry, A. Dupaquier

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The study and development of a quasi-resonant power converter, with Full Bridge - Phase Shifted - Pulse Width Modulation (FB-PS-PWM) topology is presented. The originality of the paper is the adding of resonant networks (poles) on each leg to get soft commutation (Zero Voltage Switching ZVS) over the full range of the output current. The design of the pole structure and the component ratings are described. Simulations and a [1000A-15V] converter prototype, using dual-thyristor, validate the theoretical studies.

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Abstract:
The study and development of a quasi-resonant power converter, with Full Bridge – Phase Shifted – Pulse Width Modulation (FB-PS-PWM) topology is presented. The originality of the paper is the adding of resonant networks (poles) on each leg to get soft commutation (Zero Voltage Switching ZVS) over the full range of the output current. The design of the pole structure and the component ratings are described. Simulations and a [1000A-15V] converter prototype, using dual-thyristor, validate the theoretical studies.

Introduction

The LHC accelerator requires large currents and rather low voltages for its superconducting magnets. For one-quadrant converters, resonant converters are well placed for medium or high output voltage and quasi-resonant power converter (often called Phase Shifted Converter) is deemed a good topology for high current and low voltage applications [1].
The LHC converters require a wide output current range (Imax/Imin ~50). This paper presents how to extend the soft-commutation range of a phase-shifted converter.

ZVS Phase Shifted Converter

The control of the power semiconductors running with a constant frequency is such that, instead of turning off the diagonally opposite switches in the bridge simultaneously as for a classical PWM, a phase-shift is introduced between the two legs of the bridge [2,3,4]. This phase-shift determines the output power. According to Figure 1 and the logic command in Figure 2, the set of Q1-Q3 switches is called leading-leg and the Q2-Q4 set is called lagging-leg.

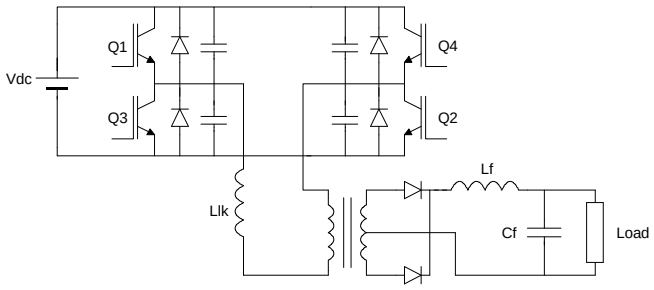

Figure 1: ZVS PWM Converter

For a full bridge, the control of the switches must include a way to compensate any DC offset in the primary current, which would saturate the transformer.

Effective duty cycle δ_e
In Figure 2 the secondary voltage v2 is present for a shorter time than the primary voltage v1. The duration difference is due to the total leakage inductance. The following equation calculated at full control duty cycle gives the relationship between the parameters:

$$L_{lk} = \frac{n.E.(1-\delta_e)}{4.I.f_{sw}}$$

n: Transformer ratio
E: DC voltage
f_{sw} : Switching frequency
δ_e: Effective duty cycle
I: Mean output current

A typical value of $0.8 < \delta_e < 0.9$ would be a good compromise.

Maximum mean output voltage
To obtain a maximum mean voltage V on the load and with the voltage drop in the diodes V_d and resistive voltage V_r the secondary transformer voltage must be V_2:

$$V_2 = \frac{(V+V_d+V_r)}{\delta_e}$$

Turn-off commutation
A snubber capacitor, in parallel with the switch, deviates the current at the turn-off of the switch. It helps to reduce the turn-off losses because the voltage increases relatively slowly up to the supply voltage; thus the current passes through the diode of the complementary switch. The switching in the leading-leg is done at a nearly constant current; the energy for the parallel switch capacitances (parasitic and snubbers) and the parasitic capacitances of the transformer comes from the series inductance, the leakage inductance and the output filter inductance. This means that the energy stored is very large. For the lagging-leg, the zero-voltage turn-on is achieved by using only the energy stored in the series inductance ("soft-commutation inductance") and the leakage inductance of the transformer.

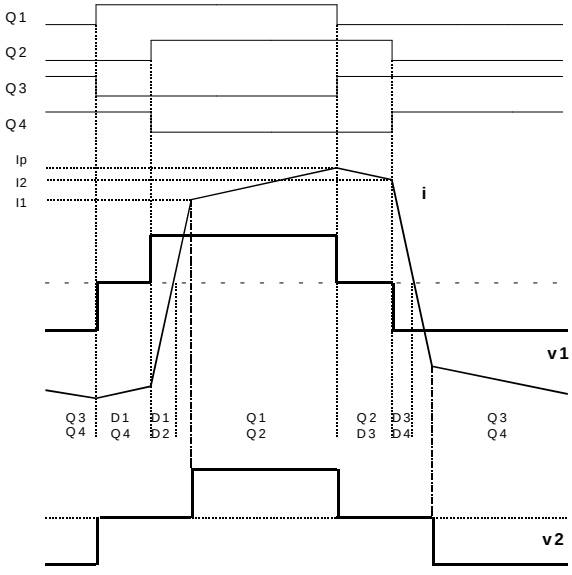

Figure 2: Phase-shifted waveforms

Turn-on commutation
When the current passing through two opposite diodes (D1-D2 or D3-D4) decreases down to zero (time τ), the turn-on of the switches (respectively Q1-Q2 or Q3-Q4) happens with zero voltage and zero current conditions, therefore without losses. A fixed delay (~1µs) between the switch commands of the same leg does not permit soft commutation when this

delay becomes greater than the time τ. Generally this happens for output current close to 40% of the maximum current. The use of the dual-thyristor logic overcomes this problem [4].

Inverter current at the turn-off

For the *leading leg* at the turn-off instant the inverter current is I_{1b}

$$| I_{1b} | = \frac{I_{fm} + \Delta I_f}{n}$$

I_{fm}: Mean Filter current (equal to load current I)
ΔI_f: Ripple amplitude of I_f.

the *lagging leg* at the turn-off instant the inverter current I_{1a} is:

$$| I_{1a} | < \frac{I_{fm} - \Delta I_f}{n}$$

This inequality is due to resistive losses in the secondary diodes and in the windings and to the voltage drop in the primary switches. Then the two secondary diodes are conductive and their current I_{dc} converges to $I_f/2$, thus the inverter current is $(I_{dc1}-I_{dc2})/n$. See the simulation waveform in Figure 3.

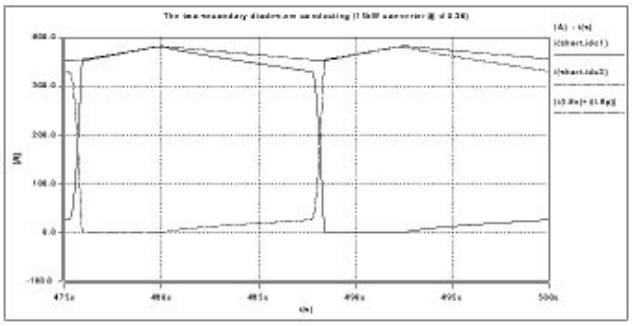

Figure 3: Inverter current waveform

Zero Voltage Switching conditions
The ZVS conditions are obtained if the energy stored in the inductances is enough to discharge the parallel switch capacitances.

For the *leading-leg* (Q1 or Q3 turn-on), the ZVS conditions are easily fulfilled due to the high energy stored in the filter inductance L_f. Soft commutation is maintained for output current greater than 3-4 percent of the maximum current. The inverter current I_{1b} must be:

$$I_{1b} > E\sqrt{2C/(n^2 L_f + L_{lk})}$$

I_{1b}: Inverter Current for the leading-leg at the turn-off time
C: Parallel switch capacitor (snubber + parasitic capacitor)
$n^2L_f+L_{lk}$: Filter and leakage inductance seen by the primary
n: Transformer ratio
E: DC voltage

But for the *lagging-leg* (Q2 or Q4 turn-on), only the energy stored in the leakage inductance L_{lk} is used. The following equation gives the condition to get soft-commutation for the lagging-leg:

$$\frac{1}{2} L_{lk} I_1^2 \geq \frac{1}{2} 2CE^2 \qquad (1)$$

It gives also the inverter current to maintain the soft commutation:

$$I_{1a} > E\sqrt{2C / L_{lk}}$$

I_{1a}: Inverter Current for the lagging-leg at the turn-off time
C: Parallel switch capacitor (snubber + parasitic capacitor)
Llk: Leakage inductance seen by the primary
E: DC voltage

The soft commutation is lost for medium load currents. The rating of the soft-commutation inductance is a compromise result: a large (leakage + additional) inductance results in a small effective duty cycle (slope of the rising and falling edges of the primary current) but ZVS is achieved over a greater current range.

At the turn-off of a switch, if the current is insufficient to discharge the snubber capacitor of the complementary switch, the antiparallel diode will not switch on. The snubber capacitor energy will be brutally dissipated in the switch at the turn-on. To limit this problem, generally no snubber capacitor is added; the price to pay is the increase of turn-off losses and then a reduction of the inverter frequency. For prototypes, without turn-off snubbers, made for the LHC, the ZVS is lost for a current equal to around 30% of the maximum current

If the dual-thyristor logic is used, the converter will stop when the soft-commutation conditions are not fulfilled.

To improve the above compromise and to increase the Imax/Imin range with soft-commutation, the use of pole networks in the quasi-resonant circuit is proposed.

Phase Shifted Converter with poles

The objective is to supply an extra current to the inverter current in order to fulfil the equation (1) [4]. This extra current is handled by passive circuits (called poles) connected to the middle point of each leg.

Pole currents
According to the commutation asymmetry of the two legs, the two-pole current can be different: a smaller current for the leading-leg than for the lagging-leg at the turn-off instant.
To minimise the conductive losses and to achieve fast change of the phase shift, the best choice is:

- a peak waveform with greater current for the lagging-leg. The control is made with fixed turn-off instants.
- a rectangular waveform with low current for the leading-leg. The phase shift is applied on this leg. This waveform does not need an over-current.

Pole circuits
Various series resonant circuits can be used as pole circuits. They can be classified in two types: peak or rectangular.
Peak waveform current for the pole of the lagging-leg:
- The three series resonant circuits in parallel quoted by Pr. Sadarnac,
- The half bridge network with L gives a triangular current,
- The series resonant circuit,
- The series resonant circuit with peak limitation by diodes

Rectangular waveform with low current for the leading-leg:
A half-bridge network with LC in series-resonance and clamped diodes on the resonant capacitors is used for the pole of the leading-leg.

Analysis of the half bridge network
This circuit is only an inductor L_{pt} placed between the pole and a constant voltage at E/2 (mid-point of two big capacitors). The current waveform is triangular with a peak value I_{pt}:

$$\hat{I}_{pt} = E \Big/ 8.L_{pt}.f_{sw}$$

It may be used for the lagging leg.

Figure 4 shows a ZVS Phase Shifted Inverter with two different pole circuits giving a rectangular waveform for one and a triangular for the other.

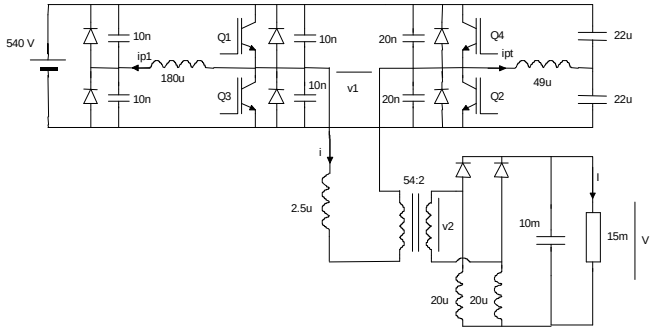

Figure 4: ZVS Phase Shifted Inverter with pole circuits

Analysis of the Lp, Cp, D network

A functioning condition is $C_p > C$, then

$k_c = C_p/C > 1$

The natural frequency of the resonant network is f_p

$$f_p = \frac{1}{2\pi\sqrt{2C_pL_p}} = \frac{\omega_p}{2\pi} \qquad \text{let} \qquad k_f = f_p/f_{sw}$$

For a same peak current $\hat{I}p$ the rate of flat top duration is a function of k_f , simulations give approximately (Fig 5)

k_f	0.85	0.9	1	2	3
flat top rate	1%	6%	22%	56%	72%

With $$L_p = \frac{E/I_p}{2\pi.k_f.f_{sw}} = \frac{E/I_p}{\omega_p}$$

And

$$2C_p = \frac{I_p/E}{2\pi.k_f.f_{sw}} = \frac{I_p/E}{\omega_p}$$

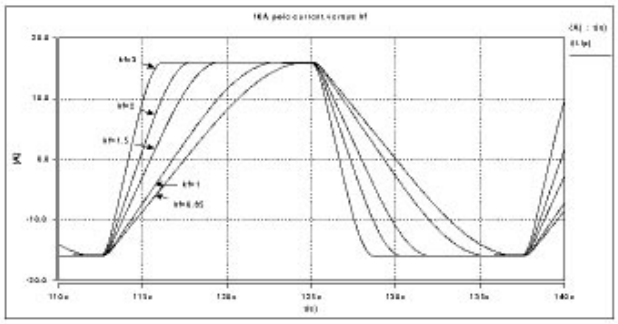

Figure 5: Pole current versus k_f

The peak amplitude (Fig 6) is given by the following expression where k_c is the variable:

$$\hat{I}_p = E.2\pi.k_f.f_{sw}.2.k_c.C = E.2.k_c.C.\omega_p \qquad (2)$$

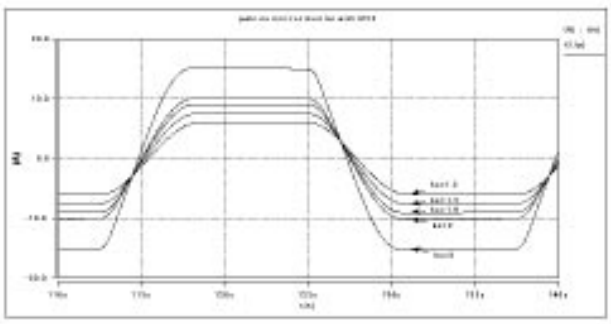

Figure 6: Pole current versus k_c

The figure 6 is drawn with C=10nF, E=505V and a constant $k_f = 2$ which gives a flat top duration of 6.5 to 7µs almost independent of the peak current.

Zero Voltage Switching conditions with poles

For the leading leg (subscript b)

The inverter current and the pole current act in the same direction. The worst case is found for no current in the transformer. During the commutation the voltage of C_p is constant, then the minimum pole current is:

$$I_{1b} = E\sqrt{2C/L_{pb}} \qquad (3)$$

Calculations and simulations have to determine the value of the components for the pole circuits as a function of the snubber capacitors. For the transitions with great variation of phase (90°) at each change, a flat top rate of 50% (k_f = 1.9) is required and for the amplitude the relation (2) must be greater than the relation (3). But the ratio k_c is free (but >1) for example $1.2 < k_c < 2$ and therefore the amplitude also. Then the inductance is:

$$L_{pb} = \frac{1/2k_c.C}{(2\pi.k_f.f_{sw})^2} = \frac{1}{2k_c.C\omega_p^2}$$

For the lagging-leg (subscript a)

The worst condition happens when the snubber capacitor current i_c changes sign before the capacitors (voltage v_c) are charged or discharged. This occurs when the inverter current is negative.

The second order network contains L_{lk}, 2C. I_p is nearly constant; the calculation gives the sinusoidal variation:

$$i_c = -(I_{1a} + I_{pa}).\cos\omega.t$$

$$v_c = E - \sqrt{L_{lk}/2C}.(I_{1a} + I_{pa}).\sin\omega.t$$

The limit is nearly reached when the voltage v_c is zero at a quarter of natural period, at this time (t_c) the inverter current I_{1c} is opposite to the pole current I_{pac}. Figure 7 shows this commutation.

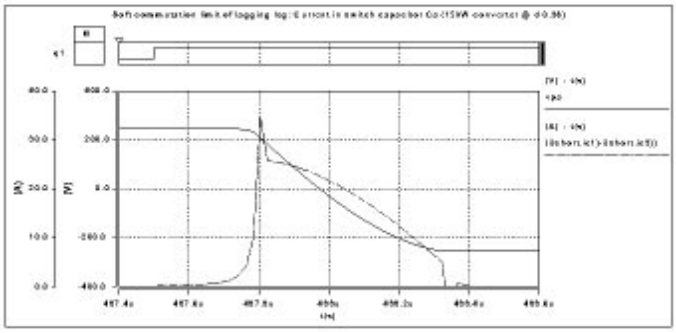

Figure 7: Optimal commutation (α =0.56)

- At the turn-off instant the inverter current is $I_{1a} = -\beta.I_{1c}$ with $0<\beta<1.1$ (see figure 3)
- At the end of the capacitor charge, the pole current has slightly decreased ($I_{pac} = \gamma.\hat{I}_{pa.}$ with $0.75<\gamma<1$).

Thus $\alpha = 1/(1+\beta.\gamma)$ and finally $0.5 < \alpha < 1$.

The required pole current must have a flat top of:

$$\hat{I}_{pa} = \alpha.E\sqrt{2C/L_{lk}}$$

This formulation is simple because α includes the values β and γ.

The optimisation of the pole components must give the current $\hat{I}_{pa}$. With the series resonance clamped by diodes we can take $k_f = 0.85$ to have a nearly sinusoidal waveform (1% flat top) and define the inductance and the capacitor:

$$L_p = \frac{E/I_p}{2\pi.k_f.f_{sw}} = \frac{E/I_p}{\omega_p} \qquad \text{and} \qquad 2C_p = \frac{I_p/E}{2\pi.k_f.f_{sw}} = \frac{I_p/E}{\omega_p}$$

The components of the two poles are calculated for C=10nF and E=505V. The switching frequency is 40 kHz.

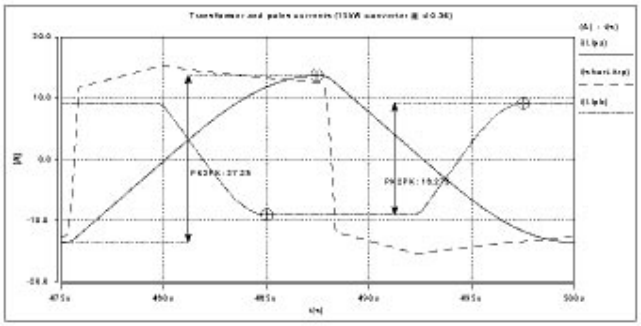

Figure 8: Optimal Poles and Inverter Currents

For the leading leg, taking a clamped resonant circuit giving a current with 53% flat top duration (k_f=2) and whose k_c=1.81:

$$C_{pb} = 18.1nF\ ,\ L_b = 109\mu H\ ,\ I_{pb} = 9.19A.$$

For the lagging leg, taking a clamped resonant circuit giving a current but with small flat top duration (k_f=0.85) and whose $\alpha = 0.75$:

$$C_{pb} = 85nF\ ,\ L_b = 129\mu H\ ,\ I_{pb} = 18.35A.$$

The simulation shown in figure 8 has pole currents whose amplitudes are exactly as calculated.

Minimisation of the power losses

A calculation of the losses in the IGBT was made with MATLAB® software to find a minimum versus the snubber capacitor. A bigger capacitor reduces the turn-off losses but implies a bigger pole current, and thus increases the conduction losses in the switch and in the pole circuit inductance. A minimum value of the losses versus the snubber capacitors was found. With the use of poles, total losses are divided by two.

For the leading leg in Figure 9 it is possible to appreciate the benefits of the pole system. The losses can be reduced to 55 %, in a region where the losses achieve the minimum value, with the snubber capacitor chosen between 10 nF to 40 nF.

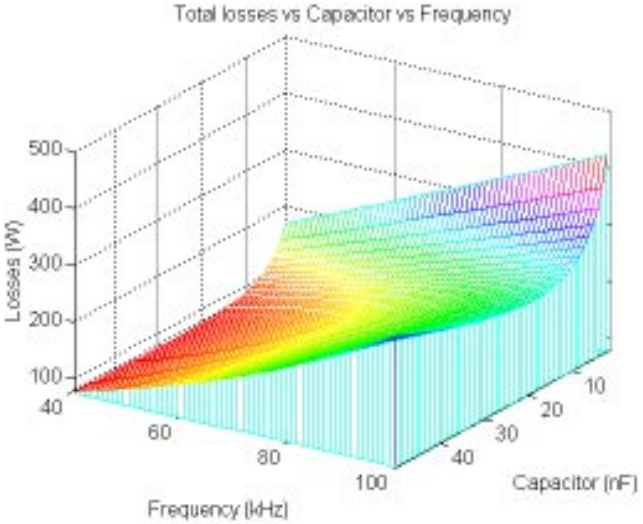

Figure 9: Total losses in leading leg switches vs frequency vs snubber capacitor

As the graphic (figure 9), shows an increase of the snubber capacitor above 10 nF does not imply a decrease of power losses. So the choice will be 10 nF for the leading leg snubber capacitor.

For the lagging leg in Figure 10, it is possible to appreciate the benefits of the pole system. The losses can be reduced below to 50 %, with the snubber capacitor chosen bigger than 10 nF.

As the graphic (figure 10) shows, an increase of the snubber capacitor above 20 nF does not imply a decrease of power losses. So the choice will be 10 to 20 nF for the lagging leg snubber capacitor.

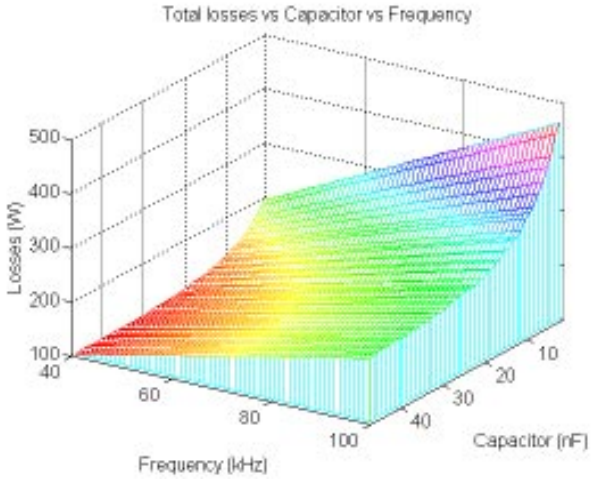

Figure 10: Total losses in leading leg switches vs frequency vs snubber capacitor

Prototype

The [1000A, 15V] prototype has been designed and built as described below.

Power converter design

A 400V three-phase rectifier produces the supply voltage. It uses IGBT switches in dual-thyristor logic with a 40 kHz fixed switching frequency. Only 5.6 nF snubber capacitors are added on each switch to obtain a total value of 10 nF.

Transformer and diodes

To minimise the voltage drop due to the rectifier diodes in a power converter with high output current, a full bridge structure was rejected in favour of a half bridge design. As centre-tap construction for the transformer implies some difficulties, we use the Sadarnac structure [5], which duplicates the filter inductance and puts it in series with each rectifier diode.

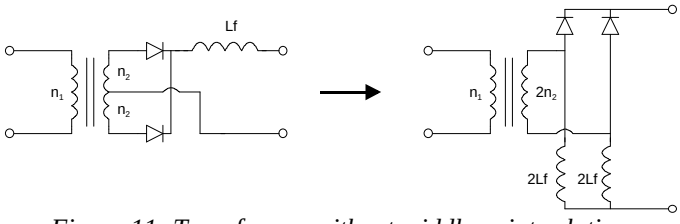

Figure 11: Transformer without middle point solution

Taking into account an effective duty cycle chosen at 0.9 and a minimal input voltage of 505V (ac mains –5%) the L_{lk} value is 8.5µH (2 µH for transformers and 6.5 µH added).

The turn ratio 27 is obtained, taking the losses in diodes and filter inductance resistor (5% of the 15mΩ), with the approximate formula with the maximal duty cycle δ=1:

$$V_2 = E\frac{\delta}{n} - \frac{4.L_{lk}.f_{sw}.I}{n^2}$$

The diodes are high-current and low-voltage type, so the voltage drop has to be very small to decrease the conduction losses.

The high output current requires the use of several transformers in parallel as well as the rectifier stages and the filter inductance. A design with 6 modules in parallel has been chosen, with the following components chosen.

Transformer ratio	Diodes	Filter inductance
27 (54:4)	BYV255V200 {255A,200V}	6*2*Lf

The L_f value is 10/6 µH

RC networks in parallel with the HF rectifier are used to damp the oscillations between the leakage inductance of the transformer and the capacitance of the Schottky diodes. Common mode inductors are placed on the dc voltage input and on the transformer primary to reduce the current via the parasitic capacitance (400pF per transformer) between transformer primaries and secondaries.

Poles

With snubber capacitors (10nF) the soft commutation would be lost for inverter current lower than a 50-65 percent of the maximum inverter current.

For the lagging leg a small clamped resonant circuit was built in accordance with the following calculated values:

k_f=0.866 α=79.07% which give L_{pa}=120µH , C_{pa}=88nF and I_{pa}=19.34A (with E=505V).

For the leading leg a clamped resonant circuit was built in accordance with the following calculated values:

k_c=2.76 k_f=1.545 which give L_{pa}=120µH , C_{pa}=27.6nF and I_{pa}=10.82A with 5µs flat top duration (with E=505V)..

Simulations

After the design, the power converter schema was simulated and all the principal waveforms were verified. The IGBT used in the simulation has the same characteristics as the dual thyristor, with inherent turn-on condition at zero voltage.

Digital simulations using SABER® software confirm the performance. Good behaviour was observed over the whole output current range and with fast change of phase-shift.

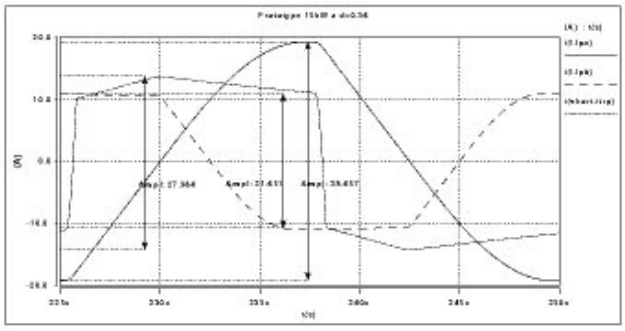

Figure 12: Current in leading pole (ip_b) and lagging pole (ip_a) compared with the primary current (i).

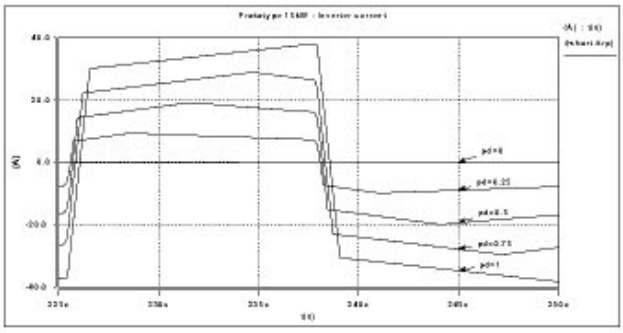

Figure 13: The primary current (i) over whole range.

The minimum output current is not exactly zero because the transformer voltage is not zero during the different discharge time of the snubber capacitors by the pole currents. To reduce this minimum current to 0.3A the leading pole current is greater than the one required by the soft commutation condition.

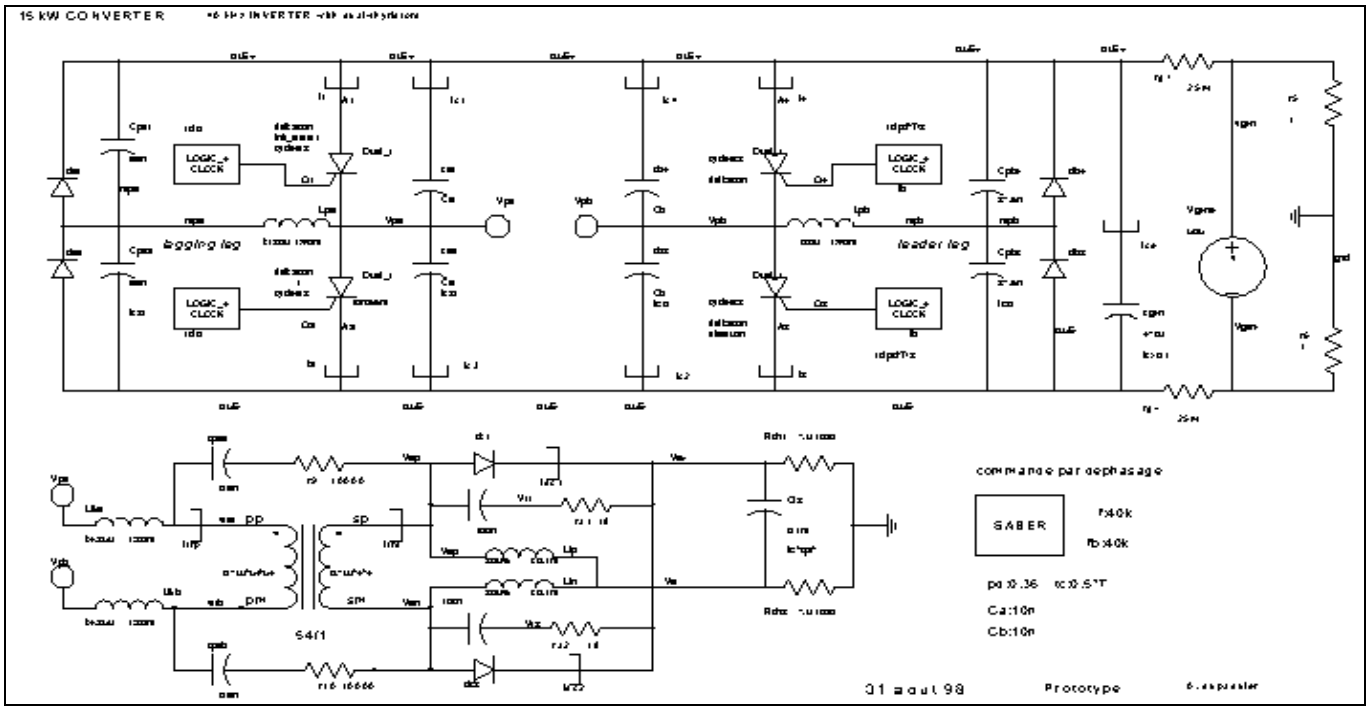

Figure 14: Simulation sketch for 15 kW converter

For a converter range between 3% to 100% the use of a lagging pole current only could be an economic solution. However it gives a minimum output current of 10%I and so this approach is not preferable.
A triangular waveform current was also tried for the pole of the lagging leg, but some low-frequency current instability was observed due to a slight variation of the mid-point voltage E/2 (capacitors of finite value).

Prototype results.

The experimental pole currents (Figure 15, 16, 17) have the same amplitude as the calculated and simulated amplitudes. Soft-commutation was effective for the whole duty range with 10 nF snubber capacitors (only capacitors of 5.6 nF are added).

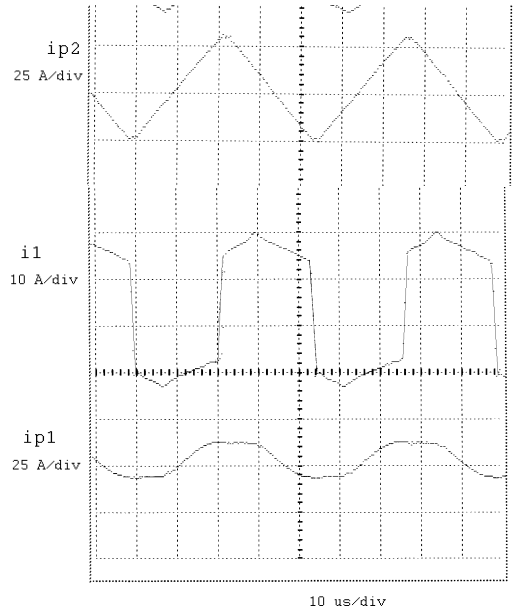

Figure 15: Current waveforms i_{pt} triangular lagging pole i_1, transformer, i_{p1} rectangular leading pole

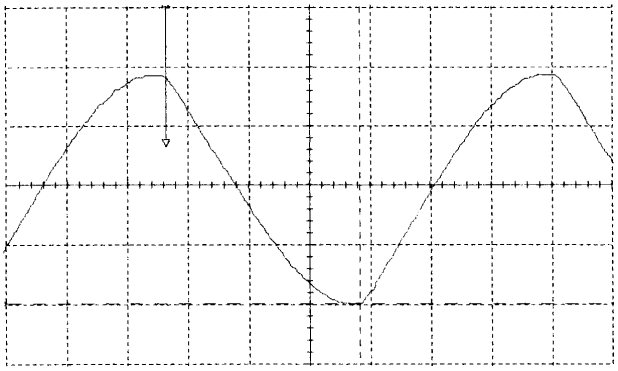

Figure 16: Current in lagging pole (19.5A with E=520V) vertical scale: 10A/div, horizontal scale: 4µs/div.

The minimum pole current to obtain the soft commutation is lower than the experimental one. The minimum output current was 1A.

The total efficiency was about 80%. It is measured between the output power and the dc input power (after the rectifier). This value is severely affected by the losses in the high-current rectifier. Figure 18 shows the relationship efficiency versus output voltage.

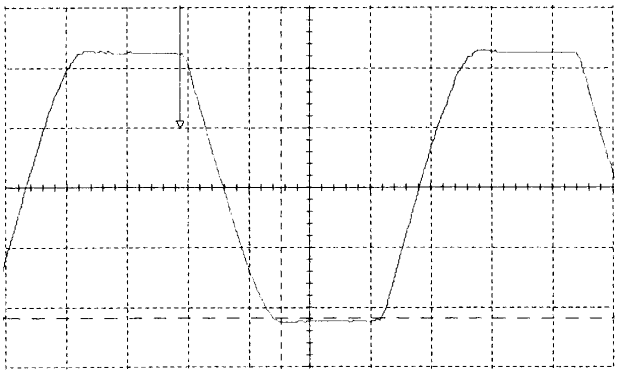

Figure 17: Current in leading pole (11.13A with E=520V, 40 kHz switching frequency) vertical scale: 5A/div, horizontal scale: 4µs/div.

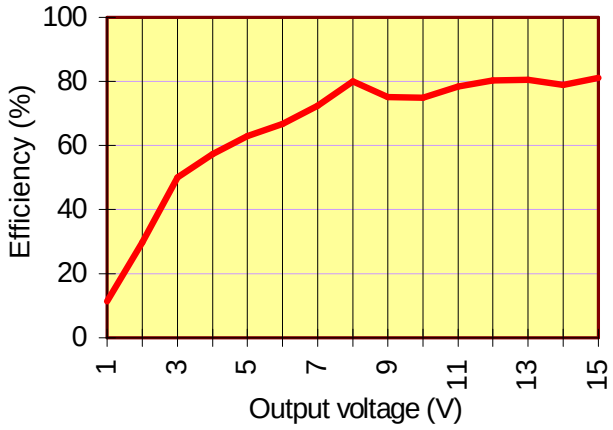

Figure 18: Efficiency

Conclusion

Due to dual-thyristor logic and pole circuits, soft commutation can be obtained over the whole duty range of a phase-shifted converter.
The results of the work described in this paper prove that, the efficiency and the switch stresses can be improved with addition of small passive components.
This topology presents many advantages for the LHC high-current, low-voltage converters.

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