TTC Distribution for LHC Detectors

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Abstract

At each of the CERN LHC experiments, timing, trigger and control (TTC) signals must be distributed to numerous electronic systems from a single location in the vicinity of the central trigger processor. A multichannel optical distribution system has been developed which can broadcast the signals to several thousand destinations from a few relatively high power laser sources over a passive optical fiber network with uncontrolled path lengths.

The system delivers the LHC timing reference and first-level trigger decisions with the corresponding bunch and event numbers. It incorporates facilities to compensate for particle flight times and detector, electronics and propagation delays. In addition it provides for the simultaneous transmission of synchronized broadcast commands and individually-addressed controls and parameters, such as channel masks and calibration data.

I. Introduction

All the subdetectors of the proposed LHC experiments require quite extensive distribution systems for the transmission of timing, trigger and control signals to numerous electronic systems located in the detector caverns and the underground electronics halls. A common solution to this TTC system requirement is expected to result in important economies of scale and permit a rationalization of the development, operational and support efforts required.

In conjunction with RD27, LHCC/LEB Project RD12 [1] has developed a multi-function optoelectronic TTC distribution system to meet the requirements of the different subdetectors of the experiments. It has been adopted for the ATLAS [2] and CMS [3] TTC system backbones and is currently being considered for ALICE and LHC-B [4].

In each experiment the TTC system must control the detector synchronization and deliver to the front-end electronics controllers the necessary fast signals and messages that are phased with the LHC clock, orbit or bunch structure. These include the 40.08 MHz bunch-crossing clock, level-1 trigger decisions, bunch and event numbers, as well as test signals and broadcast commands.

The system incorporates programmable coarse and fine deskew facilities to compensate for different particle flight times and detector, electronics, propagation and test generator delays. It can also transmit asynchronous slow controls and data such as individually-addressed channel enables and calibration parameters to several thousand destinations.

II. Architecture

To minimise the level-1 trigger latency, the trigger processors and central trigger logic will be located in the underground electronics halls as close as possible to the special direct trigger cable ducts communicating with the detector caverns. A small number of relatively high-power laser sources will be installed at these locations to distribute the TTC signals to their destinations through entirely passive all-glass networks composed of a hierarchy of optical tree couplers (see Fig. 1). At each destination, a special timing receiver ASIC (TTCrx) delivers all the signals required by the electronics controllers.

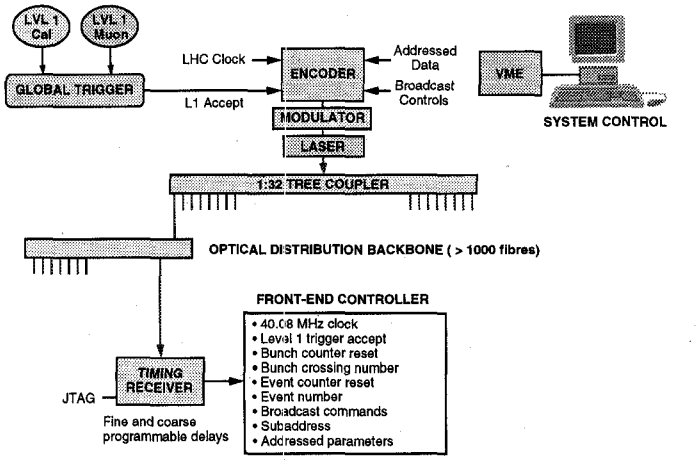

Fig. 1 TTC distribution components

The tree architecture of this distribution network is well matched to the physical configuration of the underground areas, the co-located signal sources and the dispersed destinations. It requires considerably less optical fiber than a star configuration of point-to-point links from a central fanout and permits the flexibility of extensive intermediate connectorization, since only the final destination connectors contribute significantly to the cost. The optical tree couplers have small size, low mass and unlimited bandwidth. They require no operating power and are potentially highly reliable [5].

Each laser transmitter serves a TTC distribution zone which is typically associated with a major component of a subdetector, such as an entire end-cap or barrel section. Owing to the small number of laser sources employed for the complete system, it is economically feasible to optimise performance and reliability by equipping all of them with full three-term feedback controllers providing precision temperature regulation and incorporating comprehensive low-noise stabilisation and protection circuitry.

Furthermore, continued improvements in the efficiency, reliability, intensity noise, spectral and modulation characteristics of laser diodes are to be expected during the years preceding start-up of the LHC. As new devices become available, the architecture adopted allows the TTC system to

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be upgraded much more readily than if thousands of individual LED sources had been employed.

III. LASER TRANSMITTER

Several considerations have led to the selection of 1310 nm as the operating wavelength for the TTC systems. At this wavelength the chromatic dispersion of normal optical fiber is negligible, so that Fabry-Perot laser diodes operating in multiple longitudinal modes can be used and the effect of the chirping caused by direct modulation is minimised. The overall length of fiber in each distribution path being only about 100 m, fiber attenuation is negligible. Hence in a short-range timing distribution system the minimum-dispersion wavelength of 1310 nm is more appropriate than the minimum-attenuation wavelength of 1550 nm.

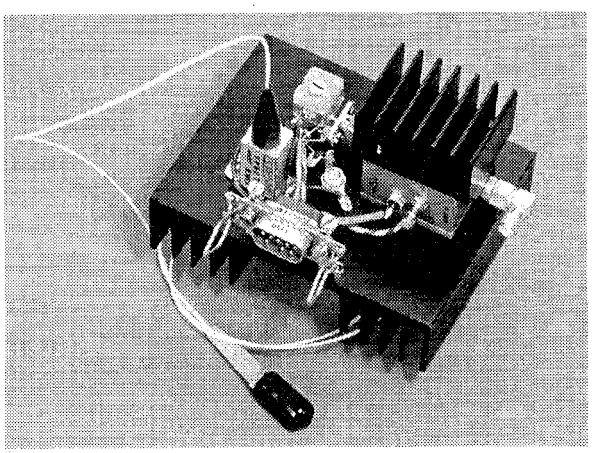

Fig. 2 Laser transmitter head module

Multimode Fabry-Perot lasers are less expensive and available with higher output powers than distributed-feedback types. They are considerably less sensitive to optical feedback noise [6] and as a result have been found to perform satisfactorily without the use of isolators in spite of the Fresnel reflection from multiple inexpensive (non angle-polish) connector interfaces in the distribution path.

At 1310 nm, even inexpensive LED sources having a relatively broad output spectrum can be used successfully for low-power test systems, whereas at 830 nm the fiber dispersion of 80 ps/nm.km (1 ns for a 125 nm wide source and 100 m length of fiber) excludes them from applications requiring precise timing. While somewhat higher laser powers [7] are currently available from the most expensive short-wavelength AlGaAs lasers than from long-wavelength InGaAsP diodes, this gap is narrowing and the projected lifetime of the latter devices is more than an order of magnitude longer.

Step index multimode fiber is unsuitable for this application because of its large multimode dispersion, while the use of monomode fiber would incur high optical tree coupler and connector costs and limit the coupling efficiency from high power laser sources, which have divergent output beams. On the other hand, 50/125 μm graded index fiber can provide adequate bandwidth over the short path length (several GHz for 100 m) and is available in boron-fluorine doped form with good radiation tolerance characteristics.

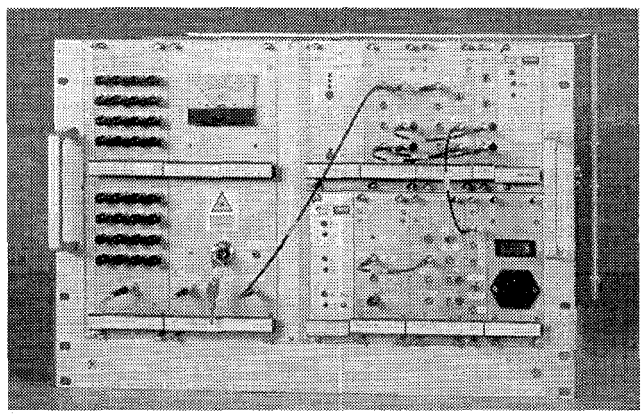

Fig. 3 TTC transmitter crate

Graded index fiber multimode dispersion varies with optical wavelength. Fiber that has low dispersion at 1310 nm is substantially cheaper than fiber that has the same dispersion at 830 nm or which has a compromise performance at both windows. Finally, both the appropriate photodetectors and the optical fiber itself are more radiation resistant at 1310 nm [8].

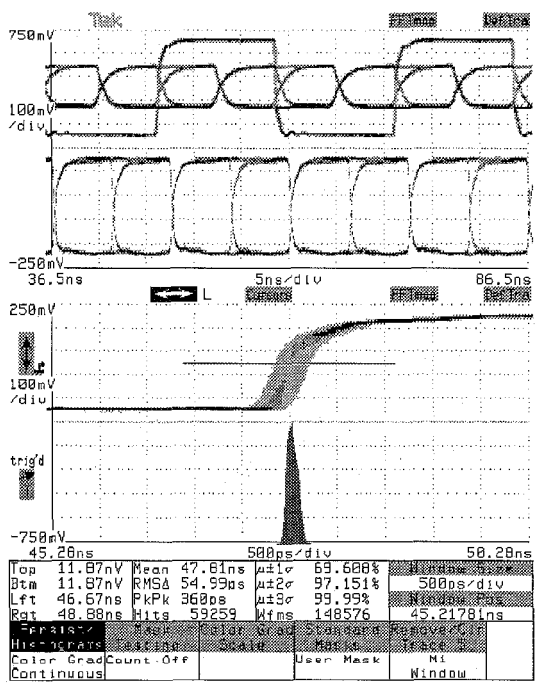

Fig. 4 *Upper trace*: optoelectronic receiver output and recovered clock
Center trace: 160.32 MBaud TDM encoder output
Lower trace and histogram: recovered clock window

External modulators are normally polarisation-dependent and have significant insertion loss. With direct modulation of currently available laser diodes it is quite feasible to broadcast reliably to groups of 1024 channels per transmitter through

100 m of 50/125 μm graded index fiber and two levels of 1:32 passive optical tree coupler.

Fig. 2 shows the laser head module of the transmitter. It incorporates a 0.4 W RF amplifier with a bandwidth of 10 MHz - 1 GHz, an inexpensive bias tee fabricated with ferrite beads and an adjustable matching network for the very low impedance input of the laser diode. The laser has an integral Peltier cooler element and monitor thermistor, which permits a compact assembly. A complete transmitter subsystem crate is shown in Fig. 3.

This transmitter is capable of distributing the TTC signals through three levels of 1:32 tree coupler (1:32768 fanout). In practice more modest fanouts will be employed to allow adequate margins for component tolerances and radiation-induced receiver degradation. Fig. 4 indicates the performance when transmitting PRBS data at 160.32 MBaud with an optical fanout of 1:1024 and fiber length of 100 m.

The overall RMS jitter from the LHC clock input at the transmitter to the remote timing reference outputs, as measured by a wide bandwidth analyser without any filtering or smoothing, is in this case 55 ps. This is less than the spread in event origin time due to the LHC bunch collision length (180 ps RMS) and expected longitudinal phase modulation of the circulating beams [9].

IV. ENCODING

As indicated in Fig. 5, the laser modulator is driven by an encoder which is phase-locked to the LHC clock and linked to an associated trigger select and serializer TTC-VMEbus interface (TTCvi) module.

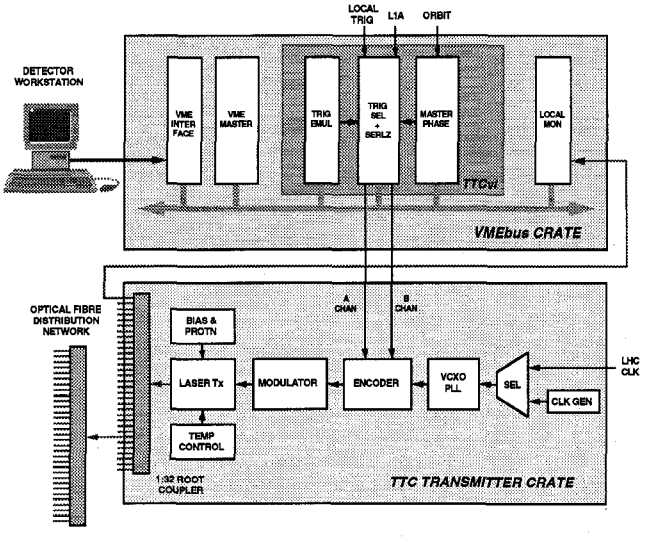

Fig. 5 TTC transmitter elements

The TTC system must deliver broadcast and individually-addressed signals to several thousand destinations. An important reduction in receiver cost, power consumption, size and mass is achieved by encoding these signals in such a way that they can be received by a single optoelectronic detector per destination. The encoding should also allow the signals to be transmitted at a relatively low rate compatible with the photodetector/preamplifier devices that are being manufactured in the highest volumes and at the most competitive prices for the LAN market.

The code employed must be balanced (DC-free) so that the phase of the extracted timing reference is quite independent of the level-1 trigger data being transmitted. The signals must be reliably decoded by receivers that may be subject to radiation-induced sensitivity changes and offset shifts, so that the use of pulse amplitude modulation and non-binary transmission requiring multiple detection thresholds is excluded.

Evaluation of a number of signalling alternatives offering different trade-offs between channel efficiency and synchronization precision led to the selection of a scheme whereby two data channels are time-division multiplexed (TDM) and encoded biphase mark at 160.32 MBaud (four times the LHC bunch-crossing rate). This is sufficiently close to the standard Sonet OC-3 (CCITT SDH STM-1) rate of 155.52 MBaud that an expanding range of photodetector/ preamplifier components produced in increasingly high volume is appropriate.

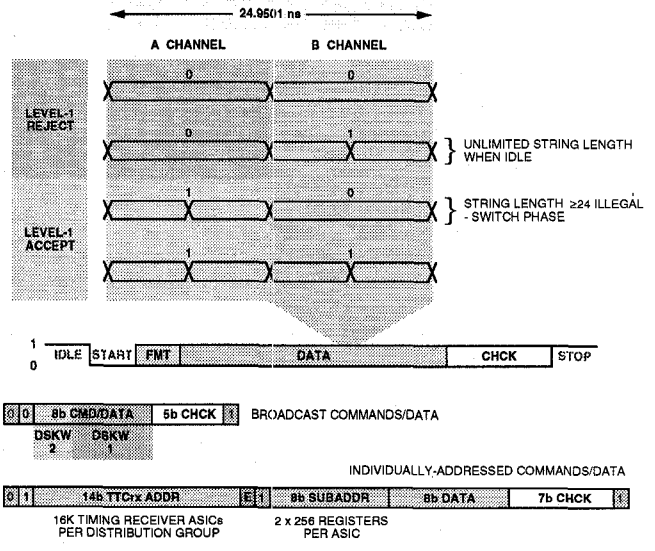

Fig. 6 TTC signal encoding

The four symbols which can be transmitted in each bunch-crossing interval are shown in Fig. 6. The DC offset is well bounded and timing reference signal transitions are generated at the start and finish of every such interval. The encoder 160.32 MHz VCXO is phase-locked to the LHC clock, or a local clock generator, by a PLL employing a high gain active loop filter with low offset drift.

Techniques have already been developed by CERN for the transmission of stabilized radio-frequency phase references over long optical fiber links [10]. By means of an oscillator having low internal noise and a narrow loop bandwidth, a 160.32 MHz output jitter of less than 10 ps RMS can be maintained for a 40.08 MHz reference clock input jitter of several hundred ps, as shown in Fig. 7. In this test the jitter of the reference clock was increased by sending it to the TTC transmitter crate over an optical fiber link with artificially increased attenuation.

The "prompt" TDM A Channel, which is designed for minimum latency, is dedicated to the broadcasting of the first-level trigger-accept signal, delivering a one-bit decision for every bunch crossing. The B Channel transmits broadcast and individually-addressed commands or data using the frame format shown in Fig. 6.

During a short programmable interval at the end of the 3.17 μs LHC extraction kicker gap in one of the beams, other transmissions are held off so that the bunch counter reset signal can always be broadcast with exactly the required phase. Although this signal arrives at the receivers at different times because of the different lengths of the optical fiber paths, it experiences the same propagation delay to any receiver as the trigger-accept signals and so does not require separate delay compensation.

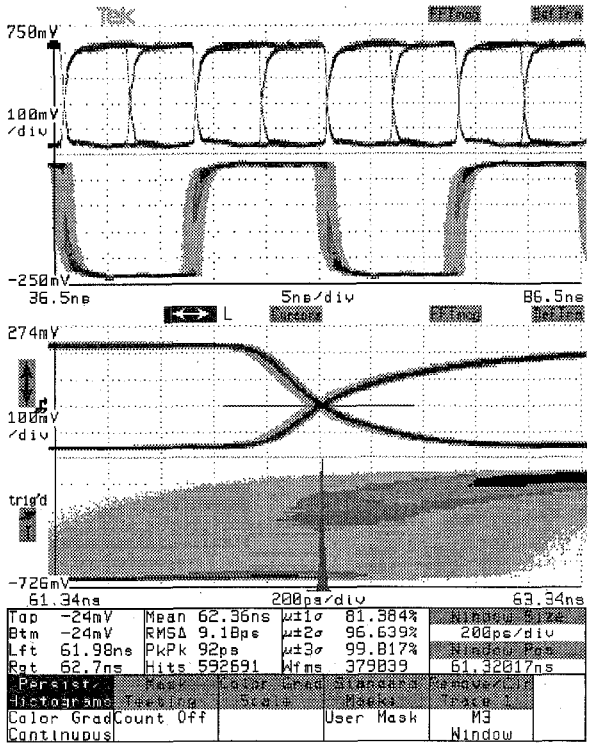

Fig. 7 *Upper trace:* encoder output (PRBS data)
Second trace: noisy reference clock input
Third trace and histogram: encoder jitter
Lower trace : reference clock input jitter

High priority is assigned to other synchronous broadcasts, while in the background the timing calibration controller can continuously scan all the timing receivers transmitting fine deskew adjustments to compensate for phase wander due to changes of temperature, fiber tension, optical wavelength, signal amplitudes, voltage drifts and component ageing.

The addressing scheme provides for up to 256 external and internal subaddresses associated with each of up to 16K timing receivers in each timing distribution group.

With standard two-channel biphase mark encoding, there is a fundamental ambiguity in the phase of the recovered clock. This is resolved automatically in the receivers by monitoring constraints on the data structure imposed by the B Channel data format. Hamming checkbits permit the forward error correction of all single-bit and the detection of all double-bit errors, as well as many others.

V. TTCvi VMEbus Interface

The TTC-VMEbus interface (TTCvi) module [11] interfaces the TTC system to the Central Trigger Processor (Global Trigger) and to the control processors or development workstations which generate commands and data to be transmitted to the electronics controllers. The module delivers the A Channel and B Channel signals to the TTC transmitter crate for multiplexing, encoding, optical conversion and distribution to the timing receiver ASICs at the destinations.

The TTCvi incorporates a programmable trigger source selector and an internal trigger emulator for test purposes. To minimise the possibility of configuration errors, the characteristics of the module and the signal routing which it controls are fully programmable from the VMEbus.

The B Channel signals can be in either of two formats:

• Short-format synchronous or asynchronous broadcast command/data cycles. The timing of the synchronous cycles is fully programmable relative to the external LHC orbit signal (or to an internally generated one for test purposes). They are used for the broadcasting of the bunch counter reset signals which control the phases of the TTCrx bunch counters, and for the transmission of other fast synchronous broadcast controls and test commands or data.

These commands are deskewed in the TTCrx ASICs to compensate for individual differences in fiber propagation delay, electronics and detector delays and particle times-of-flight.

• Long-format asynchronous individually-addressed or broadcast command/data cycles. The timing of these cycles relative to the LHC orbit is indeterminate and they are not individually deskewed in the TTCrx ASICs. They are used for the transmission of parameters, test data, calibration data and non time-critical commands, such as channel masks, to the front-end electronics.

After each trigger accept is transmitted, the contents of the 24-bit event counter in the TTCvi can optionally be broadcast together with an 8-bit trigger type parameter which is received from the Central Trigger Processor via a front panel connection. This broadcast, which is intended for check purposes, is made asynchronously and takes about 4.4 μs if the B Channel is free.

The TTCvi contains about 300 components including 10 Altera FPGAs and 20 synchronous FIFOs.

VI. Optoelectronic Receiver

Although it is foreseen that LHC detectors will have many optical links for data readout and monitoring purposes, the TTC network may be one of the few systems requiring hundreds of optoelectronic receivers located on and within certain subdetectors. The photodetectors used should have high optical signal responsivity, low sensitivity to ionising and neutron irradiation and fast rise times at a low reverse bias voltage, preferably less than 3.5v. InGaAs PIN diodes are

superior to normal Si photodiodes in most technical *characteristics* including radiation hardness.

The current packaging configuration approach for TTC optoelectronic receivers is a subminiature connectorized InGaAs PIN + Si bipolar preamplifier device with differential outputs connected directly to a separately packaged low-power timing receiver ASIC containing the postamplifier/ AGC circuit followed by all the necessary analogue and digital functions.

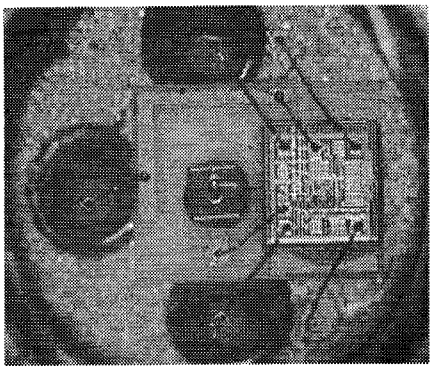

Fig. 8 PIN diode + Preamplifier

The PIN + preamplifier (Fig. 8) has a bandwidth of 160 MHz and incorporates a second amplifier for power supply noise cancellation. It has shown little performance degradation after 20 MRad ^{60}Co irradiation [12].

Several manufacturers are currently introducing monolithic InGaAs/InP receivers in which PIN or MSM photodiodes are combined with a transimpedance amplifier using HBTs or MODFETs. Although clear performance advantages relative to hybrid designs have yet to be achieved, these OEICs could eventually open the way to the high volume fabrication of very cheap components, including "smart connectors" integrating all the standard optoelectronic receiver functions.

VII. Optical Connector

While conventional optical single-fiber connectors, such as the popular ST/PC type, are quite appropriate for use in small numbers at the TTC transmitters, they are too massive for use at receivers in a particle physics detector and often contain high-permeability carbon steel springs and circlips. They are inconveniently large even for mounting on some high-density modules in external electronics readout crates.

In collaboration with our industrial partners, a new subminiature "RD12 Connector" family has been developed for this application. The connector, which is non-magnetic and manufactured only from proven radiation-hard materials, mates with an active device mount designed to accommodate the PIN + preamp with an absolute minimum of additional mass and volume (see Fig. 9). A prototype series has been manufactured and pre-production testing has been carried out, including vibration tests specified by an aircraft manufacturer which is one of the potential users of the devices.

The RD12 Connector incorporates a zirconia ceramic ferrule to ensure high reliability, but its diameter is reduced to only 1.25 mm. ARCAP alloy is used for the device housing and polyether etherketone (PEEK), a glass-fiber enhanced thermoplastic material, for the connector shell.

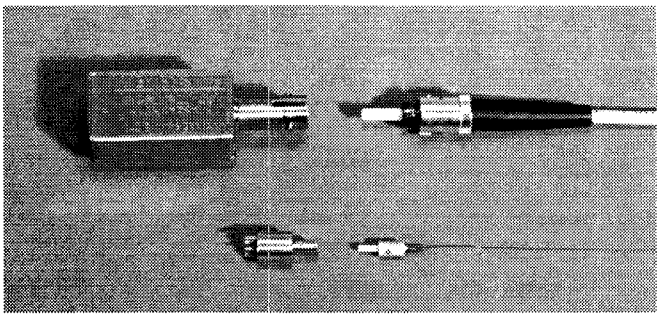

Fig. 9 Conventional ST and subminiature RD12 connectors

The PIN + preamp manufacturer actively aligns the TO-46 devices within the device mounts to ensure maximum responsivity, an operation that can be automated on a production line basis.

The connector family also includes a subminiature coupler for connector-connector interfacing at bulkheads. The coupler, which has a mass of less than 0.7 g, is compared in size with its conventional ST counterpart in Fig. 10.

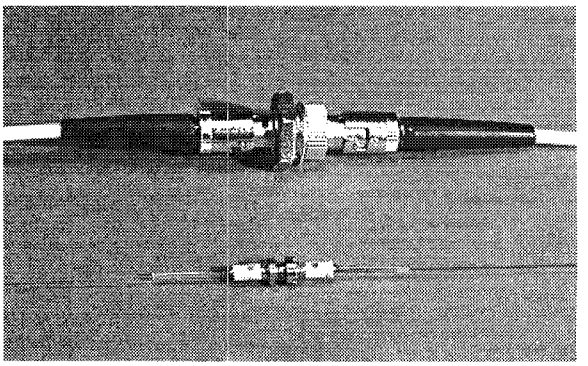

Fig. 10 Conventional ST and subminiature RD12 couplers

No really tiny affordable connector/device-mount/coupler family for single optical fibers has so far been brought to the market. The RD12 Connector may meet this need in a number of future applications in other areas where very small size and low mass are important.

VIII. TTCrx Timing Receiver

A special timing receiver ASIC (TTCrx) has been developed for the TTC systems [13]. As indicated in Fig. 11, this VLSI chip [14] accepts a single input from the TTC photodetector/ preamplifier and generates a full range of decoded and deskewed signals for the electronics controllers. The ASIC comprises an analogue part (including the postamplifier, automatic gain control circuits and clock recovery/fine deskew PLLs) and a digital part (including the decoding, demultiplexing, coarse deskew, bunch counter, event counter and command processing sections). Any

functions not required for a particular application can be disabled to minimise the TTCrx power consumption.

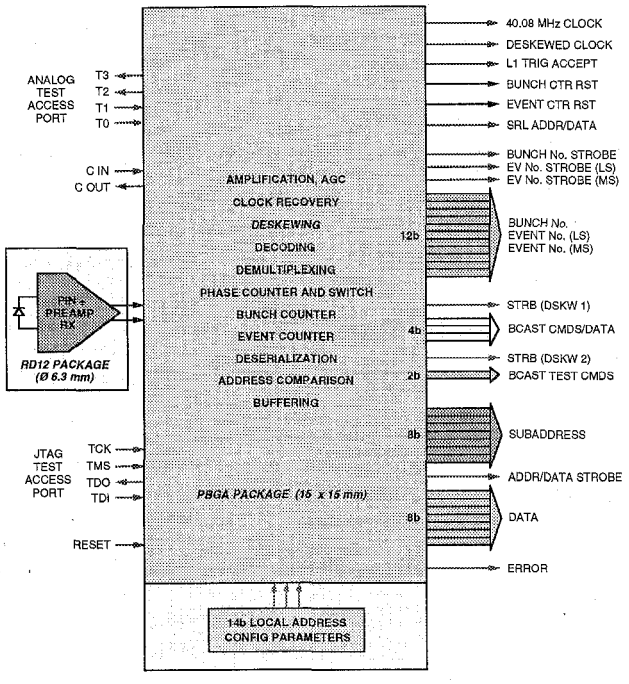

Fig. 11 TTCrx timing receiver ASIC

With suitable logic, the receiver clock recovery function can be performed by a charge pump PLL with voltage-controlled delay elements. With this technology the fine deskew of the periodic clock output can be implemented by the addition of a multiplexer since the loop inherently provides a range of output phases over the bunch-crossing interval. The technology is appropriate for monolithic integration without the use of any external components. A non-deskewed clock output is also provided for use by processors which cannot accept the minor duty factor distortion which occurs at the moment when the phase of the deskewed output is being changed by the selection of a new tap by the multiplexer.

In order to obtain a fine deskew resolution less than the gate delay, two staggered PLLs are incorporated [15], one having 16 and the other 15 stages. By appropriate output tap selection the phase may be adjusted over the full 25 ns bunch-crossing interval in steps of 104 ps. For coarse delay compensation, virtual programmable-length shift registers provide a range of 16 bunch-crossing intervals (total 399 ns) which allows a substantial margin beyond the possible maximum variation due to differences in time-of-flight and optical fiber path length. These functions, as well as broadcast command generation and bunch and event counter resets, are controlled by the data transmitted over the B Channel.

It is assumed that the optical fiber path lengths in the TTC distribution system will be dictated by installation convenience alone and that their propagation delays will not be known precisely. Glass optical fiber is a rather elastic medium so that, even if the fiber lengths were initially cut with precision, significant changes could occur during installation and when opening and closing the detectors. However, records may be kept so that a data base of approximate delays is available for the initial setting of the deskews before beam is available to allow more precise tuning.

The bunch counter reset signal is also provided for external use but a 12-bit counter, which delivers a unique bunch crossing number synchronously with the corresponding first-level trigger decision, is integrated on-chip. During the 2 clock cycles following a trigger accept, for which the central trigger logic (global trigger) inhibits the generation of new triggers, the corresponding 24-bit event number is delivered on the same 12 output lines as the bunch number. Unlike the bunch counter, the event counter need not be reset periodically but rolls over after every 16M events (about every 3 minutes at the expected level-1 trigger rate of 100 kHz). All the TTCrx event counters are initialised by a broadcast command and may be reset by such a command during any gap in the LHC bunch structure.

The 12-bit bunch number generated by the TTCrx is required by the synchronization algorithms [16] and permits the study of correlations between event data and the LHC orbit. The 24-bit event number suffices to detect possible problems of event ordering or loss in the data readout and event building. Additional information, rendering the event identification unique, will of course be added to the data at later stages of the DAQ chain.

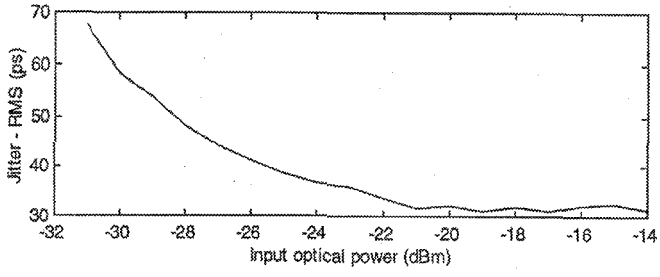

Fig. 12 TTCrx recovered clock jitter

The bunch counter reset, and non-periodic signals such as the trigger decision and broadcast commands, are deskewed by the timing receiver over a 12-bit range; 4 bits for the number of bunch-crossing intervals and 8 bits for the phase within an interval. The broadcast command outputs have two independent coarse deskew registers for the number of bunch-crossing intervals. This is to allow some of them to be used for the generation of test and calibration signals having different delay compensations (excluding time-of-flight but including test signal latency, for example) without having to reload the deskew parameters used for normal running.

The TTCrx implements a functional subset of the JTAG/IEEE 1149.1 standard to allow boundary-scan testing of the on-chip logic and board-level connectivity tests. This strategy may be extended to the subsystem level. A number of special test functions are also provided which allow timing receiver internal parameters and the local addresses to be read back via the data acquisition system for verification.

Prior to implementation in DMILL rad-hard BiCMOS SOI technology, prototype TTCrx chips were implemented in *standard CMOS* and packaged in a large Pin Grid Array (PGA). The inductance of this package was found to have an adverse effect on both the recovered clock jitter and the linearity of the fine deskewing. By means of tests in which a chip was bonded directly to a special printed circuit board it was verified that these problems could be very substantially reduced with more compact packaging.

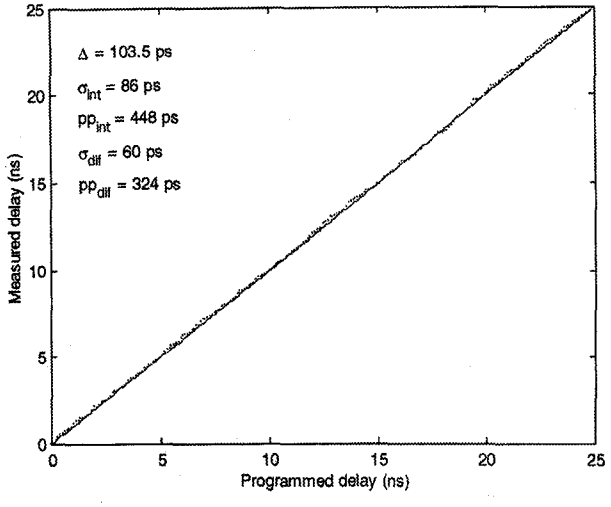

Fig. 13 TTCrx deskew function linearity

A special 15 x 15 mm Ball Grid Array (BGA) package was developed for the TTCrx by a European facility of IBM and this has substantially improved performance. Fig. 12 indicates how the recovered clock jitter (relative to the reference clock generator at the transmitter) varies with the optical power input to the receiver while random triggers and data are being transmitted on the A and B Channels respectively.

The relationship between measured delay and programmed delay for the fine deskew function of the TTCrx is shown in Fig. 13. The RMS delay error is less than 100 ps.

IX. TTCsr PMC Module

In most cases TTCrx ASICs will finally be embedded directly in the electronic systems requiring the TTC signals and services. But for the convenience of users carrying out development work before such integration a TTC simple receiver (TTCsr) board has been developed as a PCI Mezzanine Card (PMC). Such a module is also required for ATLAS Level-3/DAQ prototype development and has other applications in crate-mounted systems.

The TTCsr provides some of the principal TTCrx signals as ECL front-panel outputs, and includes FIFOs to buffer TTCrx data to the PCI port of the module. The different FIFOs store the data associated with each level-1 trigger, the subaddress and data of individually-addressed commands and the broadcast commands and TTCrx responses.

DPMs are used to implement the FIFOs and some of the registers, which allows faster data reading by PCI burst cycles. The DPMs can be written 16-bit wide at 40 MHz on the TTC side and can be read 32-bit wide at 33 MHz on the PCI side.

The module incorporates two FPGAs. One is used for the PCI protocol and includes full PCI slave functionality, the CSR registers and the DPM control. The second includes the control of the FIFOs and the routing from the output buses of the TTCrx to 3 different FIFOs. During the idle cycles when the TTCrx is not dumping data it also writes the counters of the FIFOs to part of a DPM. The functionality of the TTCrx configuration PROM is also included in this FPGA so that its contents can be changed from the PCI bus.

X. Conclusion

The challenge of developing common TTC distribution technologies for the next generation of collider experiments has been tackled in the RD12 Project by a collaboration of CERN groups, associated research institutes and industrial partners.

A system has been developed which multiplexes the first-level trigger decisions with broadcast commands and individually-addressed controls and data and encodes them for optical transmission by a relatively high power laser. It is capable of broadcasting first-level trigger accept and synchronous and asynchronous control signals and data over a passive optical fiber network to over one thousand destinations per laser source.

A VMEbus interface for the system has been developed, as well as subminiature optoelectronic receiver components and a receiver ASIC which delivers the required signals to the electronics controllers with programmable timing.

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