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## **ANALYSIS OF PARAMETER-INDEPENDENT PLLs WITH BANG-BANG PHASE-DETECTORS**

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### **Abstract**

The parameter-independent design of Phase-Locked Loops (PLLs) is investigated for the case that a bang-bang phase-detector is used. Two self-biased CMOS PLL structures are proposed and compared, one leading to a completely parameter- and frequency independent behavior. If the PLL frequency operation is constant and known in advance, however, both structures can be made independent of the transistor  $V_t$  and  $\beta$  parameters.

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# Analysis of Parameter-Independent PLLs with Bang-Bang Phase-Detectors

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## Abstract

The parameter-independent design of Phase-Locked Loops (PLLs) is investigated for the case that a bang-bang phase-detector is used. Two self-biased CMOS PLL structures are proposed and compared, one leading to a completely parameter- and frequency independent behavior. If the PLL frequency operation is constant and known in advance, however, both structures can be made independent of the transistor  $V_t$  and  $\beta$  parameters.

## 1. Introduction

Phase-locked loops are a basic element of clock and data recovery circuits. In order to achieve low jitter, the loop behavior should not depend on variations of any process parameters, and ideally, should also not change with frequency. In the case of High Energy Physics applications, the devices frequently undergo high radiation doses leading to substantial deviations of MOS transistor parameters, especially  $V_t$  and  $\beta$ . Hence a loop behavior independent of these parameters is desirable. A fully self-biased PLL using a standard *phase-frequency detector* can be found in [1]. In some applications, e.g. clock recovery, the use of a *bang-bang phase detector* is more appropriate.

This paper investigates how two different CMOS ring oscillator structures, most often used in current PLLs [1][3][4], can be used to achieve process parameter independence. The first structure uses a simple MOS transistor as voltage-controlled resistor, the second uses a “symmetrical load”, consisting of two equally sized MOS transistors.

## 2. Bang-Bang Phase Detector PLLs

A typical charge-pump PLL is shown in Fig. 1. A bang-bang phase detector consists in the simplest case of a balanced flip-flop. The input signal is thus sampled by the VCO signal, and the decision (either *early* or *late*) is

derived.

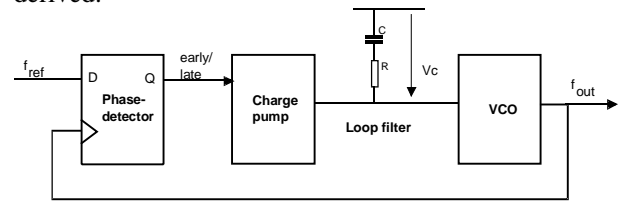


Fig. 1. A typical charge-pump PLL with a bang-bang phase-detector.

In contrast to a phase-frequency detector giving a signal proportional to the phase difference between the input signal and the VCO signal, the decision of a bang-bang phase detector is purely binary, leading to a non-linear loop behavior. The bang-bang phase-detector output usually controls a charge-pump, i.e. a bi-directional current source, steering a constant current in and out the loop filter. The loop filter typically consists of a capacitance and a resistor providing the integral part and the proportional part of the loop filter response, respectively.

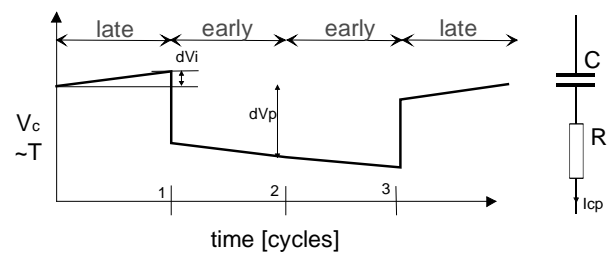


Fig. 2. Typical VCO control voltage behavior using a bang-bang phase detector and an RC-loop filter.

A typical behavior of the VCO control voltage  $V_c$  can be seen in Figure 2. Since the changes in the control voltage are small, the changes in the loop delay of the VCO are proportional to  $\Delta V_c$ :

$$\Delta T = \Delta V_c \cdot \frac{dT}{dV_c}. \quad (1)$$

Assuming a constant charge-pump current  $I_{cp}$  and a cycle time  $T$ , the voltage change stemming from the proportional part of the loop filter is

$$\Delta V_c^p = I_{cp} \cdot R, \quad (2)$$

and the voltage change from the integral part is

$$\Delta V_c^i = \frac{I_{cp} \cdot T}{C}. \quad (3)$$

The overall change of the loop period during one cycle calculates to

$$\begin{aligned} \Delta T &= \Delta T_p + \Delta T_i = \\ &= \left( I_{cp} \cdot R + \frac{I_{cp} \cdot T}{C} \right) \frac{dT}{dV_c} \end{aligned} \quad (4)$$

### 3. Parameter Independent Loop Behavior

There are two different levels of parameter independence: While the first guarantees a parameter independent loop behavior for only a *single frequency*, the other, stricter one, guarantees independence for *all frequencies*. In order to achieve stability in a bang-bang PLL, the ratio of the proportional part to the integral part should be well defined [2]. Hence the first principle of parameter independence for a PLL in a bang-bang configuration can be stated as the following:

$$\Delta T_p / \Delta T_i = \text{constant}, \quad (5)$$

for at least one operation frequency, independent of any changes in  $V_p$ , • etc.

The second principle also demands

$$\begin{aligned} \Delta T_p / T &= \text{constant}, \\ \Delta T_i / T &= \text{constant}. \end{aligned} \quad (6)$$

It can be noted from eqs. (2) and (3) that – in contrast to the proportional part – the integral part of the loop filter response is dependent on the loop cycle time  $T$ . Hence, achieving frequency independence is not possible with a simple RC-loop filter.

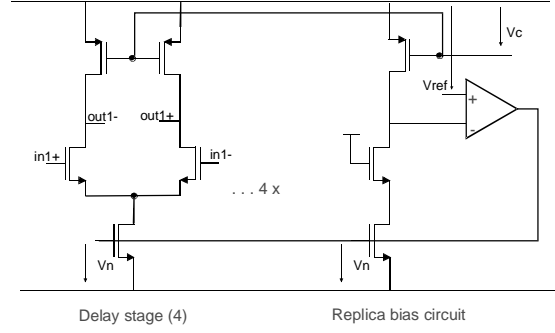


Fig. 3. VCO using single MOS-transistor as VCR.

### 4. Case A: VCO with simple VCR

The first oscillator structure [3] [4] under investigation can be seen in figure 3. The frequency is controlled via the gate-source voltage of a PMOS transistor in the triode region being used as a voltage controlled resistor. A replica bias circuit keeps the voltage swing constant. It was verified in SPICE-simulations that the relationship between cycle time  $T$  and control voltage  $V_c$  is fairly accurately given by

$$T = \frac{C}{\beta_p (V_c - V_t)}, \quad (7)$$

which can also be derived using a simple analytical model for a pMOS transistor with device transconductance  $\beta_p$  and threshold voltage  $V_t$ .

Taking the derivative of eq. (7) gives the linearized dependence between control voltage and loop delay

$$\frac{dT}{dV} = \frac{-C}{\beta_p (V_c - V_t)^2} \quad (8)$$

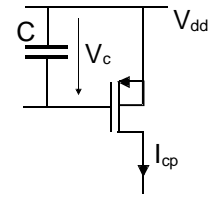


Fig. 4. Charge pump current extraction circuit.

Dividing eq. (8) by the cycle time  $T$  and substituting the expression from eq. (7) gives the relative delay sensitivity with respect to the control voltage,

$$\frac{1}{T} \frac{dT}{dV} = -\frac{1}{V_c - V_t}. \quad (9)$$

It can be seen that the relative delay sensitivity only depends on the process parameter  $V_t$ . To fulfill the requirements of frequency-independence, the following expressions, derived from eqs. (1)-(3) and (9), have to be constant:

$$\frac{\Delta T_p}{T} = I_{cp} R \frac{1}{V_c - V_t} = k, \quad (10)$$

$$\frac{\Delta T_i}{T} = \frac{I_{cp} T}{C} \frac{1}{V_c - V_t} = A \cdot k, \quad (11)$$

Solving both equations for the charge pump current  $I_{cp}$  results in

$$I_{cp}^p = \frac{k \cdot (V_c - V_t)}{R}, \quad (12)$$

$$I_{cp}^i = \frac{k \cdot C \cdot (V_c - V_t)}{T}, \quad (13)$$

as the required currents for the proportional part and the integral part, respectively.

Substituting the expression for  $T$  from eq. (7) in the expression for the desired current in the integral part, eq. (13), results in

$$I_{cp}^i = k \cdot \beta \cdot (V_c - V_t)^2, \quad (14)$$

which is just the well known equation describing the quadratic drain current-vs.- $V_{gs}$ -behavior in a long-channel MOS transistor.

## 5. Fully Process and frequency independent PLL structure

Hence, by deriving the charge pump current from a current source controlled by the loop control voltage  $V_c$  as shown in figure 4, a process and frequency independent biasing scheme is obtained for the integral part of the loop response.

To achieve the same frequency-independence for the proportional part the following scheme can be used. The resistor in the loop filter is omitted and the phase detector is extended, as shown in Fig. 5, in order to signal when a decision change has occurred (A “late” after a sequence of “early” decision, or vice versa,). In the case of a decision change the charge-pump uses a

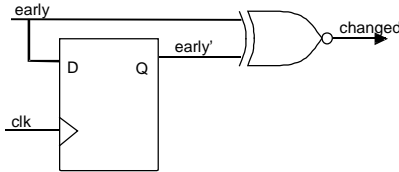


Fig. 5. The early/late difference detection circuit.

current  $I_{cp}' = \alpha \cdot I_{cp}$ , where  $\alpha$  is a constant corresponding to the ratio of the proportional part to the integral part of the loop response. Figure 6 shows the behavior of the control voltage when this scheme is used.

It should be noted that the proposed structure has also beneficial properties with respect to noise coupling to

the oscillator, since the control voltage is now directly connected to the high-valued loop-filter capacitance.

## 6. Case B: VCO with “symmetrical load” structure

Figure 7 shows the second structure under investigation, using “symmetrical load” elements [1] as voltage controlled resistors. The voltage swing in the delay elements is regulated by a replica bias circuit in order to be the same as the VCO control voltage  $V_c$ .

A formula describing the relationship between control voltage  $V_c$  and cycle time as  $T \propto 1/(V_c - V_t)$  can be found in [1]. SPICE-Simulations of the oscillator showed, however, that this formula becomes inaccurate for small values of  $V_c - V_t$ . Using

$$T = \frac{C \cdot V_c}{\beta_p (V_c - V_t)^2}, \quad (15)$$

to describe the  $T$ -vs.- $V_c$  relationship gives fairly accurate results, as can be seen in Figure 8.

Calculating the relative delay sensitivity from eq. (15) results in:

$$\frac{1}{T} \frac{dT}{dV} = -\frac{1}{V_c} \frac{V_c + V_t}{V_c - V_t} \quad (16)$$

Apparently, this formula is much less tractable than eq. (7). Nevertheless, it turns out that for a broad range of frequencies eq. (15) can be approximated by:

$$\frac{1}{T} \frac{dT}{dV} \cong -\gamma \frac{1}{V_c - V_t}, \quad (17)$$

where  $\gamma$  is a constant in the interval [1.4..1.8], depending on the expected ranges of  $V_c$ ,  $V_t$  and  $V_{dd}$  of a given VCO.

Solving again for  $I_{cp}$  gives:

$$I_{cp}^p = \frac{-\gamma \cdot k \cdot (V_c - V_t)}{R}, \quad (18)$$

$$I_{cp}^i = \frac{-\gamma \cdot k \cdot C \cdot (V_c - V_t)}{T}, \quad (19)$$

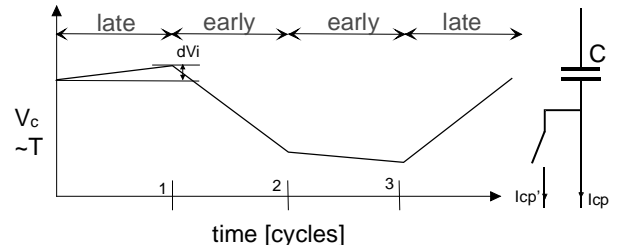
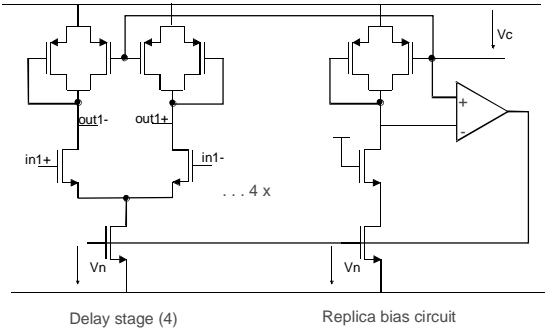
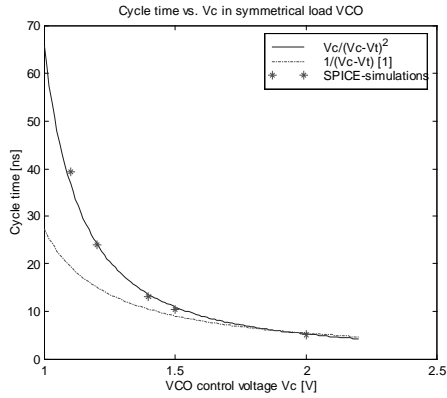


Fig. 6. The VCO control voltage behavior using an early/late difference detection circuit.



**Fig. 7.** VCO structure using symmetrical loads.



**Fig. 8.** The relationship between cycle time  $T$  and control voltage  $V_c$  in a symmetrical load VCO.

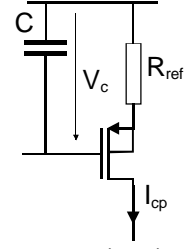
Replacing  $T$  from eq. (15) now results in:

$$I_{cp}^i = \frac{-\gamma \cdot k \cdot \beta_p \cdot (V_c - V_t)^3}{V_c}, \quad (20)$$

which cannot be achieved by a simple circuit. Hence, if frequency independent biasing has to be considered, structure A should be used.

## 7. Process independent biasing for a single frequency

If, however, the operation frequency is known in advance, both structures can equally be used together with the simple RC-loop filter described above. As equations (12), (13), and (18), (19) show, the required charge pump current  $I_{cp}$  is in any case proportional to  $(V_c - V_t)$ . To measure  $V_c - V_t$ , the circuit shown in Fig. 9



**Fig. 9.** Simple  $V_c - V_t$  extraction circuit.

can be used in the simplest case. Assuming a wide PMOS transistor, its gate-source voltage will be very close to  $V_t$ , producing a current:

$$I_{cp} = \frac{(V_c - V_t)}{R_{ref}}, \quad (21)$$

In order to achieve higher accuracy, a structure with a differential amplifier can be used.

Substituting the expression for  $I_{cp}$  from eq. (21) in eqs.(10) and (11) gives

$$\frac{\Delta T_p}{T} = \frac{R}{R_{ref}}, \quad (22)$$

$$\frac{\Delta T_i}{T} = \frac{T}{R_{ref} C}, \quad (23)$$

where the cycle time  $T$  now is constant and known in advance.

Hence, the proportional change per cycle can be very accurately predicted, since it depends on a ratio of matched resistors. Although independent of variations in  $V_t$  and  $\bullet$ , the predictability of the integral change per cycle is now determined by the process tolerances of the available resistors and capacitors in a given technology. Since many technologies today provide quite narrow tolerances for these parameters (within the +/-10% range) this is not a major handicap.

## 8. Conclusions

In this paper we presented methods to achieve parameter-independent biasing in bang-bang phase-locked loops for two basic differential oscillator structures. For the structure using a single transistor as voltage controlled resistor, we proposed a PLL architecture which achieves full process- and frequency independence by deriving the charge pump current from the loop control voltage and by extending the phase-detector to signal a decision change.

The structure using symmetrical load elements proved to be less suitable for the requirements of full process- and frequency independence caused by its more complicated relationship between cycle time and control voltage. By reducing the requirements of the PLL to work at only one frequency we could show that

choosing a charge-pump current proportional to  $V_c - V_t$  leads to independence of transistor parameter variations.

## 9. References

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