FAST FRONT-END L0 TRIGGER ELECTRONICS FOR ALICE FMD-MCP TESTS AND PERFORMANCE

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Abstract

We present design details and new measurements of the performance of fast electronics for the Forward Multiplicity Detector for ALICE. These detectors based on sector type Microchannel Plates (MCP) forming several disks give the very first trigger decision in the experiment (L0). Fast passive summators integrated with the detectors are used for linear summation of up to eight isochronous signal channels from MCP pads belonging to one sector . Two types of microelectronics design thin film summators were produced. We present test results for these summators, working in the frequency range up to 1 GHz. New low noise preamplifiers have been built to work with these summators. The new design shows a good performance with the usable frequency range extended up to 1 GHz. An upgrade of the functional scheme for the L0 ALICE pre-trigger design is also presented.

1 INTRODUCTION

The first trigger decision in the ALICE experiment is made using the Forward Multiplicity Detector (FMD) system based on Microchannel Plates (MCP). The MCPs produce very short signals (less than 2 ns), with 200 ps rise time for precise timing (about 50 ps) and with a pulse height proportional to the multiplicity. These features can be used for the fastest decision made by the ALICE pre-trigger (L0 Trigger). The FMD system provides information on (i) multiplicity in a given rapidity range, (ii) primary vertex *z* location, while (iii) allowing the rejection of beam gas events.

Using a straightforward approach one should develop about 1000 channels of fast electronics with precise timing properties to match the total number of pads in 7 MCP disks. A more feasible solution has been suggested [1, 2], which involves an analogue summation of signals from many pads belonging to one disk. This summation must preserve the timing precision and linearity of the MCP signals.

In this paper we describe further developments of [2], covering both the general upgrade of the functional L0-trigger scheme and some new practical results for the fast electronics. These include tests of industrial prototypes of an 8-channel passive summator and the development of a fast preamplifier with 250 psec peaking time.

2 UPGRADE OF ALICE L0 TRIGGER FUNCTIONAL SCHEME

This upgrade concerns simplifications and modifications of the L0-Trigger Functional Scheme presented in [2] The new scheme of the fast front-end electronics integrated for each sector of the seven FMD disks into one Front-End Electronics Card (FEEC) is shown in the Figure 1.

The scheme includes a newly developed passive summator which is integrated into the FMD-MCP detector design. It provides a splitting of timing and charge signals from the detector. These are then transferred to the FEEC. The FEEC integrates preamplifiers , QDC chips, pipe-line FIFO and a new type of fast TDC chip. A short description of the interface between the L0-Trigger electronics and DAQ system is also given.

2.1 Front-End Electronics Card (FEEC)

Each FEEC (see Figure 1) is situated as close as possible to the FMD-MCP which it serves. The electronic board contains the following (programmable) parts:

1. fast analogue single threshold discriminator (MD) for multiplicity analysis,
2. a fast timing discriminator (TD) which provides a precise time mark of the incoming analogue sum signal for a given FMD-MCP sector,
3. a fast TDC for TOF measurements,
4. eight fast QDCs for charge 0 of the individual FMD channels.
5. pipe-lines for storing charge information for each channel, and timing information for the sector.

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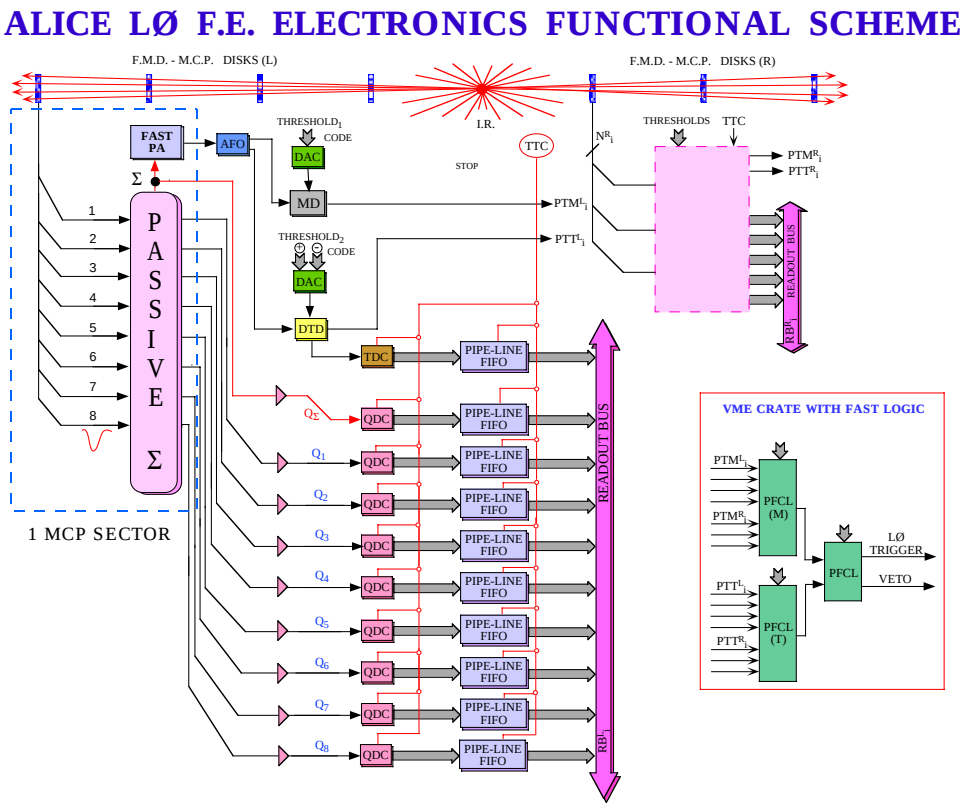

Figure 1: ALICE L0 Trigger Front-End Electronics Functional Scheme. The detailed layout for one sector Front-End Electronics Card is shown together with the layout of the Fast Programmable Logic unit serving all 7 FMD-MCP disks.

Fast input signal splitters (AFO) will be matched in impedance with transmission lines coming from fast pre-amplifiers (50 Ω) and with the inputs to MD and TD.

The FEEC should provide also a place for the TTC adaptors[3] and elements for a Digital Data Link (DDL) connection [4]).

2.2 Fast TDC for Timing

In order to get the fast logic PTTi signal giving the timing information from sector *i* we proposed previously in [2] the use of fast time-to-amplitude 0 followed by analogue discriminators.

Here we suggest another possible solution which provides both pipe-lined TOF measurements and the logic signals PTT to determine the interaction diamond.

This could be achieved using a new Time to Digital Converter chip based on a Delay Locked Loop (DLLo) CMOS ASIC [5] combined with a fast Programmable Logic (PL) to give the PTTs [6]. It is assumed that the TTC clock signal triggers the DLLo circuitry every 25 ns to start the TDC while a signal from the Timing Discriminator fixes the corresponding delay of the FMD-MCP hit. The PTT selection could be achieved using a fast programmable logic to compare the signals from different sectors.

2.3 DDL Connection to DAQ

The data transfer requirements for the FMD-MCP Detector Data Link using the Digital Data Link(DDL) proposed for the experiment, can be estimated, taking into account total amounts of data from the detector (1 Kbyte/event), a limit on the total readout time (< 200 μsec) and a suggested DDL transfer rate (100 MBytes/sec) [4].

If we read only the L1 triggered events and not the whole pipeline, then 5 DDLs will be sufficient for the whole MCP detector. We propose to use six DDLs, three on each side of the detector, in order to simplify the connections.

We intend every FEEC serving one half FMD-MCP disk to be equipped with 2 identical and parallel FEEC-DDL subsystems, to provide a bi-directional communication between FEEC and the DAQ Read-Out Receiver Cards (RORC) through their end-cap cards SIU, DIU and duplex fibre-optic lines of about 200 m length. The radiation and space constraints are being studied.

Fast programmable logic units for handling pre-

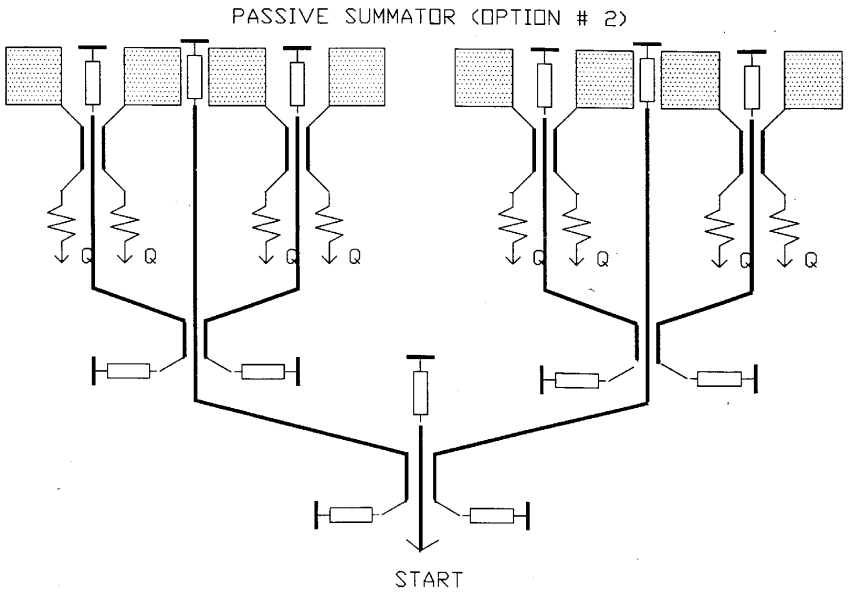

Figure 2: UHF design for a fast passive summator based on directional couplers.

triggers and making the main L0 trigger decisions will be placed in an accessible crate outside ALICE and close to the detector.

3 PASSIVE SUMMATOR PERFORMANCE

We discuss here the design and the results of performance tests for the first industrial production prototypes of fast passive summators to be used in the FMD-MCP detector.

We have designed, industrially produced and tested two types of thin-film technology UHF passive summators, (i) based on directional couplers and (ii) on ring bridges. A detailed description of the physical principles of passive summator operation for pulse signals will be described elsewhere[7]. A general design for an 8 input channel passive summator is shown in Figure 2. This summator is designed to be integrated within a sector of the MCP prototype detector. Signals from 8 pads are split into two parts: the fast components (400 MHz-1GHz frequency range) are summed for timing and total charge information, while the slow components go to the individual charge digitisation channels.

Passive summators were mounted onto a rigid frame together with the relevant input and output feed-through (see figure 3).

Thin-film technology and microelectronic design were employed. We used 200 micron thick Al_2O_3 plates of 40×60 mm^2 as a base. The design of the sector type summator shown here will be used with sector type MCP-detectors. MCP-stacks will be mounted on the back-

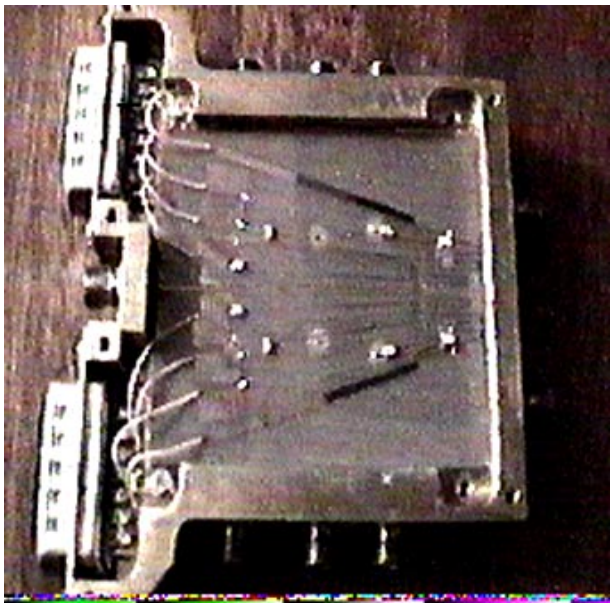

Figure 3: Photo of an industrially produced passive summator based on circular bridges.

plane of the summators with multipad readout anodes. In this prototype 8 anodes were substituted by 8 transmission lines coming from the coaxial inputs.

The tests on the summators have been performed using both a pulse generator and real MCP fast signals. The result of the analogue sum of four input signals is presented in Figure 4, for the case of four signals with different delays, and in figure 5 for the case where all the delays

are equal. One can see the sharp rise-time of the output signals and linear summation of the amplitudes.

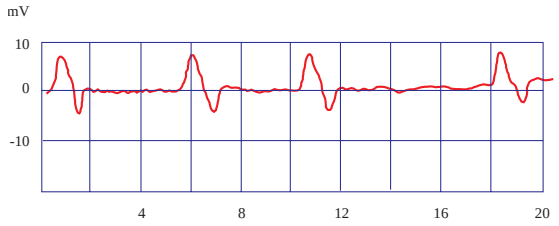

Figure 4: Oscillogram of the fast 4 signals separated by different delays shown at the fast output of the passive summator.

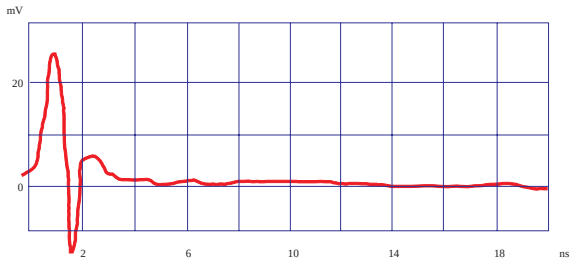

Figure 5: The same as in the Figure 4 but with the delays removed.

These two types of summators are a further development of the prototype design for which results were presented one year ago [2]. They are capable of providing linear summation of up to 8 isochronous signal channels over a wide dynamic range. The working frequency range is up to 1GHz. We found no deterioration in the S/N ratio compared to the single channel case. The level of cross-talk was found to be 55-60 dB for signal amplitudes induced in charge output channels in the case of directional couplers. A comparison of the two types shows that the circular bridge couplers give less attenuation than the the directional couplers (-13dB and -15dB respectively), but the directional couplers give better channel cross-talk characteristics.

A third type of summator will be produced, combining the best features of the two (with directional couplers for the first stage and circular couplers for the remaining stages).

4 FAST PREAMPLIFIER WITH 250PS RISE TIME

New low-noise preamplifiers, matched in impedance with the output signal channel from the passive summators, have been built. Two types of preamplifiers were initially considered for the general FMD-MCP application: (i) for precise timing and (ii) for the charge measurements. In this paper we consider the first type relevant to fast signal transfer. Tests were performed on two fast preamplifiers:-

(i) the first one was an industrial prototype, based on a modified version of the Rudge transimpedance preamplifier [8]. The main modifications concerned the first stage of the preamplifier and the hybrid board general layout. Results showed a considerable improvement in the performance, with the usable frequency range increased up to 1 GHz.

(ii) We have also designed and manufactured a prototype of another fast preamplifier (see layout in figure 6).

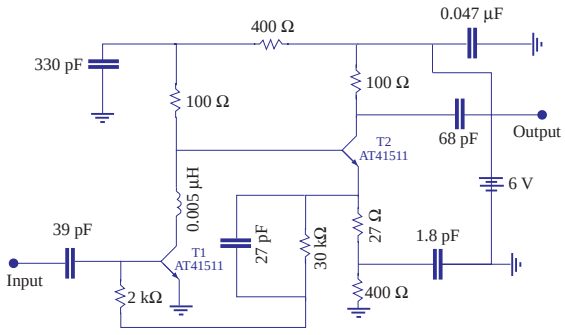

Figure 6: Fast preamplifier layout.

We used low-noise (1.4dB at 1GHz) high frequency ($\sim$ 8 GHz) AT-4511 transistors which are the same as those used in reference [8].

A gain of $\sim$ 15dB in frequency range 500-1100 MHz is achieved. The results of the measurement are shown in figure 7).

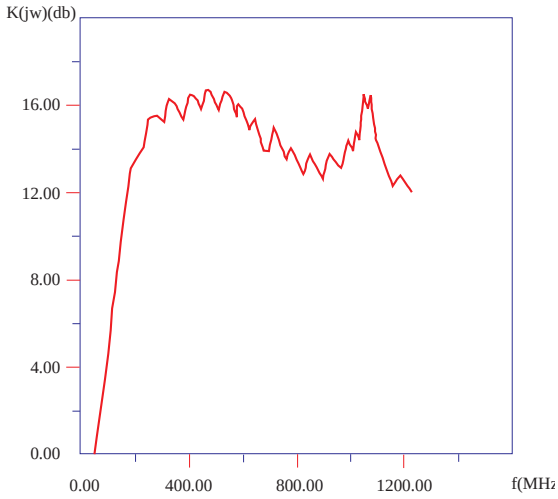

Figure 7: Gain versus Frequency Response for fast preamplifier.

The Voltage Standing Wave Ratio (VSWR) measured is less then 2.2 for the frequency range mentioned above.

This VSWR is to be improved in future developments.

The response of this pre-amplifier to the sharp (100ps) "step" signal is shown in figure 8.

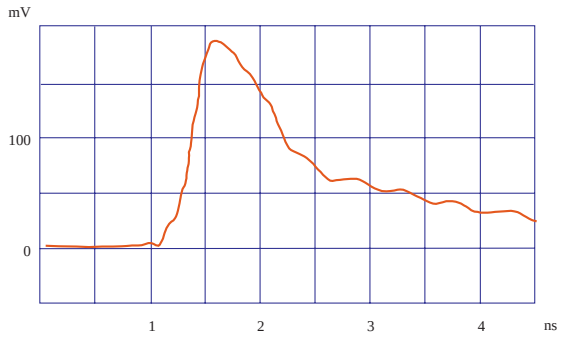

Figure 8: Transition response of the preamplifier for a 100 psec rise time step function.

A 250 ps leading edge was measured, demonstrating the dynamic properties of the pre-amplifier.

We also tested the complete fast chain for a single channel consisting of an FMD-MCP detector, passive summator and fast preamplifier. The results are illustrated in figure 9,

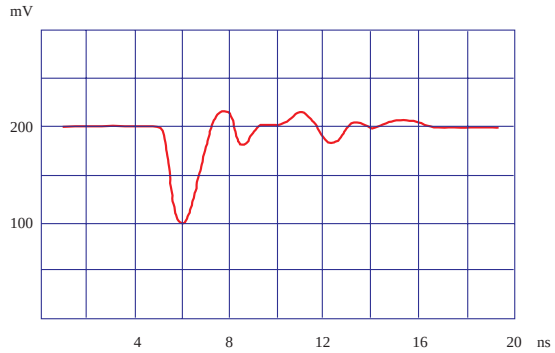

Figure 9: The shape of the MCP signal measured after the summator and fast preamplifier.

where we present the oscilloscope trace at the output of a fast preamplifier placed after the summator. The input signal from the MCP detector had an amplitude of 100 mV and a rise time of about 1 ns. One can see the undistorted transfer of the signal leading edge through all the chain. These tests of the complete chain also demonstrated the compensation of the signal amplitude attenuation passing through the summator (factor $\sim$5.5) by the gain of the pre-amplifier.

More detailed studies are needed to decide the number of channels in the summator with the gain of the MCPs and pre-amplifier, and the dynamic range of the other circuits.

5 CONCLUSIONS

The results of the first tests of the industrially produced fast components of the FMD-MCP front end electronics (passive summators and fast pre-amplifiers) have shown satisfactory performance (sharp rise-times of the transfer signals - up to 250 ps), wide frequency range (500 MHz-1000MHz) and low level of cross talk in charge channels (55-60 dB). The attenuation for the directional coupler type summator is acceptable ($\sim$ -15 dB). Less attenuation is obtained using circular bridge couplers, but with more cross-talk. A third type of summator combining the best features of circular and directional couplers is currently being designed.

6 REFERENCES

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