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The CMS Electronic Systems

G. Hall
Blackett Laboratory, Imperial College, London SW7 2AZ, UK
g.hall@ic.ac.uk

CMS Collaboration

Abstract

The electronic systems planned for use in the CMS experiment at the LHC are reviewed, with an emphasis on the motivations for the designs adopted and developments which remain outstanding. Comments are made on the notable challenges still to be faced in provision of the experiment for operation in the year 2005.

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The electronic systems planned for use in the CMS experiment at the LHC are reviewed, with an emphasis on the motivations for the designs adopted and developments which remain outstanding. Comments are made on the notable challenges still to be faced in provision of the experiment for operation in the year 2005.

1. Introduction

To attempt to review in depth each of the CMS sub-detector electronics systems is a daunting task. All of them are complex and contain a large number of elements. Many of them are still incompletely specified and a significant number of choices remain to be made, both of components and technologies. Nevertheless progress has been rapid in the past few years and all the remaining detectors (the TDR for the CMS Hadron Calorimeter has already been approved [1]) are planning to submit Technical Design Reports to the LHCC within the next few months for approval for construction to commence. These are the documents to which reference should be made in future for details of the information summarised below.

2. CMS operation at LHC

For completeness a summary is given in Table 1 of the relevant LHC operating parameters for CMS. An important point to be noted is the requirement for heavy ion operation of the experiment for a fraction of the running time each year. This places some additional requirements on elements of the system, such as data acquisition, which must be able to handle, for example, the large volume of data from the tracking system in each event.

Table 1

particles	***pp***	***Pb-Pb***
Luminosity	10^{34} cm^{-2}.s^{-1}	10^{27} cm^{-2}.s^{-1}
Average integrated luminosity	5×10^{40} cm^{-2}.y^{-1}	10^{33} cm^{-2}. y^{-1} ***?***
CM energy	14 TeV	5.5 TeV/N
$\sigma_{inelastic}$	~70mb	~6.5 b
Interactions/bunch	~20	0.001
Tracks/unit rapidity interval	~140	3000-8000
beam diameter	20μm	20μm
bunch length	75mm	75mm
beam crossing rate	40MHz	8MHz
L1 trigger delay	≈3.2μsec	≈3.2μsec
L1 trigger rate	≤100kHz	< 8kHz

3. System issues

Many of the major consequences of experiment operation at LHC are already well known. The requirement for high speed signal processing has implications for front end power, signal to noise ratios and overall performance. The high charged particle and neutron fluences in the experiment raise major issues of testing and qualification, operational reliability and long term maintenance as well as possible impact on performance. It is less commonly recognised that many of these concerns are also relevant in the outer parts of the experiment, up to the cavern walls where doses in the few krad range may be expected along with modest neutron fluences $\sim10^{11}$cm^{-2} [2,3] over a ten year operational period. Similarly the problems of detector operation in the 4T solenoidal magnetic field are well recognised but less concern is evident at the prospect of installing equipment on the surface of the detector and in the cavern galleries where stray fields up to about 500gauss are anticipated.

The very large data volumes to be transmitted require massive CPU power and fast data links to be provided. These, as well as the items mentioned above, dictate the use of technologies which are still relatively new to high energy physicists, such as telecommunication switches, radiation hard ASICs, semiconductor optoelectronics and optical fibres. Most of them are to be employed on a scale not encountered elsewhere. In some cases the R&D phase is still underway while most of them present learning curves which are just being scaled.

Some additional constraints provided by the millennium era are the shrinking resources available in budgets, manpower *and* timescale, as the LHC operation date approaches. These should have significant implications for the temptation to exploit more recently developed technologies and the planning of the large amount of testing and assembly work which must be undertaken. The challenge of meeting timescales and budgets are implicit, if not explicit, in all that follows.

Some, perhaps less obvious, consequences of the overall experiment design are that:

CMS, like ATLAS, is enormous in comparison with previous generations of experiments and most sub-systems have a very high channel count,

the sub-detector systems are highly distributed, remote and inaccessible for long periods, demanding high reliability,

application of not fully mature technologies is required for some critical elements,

many of the specifications are *extremely* demanding, such as temperature stability, magnetic field operation, radiation tolerance, material budget reduction, etc,

on-line reduction of first level data is absolutely essential, and there will be intense demands on computing resources, which must continue to evolve rapidly to meet the requirements.

Finally, there is still uncertainty regarding some important technology choices to be made over the coming few years, for example optical links, processors, software, event builder switches. One major reason why some of these are developing so rapidly at present is because they are commercially driven, which means that our community does not necessarily have the ability to influence developments to meet our specifications. Thus a certain flexibility is required so that we are sufficiently responsive to, or wary of, externally driven changes which may occur at short notice.

All of the topics above have implications for the management of the systems we plan to implement and it is already relevant to ask whether the methods which have evolved to meet the requirements of the high energy physics field in the LEP and pre-LEP eras will continue to work adequately in future.

4. CMS electronic sub-systems

4.1.1 Tracking requirements and system

The goal of the system is to "reconstruct isolated high p_T tracks with an efficiency better than 95% and high p_T tracks within jets with an efficiency >90% over the range $|\eta|<2.6$" [4]. A system based on ~80M pixels and ~10M silicon and gas microstrip detectors is proposed to deliver this; the detectors should have a low occupancy for normal proton-proton operation of ~3% in the microstrips and ~3 $x10^{-4}$ in the pixels. The parameters required to achieve this are

point measurement spatial resolution below 20µm, which is defined mainly by segmentation,

adequate momentum resolution [4], defined by spatial resolution, overall detector dimensions and magnetic field,

vertex and impact parameter reconstruction ability, defined by spatial resolution and efficiency,

pattern recognition performance, which is limited by occupancy, efficiency, software and detector layout.

The efficiency, which occurs in several of the preceding parameters, is influenced strongly by the signal to noise ratio achieved but operational reliability will be another significant factor.

The tracking system experiences one of the most severe radiation environments in the whole of CMS with 10 year doses and fluences of about 40Mrad and $8x10^{14}$ charged hadrons.cm^{-2} in the vicinity of the pixel system, ~15Mrad and $3x10^{14}$ charged hadrons.cm^{-2} at the innermost silicon microstrips and ~1Mrad and 10^{13} neutrons.cm^{-2} for the outermost MSGCs.

The electronic challenges for the system are principally to ensure a sufficiently low noise level (which determines noise occupancy) and timing to a single bunch crossing precision for silicon microstrips and two bunch crossings for MSGCs. During irradiation the silicon signal will decrease, especially in pixel detectors, while the MSGC signal is adjustable but low gain operation is preferred to minimise risk, as there is little experience of operation of large scale systems. The pixel technology is one of those which is still developing.

4.1.2 Tracker electronic design and technologies

Both microstrips and pixels will be read out using analogue electronics. The precision requirements are ~5bits for a minimum ionising particle (MIP) with a dynamic range of ~8bits. Each microstrip signal is amplified, stored in a pipeline memory and multiplexed, after some elementary analogue signal processing, to the counting room using an analogue optical link (fig.1) [5].

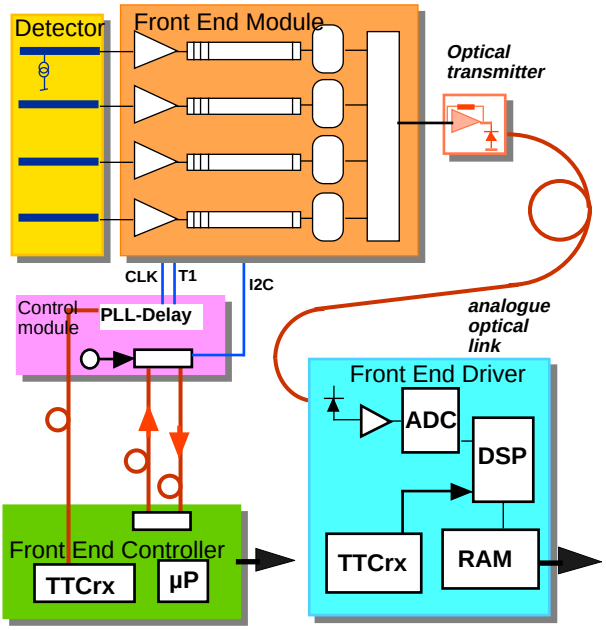

Fig.1: The basic architecture of the tracker readout and control system

Data from 256 front end channels are transferred on a single optical fibre at 40Ms/s. The link technology is based on edge emitting semiconductor laser diode transmitters which have shown excellent radiation hardness and where significant progress in developing packaged components (fig.2) has been achieved in the last one to two years in collaboration with industry.

A control system [6] utilising the same components will distribute clock, trigger and commands via a digital chip (CCU) serving a number of modules (fig.3). The exact layout can be configured, with possible redundancy, to match the layout of regions of the tracker. The external control is provided by a VMEbus Front End Control (FEC) module in the counting room

with which the CCU is in communication via digital optical links.

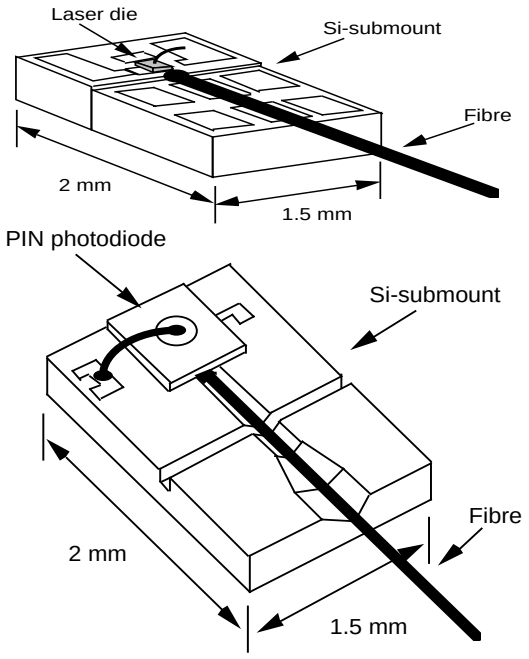

Fig.2. Laser transmitter and photodiode receiver assemblies with optical fibres on silicon submounts.

The digitisation of data, digital signal processing and zero suppression will be carried out on a 9U VMEbus module, the Front End Driver, which is expected to be a standard module utilised throughout CMS and customised for each sub-system. Work is now focused on a design making use of an internal PCI bus (fig. 5) with sub-detector specific PCI mezzanine modules mounted on the board [7]. It is expected that the FEC module will be structurally very similar and will be able to make use of the same motherboard design.

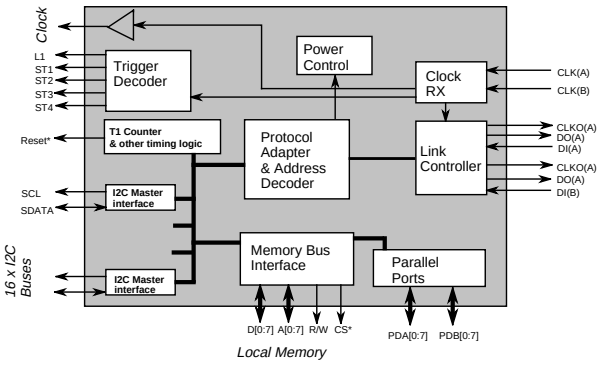

Fig.3. The architecture of the digital CCU chip.

In the case of pixels, the favoured architecture is a double column based design [8] in which a hit pixel signals its presence to the edge of the array (fig. 4). This initiates circulation of a token and, on arrival at the pixel which has registered a hit, flags its address to the peripheral logic. Multiple buffers are provided to ensure the loss of multiple hits in a column during the readout sequence is maintained sufficiently low.

A low luminosity design (single buffer depth) of 24 x 32 pixels has been built meeting the pixel size requirements of 125µm x 125µm. A high luminosity version with the same pixel dimensions has been submitted for fabrication and indium bump bonding is under investigation for use as a possible in-house assembly technique, both in Europe and the USA [9], although the final route to module fabrication is not yet chosen.

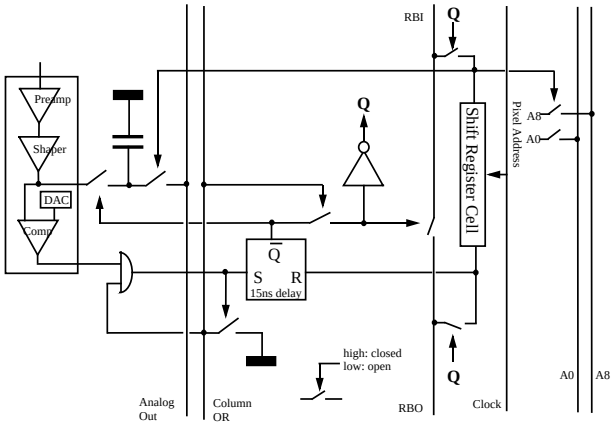

Fig.4. The proposed pixel cell schematic.

It is expected that both the control system elements and the analogue and digital optical links can be utilised in the pixel system, which is desirable to minimise development resources and for long term maintainability. Digitised pulse height data are expected to be packed for transmission at 40Ms/s to make use of the full bandwidth of the links.

The principal technologies to be used in the tracking system are:

Front End APV series chips have been prototyped in the Harris AVLSI-RA bulk CMOS process (APV6 [10]) and the design has been transferred into the Matra-MHS DMILL process (APVD [11]) to ensure that two vendors can guarantee the large number (~100k) of chips required. A multiplexer to transfer data from two 128 channel chips to one optical link has also been developed in the Harris process.

The laser driver [12] and PLL chip [13] for clock recovery are being prototyped in radiation soft form, to be transferred into DMILL next year.

The digital control chip, CCU [6], which is the chief component of the internal control and monitoring system is likely to be produced in Honeywell SoI gate array technology after prototyping in conventional form,

Materials based on III-V semiconductors are employed for transmitter and receiver optical components [14] packaged on a silica on silicon submount assembly [15]. The optoelectronics are to be used for both the analogue data and digital clock, trigger and command distribution within the tracker volume. The RD12 TTC system [16] will be used to deliver clock and triggers to the Front End Control modules from which the customised tracker system will distribute them; this avoids the internal use of a radiation hardened TTCrx chip which is requires more power and has greater functionality than necessary for the tracker system.

Fig 5. A schematic drawing of the (not yet final) modular FED design based on an internal PCI bus

There are a number of special problems for electronics in the tracker system:

all internal electronics must be radiation hard, including optical transmitters and receivers,

the optical technology is novel and raises important fibre and optical cable connection andhandling issues of which there is yet little experience,

signal to noise is unfavourable so minimal noise at, and after, the front end is mandatory; careful signal processing and avoidance of digital interference, power routing and grounding are all of great importance,

the material budget must be limited so power consumption as low as possible is essential, while cooling must be provided for local heat sources,

power provision and control is an area where, as yet, only modest progress has been made in defining the system, but is recognised to be crucial,

there are special requirements to monitor currents in MSGCs and control high voltages to avoid discharges, which are expected to be rare but could damage the chambers,

the large number of channels means that automated testing must be used as far as possible; this is under investigation, as is assembly, which could be carried out commercially,

the requirement to minimise the material budget implies advanced technologies for hybrids and small connectors, which must also be reliable.

4.2.1 ECAL requirements and system

The CMS goal for the electromagnetic calorimeter is to provide "the best possible calorimeter affordable". This is translated into a specification by the requirement to observe an intermediate mass Higgs (~80-150GeV/c^2) which would decay into two photons and places

Preshower detector in the forward region, constructed from lead layers and silicon pad detectors, which may also be installed in the barrel region for high luminosity LHC operation. This will contribute 145k channels, with a further 106k channels if the barrel Preshower detector is installed.

The crystal calorimeter performance is parameterised by contributions summed in quadrature

$$\frac{\sigma}{E} = \frac{a}{\sqrt{E}} \oplus b \oplus \frac{\sigma_{noise}}{E}$$

The first term is related to statistical fluctuations in light output from the scintillators (a<2%) and the second term is defined by systematic effects (b <0.5%). Only the third term is directly related to electronics (σ_{noise}< 150MeV equivalent). The ECAL detector should also measure the direction of the incident electron or photon with an angular resolution of < 50mrad/√E and it must efficiently reject π^0s, requirements which are principally influenced by crystal segmentation and preshower layout. The energy measurement is also limited by the degree of containment of particle showers, which is controlled by the Moliere radius, radiation length and dimensions of the crystals. For this, the hadron calorimeter supplements the ECAL shower measurement.

Regarding the radiation environment, the worst doses and fluences are expected in the forward regions but doses of up to several hundred krad are anticipated, with additional high neutron fluxes in forward region.

The principal challenges for the electronics of the ECAL and Preshower are:

the large dynamic range of signals, from 50MeV-2TeV (92dB) requiring 15-16bits, which must be measured with a precision of ≈12bits with excellent

power distribution and control, especially for the avalanche devices, are major issues and the system must operate in the 4T magnetic field

the Preshower electronics should detect minimum ionising particles for calibration purposes and should be tolerant of radiation induced leakage currents in the silicon detectors.

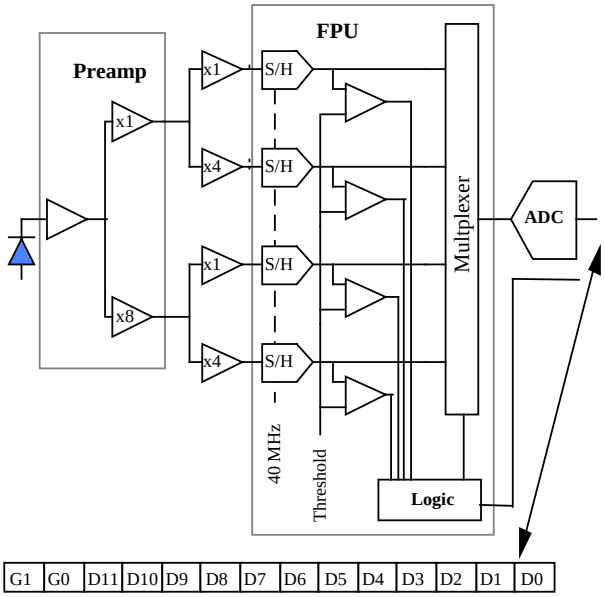

Fig.6. The ECAL front end.

4.2.2 ECAL electronic design and technologies

The functions on the detector [17] are now limited to low noise (ENC~5000e) front end amplification[18], local digitisation at 40Ms/s after gain selection (FPU) followed by digital optical data transmission (fig. 6). From the ADC 12 bits are provided with 2 bits of range information (possibly with error correction coding) leading to a requirement for links operating at ~1Gb/s.

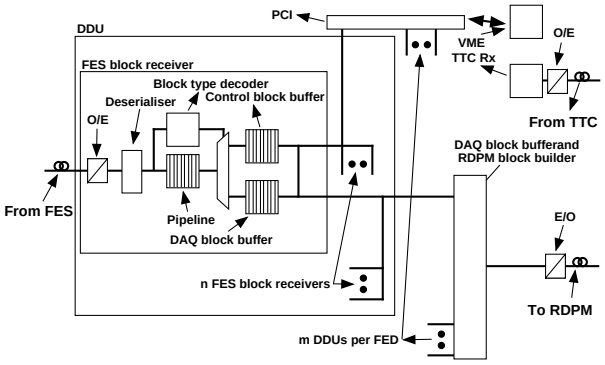

Fig. 7. Schematic of the ECAL DDU and its links to the DAQ system.

The ECAL Detector Dependent Unit (DDU) based on the FERMI system[19] is mounted on the FED in the counting room (fig. 7). It recovers the digital data, provides trigger primitives for the first level trigger and stores the data for the trigger latency. Further digital processing of the data is then expected to reduce the volume to be transferred to the higher level triggers and event builders running on the processor farm.

The Preshower detector makes use of a high dynamic range amplifier, d.c. coupled to the detectors, followed by a pipeline memory and multiplexing (32 channel PACE chip). Data are digitised following the front end chip in a custom multi-range ADC (CRIAD) at 20MHz. Data are assembled by a Data Path Unit, which selects signals above threshold for storage and converts parallel input to serial outputs, adding event identification information. Digital data are then transferred using components developed for the tracker control system (CCU and digital optical links) with groups of front end modules assembled into groups of Local Readout Units (fig. 8). If very high speed digital links become available at sufficiently low cost, an alternative architecture similar to the rest of the ECAL would be considered.

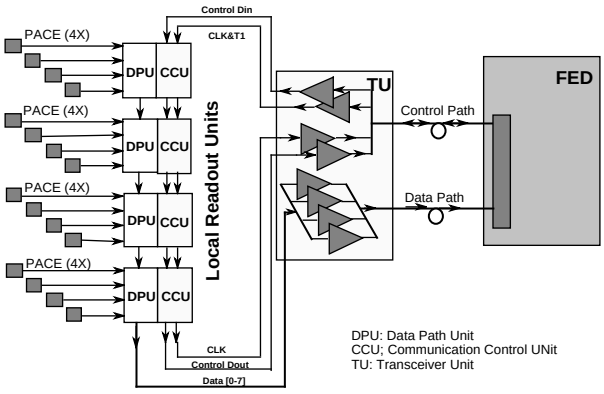

Fig. 8. The organisation of the Preshower readout and control system

The technologies proposed for the ECAL make use of radiation hard technologies to circumvent the intermediate level radiation tolerance requirement. The major components are:

a front end amplifier developed in the DMILL BiCMOS process,

a commercial 12 bit bipolar ADC which meets the radiation tolerance requirements,

DMILL ASICs, to be developed, for internal control,

a low power serialiser being prototyped using Honeywell GaAs CHFET technology is a likely solution for driving the optical links (fig. 9) unless low power radiation tolerant commercial devices become available.

For the Preshower system the front end amplifier and logic will be implemented in DMILL BiCMOS and the other components will follow those developed either for the tracker or ECAL.

The principal special problems for ECAL electronics are:

control and monitoring to ensure stability and uniformity over long periods, e.g. of temperature and APD bias, which must be accompanied by sufficient calibration, especially because of radiation induced changes in crystals and APDs,

radiation tolerance of all internal electronics is required, including optical transmitters and receivers, which is to be provided by using radiation hard ASIC processes,

the use of high speed optical technology, which raises fibre issues similar to the tracker. Power

dissipation inside the calorimeter should also be minimised and low bit error rates must be attained,

the power requirements for high bandwidth optical receivers are expected to be far from negligible and may need a specific development as the overall power consumption on VME crates in the counting room also gives cause for concern,

the digital processing technology is simplified by situating the DDU in the counting room but it must be provided at modest cost,

power provision and control, as well as cooling, are as challenging as for the tracking system, and in the ECAL design there is a proposal to make use of on-detector low voltage regulators. These do not yet exist and must be quite radiation hard as well as electrically very efficient,

testing and assembly are major labour intensive tasks.

The construction of large scale prototypes in the next few years is expected to contribute substantially to solving these problems.

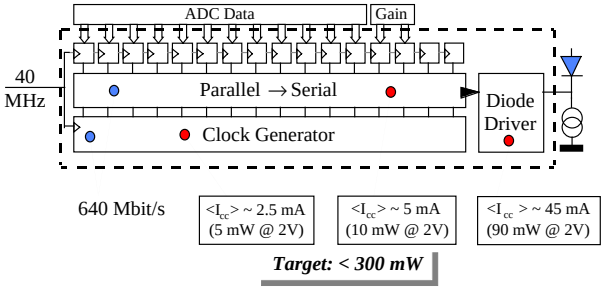

Fig 9. A schematic of the low power 1Gb/s serialiser being developed in GaAs CHFET technology.

4.3.1 HCAL requirements and system

The combined CMS calorimeter system will measure quark, gluon and neutrino directions and energies by measuring the energy and direction of particle jets and the missing transverse energy flow. The hadron calorimeter will contribute to the identification of electrons, photons and muons in conjunction with the ECAL and the muon system. The missing energy measurement provides a crucial signature for new phenomena, such as supersymmetric partners of quarks and gluons.

The barrel and endcap system [1] is based on copper absorber layers interleaved with scintillating tiles read out with embedded wavelength shifting fibres whose light is sensed using Hybrid PhotoDiodes (HPDs). The tiles are arranged as projective towers with a total of ~11k channels. There is also a forward calorimeter 6m downstream of the endcaps covering the region $3.0 < |\eta| < 5.0$. Quartz fibres embedded in a copper absorber matrix provide the active medium, sensing Cerenkov light from electromagnetic showers. The 4k channels are also read out using HPDs.

The important parameters of the system are moderate energy resolution parameterised as

$$\frac{\sigma}{E} = \frac{a}{\sqrt{E}} \oplus b$$

with a≈85-200% and b=3-5%, depending on position. The system must be hermetic so minimum gaps throughout CMS are essential. Dijet separation and mass resolution are defined by segmentation and energy resolution. MIP identification for muon trigger and off-line identification is also a requirement.

The radiation levels experienced by the electronics originate mainly with neutrons, at ~10^{11} cm^{-2} over 10 years, supplemented by low ionising doses of up to a few krad from photons, charged particles and induced radioactivity. In the forward calorimeter there is a very high radiation and rate environment but the electronics are located some distance away where levels are similar to the barrel to avoid the necessity to use hardened electronics. It is therefore practical to use a common electronic system throughout the hadron calorimeter.

4.3.2 HCAL electronic design and technologies

Each channel comprises photodetector (HPD pixel of ~5pF) with a gain of 2000, amplifier (linear 16-bit range and 3000 electron r.m.s. noise), shaper-range compressor and precise gated integrator and ADC channel, followed by cable driver, cable, and cable receiver (fig. 10). The data transmission speed is ~1Gb/s and the links are expected to be identical to those used for the ECAL. The barrel and endcap signals require integration over three beam crossings for measurement of the full amplitude while the forward calorimeter has very fast signals contained easily in 25ns. The dynamic range requirements are up to 15-16bits (91dB) with 5 bit precision.

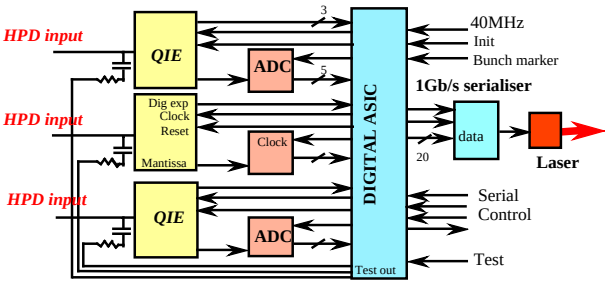

Fig. 10. The organisation of the HCAL readout.

The QIE (charge-integration-encode) circuit contains at the input a multi-range current splitter (fig.11) followed by the gated integrator. It is an ASIC whose fast bipolar input stage is based on a design already in use at 53MHz at FNAL but with higher noise (~15000e) than required for CMS. Improvements are assumed to originate from the use of better quality, finer feature BiCMOS processes.

Following the on-detector electronics, the digital processing on the FED in the counting room is expected to be very similar to that used by the ECAL, based on the FERMI concept.

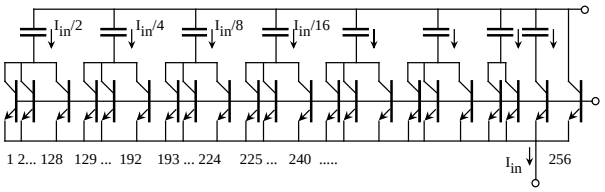

Fig. 11. Schematic of the current splitting input stage of the QIE ASIC.

The special issues for the HCAL system are:

noise reduction of the front end amplifier and the radiation tolerance of internal electronics to the neutrons and low dose levels to be experienced,

all necessary cable and service paths must be kept to an absolute minimum to minimize hadronic energy leakage or absorption by unsampled material; this requirement has an impact on the systems inside the HCAL, i.e. tracker and ECAL,

fast optical links, where concerns are identical to the ECAL,

reliability, given that the system is largely inaccessible,

power supplies and other rack electronics in the cavern, which must operate in fringe magnetic and low radiation fields.

4.4.1 Muon requirements and system

CMS was designed around the solenoidal magnet and muon system. There are three basic tasks to be fulfilled: muon identification, triggering and momentum measurement. Identification is achieved by using the iron flux return as an absorber for particles other than muons. Bending in the magnetic field in the r-ϕ plane allows momentum measurement and contributes to the trigger with the tracking system complementing the muon system measurement at lower momenta.

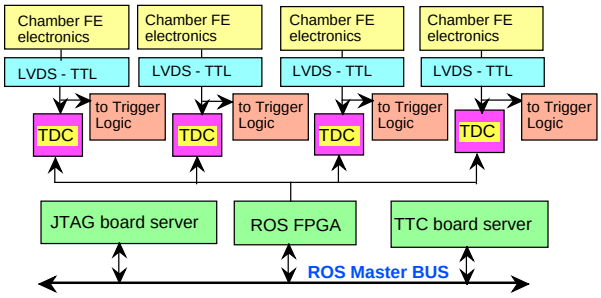

Fig. 12. The barrel muon TDC readout board structure.

There are also three readout systems. In the barrel a system of rectangular aluminium drift tubes with 11mm x 40mm cells will be interleaved in the iron (fig.12 and 13). Each station consists of 12 layers grouped as 3 super-layers providing two measurements in ϕ and one in η. Position is measured by timing with a resolution of 200μm and a meantimer [20] provides the track segments with orientation and bunch crossing association.

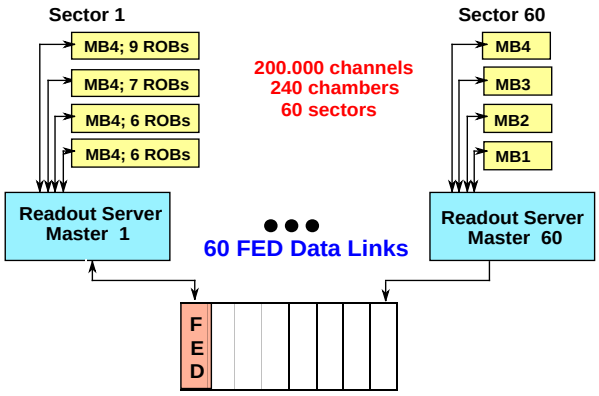

Fig. 13. Overall organisation of the barrel muon readout.

Hits are loaded into clock driven shift registers and come into alignment at a fixed time after the particle passage (fig. 14). The muon direction can be measured with a precision of ~1mrad, using the lever arm of 20cm between two stations. Low particle rates of ~10Hz.cm^{-2} and occupancy ~1% are expected. A total of 240 chambers with 200k channels are used.

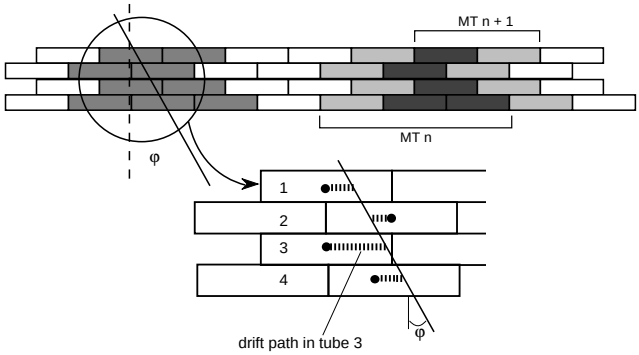

Fig. 14. Principle of the meantimer method.

In the endcap region there are higher particle rates (~1.5kHz.cm^{-2}) than in the barrel and an axial orientation of the magnetic field. Cathode Strip chambers (CSCs) are more suitable for this environment and provide a spatial resolution of 75μm to 150μm depending on location. Bunch crossing association comes from discriminated anode signals [21,22], while the cathode signals are stored and processed for cluster reconstruction and use in the trigger. After amplification, the cathode signal is split and shaped either fast, for use in the trigger logic, or slow, for pulse height measurement (fig. 15). The slow signal is stored in a 20MHz switched capacitor array. A total of 648 CSCs are required with 600k channels.

The third muon system is a series of dedicated trigger detectors based on Resistive Plate Chambers (RPCs) to provide robustness and redundancy in the trigger. These can operate efficiently up to particle rates of a few kHz.cm^{-2}. They have excellent time resolution ≈2ns for 1kHz.cm^{-2} with efficiency >97%. There is one RPC plane in each muon station except the two innermost barrel stations, where there are additional layers for low momentum muon triggering, covering the region $|\eta|<2.1$. The total number of channels is 192k (118k barrel, 74k forward).

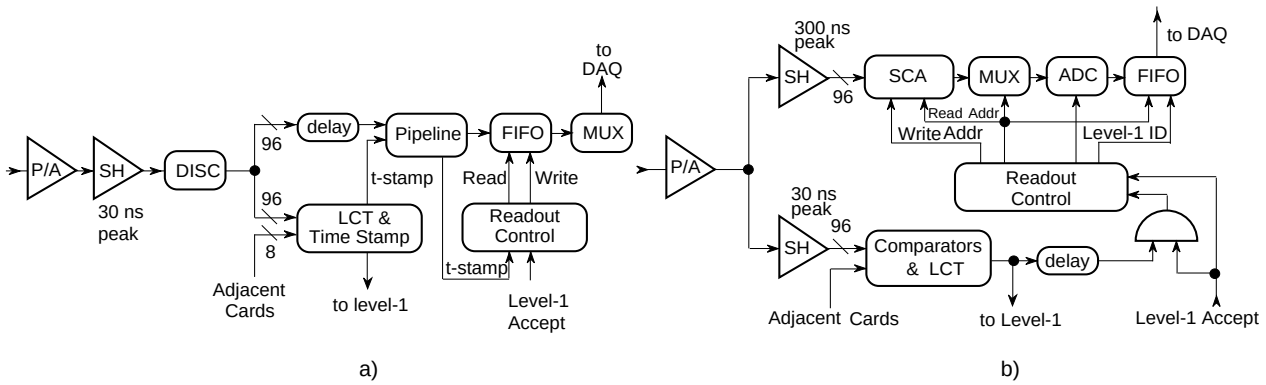

Fig. 15. CSC electronics: a) anode, b) cathodes. NB fast and slow shaping times are now 50/100ns.

4.4.2 Muon electronic design and technologies

Drift tubes require amplifier, discriminator and line driver to a TDC installed in the cavern. The system makes use of BiCMOS ASICs and FPGAs, for prototyping only, which will be replaced by digital CMOS ASICs. The high voltage system will be in the cavern and some part of it may be located on the chambers themselves, increasing the heat load.

The CSC front end [22] is based on a low noise, linear amplifier with pipeline and logic implemented in a standard CMOS process. An ENC≈7000e at 250pF with 12 bit dynamic range and 0.5% precision are to be achieved.

The RPC system [23] requires a fast amplifier, comparator and digital driver (fig. 16). It is intended that digital data should be transferred at high speed on a small number of fast optical links. A trigger processor is being constructed based on FPGAs which should finally be implemented in an ASIC.

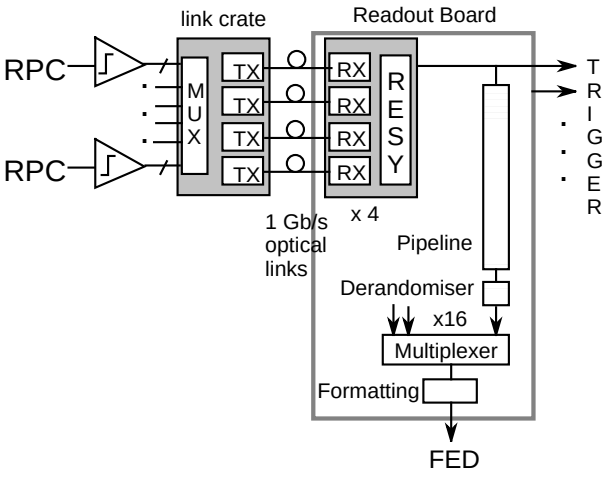

Fig.16. The organisation of the RPC readout.

The major issue for the muon system is the fact that most of the electronics are located in the cavern. Therefore low level radiation tolerance must be ensured for on-detector systems, power supplies and other rack electronics in the cavern which should also be immune to magnetic fields. If further electronics are implemented on the detectors, cooling requirements may increase. The trigger logic, especially for the CSCs, is not yet fully defined and must conform with the latency requirements of the tracker, which cannot easily be increased.

4.5 First level Trigger

Both the muon and calorimeter triggers [4] have been reviewed in previous conferences [24,25] and have not fundamentally changed.

4.5.1 Muon trigger

There are three components to the muon trigger from each readout system and data are assembled in processors dedicated to RPCs alone or CSCs and drift tubes combined before being assembled by the global muon trigger and associated with the calorimeter data.

Data from four muon RPC stations are used to make comparisons with predefined templates corresponding to different p_T ranges. Prototyping is under way using FPGAs, which will be supplanted by a Pattern Comparator Trigger (PACT) ASIC.

The drift tube hits are used by the meantimer Bunch and Track Finding Identifier (BTI) to form superlayer rϕ vectors and then combined in a Track Correlator processor to form a vector for one station.

The CSC trigger locates the centroid of each cluster from the fast shaped pulses which are fed to the local charged track processor (LCT) to find a coincidence of at least 4 out of 6 layers with predefined templates. The time, location and angle from the LCT form the trigger primitives for combination with the drift tube vectors.

The Track Finder [26] combines track segments from DT and CSC, assigns p_T and the segments are sorted by the Muon Sorter before the global muon trigger processor combines PACT and Tracker Finder data. Most of the processors are being prototyped as FPGAs for subsequent implementation as ASICs.

4.5.2 Calorimeter triggers

The electron-photon trigger is based on recognition of a large isolated energy deposit in the ECAL combined with small hadronic energy in the same region, while jet and missing E_T triggers are based on energy sums over η−ϕ regions [25,27,28].

The trigger logic is implemented as specific processor boards mounted in regional trigger 9U crates. One significant recent change is a result of the ECAL plan to transmit digitised data from every front end channel instead of undertaking digital signal processing on the detector and sending trigger primitives to the counting room.

A major issue for the trigger electronics is high speed digital interconnections, on which progress seems to be very good. Overall synchronisation is a general problem for the experiment, to define a strategy to align each detector system in time, but is particularly subtle for the trigger [29].

The overall latency is estimated at 120 beam crossings [30] with uncertainties in relatively few components. However it is maintained under constant review because of the severe penalties on production of front end electronics for the tracker where chips are already large and implemented in almost final form. The latency cannot be allowed to increase above about 128 beam crossings.

4.6 Data Acquisition

To include a review of the data acquisition system is beyond the scope of this paper. The CMS architecture has not changed fundamentally since the Technical Proposal [4] where it is outlined in some detail. It is based on a processor farm where higher levels of trigger are implemented in software (fig. 17). A high performance switch network is used as the backbone of the Event Builder, based on 1000 x1000 x 622Mb/s links connecting dual port memory buffers from the front ends to the processors in the farm [31,32].

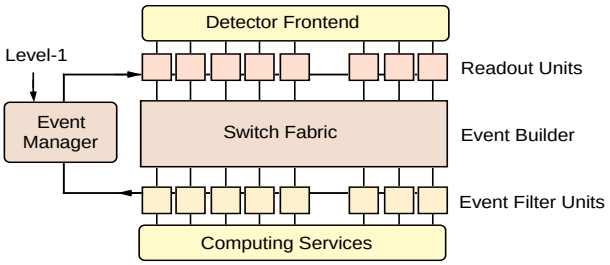

Fig. 17. Data acquisition basic structure.

The issues which seem most prominent from an electronics viewpoint are:

overall synchronisation of the readout systems of the different sub-detectors and trigger,

the physical implementation and location of the DAQ input buffers (RDPM) following the FEDs,

the choice of switch technology and the sufficiency of available bandwidth (or, alternatively, the adequacy of data reduction at the FEDs),

the matching of the front end hardware to the DAQ architecture to allow efficient transmission of partial data to the farm for higher level triggers,

the evolution of the DAQ in the coming years.

Interim DAQ systems are needed for large scale prototyping and it will be helpful if there is a planned merging of these systems into the final one rather than a dramatic transition from old to new. This problem is not unique to the DAQ. However, since the computer industry is evolving rapidly and there is a need to utilise the most cost effective CPU power at LHC start-up, there appears to be a risk of postponement of choices which may then require additional resources to develop short term DAQ solutions which are later abandoned.

4.7 Control and monitoring

It is envisaged that all the sub-system dependent hardware will be interfaced to a common controlsystem. Conceptually there could be a boundary, above which standard, possibly commercial, hardware and software is utilised. Below this would be detector specific components driven through boards connected to, e.g., VMEbus. At present it is difficult to define such a boundary in all sub-systems and the responsibilities are therefore not fully clear. Some systems already have some special requirements, such as temperature monitoring of the silicon tracker, which they may not be ready to entrust to a system outside their control. There has also been discussion of the need to utilise common field bus structures throughout the experiment. However the requirement to implement some of them in radiation tolerant form may not be practical.

Clearly, although the goal is desirable there is some way to go before a common control system can be defined. For this to span all the LHC experiments seems possible but not imminent. Meanwhile there will be a need for intermediate systems to operate in conjunction with large scale prototypes and it could be desirable for these temporary control systems to merge smoothly into the final one.

5. CMS electronics system management

To achieve a coherent management at the experiment level is a challenging task, given the individualistic nature of the high energy physics community and the many competing pressures. Up to now some co-ordination has been possible through regular sub-system co-ordinators meetings where some of the issues discussed (often many times) are listed in Table 2.

Table 2
Latency and synchronisation
Trigger, clock, command distribution
Digital optical links
VME crate standards
Cavern electronics
Radiation tolerant ASIC requirements
RADTOL R&D proposal
Planning of DMILL submissions
Low voltage power delivery and regulation
ASIC testing facility
LHC like test beam
Counting room space allocation
QA management, specifications, documentation

One concept which has been generally endorsed and is beginning to be implemented is to hold internal reviews of sub-system electronics with specialists from outside

the sub-system discussing progress, milestones, critical areas and technical issues with internal experts. However, it is too soon to say how successful this will be in guiding the experiment to completion. Nevertheless some of the benefits of co-ordination are obvious (Table 3):

One question to which a clear answer is not easy to give is whether our community can adopt techniques used elsewhere, such as industry or space science, to manage projects on the LHC experiment scale. Since such a large fraction of the experiment cost is in the electronics systems and the consequences of even partial failure are so far reaching, it is to be hoped that improved management methods will be adopted since good organisation, as well as the technical quality which the conference will demonstrate, will be crucial to timely delivery and future reliable operation of the experiments.

Table 3
Communication between sub-systems *identification of common problems*
Possible common projects or joint efforts *digital optical links, LV power, rad hard electronics costs*
Pre-empt major problems *trigger latency, radiation soft electronics in cavern, equipment in stray magnetic field*
Suggest policy on important issues *LHC like test beam, guidelines for equipment in cavern*
Comparison between sub-systems *relative progress and management, recognition of ideas/components elsewhere*

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