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RD49 Status Report
Study of the Radiation Tolerance of ICs for LHC

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Executive Summary

The RD49 project was approved in March 1997 with the twin objectives of:

1. Assessing radiation tolerant design and layout techniques applicable to commercial sub-micron technologies and making them available to LHC design teams.

2. Establishing collaborations with specialists from the space agencies and drawing on their experience and databases of measurements on the radiation tolerance of Commercial Off The Shelf (COTS) components.

The following milestones were set:

- Assess the radiation tolerance of a 0.5 μm CMOS process, based on the results from specially designed radiation tolerant test structures and on the design and evaluation of prototype chips for the ALICE pixel and TPC detectors.

- Carry out a preliminary study of the radiation tolerance of 0.35 μm and 0.25 μm CMOS processes using test structures and choose one of these technologies for further study in 1998.

- Negotiate non-disclosure agreements for access to the space agencies' COTS component databases, such that relevant information can be made available to the LHC experiments.

In the first year of the project fruitful contacts have been established with several Space agencies (ESA, CNES, NASA) and with institutes specialised in the hardening of integrated circuits (Sandia Nat. Lab., Aerospace Corporation, CEA, University of Montpellier). These contacts have been of considerable benefit and have helped the collaboration achieve the milestones set by the LHCC. Close collaboration with the electronics co-ordinators of the LHC experiments has ensured that the LHC radiation environment and the requirements in terms of radiation tolerance are beginning to be understood.

In 1997 two RD49 meetings were held at CERN in which the US and European Space communities interacted with representatives of the LHC experiments. As a result the LHC community has become aware of the importance of two new radiation tolerance issues, namely:

- *Low dose- rate effects on bipolar integrated circuits.*
  At low dose-rates (<10 rad/s), the degradation of the current gain (β) of a bipolar device caused by ionisation is much more severe than the degradation observed under the high dose-rate test methods employed in standard qualification procedures. This unexpected effect is known to be process dependent, and the underlying mechanism is still under discussion. The LHC collaboration's previous conclusions about the radiation hardness/tolerance of bipolar ASICs and COTS components need to be checked in the light of this new effect.

- *Single Event Effects (SEE)*
  A single ion (e.g. a nuclear fragment originating from an interaction in the material of the integrated circuit or its package) can deposit sufficient density of charge in the sensitive region of the circuit to upset its normal electrical operation. One form of SEE is known as *Single Event Latch-up* (SEL), in which parasitic transistors are turned on and establish a short circuit path between the supply voltage and ground. A second form of SEE is the *Single Event Upset* (SEU), which causes the flipping of a memory state, or the corruption of the integrity of a digital signal. It should be noted that SEL can be destructive, and SEU can cause system-level malfunctioning; therefore it is important to characterise the sensitivity of LHC electronics to SEE.

In order to define more precisely the required radiation tolerance of electronics at the LHC, and to understand to which extent the COTS components databases compiled by the Space Agencies are applicable at LHC, we have studied the radiation environment in the outer regions of the LHC detectors and the cavern and compared it to the space radiation environment. We begin to understand

this environment, but more work is needed to assess the impact of nuclear interactions caused by neutrons and hadrons on the modelling of Single Event Effects (SEE) in integrated circuits. We conclude that the Space COTS protocols for CMOS devices can be applied to the LHC, but new protocols are needed for bipolar devices

A preliminary list of crucial LHC COTS components has been established, and an initiative has been launched with a semiconductor company to investigate the possibility of industrial production of one of these critical COTS, namely a monolithic, low-drop radiation-tolerant voltage regulator (a component that is essential for the local powering of LHC subdetectors, but is presently not commercially available).

The radiation tolerance to total dose effects at the device level in submicron and deep submicron CMOS processes has formed the main technical study of the project. Preliminary measurements of the parameters of submicron and deep submicron CMOS devices indicate that total dose effects are strongly improved in smaller feature size CMOS processes. It has been found that the threshold voltage shifts (Vt) of PMOS and NMOS devices are less than -200mV for a 0.5μm process, less than 50mV for a 0.35μm process and less than -10mV for a 0.25μm process after total doses of 1 Mrad in the case of the 0.5μm and 0.35μm processes, and up to 10 Mrad in the case of the 0.25μm process. These values of Vt were measured without annealing. The observed drift of all electrical parameters was insignificant after neutron fluences of 10^{14} n/cm^2.

An assessment of the radiation tolerance at the circuit level has been made in a 0.5μm process with circuits designed using special layout rules which employ an edgeless geometry for NMOS transistors and surround them with a guard ring. The effectiveness of these radiation-tolerant layout rules has been verified (up to doses of more than 2 Mrad) with test circuits implemented in 2 different sub micron CMOS processes. Furthermore, in collaboration with ALICE and RD19, a pixel readout demonstrator chip has been developed in the MIETEC 0.5μm CMOS process using the same radiation tolerant layout rules. Radiation tests performed up to a total dose of 1 Mrad on the pixel readout chip have fully confirmed the effectiveness of this approach.

For the Single Event Effects, a latch-up study with heavy ions has been performed on 0.5μm special test structures. This indicated a Linear Energy Transfer (LET) threshold higher than 55 MeV.cm^2 mg^{-1}. This preliminary result indicates that submicron CMOS processes have a low sensitivity to latch-up. The measurement has been done on a small ring oscillator circuit (10 000 μm^2) and needs to be confirmed with a much larger and more complex circuit, such as a large SRAM memory.

For next year, the RD49 collaboration proposes to address the following objectives :

1. COTS:

- **COTS databases**: finalisation of the list and database of crucial, common LHC COTS components to be placed in the cavern and outer detector regions. Our preliminary list includes ADC, DAC, Fieldbus protocol chip, FPGA, voltage regulators, low-offset amplifier, etc. This list should be completed, checked with the LHC experiments and linked to the existing databases and know-how of the specialised agencies. In addition, we propose to work with Sandia Nat. Lab., ESA and CNES to draw up a recommended LHC qualification protocol for radiation tolerant COTS. On this basis, RD49 can disseminate greater awareness in the LHC collaborations about the complex COTS issues.

- **Voltage regulator**: To develop in collaboration with SGS-THOMSON and the University of Montpellier a radiation-tolerant voltage regulator based on specifications provided by LHC users. In the first phase measurements on samples from a candidate process will be made. If they show the process to be suitable SGS-Thomson will proceed with the design of a radiation tolerant voltage regulator. Industrial prototypes manufactured by SGS-THOMSON are targeted to be available by the end of 1998.

- **Bipolar low dose-rate effect**: To work together with silicon foundries and specialised institutes on the study and qualification of the low dose-rate effect in bipolar ICs. In particular, the development of a valid accelerated qualification protocol based on high dose-

rate irradiation at elevated temperature. Dissemination of awareness of the low dose-rate effect and the appropriate qualification procedure in the LHC collaborations.

2. Radiation effects on deep submicron CMOS processes

Development of a test structure in 0.35/ 0.25µm CMOS process to study total dose effect and SEU effects. This work will complement the study done in 1997, and will be focused on the assessment of the edgeless NMOS design technique and the measurement of Single Event Effect sensitivity in deep submicron CMOS processes, and on the study of SEU radiation resistant memory.

- **Total dose**: More statistical measurement will be made on different fabrication batches to verify the stability of the radiation tolerance of submicron processes. The decision concerning the choice of the submicron CMOS process will be taken after this study and the availability of the results from the 0.25 µm test transistors of SGS-THOMSON (received only in December 97 and presently under test).

- **SEE**: improve the understanding of issues related to SEE in LHC experiments with the help of institutes specialised in the field (Sandia Nat. Lab., ESA and CNES). A test structure will be developed and used to evaluate the SEL and SEU sensitivity in 0.35/0.25µm technologies. LET thresholds will be measured with heavy ion and proton beams. The overall objective is to understand how to design SEE-immune circuits.

3. The transfer of radiation tolerant design know-how to LHC design teams

- **LHC radiation tolerant ASICs**: The transfer of radiation-tolerant design know-how into those specific LHC projects with a requirement for radiation tolerance. Such developments will be in a 0.5µm/0.35µm/0.25µm CMOS process. We plan to work with the following projects in 1998:
  (i) a radiation-tolerant, low-power, large dynamic range ADC for the ALICE TPC,
  (ii) front-end circuits for the ALICE Silicon Drift Detector,
  (iii) further development of the radiation-tolerant pixel detector electronics for ALICE,
  (iii) high-speed radiation-tolerant electronics for Gbit/s digital detector readout links.

- **Radiation tolerant standard cell**: The development of a restricted number of selected radiation tolerant submicron standard cells that are immune to SEE and total dose effects. The cells developed will be those needed for the above applications. Contacts will be maintained with ESA-ESTEC and CNES, who are developing a radiation tolerant standard cell library.

1. Introduction

Since March 1997, several actions have been undertaken by RD49 to address the numerous issues related to the use of electronics components in the harsh radiation environments of the LHC experiments. First of all, the understanding of the environment itself was addressed in order to be able to benefit from the experience of the Space Agencies. In particular, it was necessary to clarify the radiation level of LHC experiments, not only in terms of total dose, but also in terms of the neutron and proton fluence and the energy spectra. Armed with this detailed information we are in a better position to assess the risk of SEE due to large linear energy transfer by heavy ions and by nuclear fragments produced as by-products of nuclear interactions in the material of the chips.

2. Comparison of the Space and LHC Radiation Environments

The first task of RD49 has been to study and compare the radiation environment of LHC experiments with the Space environment with the aim of understanding whether the qualification results of components for space applications are usable by LHC experiments. Thanks to the data given to us by M. Huhtinen and by Space agencies, this comparison has been made possible. As shown in Fig.1, the total dose and dose rate figures typical of Space applications are comparable to those expected in the calorimeters, and higher than most of the muon detector system and the cavern.

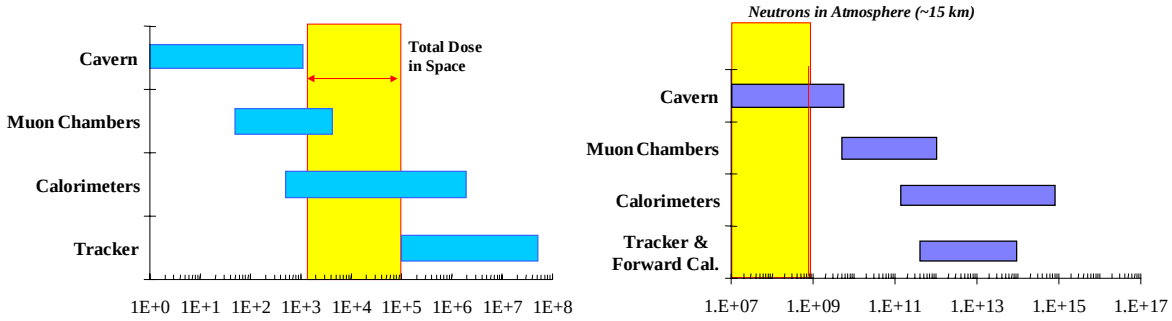


Figure1 Comparison of total dose(left) and neutron fluence (right) in the Space and in CMS. X-scale is in rad (left) and neutron/cm^2 (right) for 10 years of LHC operation.

Therefore, a similar qualification approach to total dose could be used in both environments. On the contrary, the neutron environment is very different, being not an issue for Space applications. The presence of a much higher neutron fluence at LHC has a significant impact on the radiation hardness of bipolar components, whereas it is insignificant for CMOS components. Therefore, analog bipolar COTS should be carefully tested to neutron fluence for use in LHC, especially because this is not part of the qualification procedures for components for Space.

3. Characterisation of the Radiation Tolerance of submicron CMOS Processes

Full results of this activity have been reported at the LEB conference held in September. A copy of the paper presented on that occasion is included as Annex 1(a) and further information is given in annex 1(b).

3.1 Characteristics of sub-micron processes

Our study was focused on four different processes from three manufacturers, covering three technology generations: 0.5µm (2 processes studied), 0.35µm and 0.25µm. An overview of the four

processes is shown in Table 1. The structures used have been out of normal, commercial grade CMOS fabrication lines with no special steps applied to harden the devices.

Table 1 : *overview of the four technologies studied*

	A	B	C	D
L (drawn) [µm]	0.5	0.5	0.35	0.25
t_{ox} [nm]	10	10	7	5.5
Device isolation	LOCOS	LOCOS	LOCOS	STI
Supply [V]	5-3.3	3.3	3.3	2.5
K' [µA/V^2] N/P	89/23	87/24	139/32	178/43
Vth N/P [mV]	670/-640	580/-590	630/-650	700/-550

Thanks to the new facilities available at the microelectronics group at CERN, a significant number of test structures in the four processes have been irradiated and characterised. These facilities include a calibrated X-ray machine, which allows fast irradiation of devices, and an automatic characterisation system consisting of an HP4145B semiconductor parameter analyser and a Keithley 707 switching matrix controlled by a PC.

3.2 Total dose measurements

The thickness of the gate oxide and the voltage supply are scaled down with the minimum feature size of technologies, and as a result a smaller threshold voltage shift is expected after radiation exposure. Our measurements on three generations of CMOS processes have confirmed this tendency. The trend is clearly seen in Fig. 2, which shows the threshold voltage shift of worst-case biased NMOS and PMOS transistors as a function of the total dose.

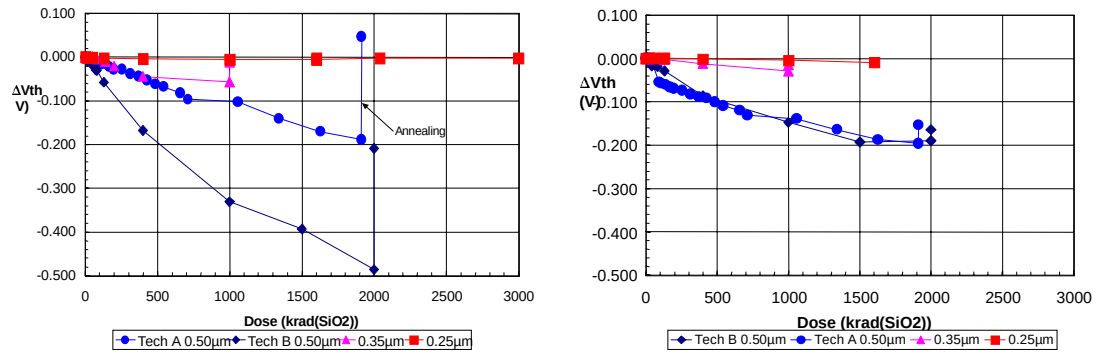


Figure 2 *Threshold voltage shift of submicron NMOS(left) and PMOS (right) from processes A,B,C,D*

After annealing for one week at 100^{o}C (the last point in the graphs), three out of four of the technologies have threshold voltage shifts well within acceptable limits. The significant difference in the performance of the two 0.5µm processes is probably due to some differences in the fabrication steps used for gate oxides. The most recent quarter micron process showed a shift of less than 10 mV after 3Mrad (SiO_2).

The excellent performance of the gate oxide of the quarter micron process is evident also in Table 2, which reports the mobility degradation of NMOS and PMOS transistors in three different technologies after 1Mrad(SiO_2) and annealing. The mobility is dependent on the quality of the Si-SiO_2 interface, and normally decreases after irradiation and annealing because of the creation of interface states. As shown in Table 2, the decrease in mobility is less important for thinner gate oxides.

Table 2 : *percentage mobility degradation for three different processes after 1Mrad(SiO2) and one week annealing at 100°C. The transistor width was 10μm in all cases. The gate length was the minimum allowed in each technology.*

Device type	Tech. B (0.5μm)	Tech. C (0.35μm)	Tech. D (0.25μm)
NMOS	-10%	-6%	-4%
PMOS	-5%	-4%	-3%

If the gate oxide thickness, and hence the radiation tolerance, scales with the feature size, the same is not true for the field and lateral oxides. Therefore, significant trapping of charge occurs in these oxides during irradiation. Whichever lateral isolation technique is employed, charge trapping in the lateral oxide can cause source-drain leakage current in NMOS transistors. A recent study of the model of the parasitic structure of the NMOS responsible for leakage has been developed in collaboration with RD49, a copy of the paper is in annex 2. Post-rad leakage is shown in Fig. 3 for the four different processes.

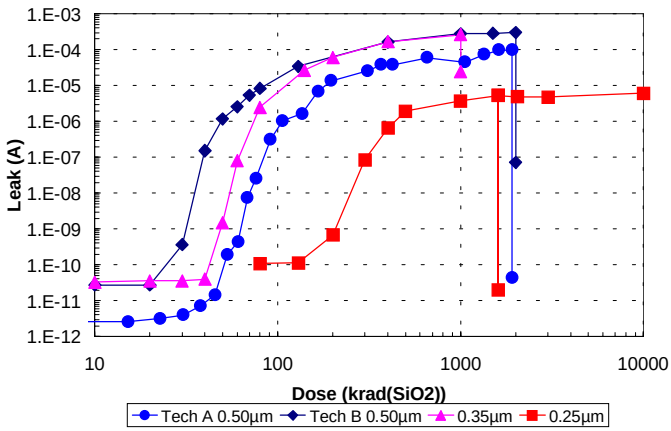


Figure 3 *Post-rad leakage current of submicron NMOS transistors*

Only the quarter micron process, with STI isolation and nominal voltage of 2.5V, does not show any leakage up to almost 150krad (SiO_2). In the other three technologies, with LOCOS isolation and nominal voltage of 3.3V, the leakage begins at doses lower than 50krad(SiO_2). Also, the saturation current is more than one order of magnitude lower for the 0.25μm technology. After the high temperature annealing, all leakage decreases considerably and in some cases it approaches the pre-rad value.

3.3 Total dose effects on noise

The preliminary noise measurements on 0.5 μm CMOS technology indicate no significant noise increase after 100 krad both for 1/f noise and white noise as shown in Fig. 4 .

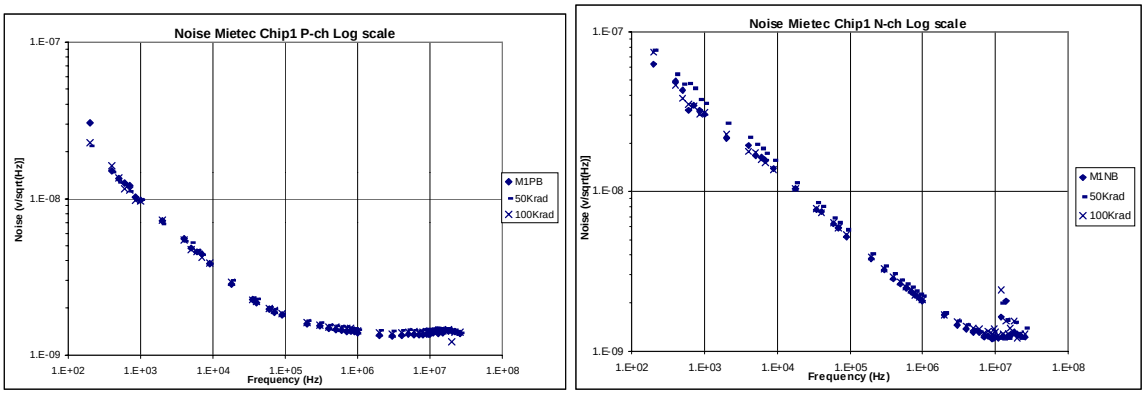


Figure 4 *Noise spectra of 0.5μm PMOS (left) and NMOS(right). Transistor size is W=2000μm, L=0.7μm*

3.4 Neutron fluence effect

It is well known that CMOS processes are not significantly sensitive to displacement damage caused by neutrons or heavy particles. Therefore, we have made only one test at neutron fluences of 10^{12} , 10^{13} and 2 10^{14} neutron/cm^2 with various transistors , test structures and ASICs. The neutron source used was very clean , 10 krad of total dose for 10^{14} neutron/cm^2. All post-rad measurements indicate no change, or very small change of the electrical characteristics of devices (VT shift, and leakage) and the performance of ASICs (gain, noise and offset).

3.5 Conclusion

The result shows that, as foreseen, the radiation tolerance of the gate oxide to total dose effects increases when scaling down towards smaller sizes. The radiation resistance to total dose effects is therefore limited by the leakage currents due to charge trapping in the thick field and lateral oxides. Nevertheless, the results suggest that these technologies, preferably the quarter micron, could be used without following any special design rules to design ASICs for moderate radiation environments in LHC (such as the cavern or the muon chambers). The neutron fluence, even up to 2.10^{14} n/cm^2, does not degrade the performance of submicron CMOS ICs.

4. Annealing Effects in CMOS Devices and Qualification Procedures

The qualification procedures presently recommended by the major space agencies prescribe a fast irradiation followed by high temperature (100^{o}C) annealing for 168 hours. To be accepted the component should pass both the test immediately after irradiation and after annealing. The measurement after irradiation gives the worst case behaviour for the effects of charge trapped in the oxide, whilst after annealing the worst case refers to the effects of interface states. In the LHC, the dose-rate will be lower (1.4 krad/h to less than 0.027 krad/h) and the annealing will occur during irradiation. Particularly for submicron and deep submicron circuits (both ASICs and commercial circuits), where the dominant effect for failure comes from the oxide trapped charge, the use of the standard qualification procedure might discard circuits which, in a low dose-rate environment, could well survive. The availability of a qualification procedure able to predict the low dose-rate behaviour of components tested at high dose-rate would therefore be extremely helpful in choosing the components for LHC.

In 1997, the RD49 collaboration has started to work in this direction. The initial step was a long term irradiation performed, at a dose-rate comparable to the range of the LHC outer regions (0.13 krad/h), with a ^{137}Cs gamma source. The measurements were done on elementary transistors from two submicron processes, up to a total dose of about 60 krad. The results were compared to those obtained irradiating the same devices with a high dose-rate, using an X-ray generator. This work was presented at the LEB workshop held in September 1997 (London), and a copy of the paper presented on that occasion is annexed to this report (Annex 3). The conclusion is that, especially for the thick oxides where bulk charge trapping dominates, the degradation at high dose-rate is significantly higher. After the annealing that follows the high dose-rate irradiation, the radiation effects often almost disappear, but also this is not representative of the low dose rate environment. Only the knowledge of the energy distribution of the traps in the oxide for each technology would permit the prediction of the low dose-rate behaviour.

A methodology to study the energy distribution of traps in the bird's beak of the transistors has recently been proposed (see Annex 2). A similar approach is followed by the University of Montpellier, with the aim of being able to apply it to the generic circuit, without knowing details about the technology. Our objective is the definition of a test procedure to recommend for the prediction of CMOS circuit degradation in a low dose-rate radiation environment.

5. Assessment of the Special Radiation Tolerant Design Layout Rules

As shown above, the main radiation tolerance limitation in submicron technologies is the leakage currents originating from charge trapping in thick oxides. The use of “enclosed” or “edgeless” NMOS structures prevents the leakage along the edge of the transistor (bird’s beak), by eliminating the lateral thick oxide. Also, the use of guard-rings around n-channel transistors is effective in eliminating parasitic inversion channels under the thick field oxide, and hence assures the isolation between devices. The guard-rings are also effective in reducing the latch-up sensitivity. An example of these layout techniques is given in Figure 5.

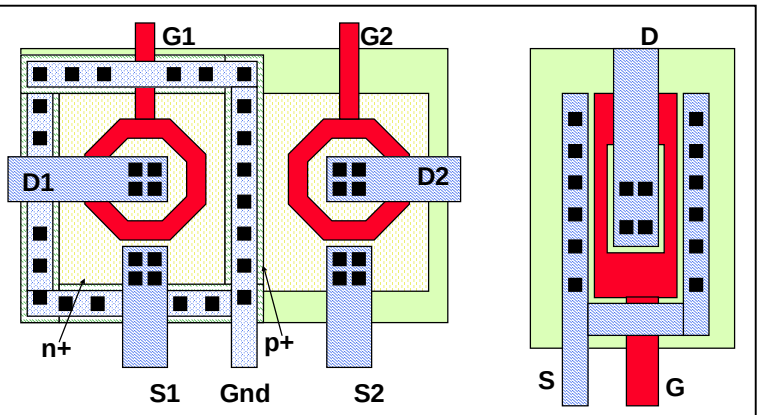


Figure 5 *Radiation tolerant layout of NMOS transistor*

We have designed dedicated test structures containing elementary transistors, ring oscillators and shift registers to assess these techniques. The integration in silicon was done in the two 0.5µm processes.

5.1 Measurements of the rad tolerant test structures

The measurements on the 0.5µm test structures have demonstrated that, using enclosed devices and guard-rings, the charge trapping in the thick oxides no longer plays a role in the radiation response of the devices. Figure 6 shows the source-drain leakage current for the enclosed transistors as a function of total dose, and compares it to the normal transistors.

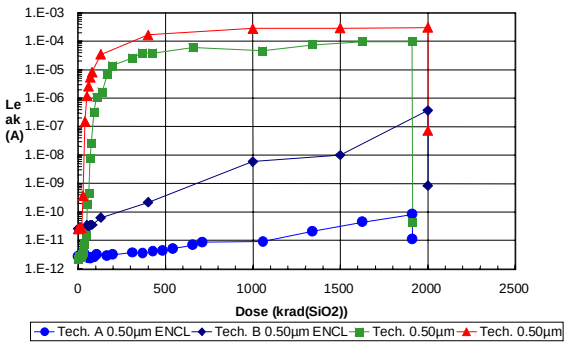


Figure 6 Post-rad leakage current of 0.5 µm NMOS.

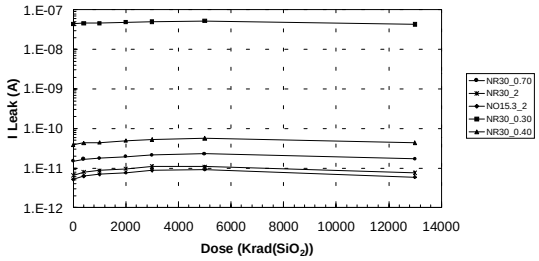


Figure 7 leakage current of 0.25µm NMOS

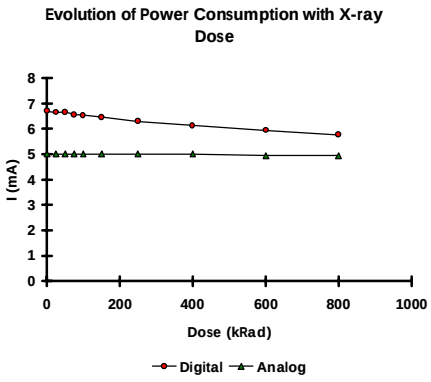
The residual leakage current of enclosed transistors, which is different in the two measured 0.5µm technologies, is determined by the threshold voltage shift. Therefore, the radiation resistance is determined by the gate oxide radiation characteristic, and should improve in deep submicron devices. A confirmation of this expectation is given by the leakage current measurement of enclosed transistors in the quarter micron process, shown in figure 7 for total doses up to 13Mrad(SiO_2).

In conclusion, the dedicated test structures have shown that the layout technique proposed (enclosed transistors with guard-rings) is effective in eliminating leakage currents due to charge trapping in the thick lateral and field oxides. Notice that this technique is based on the knowledge of the physics of radiation effects on CMOS technologies, and is only weakly dependent on specific process characteristics. It therefore is immune to sudden and unannounced process modifications.

In order to demonstrate this technique in complete circuit, a prototype version of a new pixel read-out chip for ALICE was designed together with the RD19 collaboration using the hardened layout technique. The design was manufactured in one of the two 0.5μm processes.

5.2 Pixel prototype readout chip in a 0.5 μm process

A new pixel readout prototype has been developed for the ALICE pixel detector. It consists of a 65 by 2 matrix of identical 50μm x 420μm pixel readout cells. It is a small test chip to evaluate some improvements over previous readout chips with regard to both front end performance and radiation tolerance. Each readout cell comprises a preamplifier, a shaper filter, a discriminator and readout logic. Because it is not the intention to bump bond it to a detector, an input structure has been added to the cell to simulate detector capacitance and leakage current. The chip occupies about 10 square mm, and contains about 25000 transistors.



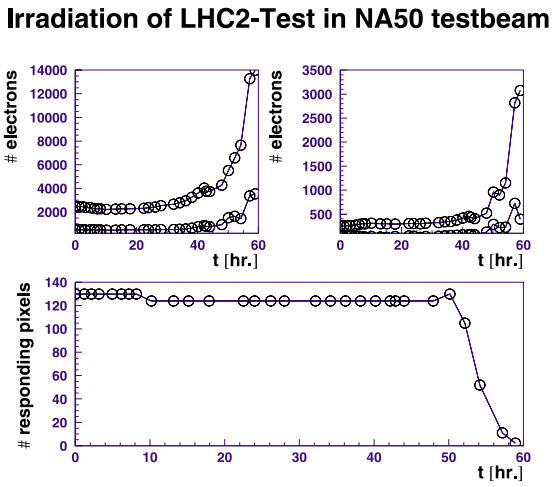


Figure 8 *Pixel chip supply current consumption as a function of the X-ray total dose.*

Figure 9 *Irradiation of the pixel chip in NA50 experimement.Upper left:rms threshold spread as a function of total dose. Upper right: rms and average noise as a function of total dose. Bottom: Number of pixel responding above 20 000 e- . X-scale is 2 Mrads for 40 hours.*

The radiation tolerance of this circuit, implemented in a commercial 0.5 μm CMOS technology, has been enhanced by using edgeless NMOS devices and guard rings. At an X-ray dose-rate of 4 Krad/min the chips started to degrade significantly only after 600 Krad. Fig. 8 shows that with increasing X-ray dose the analogue power consumption remains unchanged and that the digital power consumption decreases. This illustrates on a global scale that edgeless NMOS devices and guard rings prevent radiation induced field oxide and bird's beak leakage.

In the NA50 experiment, where a chip was placed right behind the target but slightly offset with respect to the particle beam, significant degradation set in after a total dose of about 2 Mrads received in about 40 hours. This is illustrated in Fig. 9, which shows average (for all pixels) and rms spread of the threshold in the upper left plot, average and rms noise in the upper right plot, and the number of pixels responding below 20000 electrons at the bottom. In the bottom plot the drop from 130 to 126 and the rise back to 130 is an artefact. The drop to zero after 40 hours is real. The degradation after two Mrad (40 hours) is evident, but some recovery can be observed immediately after 40 hours when the beam was off for a couple of hours. The irradiation was continued up to 3 Mrads, at which point no pixels were responding below 20000 electrons. After a month of annealing at room temperature the

average threshold has come down again to about 7500 electrons, and the average noise to about 500 electrons.

6. Preliminary Study of SEE

Single Event Latch-up (SEL) is a major concern in space, where heavy ions can deposit enough ionisation energy in the electronics to turn on one of the bipolar parasitic transistors inherent in the CMOS structure. In LHC, the fluxes of particles will be dominated by charged hadrons and neutrons, and the nuclear interactions between these high energetic hadrons and the materials constituting the devices will generate heavy and highly ionising fragments (mainly alpha particles, but also metal or silicon ions). As latch-up can destroy the devices, it is essential to evaluate the probability of such an event occurring in the LHC environment. The activity of RD49 in this respect has been twofold: we have studied the radiation environment in the experiments to estimate the energy released by nuclear fragments in the devices, and we have performed some latch-up measurements at a heavy-ion accelerator. Further information on latch-up measurements is given in the Annex 4.

The estimate of the energy released in the materials by secondary fragments originating from in nuclear reactions is a complex problem that can only be quantitatively approached with the help of powerful simulators such as FLUKA. For the simulations, we have worked in collaboration with M. Huhtinen (CERN/PPE), who's in charge of the simulations of the radiation environment in CMS. The first results from the simulations have been obtained, giving the energy deposition spectrum for the secondary particles in a volume of silicon 4μm thick. The spectrum peaks at about 100-200 keV (secondary protons), with the maximum energy deposition at about 30MeV. More work needs still to be done in the interpretation of the data, and on the correlation of these results with the SEL measurements on specific components, which are normally done with heavy ions.

The first latch-up measurements were performed with a ^{252}Cf source at the University of Montpellier. The Mo and Ba fragments emitted by this source have an initial LET of about 45 $MeVcm^2mg^{-1}$, rapidly decreasing with the penetration depth in silicon. The test was done on simple and small structures integrated in two 0.5μm commercial processes. They were ring oscillators made up of elementary inverters, NAND and NOR gates, both with standard and hardened layout (enclosed n-channel transistors and guard-rings). Structures with hardened layout are expected to be less sensitive to SEL. No latch-up was observed on either structure, indicating that the LET of the ions at the critical depth for triggerring the phenomenon was not high enough. To get higher LET and penetration depth, we went to the Tandem Van De Graaff accelerator at IPN (Institute de Physique Nucléaire) in Orsay, where we did some measurements in collaboration with the French space agency, CNES. No latch-up was observed during irradiation with Bromine and Iodine ions, up to a maximum LET of 60 $MeVcm^2mg^{-1}$ (decreasing to 50 after a penetration of 10μm in silicon). These promising results, even though obtained on simple structures, show that neither 0.5μm technologies are very sensitive to SEL, and this is in agreement with the general trend that submicron processes are less and less sensitive to latch-up. Nevertheless, this potentially destructive phenomenon is strongly dependent on the layout, therefore the sensitivity can be very different for different circuits.

We intend to perform further measurements on more significant structures, with a larger area and higher device complexity. To do so, the experimental set-up developed, with the help of the University of Montpellier, to perform this first latch-up study will be very valuable.

7. COTS for the LHC Experiments

The LHC experiments plan to use standard instrumentation (integrated circuits, electronics boards and crates) to equip the outer regions of the experiments and the caverns. For the inner tracking regions, severely exposed to a high level of radiation, special precautions are taken, such as the use of radiation hard electronics and the qualification of all components used. In the case of the outer regions of experiments (calorimeter to muon detector system) and the cavern, a large variety of "Commercial-Off-The-Shelf" components (COTS) is planned to be used. Only recently, through the

discussions triggered by RD49 meetings, have the LHC detector teams become aware of the complex radiation tolerance issue for this type of component.

7.1 List of COTS for LHC

It is presently almost impossible to compile the detailed list of radiation tolerant standard components needed for LHC experiments. Systems level designs are not yet sufficiently established, and several integrated circuits embedded in electronic equipments are not known. Therefore, we have decided in RD49 to first address the crucial COTS which have a wide commonality between LHC sub detectors and experiments, and will have to be procured in large quantity. The following list contains the crucial radiation tolerant COTS already identified; the list is not exhaustive and will certainly evolve in 1998:

1. Voltage regulator; everywhere required in sub detectors and cavern for local powering
2. Analog to Digital Converter; required in several places, but especially needed in large quantity for data conversion of the calorimeter readout.
3. Digital to Analog Converter; needed in the calibration system of calorimeters.
4. FPGA; is mainly used in the muon system.
5. Low offset amplifier; for calibration system of calorimeters and pervasive use.
6. SRAM memory, pervasive use expected.
7. FieldBus; in the slow control system.
8. Gigabit link components; in high speed digital read out systems.

In addition, many other COTS, probably in smaller quantities, have to be used in LHC. For some of them previous Space qualification could exist. A first natural approach would be to search in existing databases for qualified COTS. We have already identified several databases with free access, ESA, CNES, JPL-NASA, Goodard-NASA. Sandia lab has a extensive experience in COTS up-screening and is ready to collaborate with us under a specific consultancy contract. There are other databases in companies working for Space, but those databases are usually kept confidential and are not accessible for commercial reasons. However, the validity of data in COTS databases has on average a short lifetime of the order of 18 months, and existing databases are for this reason partly obsolete. Great care must be exercised in using them.

For this reason the Space community is adopting a different procurement strategy; the single buy strategy in which a commercial silicon vendor reserves a production batch. The Space agencies then test (to radiation) samples of the batch and proceed to qualification. Only components from the reserved and qualified batch are purchased. LHC could profit from this strategy in collaboration with the Space agencies if we are able to precisely define our needs in terms of COTS types and quantity, and buy them in advance.

In the LHC cavern and the muons systems, the level of radiation (in total dose) is moderate, ranging from a few krad to a few tens of krad. Though this total dose seems to be low, failures at such levels have been reported. In addition, the presence of a high neutron fluence in these regions, 10^{11} to $2\ 10^{12}$ n/cm^2, threatens the functionality of COTS components using lateral bipolar transistors. In the framework of the study of the radiation tolerant voltage regulator, we have tested lateral bipolar transistors to neutron fluences of 10^{12} and 10^{13}/cm^2. As shown in Fig. 10, the BETA drop after a neutron fluence of $2\ 10^{12}$ is huge. Therefore, it is clear that COTS using lateral bipolar transistors should be avoided.

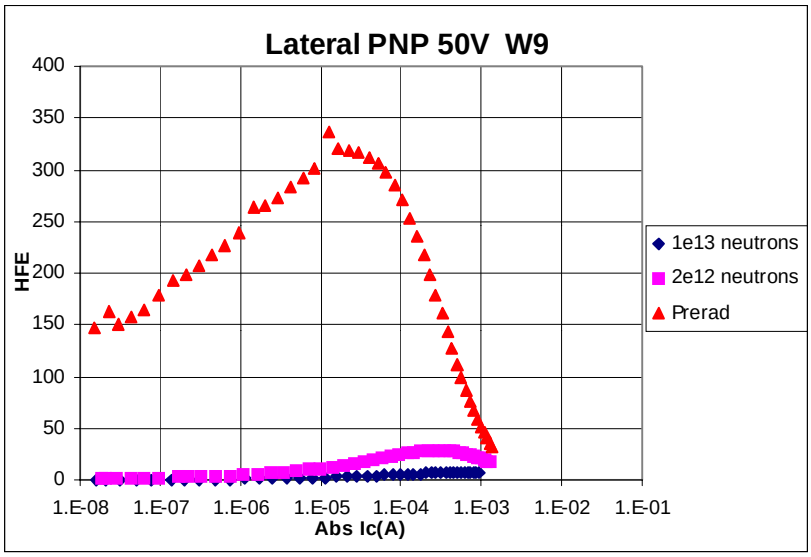


Figure 10 BETA drop of lateral PNP after a fluence of 10^{12} and 10^{13} n/cm^2

7.2 Qualification method

We have also realised that the radiation tolerance issue of COTS is more complex and challenging than expected, in particular for the selection and qualification procedures. The method used to take into account the annealing effect after accelerated radiation exposure of COTS fabricated in CMOS technology strongly influences the qualification result. In addition, the newly discovered low dose-rate effect on bipolar ICs puts into question the existing state-of-the-art qualification methods. A preliminary study has been launched to assess the feasibility of qualification based on a high dose-rate irradiation at elevated temperature (90 °C to 130 °C) .

Space Agencies and specialised institutes such as the Sandia National Laboratory have a long experience in the methodology of COTS qualification for Space applications. Following several contacts and meetings held with them in the framework of RD49, it appears that the radiation environment of Space is quite close the radiation environment of LHC, except for the neutron fluence which is much higher at the LHC. Therefore, for total dose effects, which is almost the only effect for COTS manufactured in CMOS technology, the Space qualification protocols can be equally well applied to CMOS COTS for the LHC.

However, COTS manufactured in bipolar processes are sensitive to neutron and proton displacement damage. Therefore, Space qualification protocols are not sufficient for LHC bipolar COTS, and it will be necessary to introduce additional qualification tests for taking it into account. In addition, the low dose-rate effect, as reported in the next section, increases the difficulty of qualification of bipolar COTS components.

7.3 Low dose-rate effect in bipolar processes

Recent measurements of the radiation tolerance of COTS components such as voltage regulators, amplifiers and ADCs manufactured in commercial bipolar processes have revealed an enhancement of the β drop for low dose-rates. This low dose-rate effect starts to be noticable below a dose-rate of 10 rad/s and continues to increase for lower dose-rate. This effect seems to be related to charge transport in oxide which depends of the space charge density, and consequently on the dose-rate. The current hypothesis is the following: the filling of metastable traps in the oxide, which play a key role in oxide charge transport, depends of the oxide space charge density. If the dose-rate is sufficiently low, an important fraction of the population of metastable traps are empty and they speed up the charge transport to the oxide-silicon interface, where recombination centres are built up. The final density of recombination centres at the interface, which depends on the dose-rate, determines the actual current

gain drop of the bipolar transistor. The amplitude of this effect strongly depends on the bipolar process characteristics, and therefore can not be easily modelled.

The main issue with the low dose-rate effect is the qualification protocol. Measurements indicate that the saturation effect in some cases is reached for very low dose-rates, such as 0.01 rad/s, excluding in practice the use of a similar dose-rate for the qualification protocol. A methodology presently under investigation is to perform a high dose-rate irradiation exposure at elevated temperature. This technique enables the thermal energy to increase charge mobility in the oxide and give a similar effect as for lower dose-rates at room temperature. We plan to do similar tests with samples of the bipolar process being evaluated as a candidate for the radiation tolerant voltage regulator.

7.4 Radiation tolerant voltage regulator

A preliminary study of the radiation tolerance of a 50V bipolar process carried out in the framework of the development of a radiation tolerant voltage regulator with SGS-THOMSON indicates that the lateral PNP bipolar transistor is very soft to total dose, as well as neutron fluence, as shown in Fig 11. Vertical PNP and NPN devices exhibit a better hardness as shown in Fig. 12 for the NPN device. However, its hardness is not sufficient to design a radiation tolerant voltage regulator standing 500 krad and more than 10^{13} neutron/cm^2 as needed at the LHC.

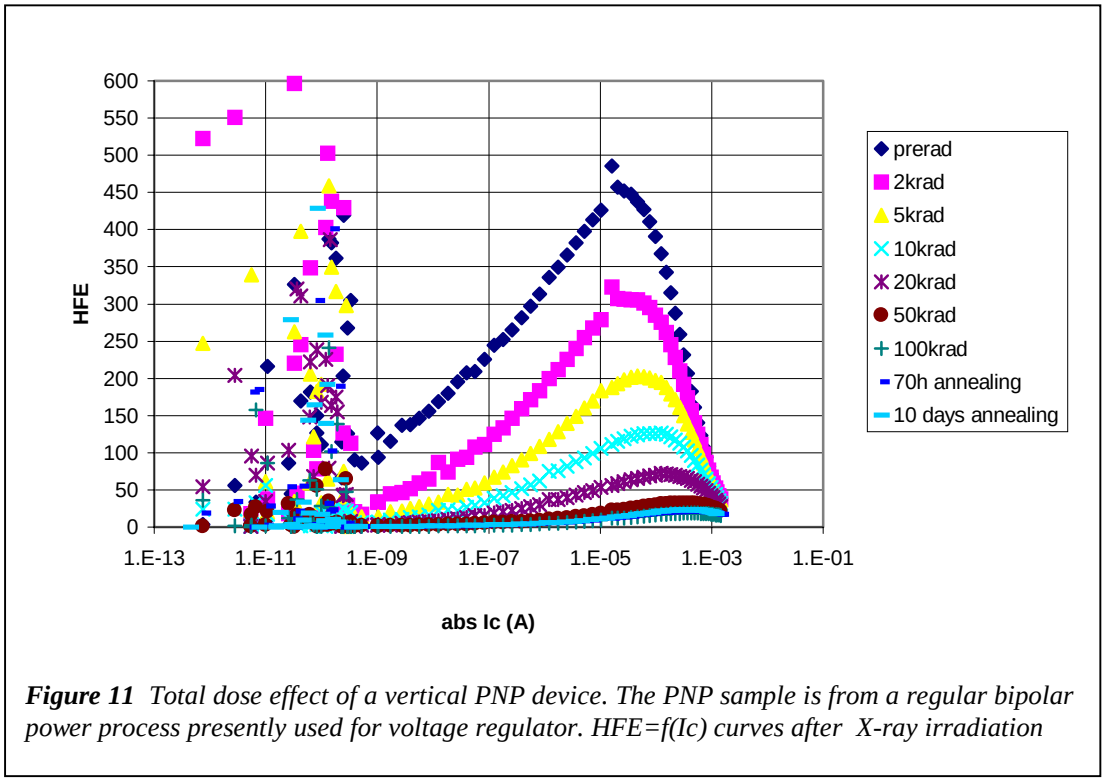


Figure 11 *Total dose effect of a vertical PNP device. The PNP sample is from a regular bipolar power process presently used for voltage regulator. HFE=f(Ic) curves after X-ray irradiation*

We have therefore decided in collaboration with SGS-THOMSON to investigate the radiation hardness of a more modern 12V high speed bipolar process available in the company.

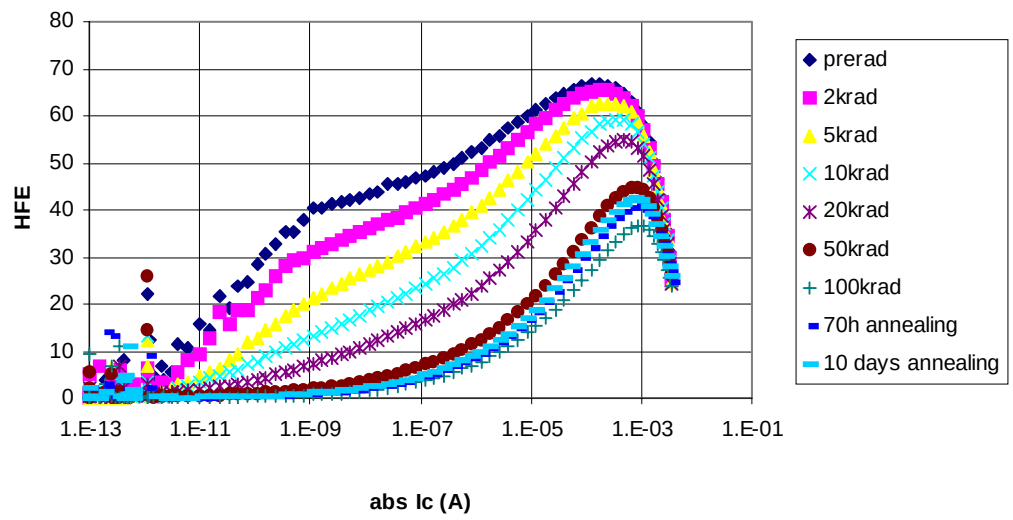


Figure 12 *Post rad current gain behavior of a vertical NPN device. NPN sample is from a regular bipolar power process presently used for voltage regulator. HFE=f(Ic) curves after X-ray irradiation*

The main advantage of a high speed bipolar process with small base width is its hardness to neutron displacement damage, essential for LHC applications. A preliminary evaluation of the process is under way.

8. Proposed Objectives for 1998

The objectives are listed separately for CERN and for the other institute members of the collaboration. For the specialised institutes, these objectives are part of their internal program. Their results will be shared in the framework of RD49, and the LHC community will be able to profit from them.

CERN

1. COTS:

- **COTS databases**: finalisation of the list and database of crucial, common LHC COTS components to be placed in the cavern and outer detector regions. Our preliminary list includes ADC, DAC, Fieldbus protocol chip, FPGA, voltage regulators, low-offset amplifier, etc. This list should be completed, checked with the LHC experiments and linked to the existing databases and know-how of the specialised agencies. In addition, we propose to work with Sandia Nat. Lab., ESA and CNES to draw up a recommended LHC qualification protocol for radiation tolerant COTS. On this basis, RD49 will disseminate greater awareness in the LHC collaborations about the complex COTS issues.

- **Voltage regulator**: To develop in collaboration with SGS-THOMSON and the University of Montpellier a radiation-tolerant voltage regulator based on specifications provided by LHC users. Measurements on samples from a candidate process will be made. If they show the process to be suitable SGS-Thomson will proceed with the design of a radiation tolerant voltage regulator. Industrial prototypes manufactured by SGS-THOMSON are targeted to be available by the end of 1998.

- **Bipolar low dose-rate effect**: To work together with silicon foundries and specialised institutes on the study and qualification of the low dose-rate effect in bipolar ICs. In particular, the development of a valid accelerated qualification protocol based on high dose rate irradiation at elevated temperature. Dissemination of the awareness of the low dose-rate effect and appropriate qualification procedure in the LHC collaborations.

2. Radiation effects on deep sub micron CMOS process

Development of a test structure in 0.35/ 0.25µm CMOS process to study total dose effect and SEU effects. This work will complement the study done in 1997, and will be focused on the assessment of the edgeless NMOS design technique and the measurement of Single Event Effect sensitivity in deep submicron CMOS processes, and on the study of SEU radiation resistant memory.

- **Total dose**: More statistical measurement will be made on different fabrication batches to verify the stability of the radiation tolerance of submicron processes. The decision concerning the choice of the submicron CMOS process will be taken after this study and the availability of the results from the 0.25 µm test transistors of SGS-THOMSON (received only in December 97 and presently under test).

- **SEE**: improve the understanding of issues related to SEE in LHC experiments with the help of institutes specialised in the field (Sandia Nat. Lab., ESA and CNES). The test structure developed will be used to evaluate the SEL and SEU sensistivity in 0.35/0.25µm technologies. LET thresholds will be measured with heavy ion and proton beams. The overall objective is to understand how to design SEE-immune circuits.

3. The transfer of radiation tolerant design know-how to LHC design teams

- **LHC radiation tolerant ASICs**: The transfer of radiation-tolerant design know-how into those specific LHC projects with a requirement for radiation tolerance. Such developments will be in a 0.5µm/0.35µm/0.25µm CMOS process. We plan to work with the following projects in 1998:
  (i) a radiation-tolerant, low-power, large dynamic range ADC for the ALICE TPC,
  (ii) front-end circuits for the ALICE Silicon Drift Detector
  (iii) further development of the radiation-tolerant pixel detector electronics for ALICE,
  (iii) high-speed radiation-tolerant electronics for Gbit/s digital detector readout links.

- **Radiation tolerant standard cell**: The development of a restricted number of selected radiation tolerant sub micron standard cell immune to SEE and total dose effects. The cells developed will be those needed for the applications. Contacts will be maintained with ESA-ESTEC and CNES who are developing a radiation tolerant standard cell library.

8.2 CERN LHC machine

Development of a radiation tolerant ASICs for the readout of the cryogenic temperature sensor of the LHC superconducting magnets. A precision of 0.25% of read value (corresponding to 5 mK at T=2 K) is needed, and a resolution of 1mK @ T=2 K have to be achieved with a radiation tolerant design. Know-how in RD49 will be made available to C4I/Archamps-F and the University of Madrid which are the institutes in charge of this development.

8.3 Institutes members

BNL

Design and fabrication of a radiation tolerant test chip in the HP process CMOS 0.5µm with appropriate structures to study radiation tolerance. VT shift, leakage current and noise measurement will be performed with a Co-60 source up to 100krad. This work is in the framework of the ATLAS muon system. The processing will be done via the MOSIS prototype service.

University of Padova

- Study of radiation effects on deep submicron CMOS process, with comparison of the radiation effects between total dose and Co-60.

- Study of the short channel effects associated with edgeless NMOS. Characterisation and modeling of the edgeless NMOS with a SPICE model, and comparison between physical and analytical model.
- Failure mechanism in thin oxide, with comparison between electrical stress and radiation effects.

University of Montpellier
Study of the radiation tolerance of bipolar processes for the development of a radiation tolerant voltage regulator. The study includes the low dose-rate effect.

University of Torino, INFN
Development of a radiation tolerant front end ASIC for the readout of the ALICE silicon drift detector.

LEPSI Strasbourg
Study of latch-up of an ASIC fabricated in the AMS CMOS process for the readout of the ALICE silicon strip tracker.

ESA-ESTEC
- Contribution to the LHC COTS databases.
- Collaboration on the development of radiation tolerant digital standard cell library.
- Development of a RADFET active dosimeter with its associated fieldbus electronics in collaboration with NMRC University of Cork.
- Access to the ESA Heavy ion and neutron SEE test facility at Louvain la Neuve.

CEA Bruyeres-le-Chatel
- Development of a qualification tool to predict radiation and annealing effects on complex integrated circuits based on the characterisation of elementary devices.
- Study the model of parasitic MOS structures responsible for post radiation leakage on 0.25µm and 0.18µm CMOS processes.
- Contribution to the understanding of the mechanism of the low dose-rate effect observed in bipolar technology

CNES Toulouse
- Study of the low dose-rate behaviour of the power bipolar process intended to be used for the development of the voltage regulator.
- Study of hardening at the system level.
- Help in analysis of the COTS for the LHC experiments.
- Collaboration in SEE hardening, characterisation and facilities.

LAPP Annecy
Study of the radiation tolerance of a high precision 12bit Digital to Analog converter for the calibration of the CMS calorimeter.

Institute of Physics Cracow
Study of the low dose-rate effect on a high frequency bipolar process.

Indian Institute of Technology Bombay
- Modeling of the annealing effects on sub micron 0.5 µm CMOS process.
- Comparison of total dose effects of X-ray and Co-60 irradiation.
- MOS dosimeter for active LHC total dose monitoring.

Annex

Annex 1(a)	Total Dose behaviour of submicron and deep submicron CMOS technologies, LEB'97 Proceedings London.
Annex 1(b)	Total dose study on 0.5um CNET_ST CMOS
Annex 2	Modelling of the radiation effect parasitic MOS structure, RADECS 97

Annex 3 Total dose behaviour of commercial submicron VLSI technologies at low dose rate, LEB ’97 Proceedings London .

Annex 4 Latch-up test on 0.5um CNET_ST CMOS