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The Drift Chamber Electronics and Readout for the NA48 Experiment

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Abstract

A drift chamber readout system for about 8000 channels with continuous sensitivity, i.e. concurrent data recording and readout, is described. Drift times are measured in bins of 1.56 ns with respect to a continuously running 40 MHz clock. The clock interval of 25 ns is divided into 16 bins by means of a 16 element delay chain. The length of this chain is linked to the clock interval by a phase locked loop. An ASIC chip was developed to perform time measurements and data storage for 16 channels. In an asynchronous readout of this chip, data are tranferred to intermediate buffers, for use in a first level trigger and eventual final readout. The design of the electronics is described and results from data taking runs are presented.

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1.The drift chamber spectrometer

The magnetic spectrometer of the NA48 experiment ([1]) consists of four drift chambers (fig.1), two upstream and two downstream of a diplole magnet with a bending power of 0.9 Tm. Each drift chamber is composed of 8 planes of wires arranged in 4 views (x,y,u,v) with 2 planes of staggered wires in each view to resolve right-left ambiguities. The wire orientations in the x,y,u,v views are at multiples of 45^0 to the horizontal plane and perpendicular to the beam. Sense wire spacing is 1.0 cm; one wire plane extends over 2.40 m and has 256 sense wires. The drift velocity in a 50/50 mixture of Ar/Ethane is 50 μm/ns. The chambers are normally operated with a gas amplification of $2 \cdot 10^4$ at 2.25 kV between potential and sense wires . The spectrometer is designed to measure K^0-decays ; the positioning accuracy of a track is specified as 100 μm. The mechanics of the chambers is described in ([2]).

Further detectors in the NA48 experiment are a liquid Krypton calorimeter with approximately 13000 cells of 2*2 cm^2, downstream of the magnetic spectrometer, a hadron calorimeter and various scintillation counter arrays for timing and vetoing purposes.

2. A deadtimeless readout and data acquisition (DAQ) system

The experiment is designed for high rates; it extends over approximately 150 m in space. Deadtime in the readout due to cable lengths and trigger processing time is avoided by a continuous data recording and filtering system. Individual subdetectors store the local information for a limited time in buffers, while trigger processors continuously collect this information and take decisions to accept or reject events. A readout command is issued from the trigger supervisor to all subdetectors for each accepted event, causing them to readout their local buffers. The arrival time of the event is used in the command to identify the event. A common 80 MHz clock is distributed among all subdetectors; it is interrupted for a few cycles before the beginning of each burst (every 14 s), to allow synchronisation of the subdetectors.

In the drift chamber readout system (fig.2) data pass through the front end, a zero suppression and a high multiplicity suppression filter to reach the central local buffer. This buffer is organized as a circular memory with 512 time sclices of 400ns width; in each slice there is room for 15 hits with 32 bits of information for each hit. Data are stored according to the arrival time of the hit; the wire address and the detailed time information are contained in the recorded data word.

The central buffer is continuously filled with data from an input queue. It is regularly overwritten, one slice at a time, with a clock derived from the experimental clock, about 200 μs after the arrival of a detector signal. During these 200 μs, data can be extracted , nondestructively, from the buffer. One of these extractions is on request from a level 1 (LV1) trigger; data are sent to a trigger processor which

looks for two- track events and selects them on the basis of the decay point position and the invariant mass. The decision of the LV1 trigger processor is passed to the trigger supervisor which then in turn takes the decision to keep or reject the event. If the event is to be kept, the drift chamber buffer is read a second time, including information from three adjacent time slices. Data are transported via an optical link to a data merger, where they are combined with data from other subdetectors .

3. Front End Amplifiers

The requirements for the amplifiers on the drift chambers are to provide the best possible timing accuracy with the smallest possible cross talk and pickup problems. The actual solution is influenced to some extent by the chamber geometry. For the large drift chambers of NA48 a scheme with front end amplifiers and discriminators on the chamber and transport of standardized signals to central time-measuring circuits (TDC's) was adopted.

The chamber frames are enclosed in a Faraday cage of Cu plates adapted to the geometry , such that only the connectors to the amplifier cards are left unshielded. Amplifiers for 16 channels are on one card. A 64 pin ELCO 3182 connector of 9.5 cm length is used for connection. It has two rows of 32 pins. One of them ends on the back metallization of the chamber PC boards and is connected to ground. In the other row every second pin is connected to a signal wire; the remaining pins end on grounded strips between the signal lines on the PC board. The amplifiers are build in SMD- technology on a four layer board. The signal layer is separated from the power supply layer by a ground plane. A fourth layer is used for signal connections. The analog part of the circuit occupies a space of 7mm $\times$ 40 mm for one channel.

The amplifier (fig.3) consists of a grounded emitter input stage with feedback from a subsequent emitter follower and an output stage with frequency dependent gain. The amplifier transfer function is 30 mV/μA; the input impedance, at 50 MHz, is 170 Ω, the rise time (10% to 90 %) is 8 - 10 ns. Crosstalk from neighbouring channels for pulses with 10ns risetime is suppressed with >46 db. The output is AC-coupled to a commercial discriminator chip (LeCroy MVL407) on the board. The discriminator threshold is derived from an external differential DC- voltage. In the NA48 experiment a threshold of 30 mV is applied; in test beams the amplifiers were also run at 20 mV. The discriminator output is shaped to a standard differential ECL pulse with 50 ns width followed by 50 ns of deadtime by means of a flipflop which resets itself with a delay line . A second hit arriving within 100ns of the first hit is therefore ignored. Pulse shaping with this limitation facilitated the design of the TDC circuits; it does not harm the measurement of two-body decays in NA48. The output pulses are then transported via 12 m twisted pair cables to the TDC's. The power consumption of the amplifier is 3.3 W for 16 channels, dominated by the logic circuitry.

The inputs are protected against sparks by diodes. The protection was tested with pulses from a 50 pF capacitor charged to 5 kV. This is more charge than a spark in the chamber can deliver; high voltage (typically 2.25 kV) is supplied individually to the potential wires with capacitances of less than 20pF through high impedance resistors.

Test pulses can be given to the inputs of all even or all odd channels simultanously. They are derived from standard differential ECL- pulses with fixed (1:10) attenuation. The sensitivity of the amplifiers can then be controlled by variation of the threshold.

4. A 16 channel TDC ASIC

In order to obtain drift times, both the arrival time of the ionization cloud at the anode wire and the time of passage of the charged particle are measured with respect to a common clock. The arrival time of the charged particle is obtained from a scintillation counter hodoscope. In order to measure the time of a drift chamber pulse with a precision of < 1 ns, a special circuit was developed in CMOS technology ([3]). The basic principle of the design is to use a delay chain with 16 elements of 25ns/16 individual delay, into which the clock pulse enters at the beginning of the clock cycle and from where it exits at the end of the cycle (fig.4). The time of a chamber pulse is then given by the location of the travelling clock in the delay chain at the time of the pulse. Drifts of the delay elements with temperature or supply voltage are avoided by the principle of a phase locked loop (PLL). The time of the exit of the clock pulse from the delay chain is compared to the arrival time of the next clock pulse . If there is a difference, a control voltage, upon which the individual delays depend, is changed, until the difference disappears. The control voltage is obtained from a capacitor, which is charged or discharged.

The delay elements are realized as current starved inverters (fig.5). The current in a CMOS inverter is controlled by the gate voltage of a series transistor. At low current the discharge of the output node is slow and therefore the falling edge of the output is delayed. The current starving transistor is bypassed by a small constant current in order to guarantee a smooth operation at low control voltage. Two such inverters are used, one for the delay of the leading edge and one for the delay of the falling edge. Two additional inverters reshape input and output signals.

The phase detector is made from three RS latches (fig.6). Depending on which input signal is first, the output is in the 0 or 1 state. The output determines the sign of of the current given to the filter capacitor. The design of this capacitor is influenced by the available technology. The chosen solution is to use the gate capacitance of a PMOS transistor operated in accumulation mode with the N well connected to ground, and a small capacitor between metal 1 and metal 2 in parallel to improve the high frequency performance. With the smallest of four selectable

currents the charging of the filter capacitor of 200 pF to 5V takes 40000 clock cycles; the PLL stabilizes after 20000 cycles. In the actual application the smallest current turned out to be always sufficient. The PLL can run between 16 MHz and 84 MHz; the frequency used is 40 MHz. All circuits involved in the time measurement are full custom design. Sixteen TDC channels are incorporated in one chip of 25 mm^2 area made in 1.0 μm technology. The chip is packaged in a 68 pin PLCC package ($\approx 2.5cm \times 2.5cm$).

In the actual chips the individual delay elements show characteristic deviations from the nominal values (fig.7); these deviations are however well below the measurements errors (0.5 ns) due to time binning.

For each hit the wire address and the delay with repect to the clock, encoded in 4 bits, as well as the lowest 13 bits of the clock cycle number, are recorded in an output FIFO register with 128 locations on the TDC chip. The clock cycle number counter is on the chip; it is loaded with a preset value at each synchronization of the subdetectors. The number of hits arriving at the input of the chip during a clock cycle is separately available as a 4-digit number, synchronously with the clock. This number is used in the present design of the readout to make a fast multiplicity sum over all wires in a plane.

A microprocessor (SAB80C166) controls all the TDC chips on one board with four differential signals: data in, data out, clock and strobe. The control logic satisfies the JTAG protocol. A number of internal registers of different sizes is available in the chip for test puposes. A pattern of hits and times can be generated and loaded into the output buffer . Channels can be individually enabled or disabled. It is therefore possible to test independently with preamplifier pulses and with test patterns. Other registers are used for initialization and control of the PLL.

5. Readout of TDC chips and fast multiplicity filter

The TDC chips are mounted on 8 layer VME boards in 9U format. The 16 chips corresponding to the 256 wires in a plane are on one TDC board. The ECL signals from the front end amplifiers are converted to TTL on the board, outside the TDC chip. The chips are read out in 50 ns intervals to two data streams, each serving 8 chips. The readout is started by a non-empty signal in any of the TDC FIFO's. Data are then collected in an output FIFO on the TDC board, from where they are transferred automatically to their storage in a circular buffer. A data word for one hit has 32 bits, of which 8 bits are for the wire address and 17 bits are for time.

Zero suppression is inherent in this readout scheme, since empty wires are not recorded . A fast adder with Registered EPROMS (CY7C265) is used to calculate the total multiplicity seen in an interval of 100ns (corresponding roughly to the longest drift time). Inputs to this calculation are the synchronous multiplicity outputs of the TDC chips . There is an option to reset the FIFO's in the TDC chips

whenever the plane multiplicity exceeds a given value (8 or 16). This option is used in the experiment to avoid overloading of the readout with unwanted events, e.g. showers. Any hits in the TDC FIFO's will be erased by this reset. Normally events preceeding a shower will have left the TDC's by the time of the reset pulse, since the multiplicity calculation takes 300ns. Every reset is flagged by adding a word to the data stream.

6. Intermediate storage and handling of data

Data are transmitted from the ouput FIFO's on the TDC boards to a central circular buffer, one for each plane of wires, which is ordered in time. The elements of the buffer represent consecutive time slices of 400ns; the total length of the buffer is 512 time slices. Hits are stored according to the time of the hit. In each time slice there is room for 15 hits; any additional hits are lost. The buffer is implemented as 8k$\times$ 8bit dual port static RAM (CY7B144). The limitation to a reasonably small multiplicity represents a bias only against accidental activity. It simplifies the layout; it also increases the rate capability of the DAQ system. If several subdetectors are involved in a trigger decision, the event rate is limited by the longest possible processing time of an event.

Data are nondestructively extracted from the buffer, on request from level 1 (LV1) and level 2 (LV2) triggers, with different destinations.

For LV1 triggers the data are given to processors which look for two-track events having a vertex in a certain fiducial volume and invariant mass compatible with a $K \to 2\pi$ decay, within wide limits. The extraction is in parallel for all planes.

The realization of the LV1 trigger with fast processors will be discussed in a subsequent publication. The computation time for events with accidental hits is long. An upper limit of 100 μs is imposed to allow readout of all subdetectors in the remaining 100 μs of storage.

LV2 extraction proceeds also in parallel for all planes. Electronics for all eight planes of a chamber is accomodated in one VME crate. Events are stored in local output buffers, and then sequentially transmitted, plane by plane, over a special data bus on the backplane of a chamber VME crate . A crate collect card organizes the transmission of data through 24 m twisted pair cable to a master crate . The speed is limited to 10 MHz of 32 bit words. In the master crate, with standard 6U VME format, the data arriving in parallel from all four chambers are assembled, formatted and transmitted to the data merger. The transmission proceeds through an optical link with 120 Mbit/s bandwidth, of which one third is used on average. In the data merger the data from all subdetectors are collected.

The use of a DSP (Motorola XC96002RC40) in the last step of the drift chamber data collection allows a limited amount of data to be stored on a local disk for monitoring and debugging purposes. All data transmission in crates is by special

fast busses. The VME bus is only used for slow control, i.e. configuration of local microprocessors, of the TDC chips, and for test mode operation. Daisy chained crate to crate connection over a maximum of 20 m distance is made with a Versatile Intercrate Connect (VIC) bus. The central intelligence is provided by a FIC8234 computer in the master crate, connected by ethernet to the terminals in the control room.

7. Performance in test beams and in the NA48 experiment

The front end amplifiers were first tested in small drift chambers ([4]) with the same wire configuration as the final chambers in pion and muon beams from the CERN SPS during the years 1990- 1992. In these tests the chambers were operated with an Ar/Isobutane mixture of 70/30 bubbled through isopropylic alcool at 2^0C . The accuracy (rms) of the coordinate measurement in one plane depends on high voltage and discriminator threshold as shown in fig.8 . The measurement of a coordinate with two staggered planes is a factor $\sqrt{2}$ more precise . The edge of the efficiency plateau for a threshold of 30 mV is at 2.05 kV; the accuracy reaches saturation about 250 V above this edge.

In the large chambers of NA48 a gas mixture of Ar/Ethane 50/50 with 1% of H_2O is used. The edge of the plateau under these conditions is also near 2.05 kV. At 2.25 kV the average accuracy of one plane is around 200 μm, whereas from the test beam result one would expect 110 μm. The disagreement is to a certain degree due to the attenuation of the signal on long wires. In the test beam , however, no degradation of the resolution in a special chamber with 2 m long wires was observed, when the chamber was operated with 2.3 kV. Since in NA48 a coordinate is usually measured from four planes, the coordinate accuracy is found to be 110 μm, close to the specification of 100 μm.

The performance of the readout in the first runs of the NA48 experiment, including the performance of the TDC chips , has been very satisfactory.

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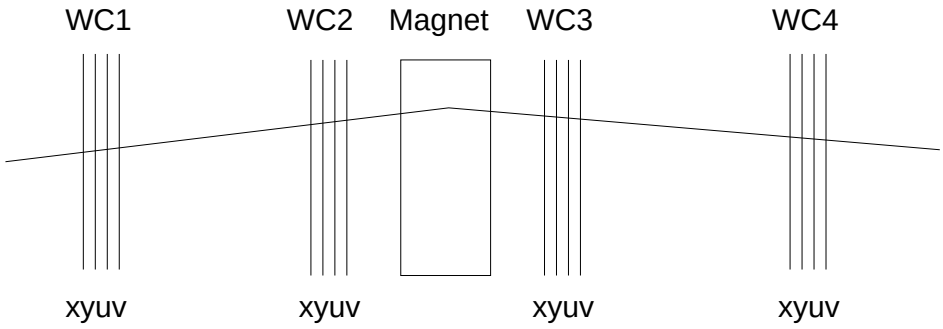
Figure captions

1. a) Layout of the magnetic spectrometer
   b) wire configuration in one view
2. Schematic drawing of the drift chamber readout
3. Amplifier circuit diagram
4. Principle of drift time measurement
5. Circuit diagram of a delay element. Rising and falling edge of a pulse are separately delayed. The delay depends on the control voltage V_{ctrl}.
6. Phase detection circuit realized with three RS latches.
7. Deviation of delay elements in the chain from nominal values.
   The error bar represents the spread (rms) of the individual offsets.
8. Resolution (l.h. scale) and efficiency (r.h. scale) as obtained
   in a small prototype chamber.

a)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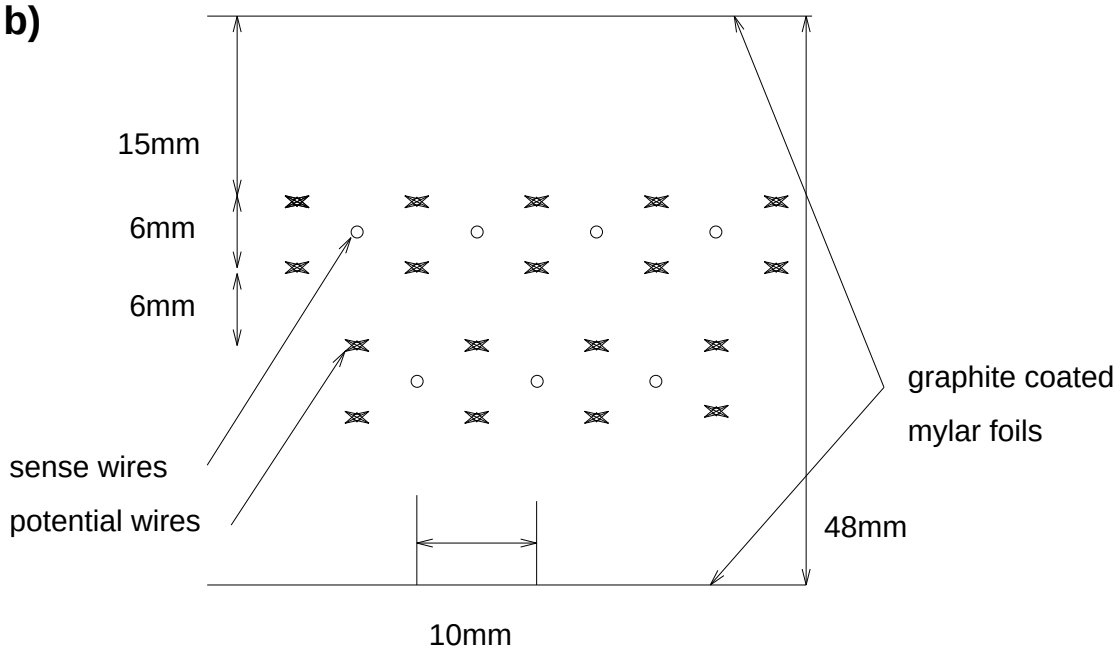
WC2
Magnet
WC3
WC4
xyuv
xyuv
xyuv
xyuv

b)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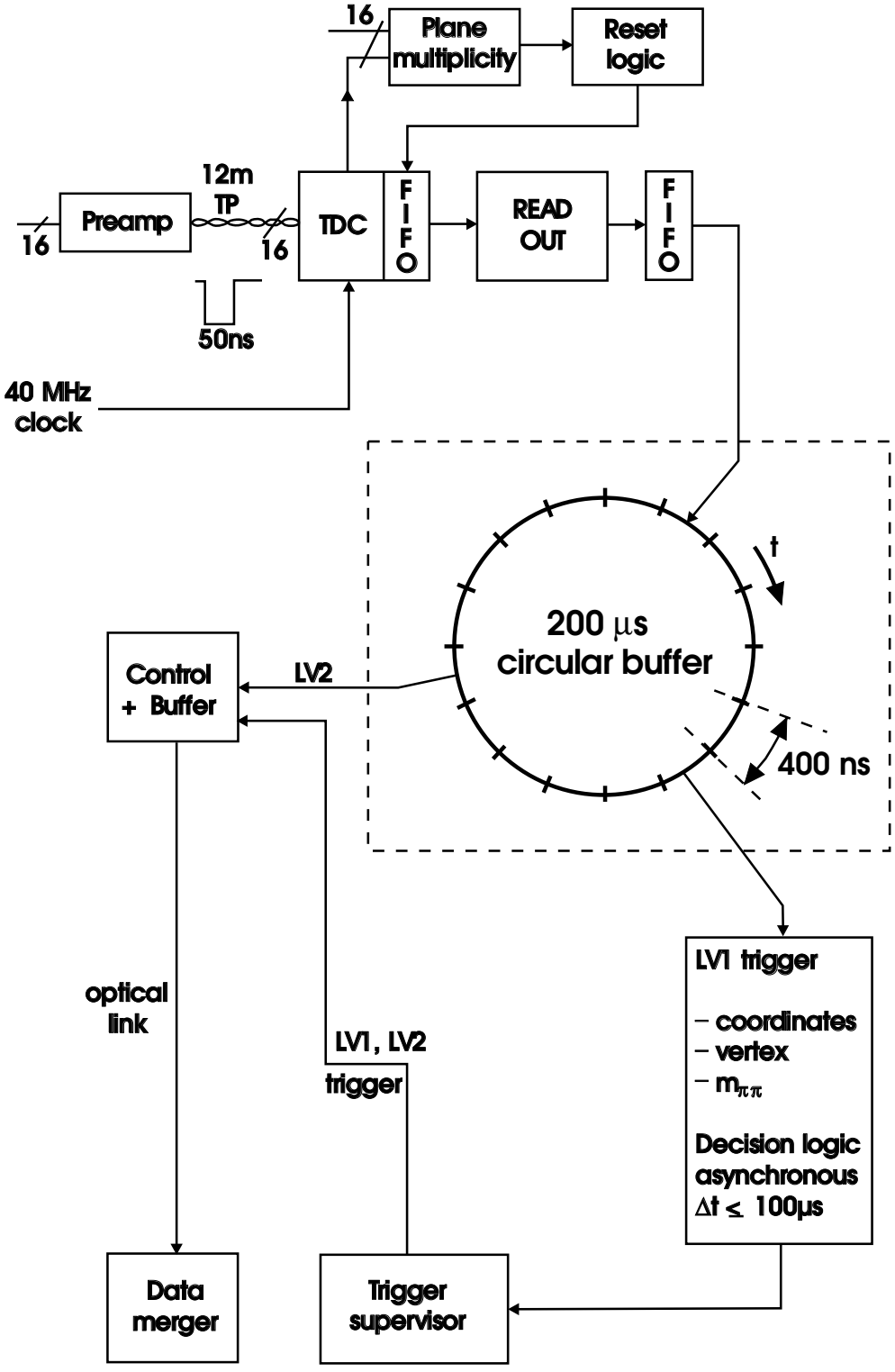
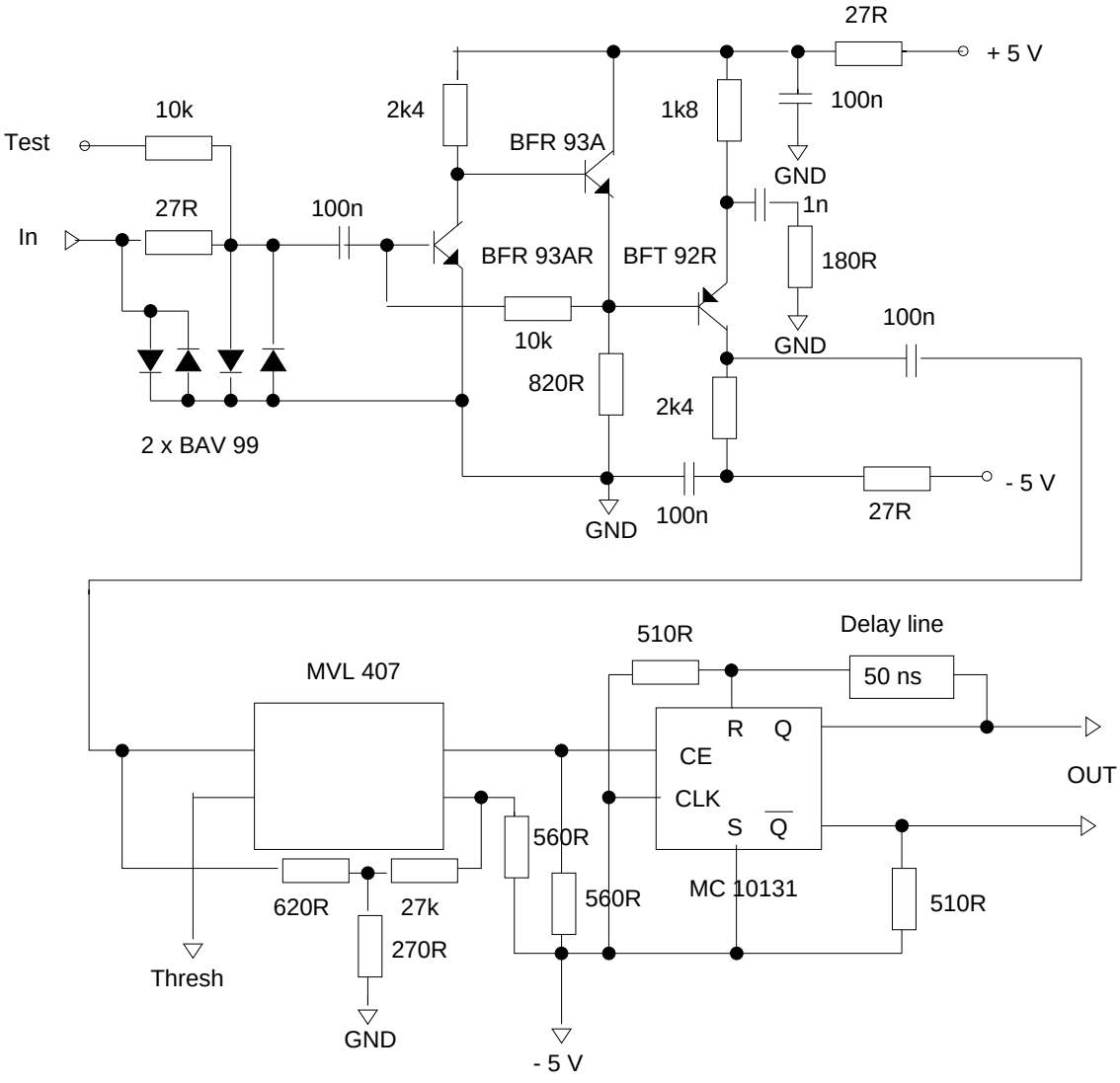
6mm
6mm
sense wires
potential wires
graphite coated
mylar foils
48mm
10mm


16
Plane multiplicity
Reset logic
12m TP
Preamp
16
16
TDC
FIFO
READ OUT
FIFO
50ns
40 MHz clock
200 μs circular buffer
t
400 ns
Control + Buffer
LV2
optical link
LV1, LV2 trigger
LV1 trigger
– coordinates
– vertex
– $m_{\pi\pi}$
Decision logic asynchronous
Δt ≤ 100μs
Data merger
Trigger supervisor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+ 5 V
10k
2k4
1k8
100n
Test
BFR 93A
GND
27R
100n
1n
In
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BFT 92R
180R
10k
GND
100n
820R
2k4
2 x BAV 99
- 5 V
GND
100n
27R
510R
Delay line
MVL 407
50 ns
R
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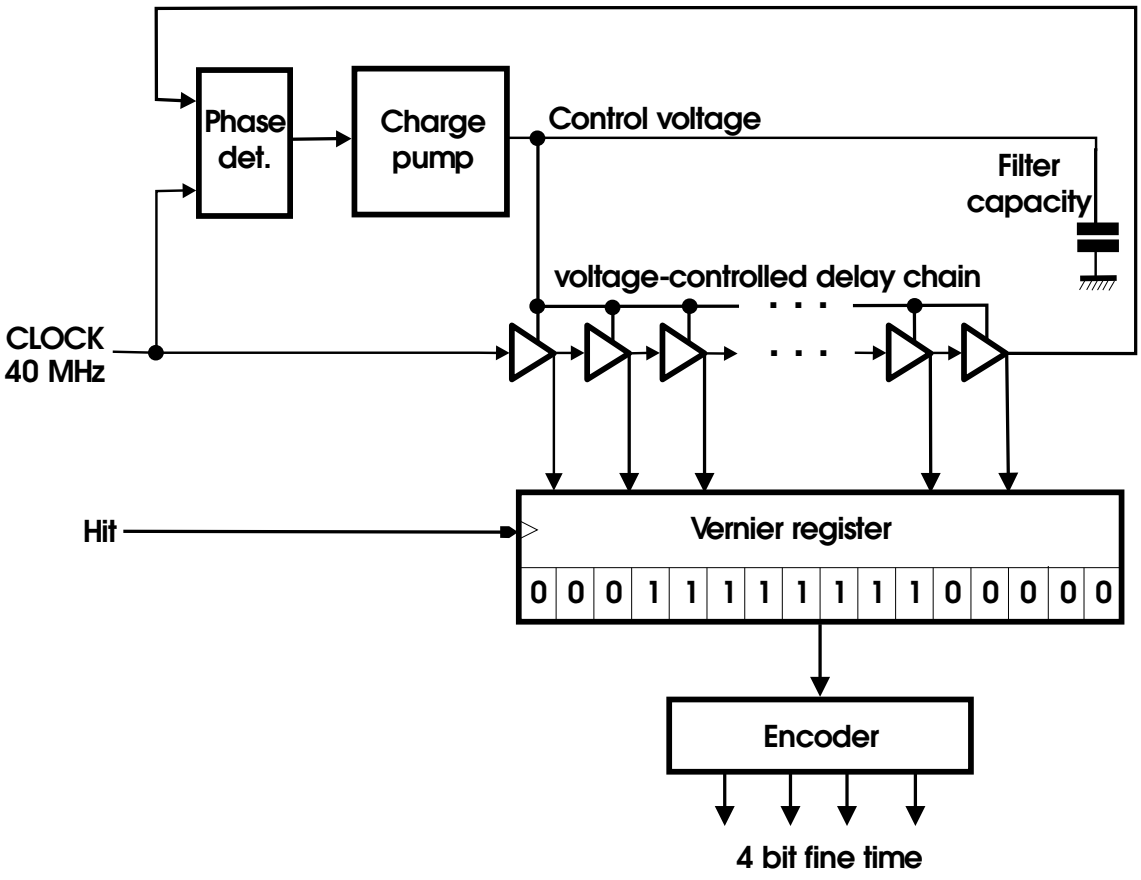
Thresh
GND
- 5 V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det.
Charge
pump
Control voltage
Filter
capacity
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CLOCK
40 MHz
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Vernier register
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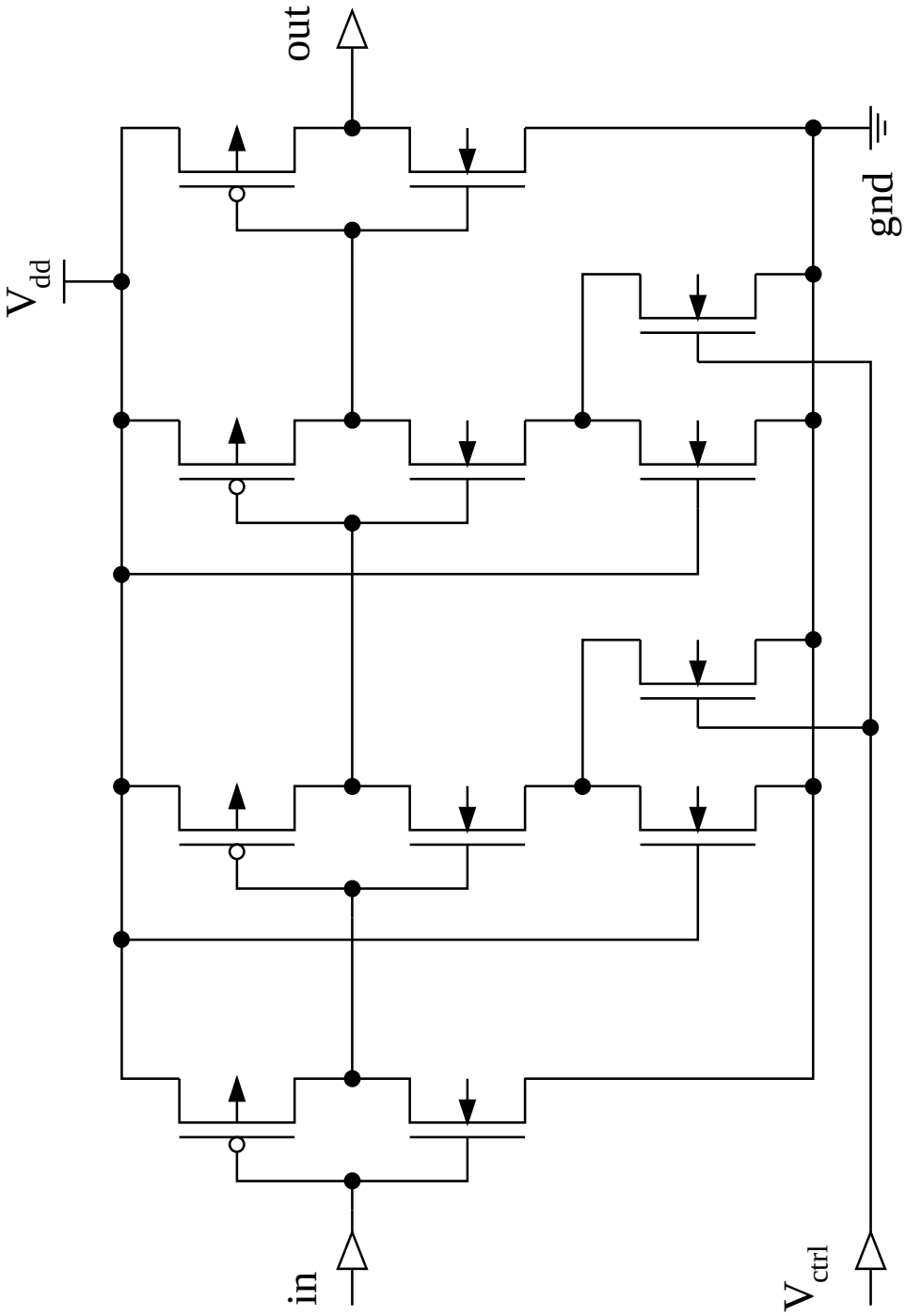
Encoder
4 bit fine time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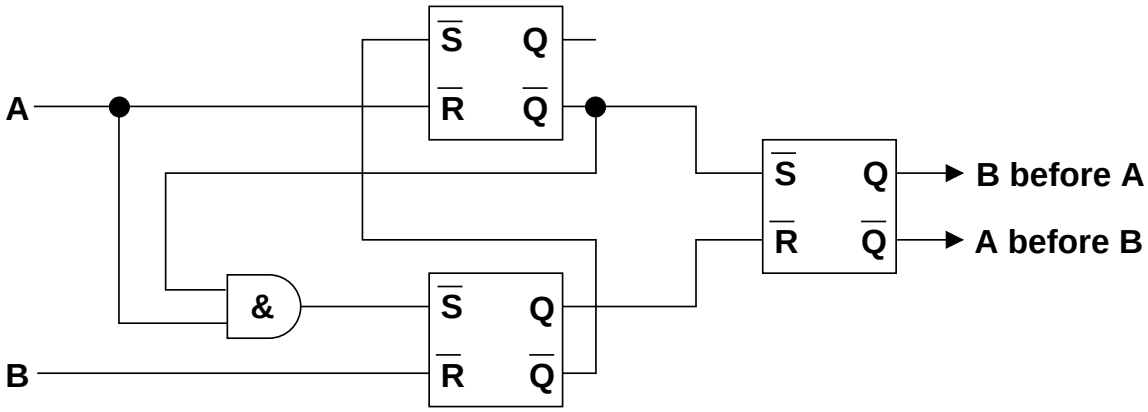
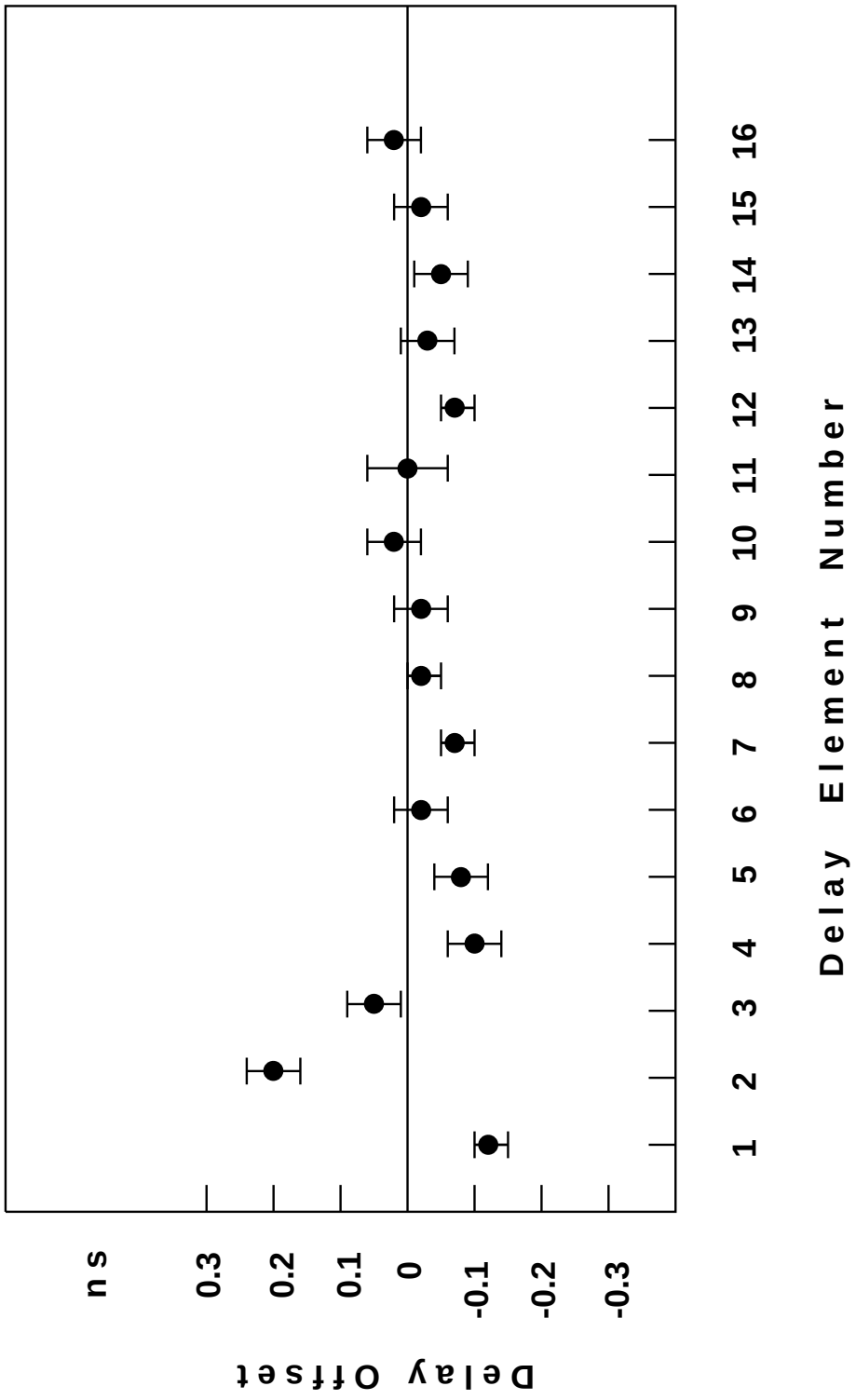
gnd
V_{dd}
in
V_{ctrl}


A
B
S
R
Q
Q
&
B before A
A before B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0.1
0
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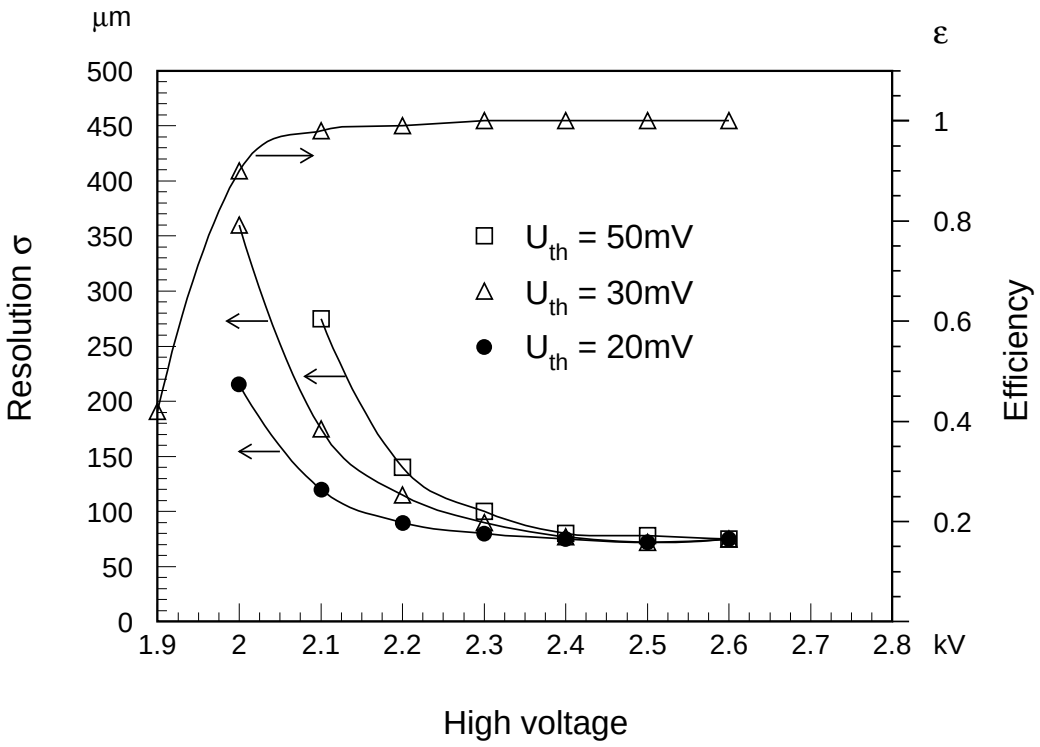
-0.2
-0.3
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Delay Element Number


μm
ε
500
450
400
350
300
250
200
150
100
50
0
1
0.8
0.6
0.4
0.2
1.9
2
2.1
2.2
2.3
2.4
2.5
2.6
2.7
2.8
kV
Resolution σ
Efficiency
U_th = 50mV
U_th = 30mV
U_th = 20mV
High voltage