

REVIEW OF THE OUTCOME OF TWO WORKSHOPS ON ELECTRONICS FOR LHC EXPERIMENTS

François Bourgeois,
CERN, 1211 Geneva 23, Switzerland

ABSTRACT

Two Workshops were organized since September 1995 by the CERN LHC Electronics Review Board, LERB. Radiation-hard processes, opto-electronics, trigger and event building systems, electronics for calorimeters, muon detectors and trackers, were discussed in detail. During the first Workshop a variety of designs were presented in the light of the major requirements set by the detector collaborations. The second Workshop held in Hungary last September confirmed that a number of technological choices had been made. Some of the more salient designs are presented.

1 - INTRODUCTION

Two Workshops on Electronics for LHC Experiments were successfully organized in September 1995 and September 1996 by LIP Lisbon and RMKI Budapest respectively. These meetings took place on behalf of CERN's LHC Electronics Review Board (LERB), not only for the LERB to have a thorough review of the activities in the field, but also to promote cross fertilization in the engineering community involved in the design of electronics for LHC experiments.

Each Workshop gathered more than 150 physicists and engineers from 20 countries including USA and Japan. The format was very similar for the two meetings. It comprised six sessions, and more than 100 oral and poster contributions were given each time with special focus on radiation-hard microelectronics processes, electronics for tracking, calorimetry and muon detectors, opto-electronics, trigger and data acquisition systems.

In September 1995, each topic was introduced by an invited speaker who reviewed the requirements set by the application of the particular detector technology at LHC. In September 1996, review talks were addressing subjects of interest to the LHC community (e.g. NA48 calorimeter electronics [1] or opto-electronic packaging [2]). At the end of each session, fruitful panel discussions were chaired by each invited speaker.

This paper summarizes the progress made by the LHC electronics community since 1994 as seen through the outcome of these two Workshops. Salient designs and author's views in the fields of radiation hardness, electronics for tracking and calorimetry, opto-electronics are presented first. A brief summary of the other sessions is given in the last section.

2 - RADIATION HARDNESS

Radiation effects and radiation levels in LHC experiments were presented in [3]. Ionizing dose rate (up to 1 MRad/year of operation) and neutron fluence (up to 10^{14} n/cm²) at LHC are different from those seen in military (very large dose rate) or space (low dose rate) applications. Semiconductor damage is however qualitatively very similar for the three environments.

Threshold voltage shift of CMOS transistors results from the trapping of holes in the silicon oxide; it is inversely proportional to the gate thickness. Similarly, reduction of the carrier mobility, and increase of the noise (thermal and $1/f$) are produced by charge trapping at the gate-substrate interface. Speed and gain of bipolar transistors are affected by changes in carrier lifetime resulting from hadron damage to the bulk. Annealing, a partial recovery after some time, is often seen when exposure to radiation stops.

Heavily ionizing particles can also produce latch-up and single event upset SEU.

Latch-up affects bulk processes : it is the creation of a low impedance path with the power supply through parasitic lateral structures. Without current limitation it can be destructive.

Single event upset SEU is a non-destructive state change which may have serious consequences in the control part of the electronics (e.g. execution of a branch operation to an unexpected location).

Hardening is basically obtained with thinner gate oxide layers, isolation of the active devices from the field oxide and with the isolation of the structures from the bulk.

The most sophisticated process is the MHS-DMILL [4], an $0.8\mu\text{m}$ SOI BiCMOS process with provision for JFET transistors. It has been developed since 1990 by the French CEA in its LETI laboratory and it is becoming commercially available from MHS. DMILL is qualified for 10 MRad, 10^{14} n/cm^2 and it can be used at cryogenic temperatures (JFET structures).

Harris [5], Honeywell [6], MHS [4] and Thomson [7] (in 1995 only) actively contributed to the two Workshops. Their participation gave assurance to the LHC community that at least two processes would remain available as long as there is business in the years to come. Even though this was excluded by those present in Lisbon, the 1996 Workshop showed that a trend was developing to have radiation-hard processes as by-products of other ones with a better market share.

A non exhaustive list of processes is given in table I.

TABLE I

A number of radiation-hard processes (rad-tolerance of the MIETEC and ST processes to be assessed).

MANUFACTURER	Process name	Radiation hardness	Process type
Harris	AVLSI-RA	Tested @ 10 MRad	Bulk CMOS 1.2μ
Honeywell	RICMOS IV	Tested > 2 MRad	SOI 0.7μ
	CHFET	Tested > 10 MRad	GaAs 0.7μ
MHS	DMILL	Qualified for 10 MRad	BiCMOS + JFET
MIETEC		Rad-tolerant (?)	Bulk CMOS 0.7μ
		Rad-tolerant (?)	Bulk CMOS 0.5μ
		Rad-tolerant (?)	Bulk CMOS 0.35μ
ST		Rad-tolerant (?)	Bulk CMOS 0.5μ
		Rad-tolerant (?)	Bulk CMOS 0.35μ
AT&T			Bipolar ft = 5-10 GHz
Maxim	CB2	Tested @ 10 MRad	Bipolar ft = 5-10 GHz
TriQuint			GaAs
Vitesse			GaAs

A number of the radiation hard processes in table I were used in the design and the test of front-end electronics for trackers at LHC. The staged exposure of the electronic circuits during the 10 year operation of the LHC, combined with the dose rate of 1 MRad/year, have forced the community to set-up its own set of tests rather than base qualification on military or space standards.

Most experimental measurements shown at the Workshops confirmed that at least 3 processes would withstand the expected exposure at an acceptable level of degradation of the analogue performance of the channel (e.g. <100 mV threshold voltage shifts). Latch-up does not seem to exist with the Harris AVLSI-RA $1.2\mu\text{m}$ bulk process to be used for the CMS tracker electronics [8,9]. Little was reported on SEU problems the reason being that given the basic functionality of the front end electronics (preamplifiers driving systolic analogue or digital pipelines without feed-back), such effects cannot significantly harm the operation of the system.

In the course of the second Workshop, it was however agreed that sophisticated electronic systems would be located in areas exposed to radiation levels similar to those of space applications (>10 KRad). This demonstrated that more awareness on the consequences of SEU effects should develop in the LHC community and that radiation tolerant processes would have to be identified.

Expertise is now widespread but the point was made that “getting a radiation hardened system would take a lot more than just buying radiation hardened devices from one of the three device manufacturers willing to supply them” [10].

3 - TRACKING

Tracker requirements were discussed at length during the first Workshop [11]. A large number of papers were presented in 1995 and 1996. Inner trackers at LHC do not participate in the first trigger level. To the exception of the pixel detectors, the most common tracker front end architecture comprises a preamplifier, a pipeline (analogue or digital) and an ADC with 2-10 bit accuracy, before or after the pipeline (in the latter case, the ADC is multiplexed between several channels). Switched capacitor arrays SCA, 128 cell deep, are used in applications aiming at a better control of the leakage current drifts as a function of time and radiation. The three basic architectures are shown in Figure 1.

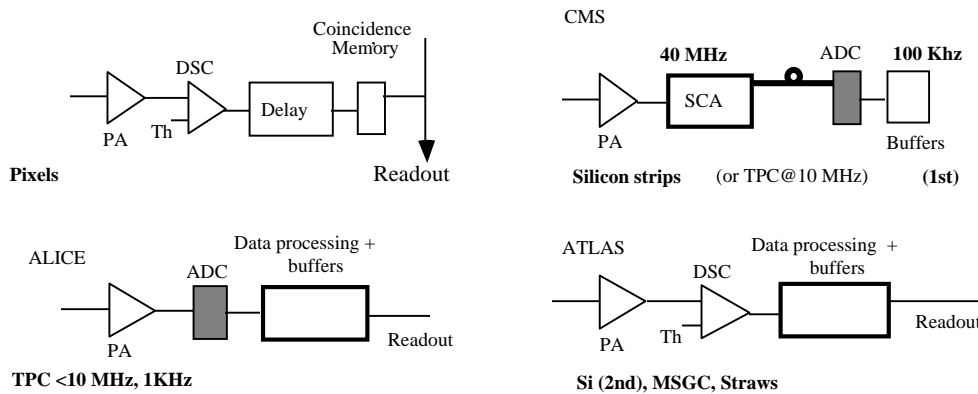


Figure 1 : block diagrams of the four typical tracker front-end architectures to be used in LHC experiments.

3.1 Pixel detectors

Pixel detectors (high resistivity silicon) are bump bonded to the readout chip in a flip-chip hybrid assembly. They have a binary readout and hits are gated by the trigger signal. The silicon area available for the implementation of the front-end is limited by the pixel size and much effort has been placed in the design of a delay scheme that would use as little silicon area as possible. The Omega 3/LHC architecture presented in [12] provides for satisfactory delay adjustment and a good level of testability. The delay function is implemented with a ladder of inverters which propagation delay is current controlled thus allowing for adjustment of the delay. After fine tuning, a spread of 25 ns full width at the base was achieved on a single chip (2048 pixels). This figure is smeared to reach 75 ns for an array of 24 chips representing 50K pixels. The chip design of 0.8 M transistors over 1 cm² silicon area, is among the largest full custom analogue chips ever made in the community. Known good dies are selected prior to bump bonding (50% yield). Other readout schemes are currently under study for ATLAS and CMS but they were meagerly presented during the Workshops. Various results were reported on bonding techniques [13,14].

3.2 Silicon strip detectors and MSGC

Silicon strip detectors are widely used in trackers at LHC. The most challenging front end architecture is the one selected for CMS on the basis of the work of RD20 [8,9] and RD23 [15,16]. The preamplifier has a 75 ns peaking time. Samples are stored in an SCA clocked at 40 MHz. When a trigger signal is received by the front-end chip, three samples are processed by an Analogue Pulse Shape Processor APSP that deconvolves the pulse (weighted sum of 3 samples) and associates the analogue result with the particular bunch crossing. The analogue sample of interest (weighted sum or peak) is transmitted to the digitizer (10 bit multiplexed ADC) through optical fibers [15]. The 128 channel front end has been implemented in the Harris AVLSI-RA process (0.72 cm²). The basic building blocks were successfully tested since 1995. A final chip was delivered in February 1997 and it seems to comply with the major requirements. The same architecture will be used for the readout of the MSGC.

Binary readout schemes are being preferred to analogue ones for the readout of the ATLAS silicon strip detectors. A bipolar preamplifier/discriminator chip CAFE is combined with a CMOS digital pipeline and derandomizer ABC [17]. A single chip BiCMOS version implementing both functionalities is being developed in the DMILL technology. This new design was successfully prototyped as a 32 channel chip : the SCT32-B [18]; a 128 channel version will soon be delivered by MHS. As one might have expected, the single chip approach has a lower power budget yet offering better performance. Further tests are however needed to confirm these promising results.

The very different architectures chosen by ATLAS and CMS for their silicon strip detectors seem to have similar signal to noise ratio (15 x) and overall performance (in particular <3 mW/channel). There is at this stage no clear argument in favor of one or the other. It remains that both systems have to withstand high radiation levels in a rather confined area. Frequent access to the electronics is excluded and it might turn out that reliability is the overriding selection criteria.

3.3 Straw trackers

The general trend towards a single chip design is also seen in the readout of the ATLAS TRT straws [19]. At present, the wire signal is discriminated at high and low thresholds (ASDBLR 8 channel chip in bipolar technology) for both transition radiation detection and minimum ionising particle detection. The two output bits are timed (3 ns bin, low threshold only), pipelined (128 cells) and derandomized in the DTMROC (16 channel in CMOS). A BiCMOS design will be undertaken shortly to combine the functionality of both chips in a single integrated circuit in order to minimize cost, simplify the front-end board design and decrease the power dissipation.

3.4 Other aspects

The sophistication of the timing trigger and control system TTC [20] was found to exceed the needs of the timing of the tracker electronics (10 x less demanding stability). Simpler techniques are used to distribute the various clock and trigger signals to the on detector hybrids. Copper connections are taking over from fiber links for the readout of the front end hybrids. It is interesting to note that CMS may turn out to be the only experiment to make extensive use of analogue optical fiber connections between the tracker front-end and the first level of the readout system.

4 - CALORIMETRY

An excellent review of the requirements of electronics for calorimetry at LHC was given during the Lisbon Workshop [21]. Crystal or liquid (argon and krypton) electromagnetic calorimeters offer excellent energy and space resolution combined with high rate capabilities. At LHC, it is however not possible to fully exploit these characteristics with conventional charge integrating digitizers due to their long conversion times.

Since 1990 a number of developments have been undertaken within the framework of the Research and Development effort around experiments proposed for the SSC and LHC. These designs have been based on piecewise linear conversion techniques (see Figure 2) and include a pipeline to allow for the synchronization of the data with the arrival time of the first level trigger signal.

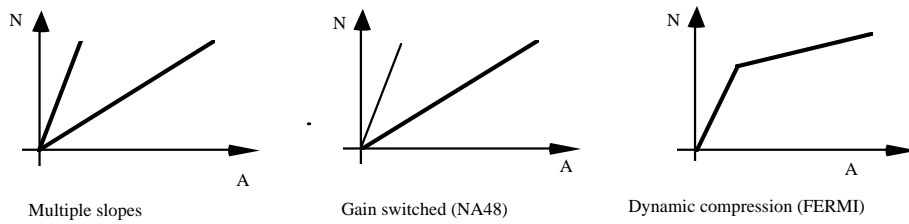
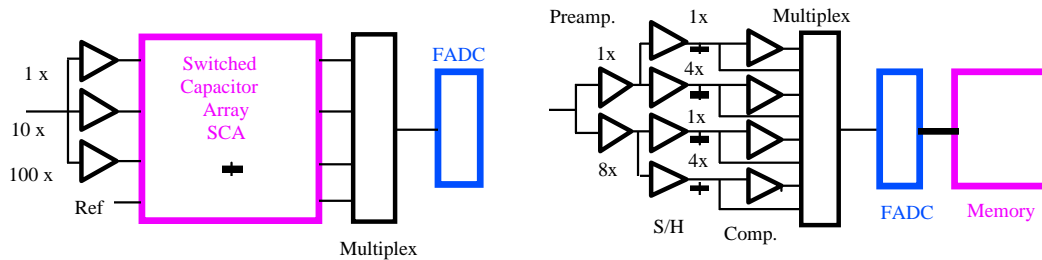


Figure 2 :

the basic schemes used in dynamic range expansion. Two simultaneous measurements (left); single measurement after gain selection (middle) and piecewise linear dynamic compression.

The basic building blocks of such systems are (see Figure 3):

- A preamplifier followed by a filter to maximize the signal to noise performance and limit the frequency bandwidth of the signal while optimizing the time resolution;
- A fast ADC system (Flash or multiplexed Successive Approximation);
- A pipeline storage placed either in front of the ADC (switched capacitor array SCA) or on the digital output (memory).



Figure

3 : block diagrams of the ATLAS (analog, on the left) and CMS (digital, on the right) calorimeter front ends

All systems aim at a dynamic range in excess of 16 bits with an accuracy of at least 11 bits. This can only be achieved when the required logarithmic response of the system is approximated by means of a piecewise linear conversion.

Systems with 128 cell deep switched capacitor pipelines are under development for ATLAS [22,23]. As shown in Figure 3, the technique consists of driving three rows of cells with 1x, 10x and 100x amplifiers hence approximating the logarithmic response with three linear segments. Cell

to cell dispersions must be minimized to achieve the required accuracy. To this end, a dummy row of capacitors, one per group of 4 channels, is used as a reference to allow for a first order correction of the column to column pedestal variations. The ADC at the output of the capacitor array is a 12 bits 10 Mhz device. It is multiplexed over 8 channels.

For systems based on Flash converters and digital pipelines the accuracy is constrained to a maximum of 12 bits as a result of the prohibitive cost and power budget of fast (>40 Mhz) and accurate Flash ADC devices . Hence it is necessary to partition the response into more than two linear pieces. For such systems a dynamic compressor must be placed in between the channel input and the ADC. To illustrate the problems associated with FADC based systems, the NA48 experiment was invited at the second Workshop to report on the performance of its calorimeter readout system [1].

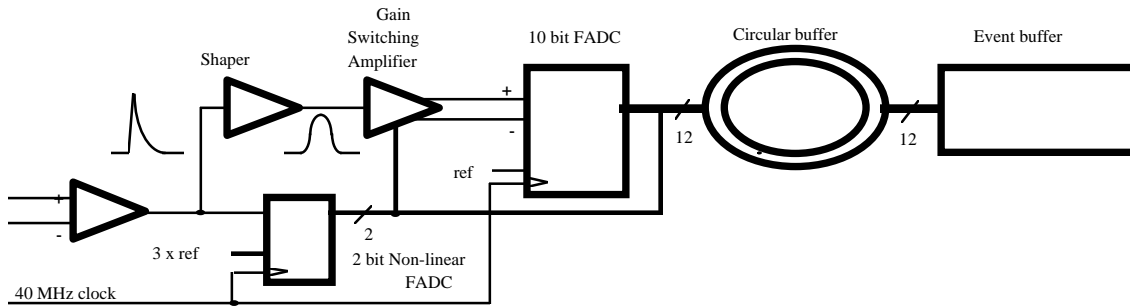


Figure 4 : Block diagram of the NA48 gain switching digitizer

In contrast with the FERMI approach [24,25], whereby the calorimeter signal is amplified by a ladder of four differential amplifiers, each of which reaches cut-off as the amplitude of the signal grows, the NA48 design makes use of the amplitude of the fast raw signal to select the gain value to be applied to the shaped pulse. The selected gain is kept for a sufficient number of clock cycles before it reverts to its value at rest i.e. maximum gain.

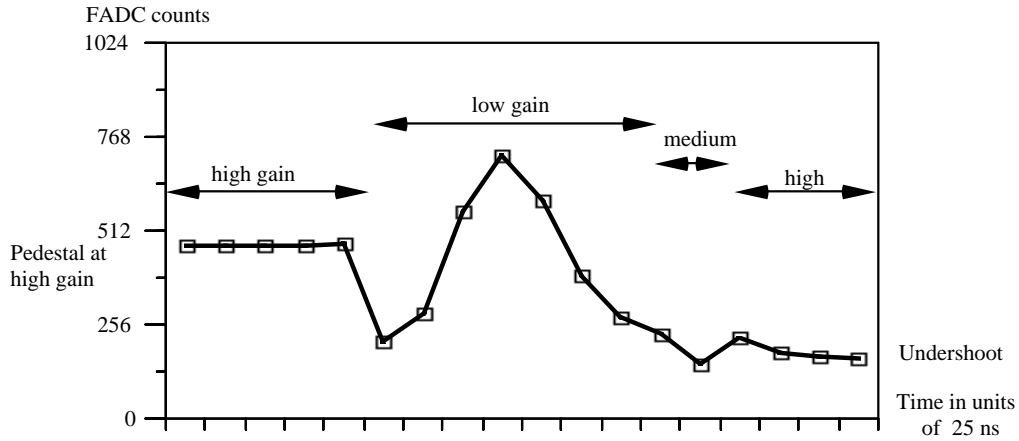
The main building blocks of the NA48 system are:

- A single ended preamplifier (in the LKr vessel).
- A differentiating transceiver with balanced outputs (at ambient temperature).
- The Calorimeter Pipeline Digitizer (CPD, FASTBUS, 3U width).

Each channel consists of a full-custom ASIC which performs pulse shaping and gain switching, and a 10-bit 40 MHz FADC converter (Philips). The module also includes digital circular buffers and event memories to allow for a deadtime-less operation with 200 microsecond storage capacity before trigger and readout. A schematic of a CPD channel is given in Figure 4 and a typical signal shape after the gain switching stage in Figure 5.

The shaper is a 6th order Bessel filter which provides the required quasi-gaussian shape and the necessary 125 ns delay while optimizing the time resolution (200 ps). The gains are set to 1x, 2.5x, 6x and 18x and they can be individually forced in order to allow for cross calibration of the four ranges.

The ASIC was designed by CISS / Austria in an AMS 1.2 micron BiCMOS process on the basis of a discrete component prototype.



Fig

ure 5 : typical signal shape after the gain switching amplifier of NA48

This gain switching technique has been found to give the required performance for both amplitude and time resolution. The pipeline storage provides ample time for trigger decisions. A 768 channel system was successfully used in a beam test in September 1996 and the calorimeter is now fully instrumented (13'500 channels). It must however be said that the design is power hungry ($> 5W/\text{channel}$). In addition, at threshold, gain switching can be affected by the slewing time and the metastable states of the comparators. This effect was seen to be 10 x more frequent in the beam test as compared to tests in the laboratory (incoherent noise contribution). The filter makes use of a large number of accurate external resistors and capacitors and a straightforward mapping of the technique for use at LHC does not seem to be advisable [26].

The second Workshop showed that the dynamic compressor of the FERMI microsystem [27] could not meet the requirements set by the crystal calorimeter of CMS [25]. The FERMI compressor is now replaced by a floating point unit FPU [28] which drives a single commercial ADC (Analog Device, 12 bit 40 Mhz). In contrast with the NA48 architecture, the calorimeter signal is sampled and held on capacitors at the output of a ladder of 1x, 4x, 8x and 32x amplifiers (see Figure 3, right). Fast comparators select the capacitor with the highest in-range voltage and this signal is multiplexed to the input of the Flash ADC. This FPU scheme has in fact similarities with the input and output sections of the SCA architecture of ATLAS exactly as if the missing part was the SCA proper. The more fundamental difference comes from the fact that in the CMS architecture digitized samples are readily available for use in the trigger level one. This is at the expense of a higher power budget and, possibly, a somewhat longer latency (extra 5-10 bunch crossings) in the lateral filter processing the raw data as compared to the analogue sums of the ATLAS trigger scheme.

It must be said that sizable prototypes of the proposed systems will have to be built in a radiation tolerant process before one can be sure that electromagnetic showers covering up to 64 calorimeter cells can be measured with a level of noise (coherent and incoherent) that shall not impair the physics goals

5 - OPTO-ELECTRONICS

A good overview of the requirements for optical links in LHC experiments was given at the Lisbon Workshop [29]. The very large number of detector channels ($> 10^6$), the data rates (Gb/s) and the overall dimensions of the detectors (25 m) are key factors in favor of the extensive use of optical connections in LHC experiments. Until the end of 1996, several types of optical links were under consideration for the point-to-point connections in front-end and read-out systems. The first type is based on the direct modulation of an emitter (LED or laser diode), the fiber and a receiver. In the second type, with external modulation, the emitter consists of an electro-optic modulator.

Inner optical links in LHC experiments are exposed to high radiation levels. Single mode fibers at 1.3 (or 1.5) micrometer wavelength (pure silica core) are fortunately both radiation hard and commonly available at an affordable cost (because of their widespread use in submarine and long distance telecom applications). Connectors are expensive and they must be handled with care to minimize insertion loss. The number of connections in a link must therefore be limited to the minimum required not to impair access to the electronics for service (< 4).

5.1 Analogue optical links

Since 1992, a large fraction of the R & D effort has been placed in the field of the analog transmission of the data samples generated by the tracker (and presampler) front-ends. The basic goals were i) to minimize the amount of radiation-hard Silicon in the front-end chip; ii) to move the analog to digital conversion out of the detector volume; and iii) to minimize the power budget and the cost of the system. For such applications external modulation appeared to be a promising choice because it kept the light sources outside of the tightly confined detector area, thereby minimizing power dissipation at the front ends. Lithium-niobate Mach-Zendher modulators had already been tested by US [30] and Japanese laboratories at the beginning of this decade. The CERN RD 23 project [15] made from 1992 to 1996 a thorough study of the modulator technology in collaboration with GEC Marconi. After a year, it was shown that Multiple Quantum Well MQW reflective modulators were a better choice because i) they had smaller dimensions, ii) they were the most radiation hard amongst the opto-electronic device options and iii) they could be made in arrays of 8 or more devices. An 8 bit dynamic range was achieved on a number of test samples. An affordable level of degradation of the characteristics was seen under radiation for all components in the system [31]. It however appeared in 1996 that the proprietary InGaAs/InP technology of GEC, added to the rather specific requirements of HEP experiments, did not allow for economies of scale and a cost effective mass production of the device.

Since 1996, efforts have focused on the direct modulation of lasers either edge emitting or vertical cavity surface emitting laser diodes VCSELs [32,33,16]. Radiation hardness was demonstrated with both technologies but it seems that VCSELs have yet to mature before one can reach the required level of reliability. Excellent results were obtained with telecom edge emitting lasers both in linearity of transfer and in radiation hardness. Edge emitting lasers at 1300 nm have been chosen for use in the CMS tracker.

5.2 Digital links

Commercially available (commodity) components are likely to match the needs in the upper levels of the readout and event building part of the electronics. Several examples were given during the two Workshops e.g. HP G-Link or FibreChannel components.

The standard multichannel optical system developed for the transmission of timing, trigger and control signals to the front-end electronics controllers TTC was presented at the first Workshop [20]. Its performance (50 ps stability) complies with the requirements set by the time critical detectors. It will be used by all four LHC experiments in the trunk and the main branches of the fan-out tree. As indicated above, it is a sophisticated system and it may not be used at the lowest levels of the front-end electronics for detectors that can live with >1 ns timing accuracy.

6 - OTHER SESSIONS

6.1 Muon

Muon detectors at LHC contribute to the trigger. They are basically wire chambers in various flavors.

Resistive Plate Chambers RPCs give fast (1ns), large (1 pC) signal on (x, y, u, v ...) strips. Hit patterns are fed in track finding matrices which give level one trigger information (see Figure 6).

Refined and accurate track position is given by drift tubes. As shown in Figure 6 mean timers calculate the impact parameter of each track segment and associate it with its corresponding bunch crossing. Missing hits can be accepted (1 out of four planes). Track segments are then linked with each other to form muon tracks.

There was a limited number of contributions at both Workshops, and work on the design of electronics for muon detectors at LHC was not well covered. It was very fortunate that the invited speakers highlighted the importance of muon detectors for physics at LHC [34,35] and made a detailed analysis of the problems.

In the discussion it was agreed that system aspects had to be addressed, in particular synchronization over large areas and trigger generation from overlapping events.

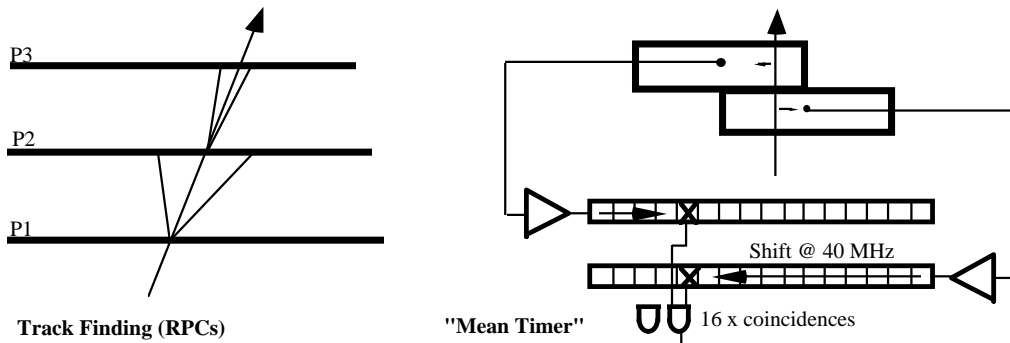


Figure 6 : schematics illustrating the two main schemes used for track finding in muon detectors. Hit patterns are compared against prediction windows of narrowing width in three or more sets of RPCs (left). A coincidence of wire signals from staggered drift chamber planes has a constant delay with respect to the beam crossing provided each signal is shifted in a “mean timer” as shown on the left hand side of the figure.

6.2 Trigger and Event building

Trigger, event building and data acquisition problems in LHC experiments were thoroughly described by the invited speakers A. Lankford (Lisbon 1995) [36] and M.Letheren (Hungary 1996) [37].

During the second Workshop, a number of contributions gave a good overview of the ATLAS and CMS trigger systems.

Cluster finding algorithms with isolation criteria for calorimetry, coincidence matrices and mean timers for the muon detectors, supply central trigger processors with the required transverse energy and topological information. The concept of regions of interest ROI explicitly appears in the ATLAS system. It was said to also exist in the CMS trigger concept. Most level one systems were described and simulated in Verilog or VHDL and several FPGA based prototypes were successfully tested.

Dedicated backplanes and point-to-point links in 9U VME crates are under consideration. It is likely that VME will be used in LHC experiments for the 10 years to come.

The use of neural networks in the classification of events at level 2 or 3 was discussed[38].

Several speakers reported on event building with switch fabrics. The case was made for packet switching architectures in ATM and it was agreed that it was the best bet for ATLAS, CMS and LHC-B. Conversely, it was accepted that connection switching with FibreChannel might be a better choice for event building and mass storage in ALICE even though large FibreChannel switches may not be available. It was widely accepted that the final choice would be driven by the multimedia/ telecommunication market.

7 - CONCLUSION

These Workshops were very successful in that they identified areas and encouraged efforts for rationalization and common developments within and between the different detector groups.

The format of the sessions (invited talk, oral contribution and panel discussion) helped identify work and designs of interest. As a result, more awareness has developed on radiation tolerance (a real problem), test and system aspects. Major progress was made in several domains as may be inferred from this review. It was however clear that room was left for more rationalization and a that there was a need for more focus on common developments both inside and across experiments.

8 - ACKNOWLEDGEMENTS

I am pleased to acknowledge the most appreciated contribution of Catherine Decosse in the timely edition of the proceedings of both Workshops. The participation of the LERB secretary, Michael Campbell, was an asset in the writing of the panel discussion summaries. The proceedings and the summaries played an important role in the preparation of this paper.

I would also like to thank the Members of the LERB for their active participation to the meetings and their share in the success of the Workshops.

9 - REFERENCES

- [1] FANTECHI Riccardo et al. (INFN Sezione di Pisa, Italy) for the NA48 Collaboration The Readout Electronics of the NA48 Liquid Krypton Calorimeter, CERN/LHCC/96-39, 21 October 1996, p. 33
- [2] HUNZIKER Werner (Swiss Federal Institute of Technology, Zürich, Switzerland) Packaging of Opto-electronics Components, CERN/LHCC/96-39, 21 October 1996, p. 365
- [3] HEIJNE Erik (CERN - ECP Division) Radiation Effects on Electronics for Experiments at the TeV Hadron Collider, CERN/LHCC/95-56, 1 October 1995, p. 19
- [4] CORBIERE Thierry (MATRAS MHS, Nantes, France) DMILL, A Mixed Analog/Digital Rad Hard Technology, CERN/LHCC/96-39, 21 October 1996, p. 404
- [5] VAN VONNO Nick (Harris Semiconductor, Melbourne, USA) Accessible Hardened Technologies for Front-End Electronics, CERN/LHCC/96-39, 21 October 1996, p. 411
- [6] LIU Mike (Honeywell Solid State Electronics Center, Plymouth, USA) Radiation Hard SOI and CHFET Technologies for LHC Applications, CERN/LHCC/96-39, 21 October 1996, p. 407
- [7] REDOLFI Jean (THOMSON-CSF Semiconducteurs Specifiques (TCS)) SOI Standard Products and ASICS at TCS, CERN/LHCC/95-56, 1 October 1995, p. 38
- [8] HALL Geoffrey et al. (Imperial College) The Electronic Readout of the CMS Tracking System CERN/LHCC/96-39, 21 October 1996, p. 114
- [9] FRENCH Markus et al. (Rutherford Appleton Laboratory, Didcot, UK) APV6-RH a 128 Channel Read-Out Chip for the Silicon Tracker in CMS, CERN/LHCC/96-39, 21 October 1996, p. 463
- [10] RITTER James (Naval Research Laboratory, Washington, USA) Future Trends in Rad Hard Technologies with Examples From Space Systems, CERN/LHCC/96-39, 21 October 1996, p. 403
- [11] HILKE Hans Jürgen (CERN-PPE Division) Inner Tracking at LHC, CERN/LHCC/96-39, 21 October 1996, p. 75
- [12] CAMPBELL Michael et al. (CERN, Geneva, Switzerland) Tunable Timing in the Omega3/LHC1 Silicon Pixel Detector Array, CERN/LHCC/96-39, 21 October 1996, p. 435
- [13] PINDO Max (University and INFN Milano) Radiation Hardness and Resistance to Electromigration Effects of Conductive Glue Bonds for Hybrid Pixel Detectors Realization, CERN/LHCC/95-56, 1 October 1995, p. 135
- [14] GRIM Gary et al. (University of California at Davis) Progress on Pixel Detector Hybridization, CERN/LHCC/95-56, 1 October 1995, p. 140
- [15] VASEY François et al. (CERN- ECP Division) Modulator-Based Lightwave Links for Analogue Signal Transfer at LHC, CERN/LHCC/95-56, 1 October 1995, p. 175

- [16] GILL Karl et al. (CERN, Geneva, Switzerland) Neutron Damage Studies of Semiconductor Lasers for the CMS Tracker Optical Data Links, CERN/LHCC/96-39, 21 October 1996, p. 387
- [17] CAMPBELL Dave et al. (Rutherford Appleton Laboratory, Chilton, UK) The ATLAS Binary Chip, CERN/LHCC/96-39, 21 October 1996, p. 478
- [18] KAPLON Jan et al. (CERN, Geneva, Switzerland) Development of Front-End Electronics for Silicon Strip Detectors Using the DMILL BiCMOS Rad-Hard Process, CERN/LHCC/96-39, 21 October 1996, p. 483
- [19] LICHARD Peter et al. (CERN, Geneva, Switzerland) for the ATLAS TRT Collaboration The ATLAS TRT Read-Out System CERN/LHCC/96-39, 21 October 1996, p. 442
- [20] TAYLOR Bruce (CERN-ECP Division) TTC Distribution, CERN/LHCC/96-39, 21 October 1996, p. 180
- [21] RADEKA Veljko (Brookhaven National Laboratory) Electronics for Calorimetry. An Overview of Requirements, CERN/LHCC/96-39, 21 October 1996, p. 235
- [22] PARSONS John et al. (Nevis Labs, Columbia University) Analog Memory Readout Electronics for the ATLAS LAr Calorimeter, CERN/LHCC/95-56, 1 October 1995, p. 265
- [23] GINGRICH Douglas M. et al. (Center for Subatomic Research, University of Alberta) A Pipeline Controller for the ATLAS Calorimeter, CERN/LHCC/95-56, 1 October 1995, p. 270
- [24] LOFSTEDT Bo et al. (CERN-ECP Division) FERMI a Digital Front End and Readout Microsystem for High Resolution Calorimetry, CERN/LHCC/95-56, 1 October 1995, p. 283
- [25] KURZBAUER Werner (CERN, Geneva, Switzerland & TU-Graz, Institute of Electronics, Graz, Austria) Bandwidth Requirements for Dynamic Range Compression, CERN/LHCC/96-39, 21 October 1996, p. 81
- [26] BERSET Jean-Claude et al. (CERN-ECP Division) Study of the Applicability of the NA48 Gain-Switching Technology to Liquid Calorimetry at LHC, CERN/LHCC/96-39, 21 October 1996, p. 406
- [27] LOFSTEDT Bo et al. (CERN, Geneva, Switzerland) FERMI : A Digital Front End and Readout Microsystem for High Resolution Calorimetry, CERN/LHCC/96-39, 21 October 1996, p. 84
- [28] DENES Peter (Physics Department, Princeton University, USA) CMS Electromagnetic Calorimeter Readout, CERN/LHCC/96-39, 21 October 1996, p. 48
- [29] STEFANINI Giorgio (CERN-ECP Division) An Overview of Requirements for Optical Links in LHC Experiments, CERN/LHCC/95-56, 1 October 1995, p. 157

- [30] TSANG.T., V.Radeka, T.Srinivasan-Rao and W.J. Willis, "A study of Electro-Optical Modulators for Transfer of Detector Signals by Optical Fibers". BNL-45393
- [31] VASEY François et al. (CERN, Geneva, Switzerland) for the RD23 Collaboration Performance of Optical Links Based on Electro-Optic Modulators, CERN/LHCC/96-39, 21 October 1996, p. 373
- [32] DINKESPILER Bernard et al. (CPPM Centre de Physique des Particules, IN2P3-CNRS et Université d'Aix Marseille II, Marseille, France) Analogue Optical Links for the Front-End Read Out of the ATLAS Liquid Argon Calorimeter, CERN/LHCC/96-39, 21 October 1996, p. 377
- [33] BERINGER Jürg et al. (Laboratory for High Energy Physics, University of Bern, Switzerland) First Results of a Comprehensive Life Time Test of Irradiated LEDs and VCSELs, CERN/LHCC/96-39, 21 October 1996, p. 382
- [34] NISATI Aleandro (INFN Roma) Muon Systems for p-p Experiments, CERN/LHCC/95-56, 1 October 1995, p. 187
- [35] DOSSELLI Umberto (INFN sezione di Padova, Italy) Muon Detector for Collider Experiments, CERN/LHCC/96-39, 21 October 1996, p. 283
- [36] LANKFORD Andrew J. (University of California) Trigger and Event Assembly for LHC Experiments, CERN/LHCC/96-39, 21 October 1996, p. 313
- [37] LETHEREN Michael (CERN, Geneva, Switzerland) Architectures and Technologies for Data Acquisition at the LHC Experiments, CERN/LHCC/96-39, 21 October 1996, p. 125
- [38] KIESLING Christian et al. (Werner-Heisenberg-Institut, München, Germany) Triggering on Secondary Vertices : First Study Towards a Network Algorithm for LHC Experiments, CERN/LHCC/96-39, 21 October 1996, p. 199