Cours/Lecture Series

1990–1991 ACADEMIC TRAINING PROGRAMME

SPEAKER	:	S. CITTOLIN / CERN–CN
TITLE	:	Trigger and data acquistion techniques overview
DATES	:	26 & 28 November
TIME	:	11.00 hrs
PLACE	:	Auditorium

Digital Signal Processing, Trigger and Data Acquisition at LHC Overview

S. Cittolin/CERN-ECP 26 Nov. 90

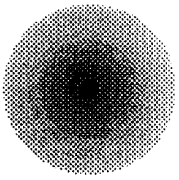
- **Introduction**
  - CERN $Sp\bar{p}S$ Collider (UA1)
  - Trigger and Digital Signal Processing (DSP)

- **CERN LHC Super Collider**
  - Rate and Data Volume
  - Data Acquisition at LHC
  - Front end, Trigger Levels

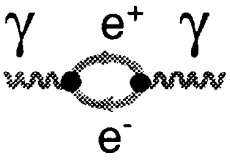
- **Technologies**
- **Readout and Computi**
- **Software**

Short History

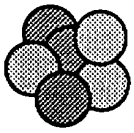
$\lambda = \hbar / p$ $\quad T \approx t^{-1/2}$



10^{-10} m $\quad <$ Kev $\quad >300.000$ Y $\quad$ 1900.... Quantum Mechanics

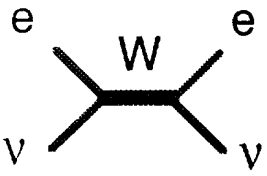


1940-50 Quantum Electro Dynamics

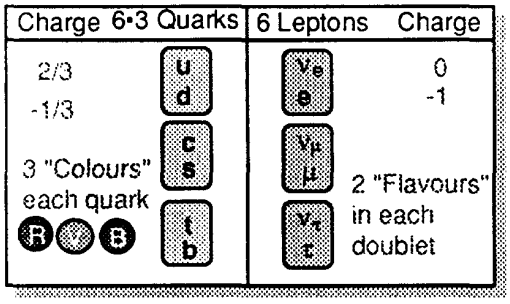


10^{-15} m $\quad \approx$ Gev $\quad \approx 300$ sec $\quad$ 1950-60 Symmetries Field theories

10^{-16} m $\quad >$ Gev $\quad \approx 10^{-6}$ sec $\quad$ 1960-70 Quarks Gauge theories



10^{-18} m $\quad$ 100 Gev $\quad \approx 10^{-10}$ sec $\quad$ SPS $p\bar{p}$ 1970-83 ElectroWeak QCD, Unification



LEP 1990 3 Families .....

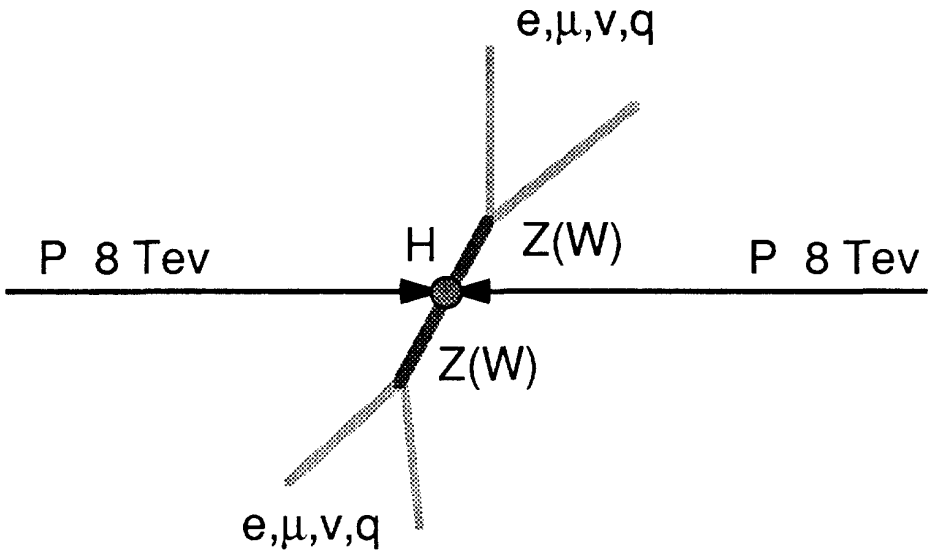
10^{-19} m $\quad \approx$ Tev $\quad \approx 10^{-12}$ sec $\quad$ LHC 1990-2000 Origin of masses The next step...

MATTER ?

Big Bang

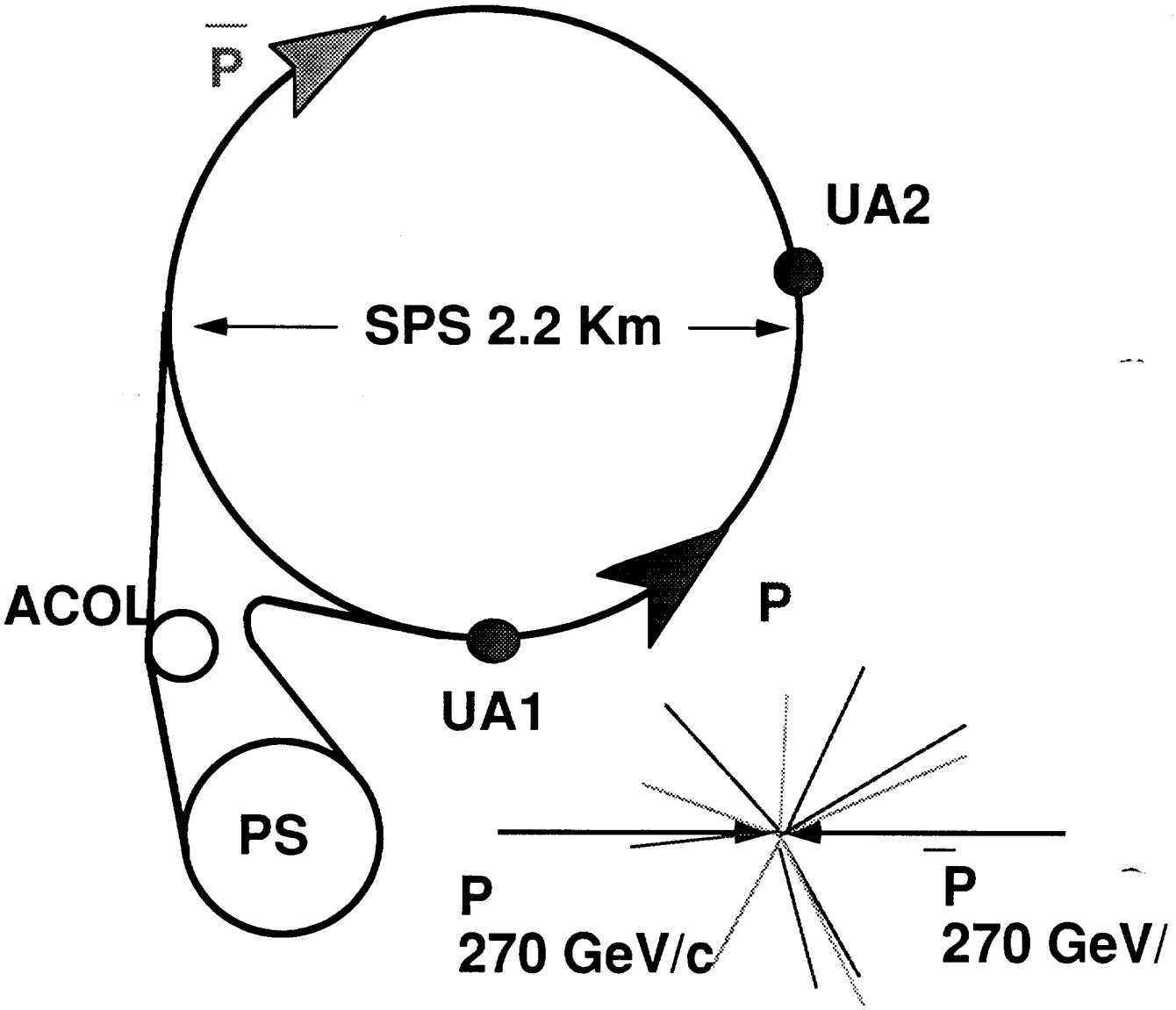
The Next Step

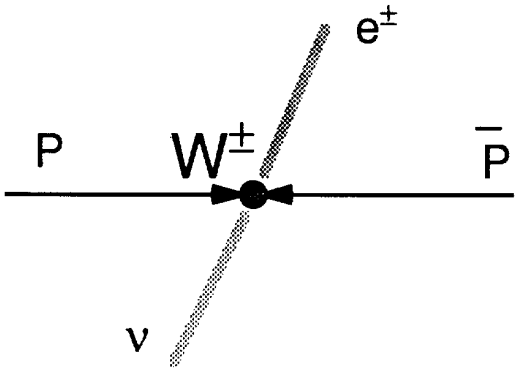
- **HIGGS**
  Electroweak symmetry breaking
  Origin of masses

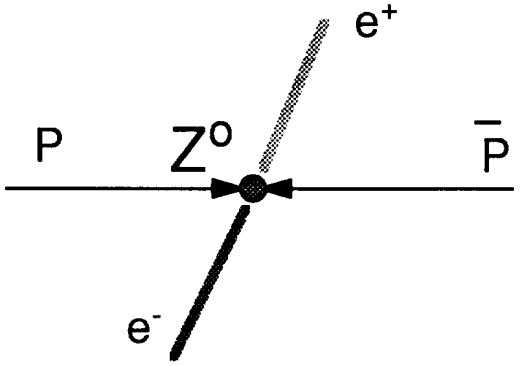


New forces (symmetries)
New particles
Super symmetries
Next step in compositness
.....

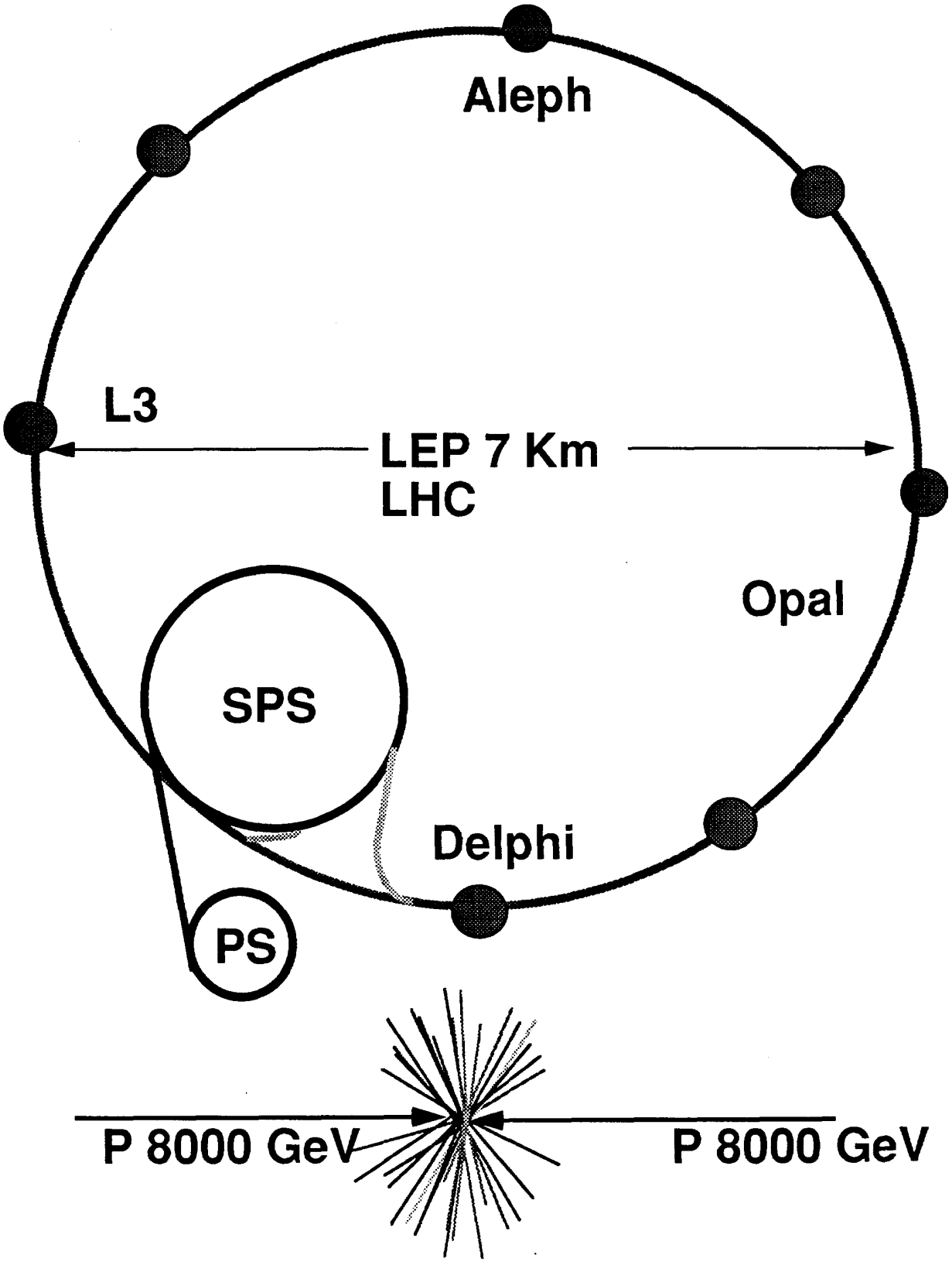
CERN SppS Collider



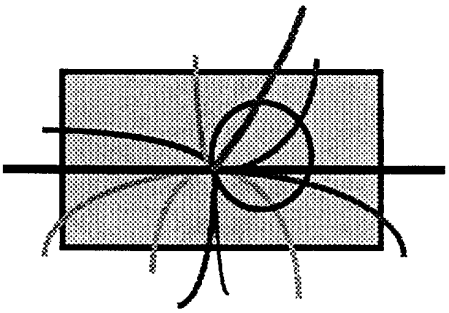




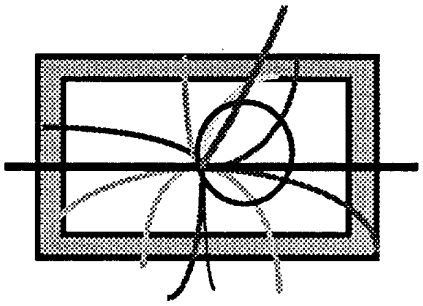
LHC (Large Hadron Collider)



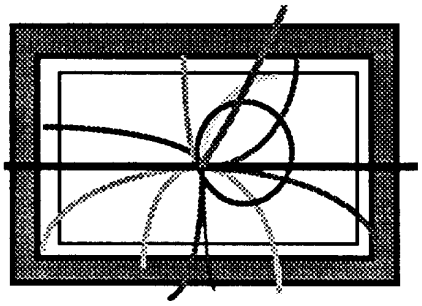
UA1 detectors



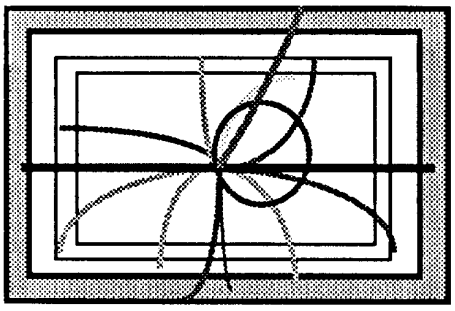
Central detector
- Charged particle imaging
- Momentum



Electromagnetic calorimeter
- Electron, gamma identification
- Energy



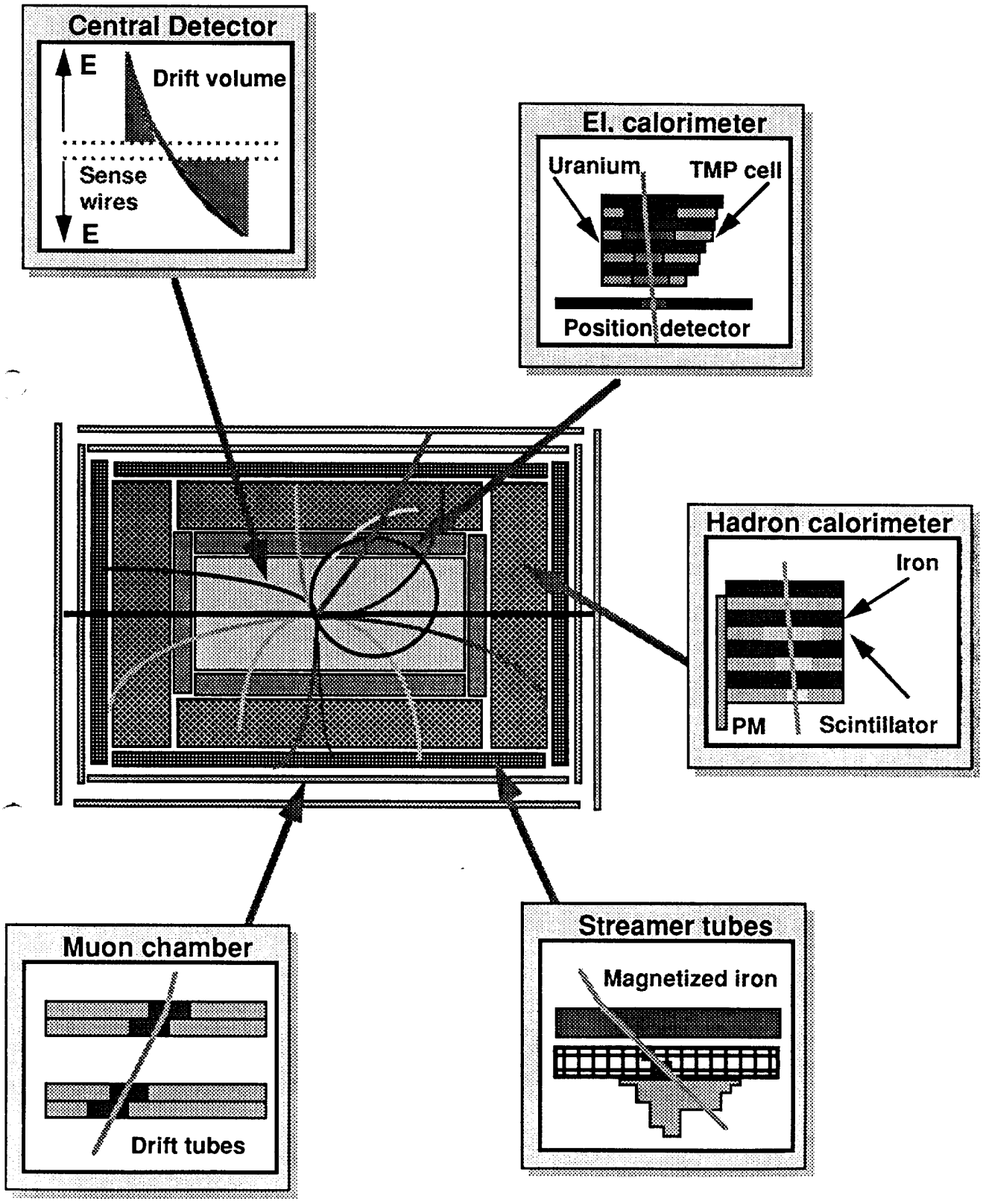
Hadronic calorimeter
- Hadron identification
- Energy



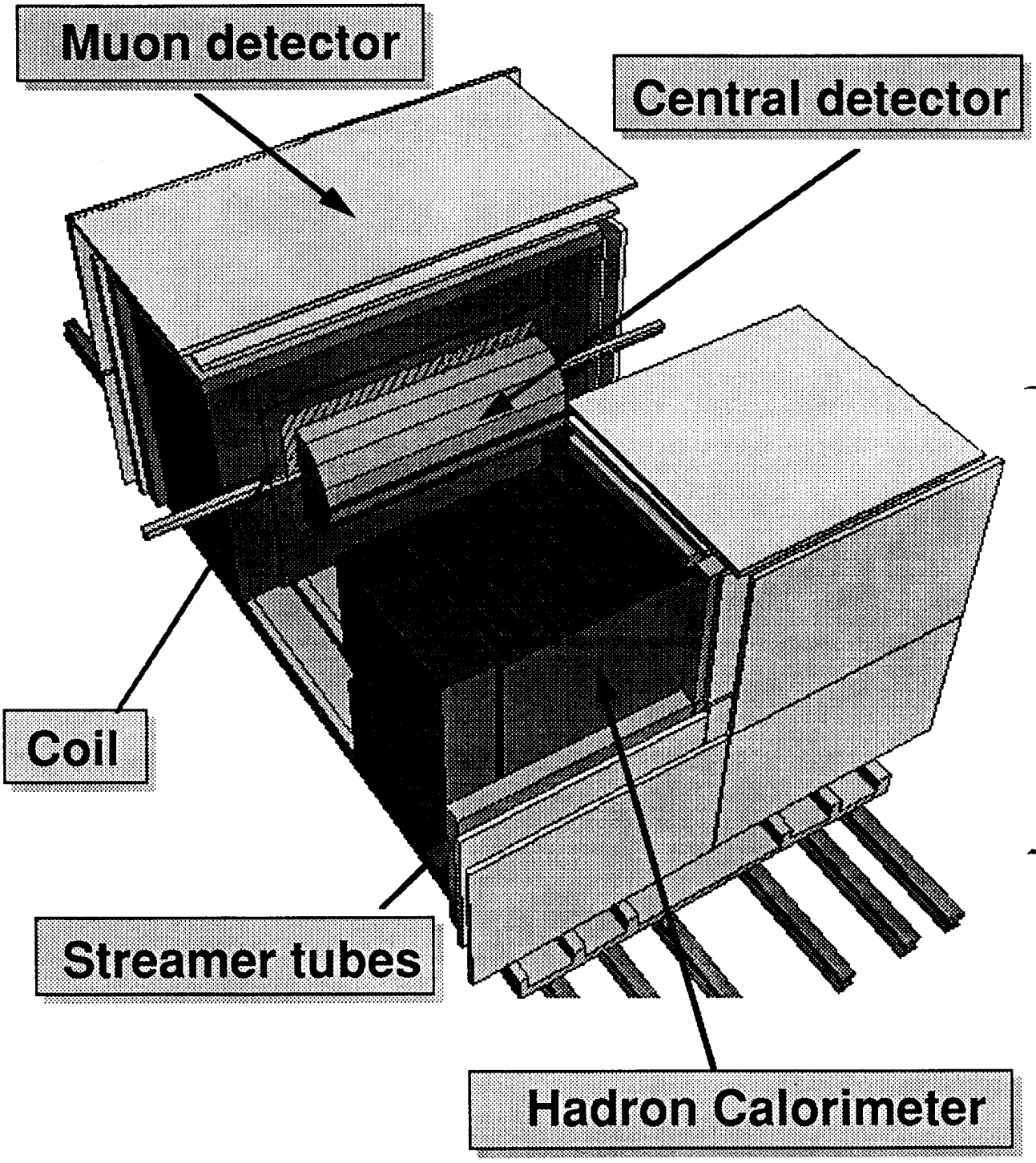
Muon detector
- Event tagging
- Momentum

4π ermeticity
- Missing energy, neutrinos

UA1 detectors

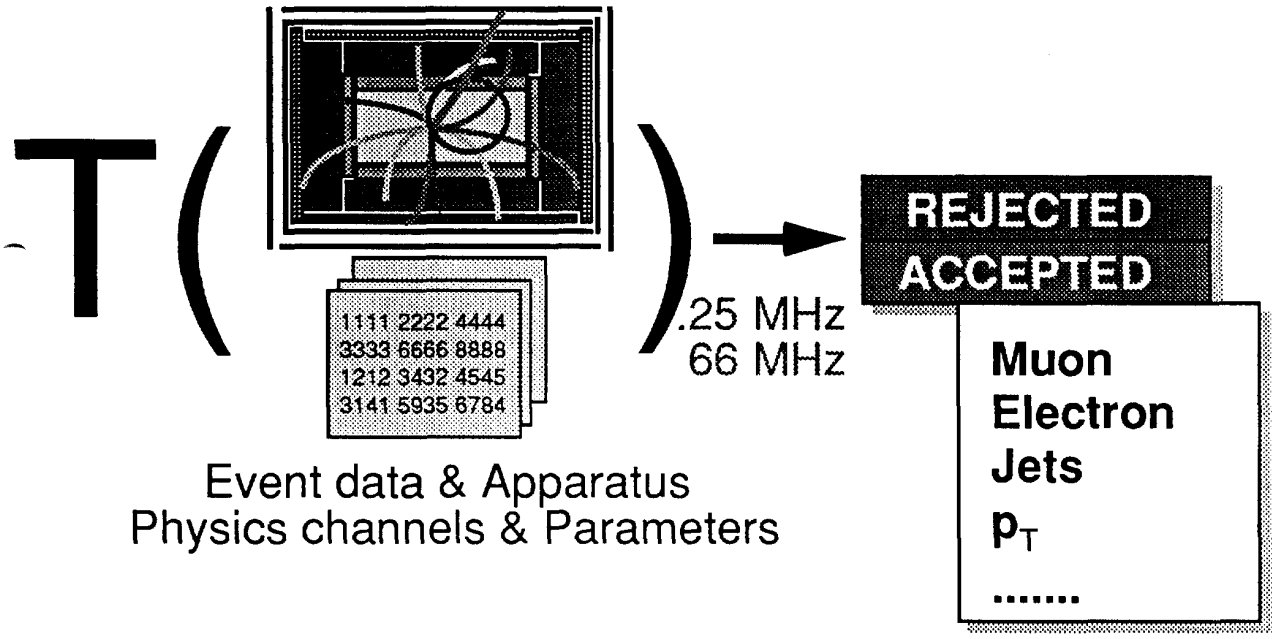


UA1 layout


Muon detector
Central detector
Coil
Streamer tubes
Hadron Calorimeter

Trigger

The trigger is a function of :



Since the detector data are not all promptly available and the function is highly complex, T(...) is evaluated by successive approximations called :

TRIGGER LEVELS
(possibly with zero dead time)

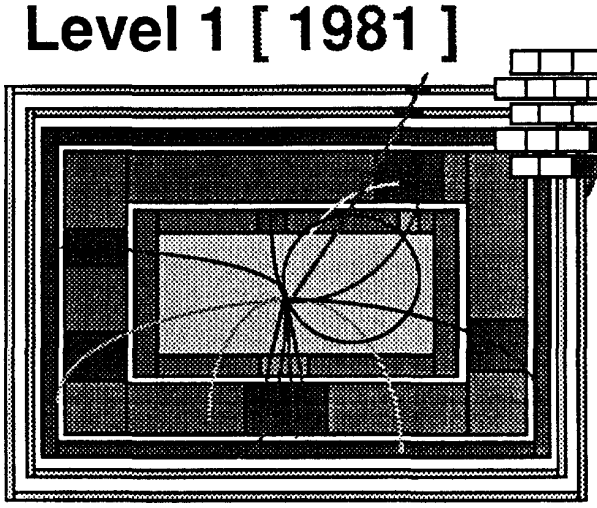
The final aim is to look for ≈ 1/1000000000
1/1000000000000

Trigger Levels (UA1)

CERN Collider (1981-1989)

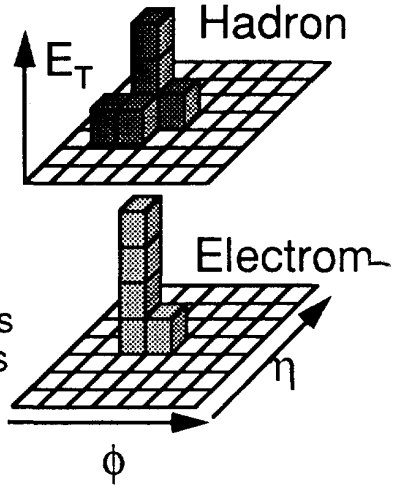
Luminosity	**10^{30} $s^{-1}cm^{-2}$**
Bunch separation	**4 μs (250 kHz)**
Event rate	**< 10^5 Hz**
No. channels	**≈ 10^5**

Level 1 [1981]

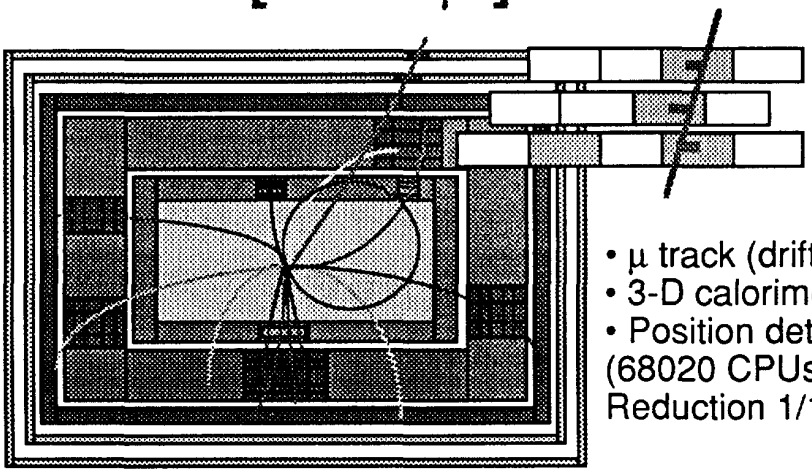


- μ segment
- em showers
- Jets
- E_T

Hardwired processors
(640+548 cells, <4μs
Reduction 1/10000)

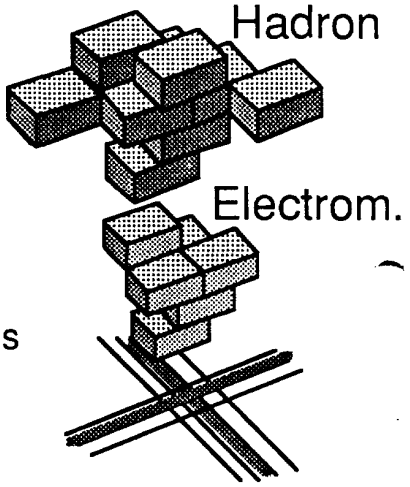


Level 2 [1988.μ]

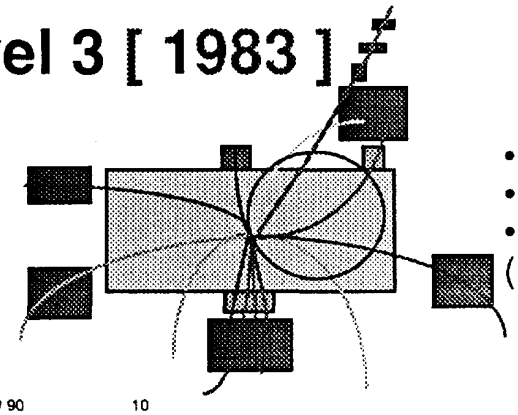


- μ track (drift time)
- 3-D calorimetry
- Position detector

(68020 CPUs ≈ 7 ms
Reduction 1/10)



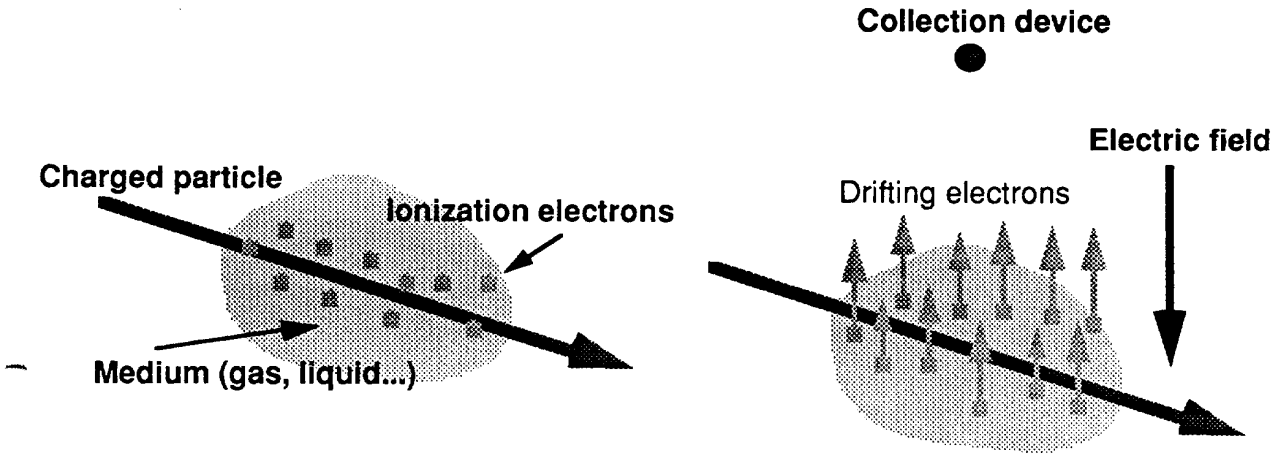
Level 3 [1983]

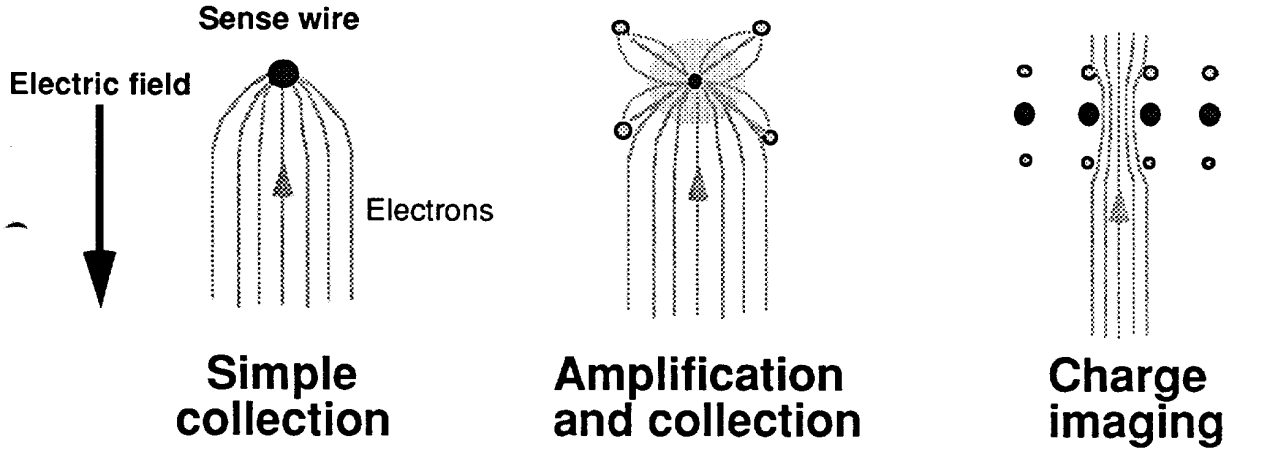


- Partial event reconstruction
- Calorimetry & Tracking
- Event topology

(3081E farm, ≈ 100 ms Reduction 1/3)

Electron drift detectors





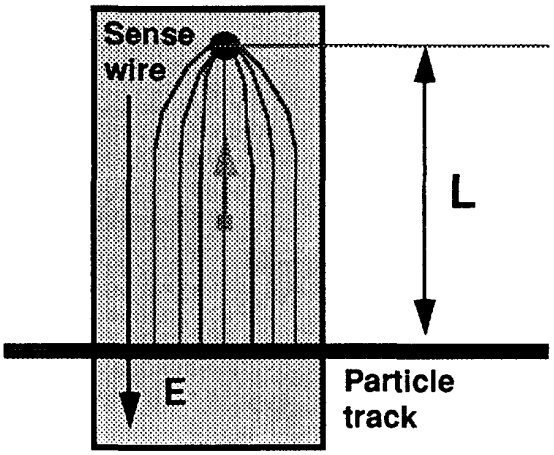
Simple collection

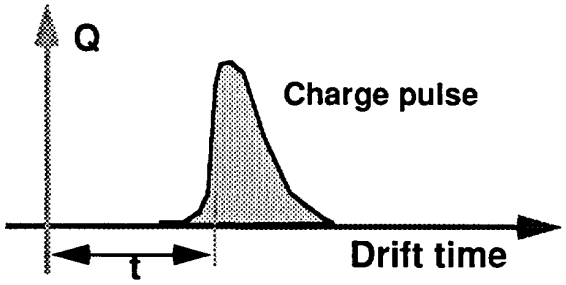
Amplification and collection

Charge imaging

Single wire drift cell

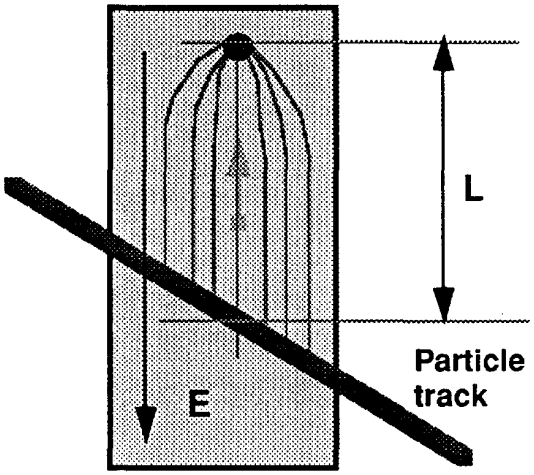
Track normal to drift

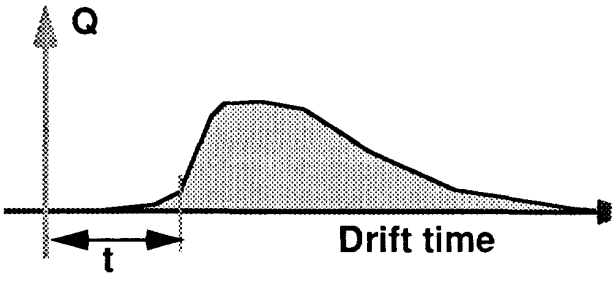




$$L = Vd \cdot (t - to)$$

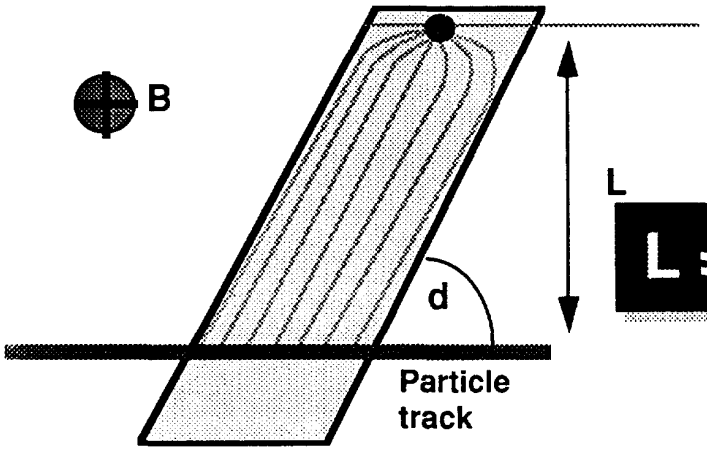
Track at smaller angle to drift





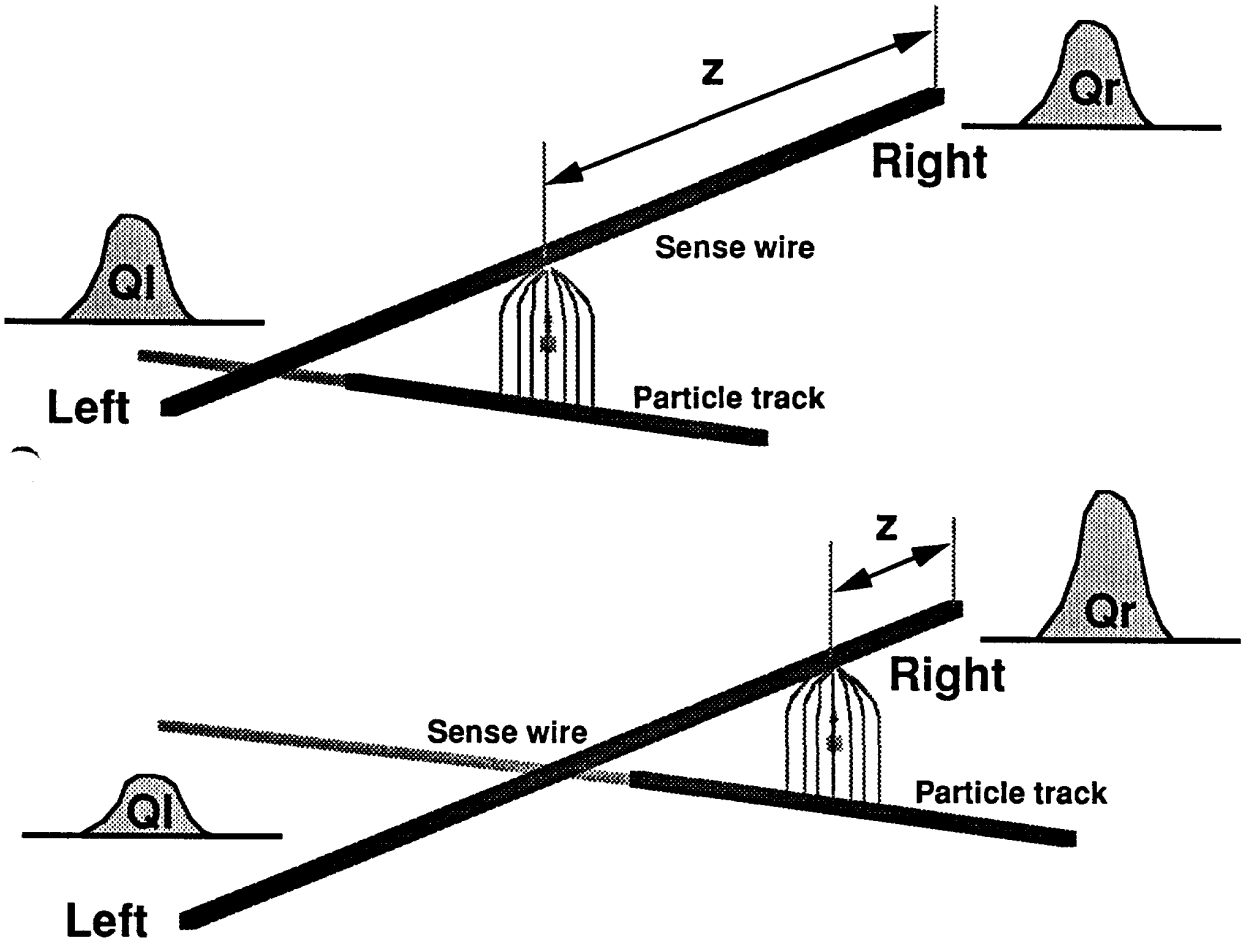
$$L = Vd \cdot (t - to) + DL$$

Track in a magnetic field parallel to sense wire



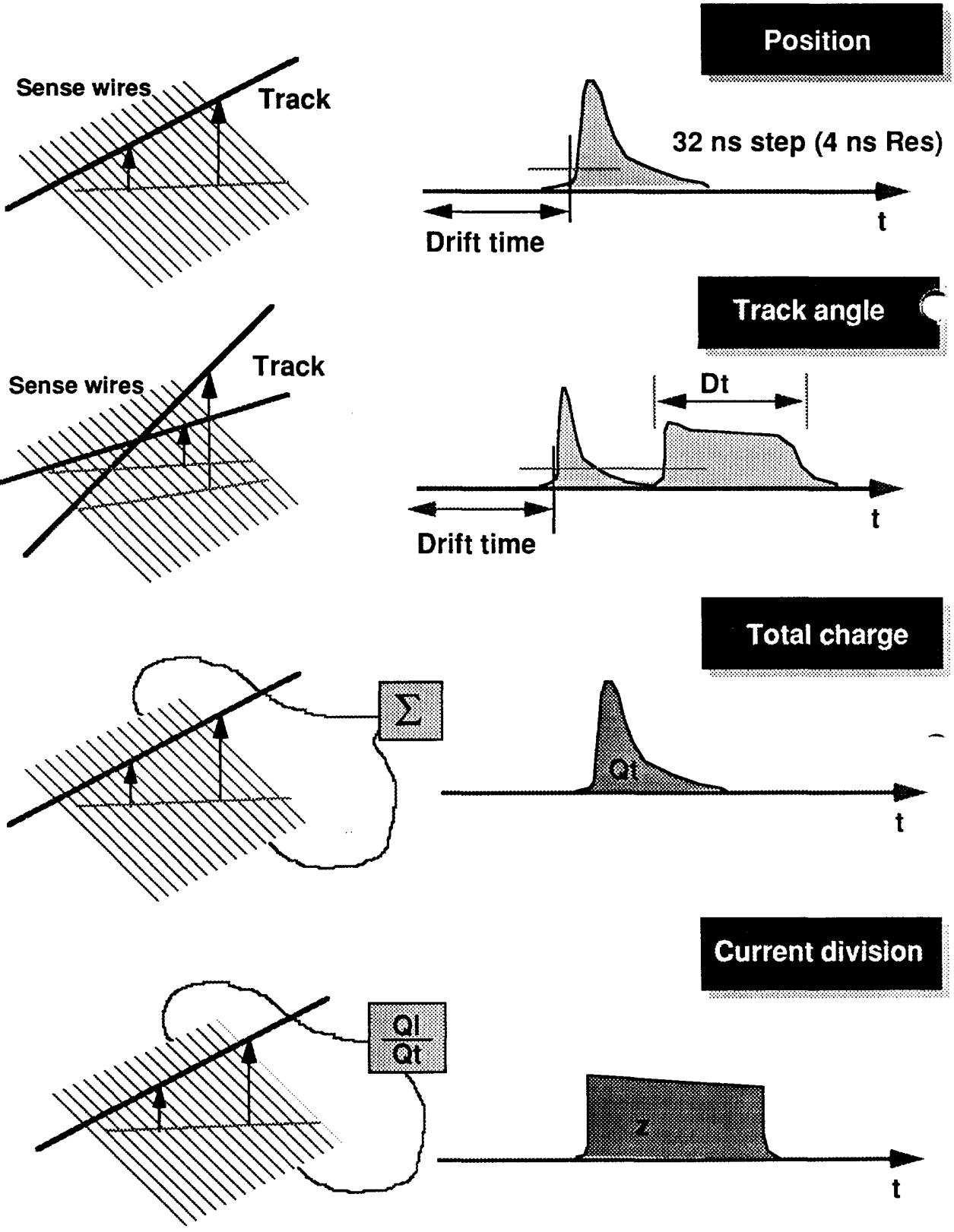
$$L = Vd \cdot (t - to) \cos(d)$$

Current division

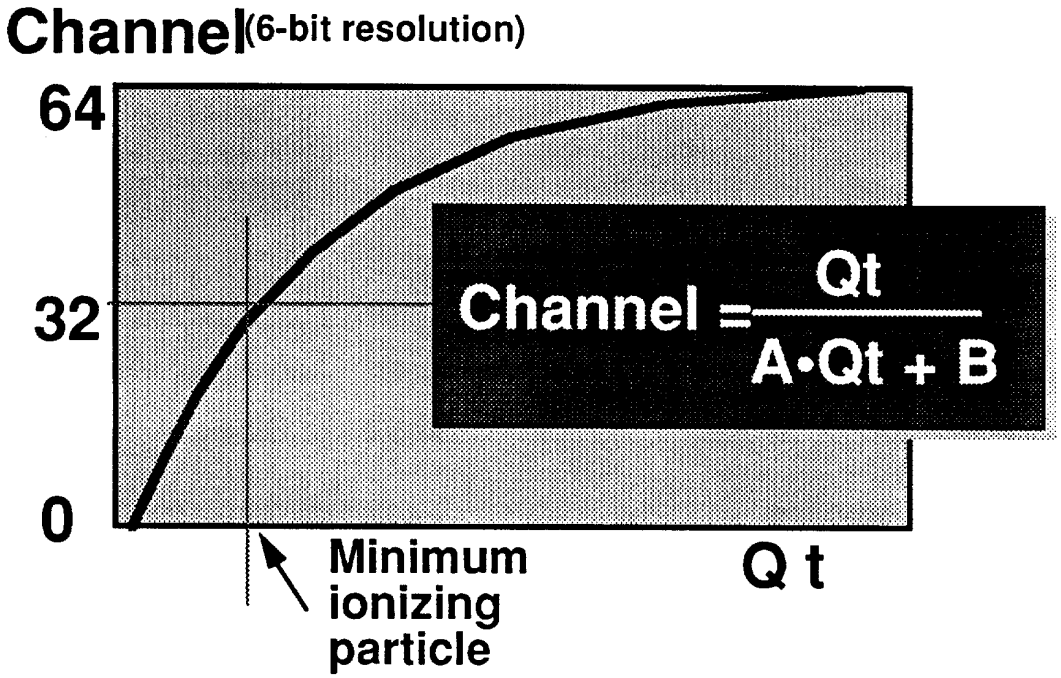


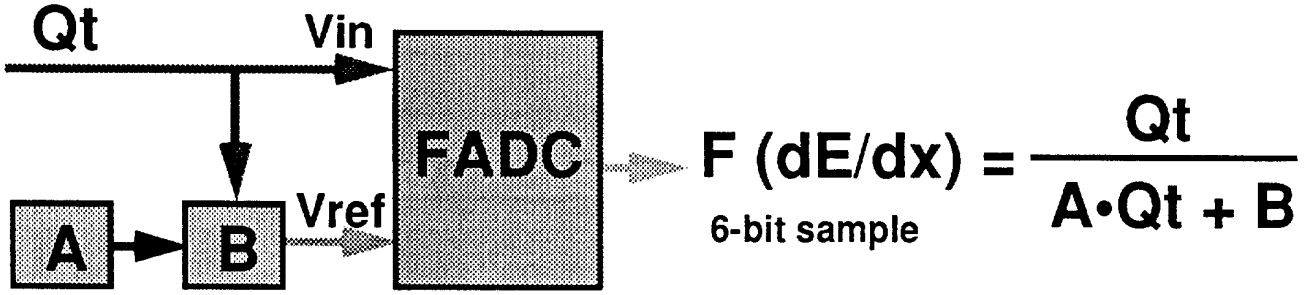
$$z = Ql / (Ql + Qr) = Ql / Qt$$

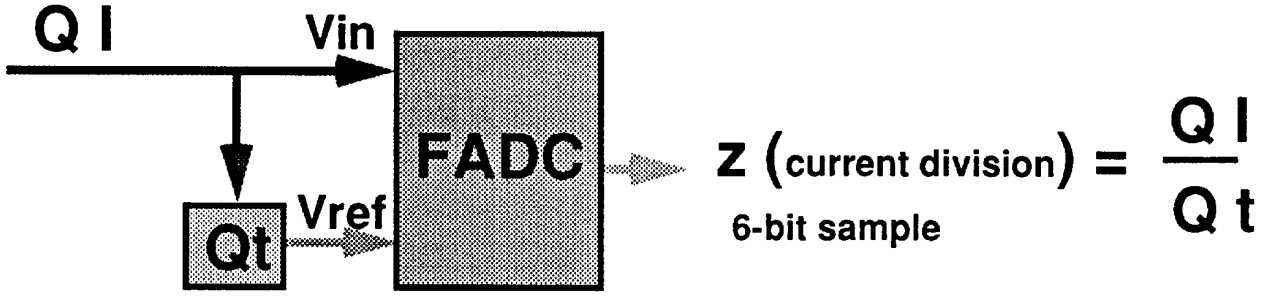
Imaging parameters



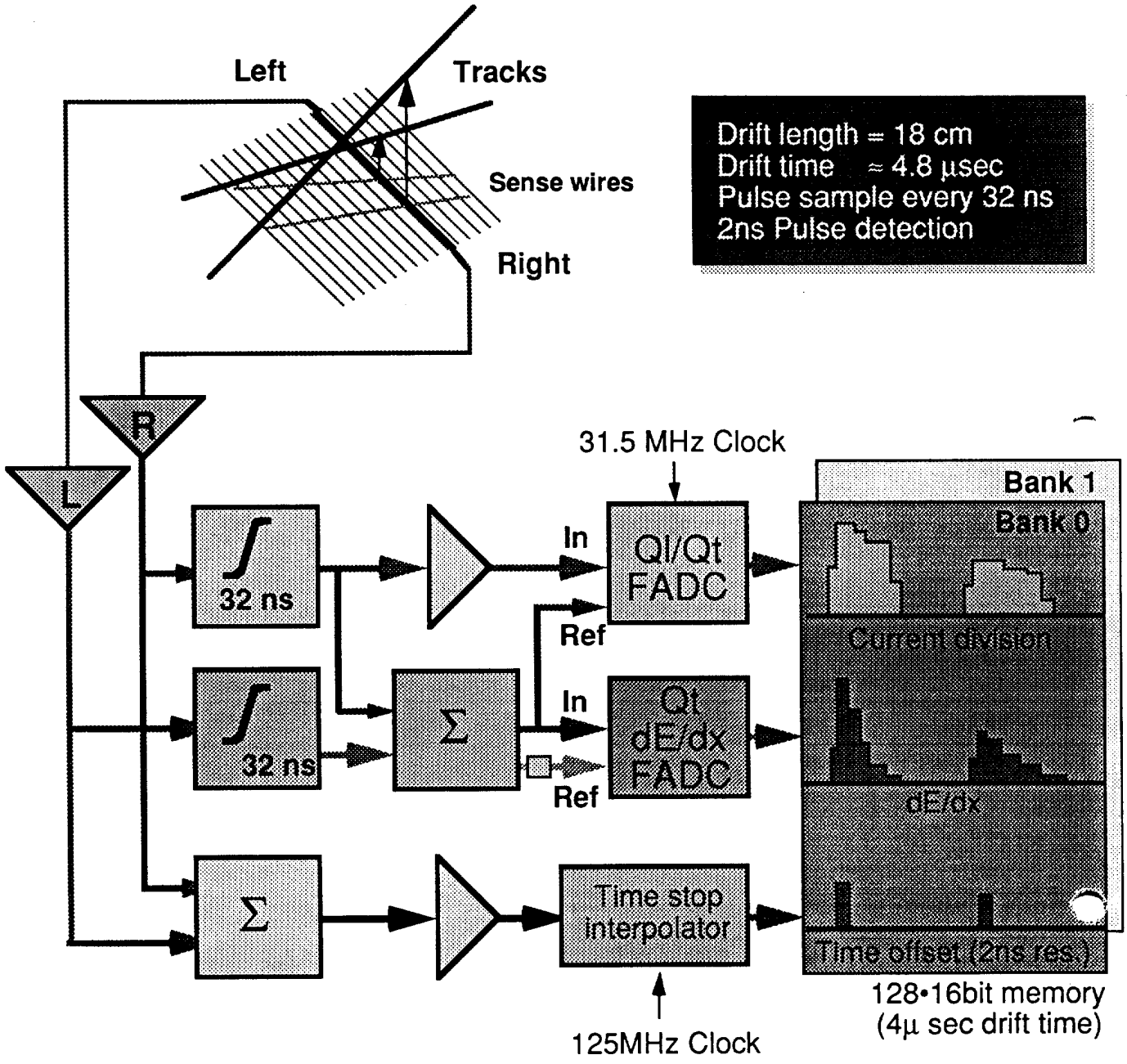
FADC application







Central detector channel electronics



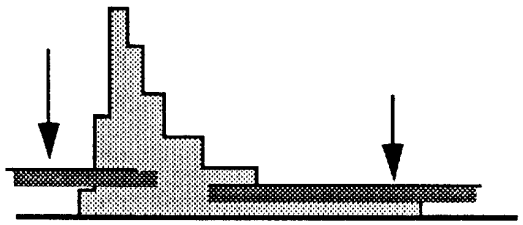
$$F(dE/dx)_{\text{6-bits}} = \frac{(Qt + b)}{(A \cdot Qt + b + B)} \qquad Z_{\text{6-bits}} = \frac{Q\,l}{Q\,t} \qquad \text{Toff}_{\text{4-bits}}$$

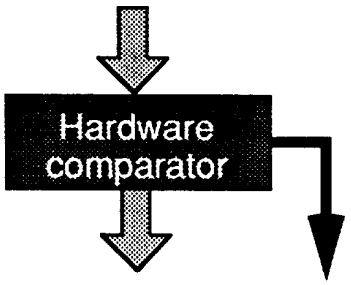
A = .8162 compression constant
B = base line
b = scaling factor

Pulse analysis basic tools

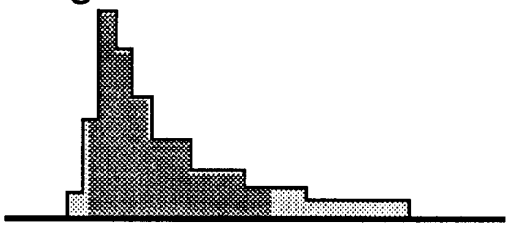
Numeric pulse analysis needs some fast tools directly available on the data stream. Such as :

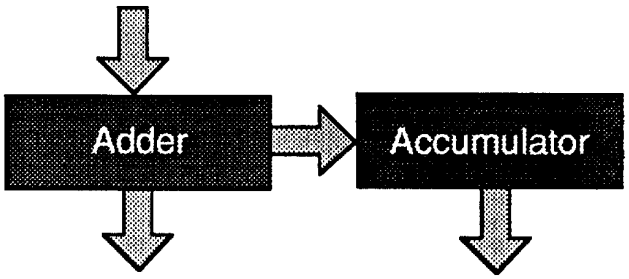
Comparator



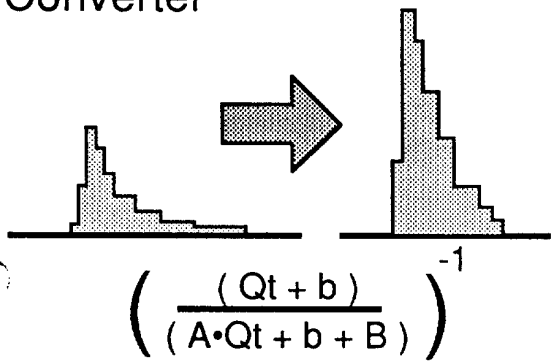


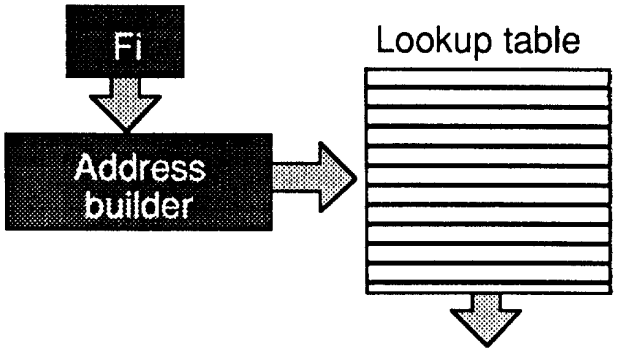
Integrator



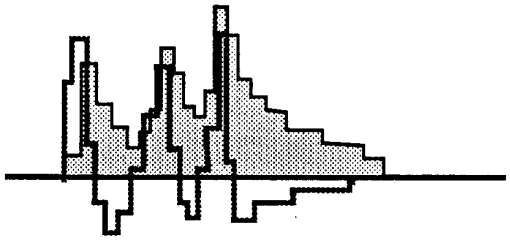


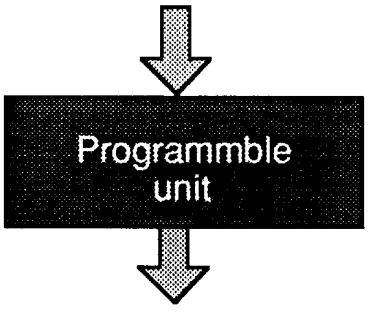
Converter





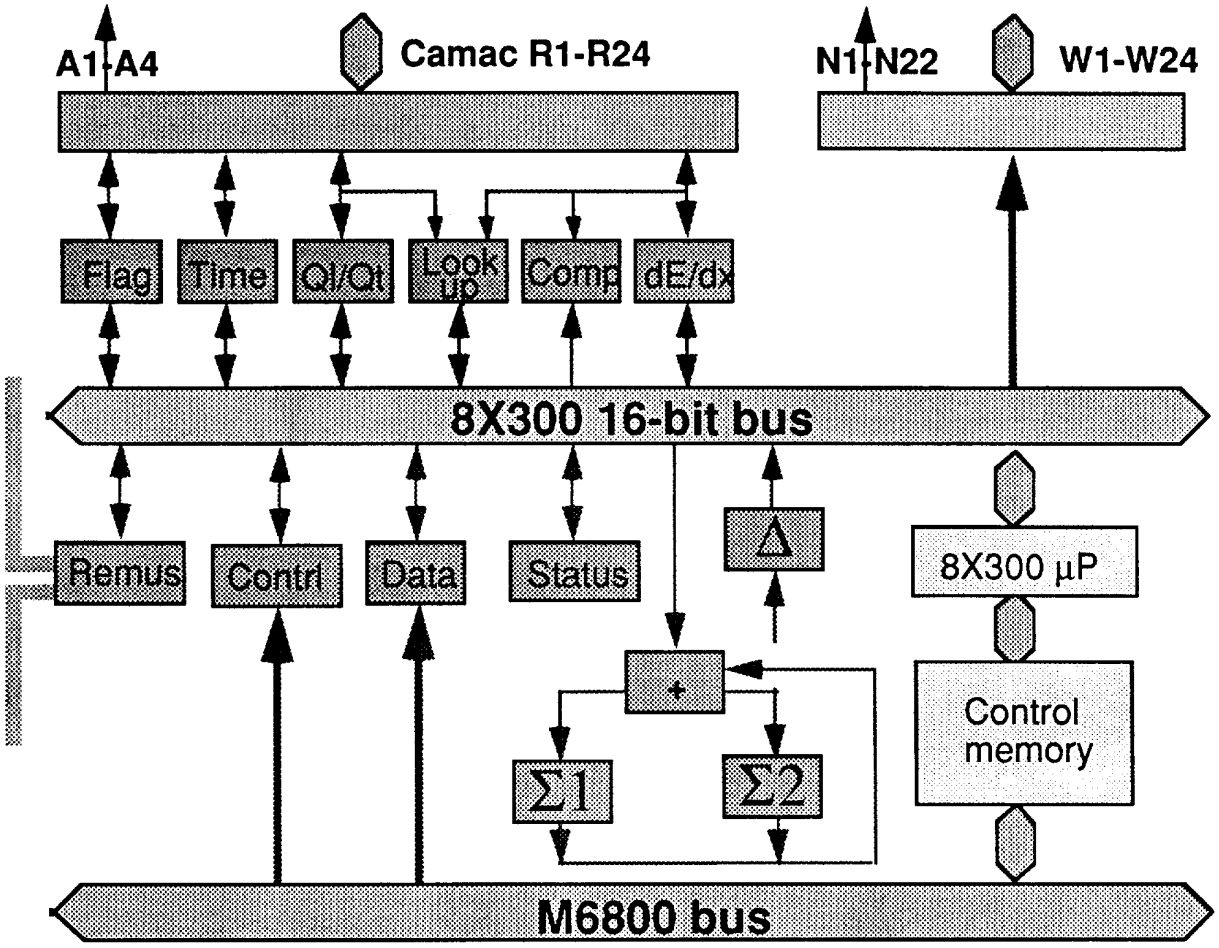
Differentiator



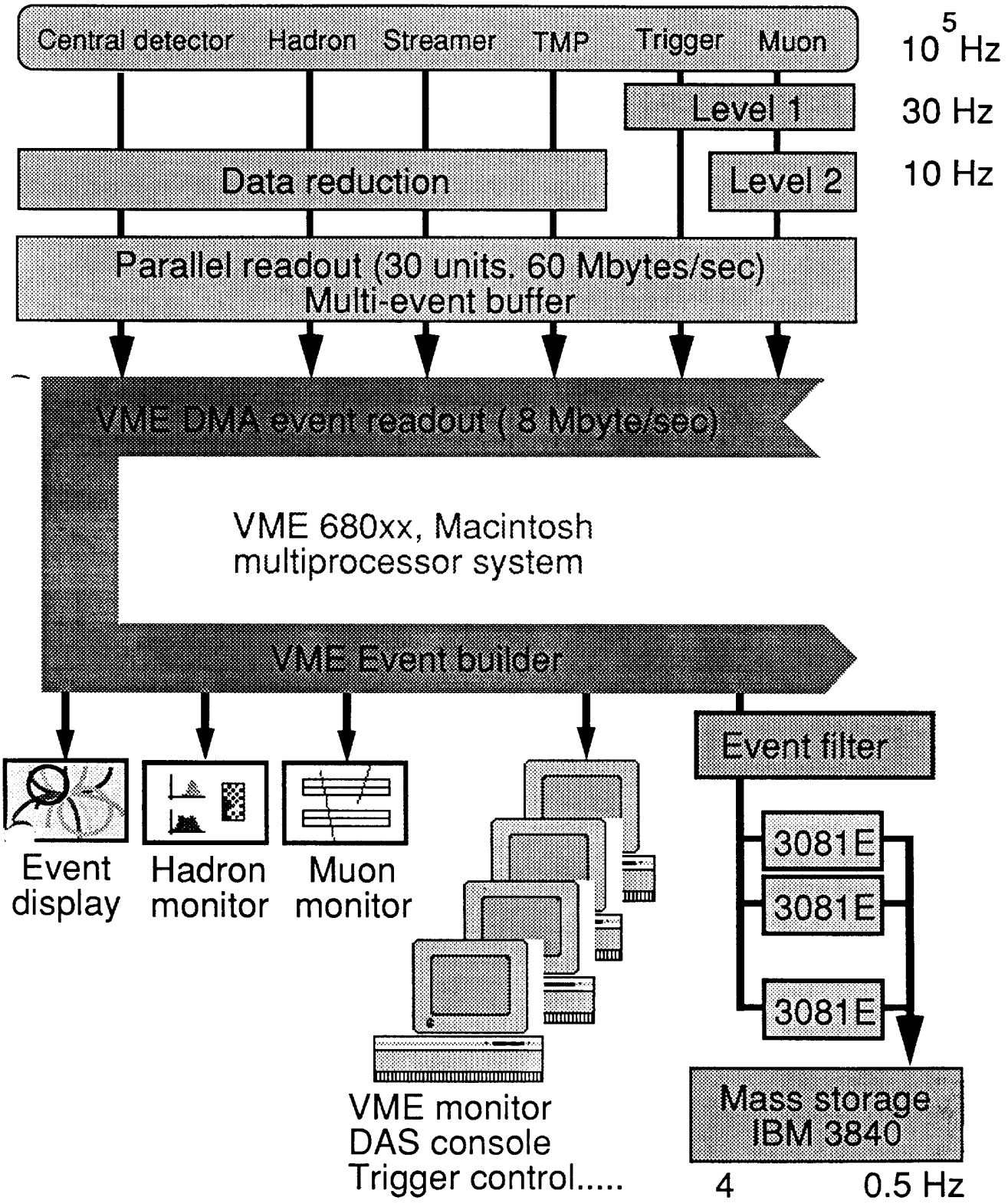


+ channel calibration and monitoring tasks (programmable device

Readout Processor structure

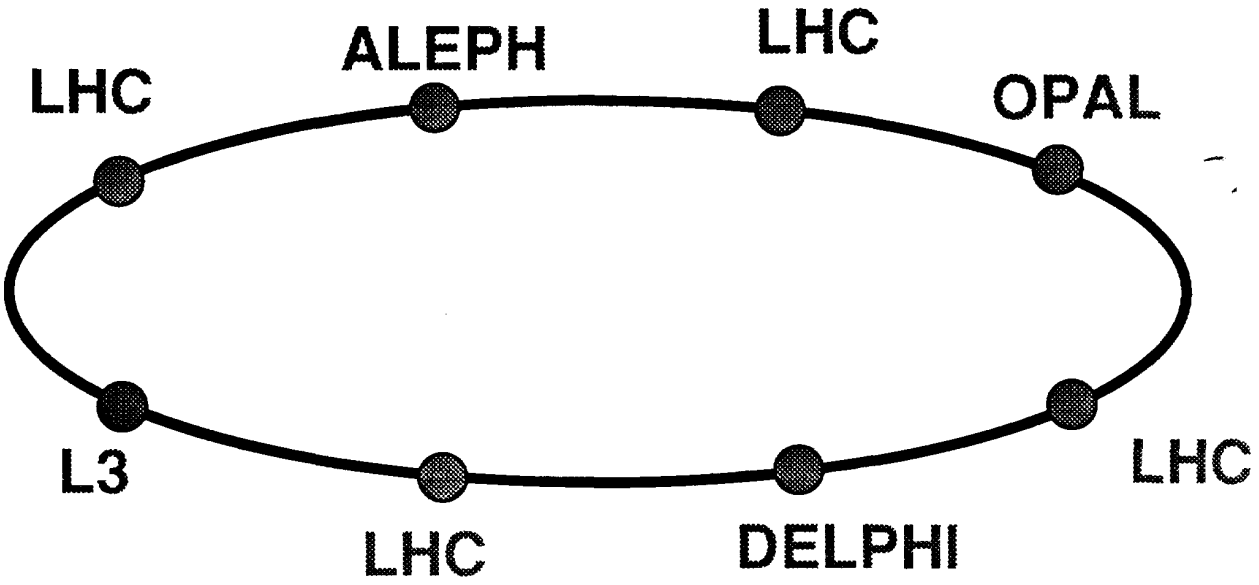


UA1 data acquisition



LHC Layout

Three dedicated interaction regions
(in addition to the LEP crossings)



			√s		Luminosity
LEP	e^+	e^-	200	GeV	$3 \cdot 10^{31}$ cm^{-2}s^{-1}
			√s		Luminosity
LHC	p	p	16	TeV	10^{34}
	e	p	1.7	TeV	10^{32}
	P_b	P_b	1312	TeV	10^{27}

Parameters

P-P LHC (8+8 Tev)

Luminosity	**10^{33} - 4•10^{34} $s^{-1}cm^{-2}$**
Bunch separation	**15 ns** (66 MHz)
Event rate	**$\leq$ 2 GHz** ($\approx$ 40 Ev/bunch)
No. channels	**10^6 - 10^7**

General Purpose Experiment

CERN Collider (270+270 Gev)

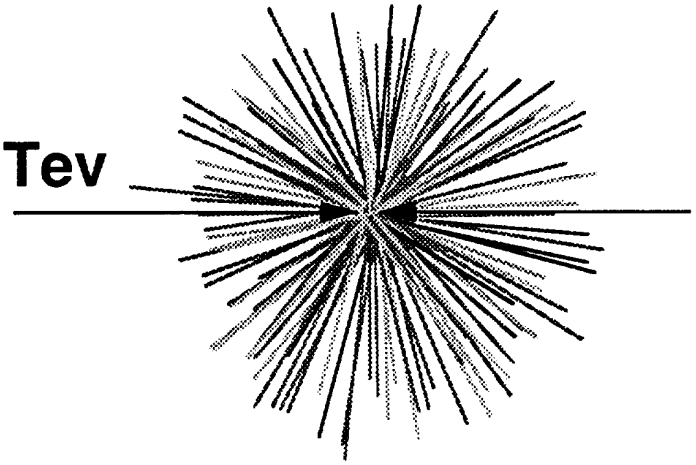
Luminosity	**10^{30} $s^{-1}cm^{-2}$**
Bunch separation	**4 μs** (250 kHz)
Event rate	**< 10^5 Hz**
No. channels	**$\approx$ 10^5**

LHC Events

Luminosity	**10^{33} - $4 \cdot 10^{34}$ $s^{-1}cm^{-2}$**
Bunch separation	**15 ns** (66 MHz)
Event rate	**$\leq$ 2 GHz** ($\approx$ 40 Ev/bunch)
No. channels	**10^6 - 10^7**

General Purpose Experiment

P 8 Tev



P 8 Tev

$\approx$ 90 tracks/event

$\approx$ 10 Events/bunch

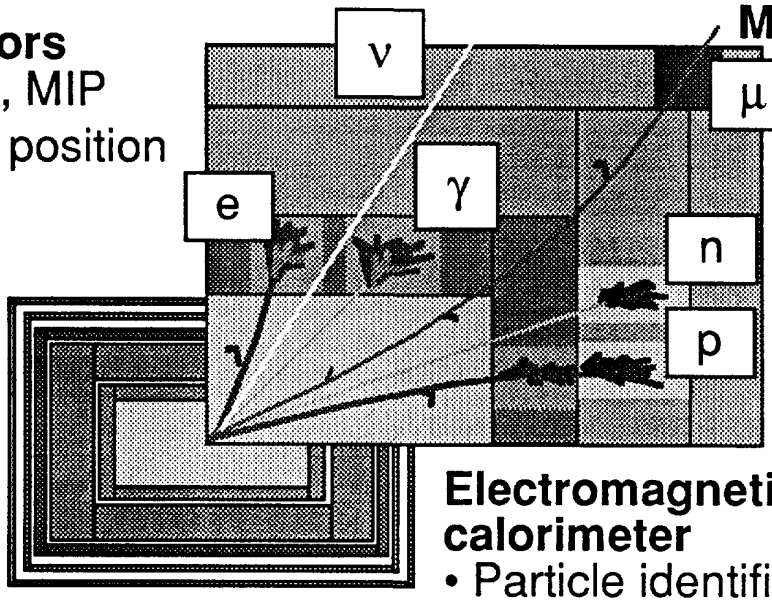
at Luminosity = 10^{34} $s^{-1}cm^{-2}$

$\approx$ 1000 tracks/15ns

Apparatus

Basic Detectors

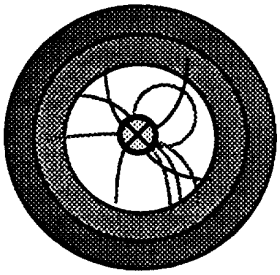
Track detectors
- Tracking, p_T, MIP
- Em. shower position
- Topology
- Vertex



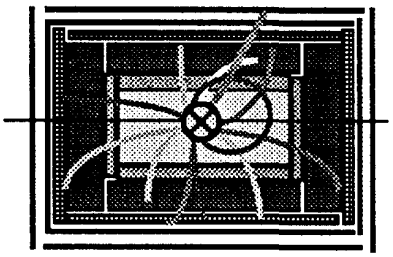
Muon detector

Electromagnetic / Hadron calorimeter
- Particle identification (e, μ, Jets, Missing p_T)
- Energy measurement

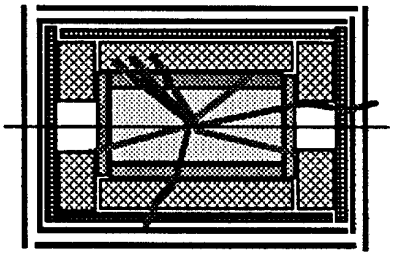
Magnetic field



Solenoid

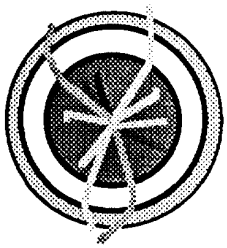


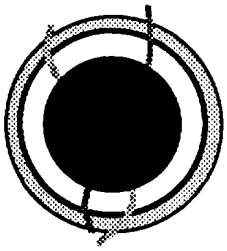
Dipole



No central field
External toroid

General Purpose / Dedicated experiment





Number of Channels

Examples of:

Inner tracking

- Track-preshower (pads) : $2 \cdot 10^7$ channels
- TRD straw tube (projective): $4 \cdot 10^5$
- Scintillating fibers (projective) : $\approx 10^6$

Expected occupation 10^{-3} - 10^{-2}

Calorimetry (dominated by e.m.)

granularity $\Delta\eta \cdot \Delta\phi = 0.02 \cdot 0.02$

(at least two sampling, $|\eta| < 3$ $2 \cdot 10^5$ channels

Expected occupation 10^{-2} - 10^{-1}

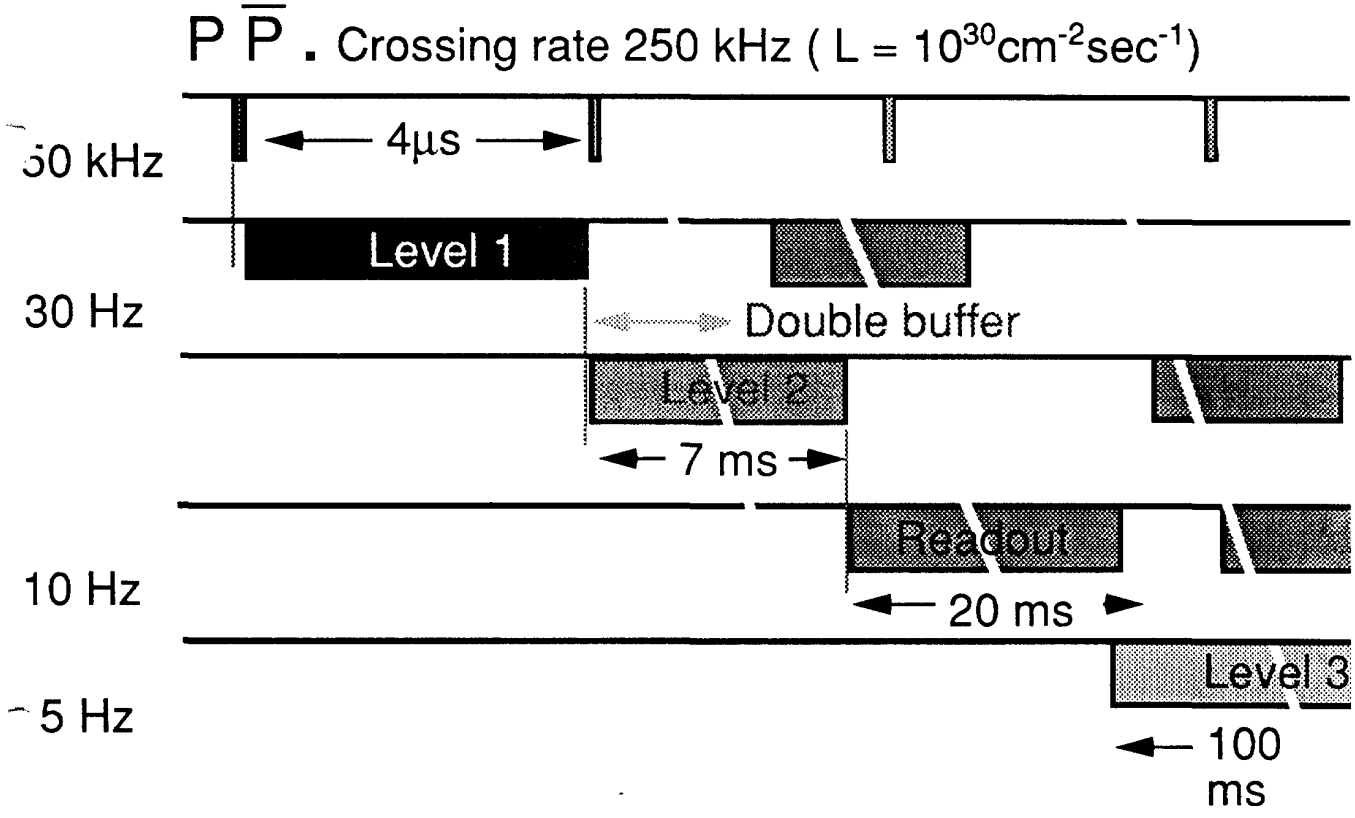
Muon tracking

- Resistive plate chamber 10^5 - 10^6 channels
- Drift chambers

Expected occupation 10^{-5} - 10^{-6}

CERN Collider Trigger Levels

UA1 Timing



- **Level 1 trigger inter bunch crossings**
- **Detector cell memory less than 4μs**
- **Almost no event overlapping. Clean even**
- **Most of electronics outside the detector**

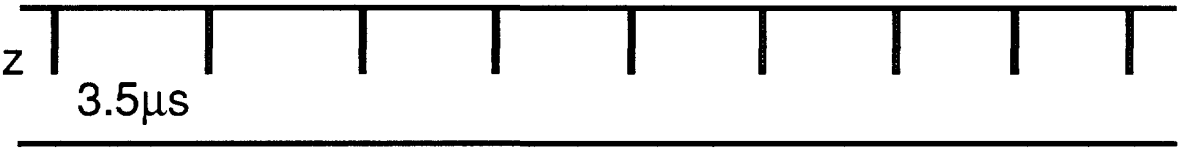
LEP, HERA...

LEP. Crossing rate 30 kHz

≈ kHz

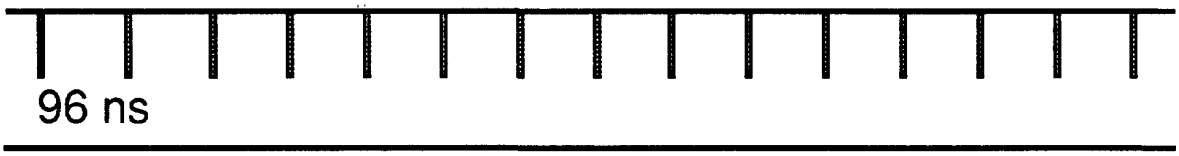
Tevatron. Crossing rate 280 kHz

≈ 100 kHz

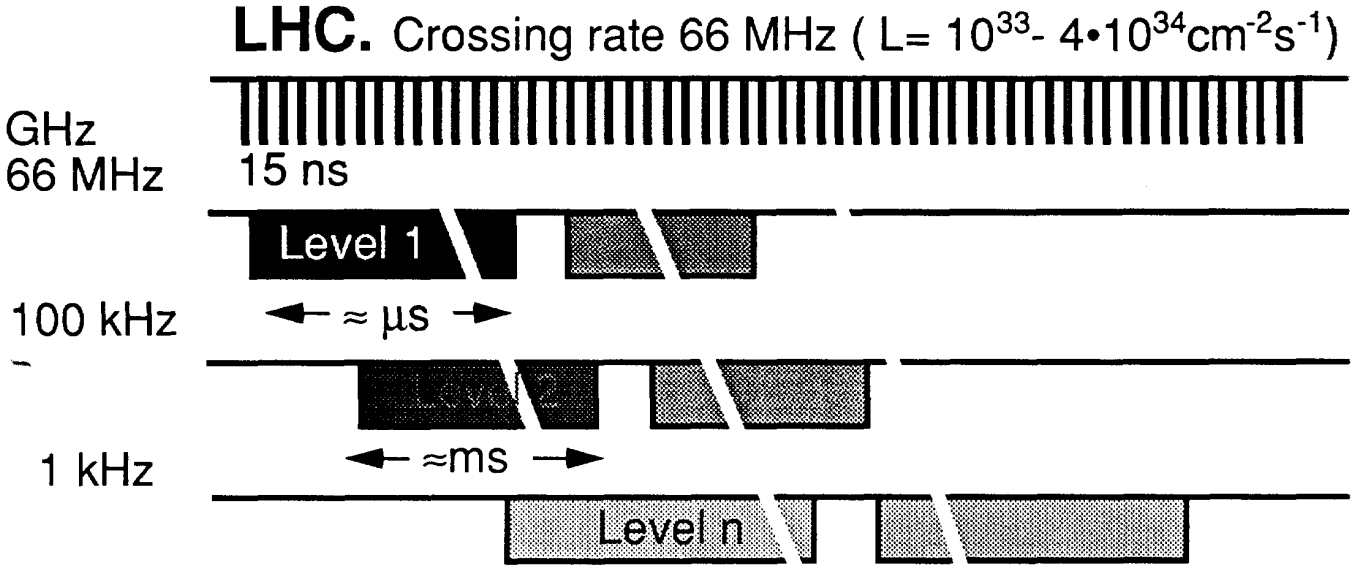


HERA. Crossing rate 10 MHz

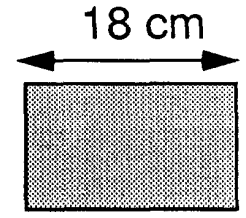
≈10 kHz



LHC Trigger Levels



- **Level 1 trigger time exceeds bunch interval**
- **Detector cell memory greater than 15 ns**
- **Event overlap & Signal pileup**
- **Very high number of channels**



UA1 drift cell
T_{max}=3.8µs

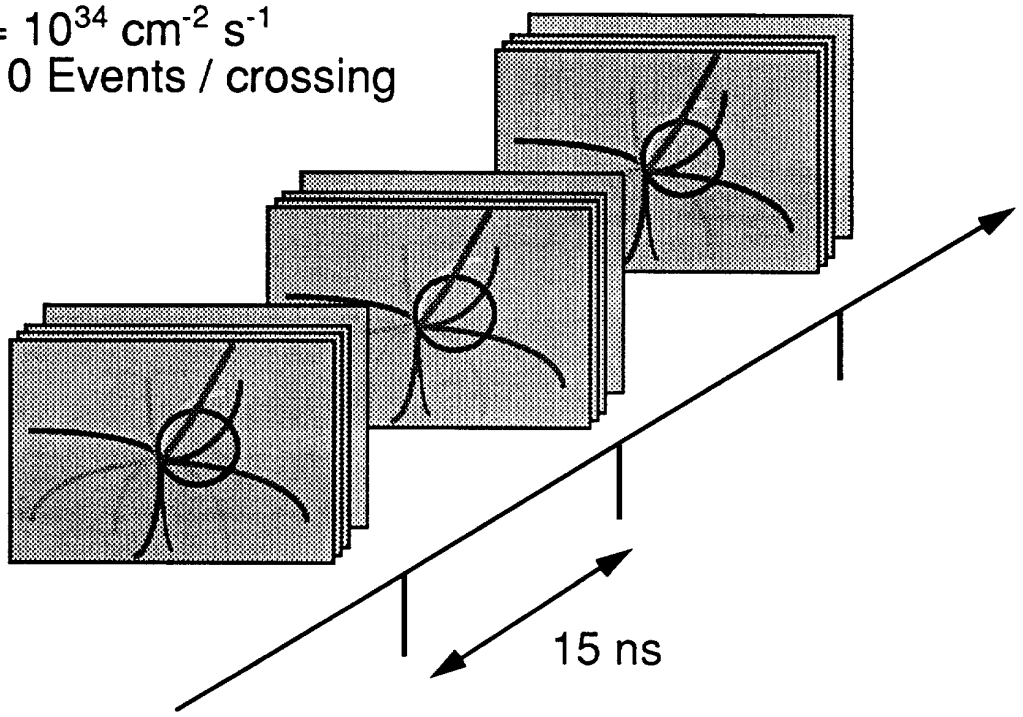
V_D = 50 µm/s

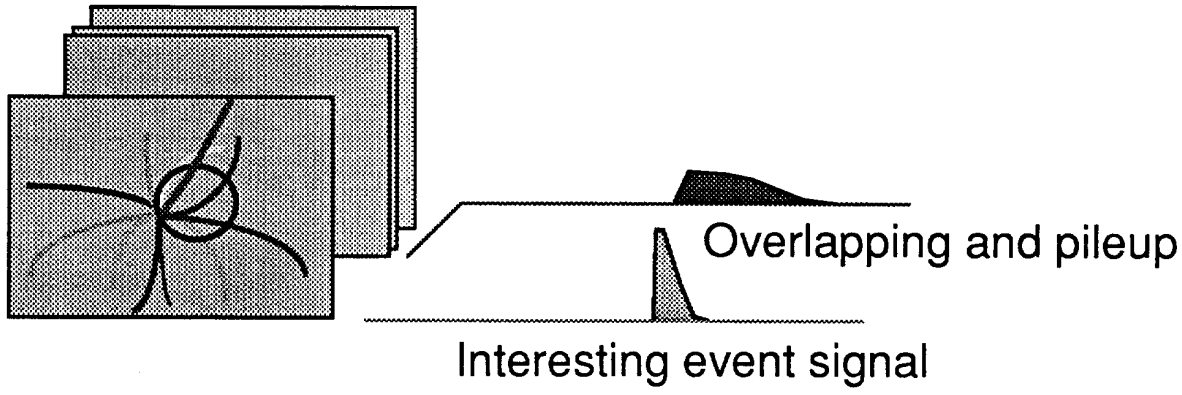
4 mm

LHC drift cell
T_{max}= 40 ns
Multiple crossing resolution

Multi Events and Pileup

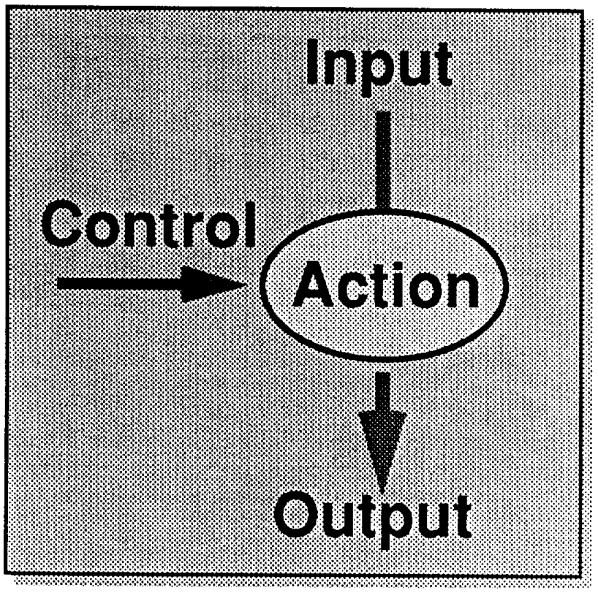
$L = 10^{34}\ cm^{-2}\ s^{-1}$
$\approx$ 10 Events / crossing

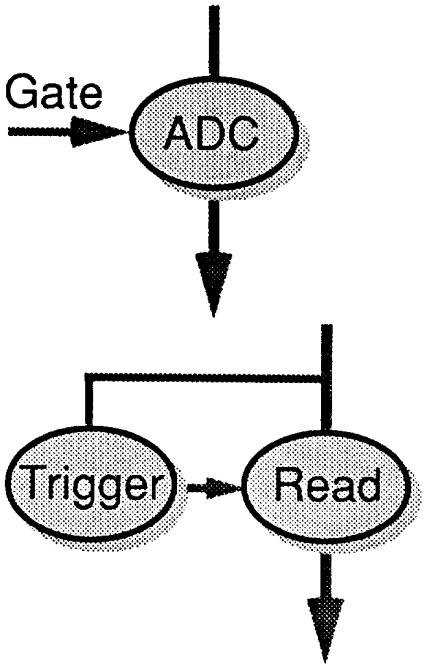




Basic DAQ

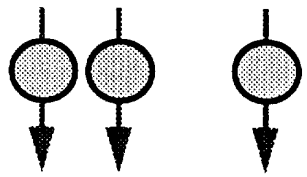
Basic DAQ data flow





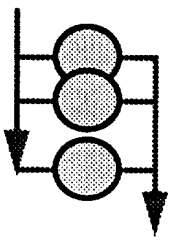
STRUCTURES

Parallel **Pipeline** **Farm** **Data driven**

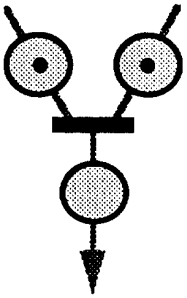


Event partition

Time/function partition

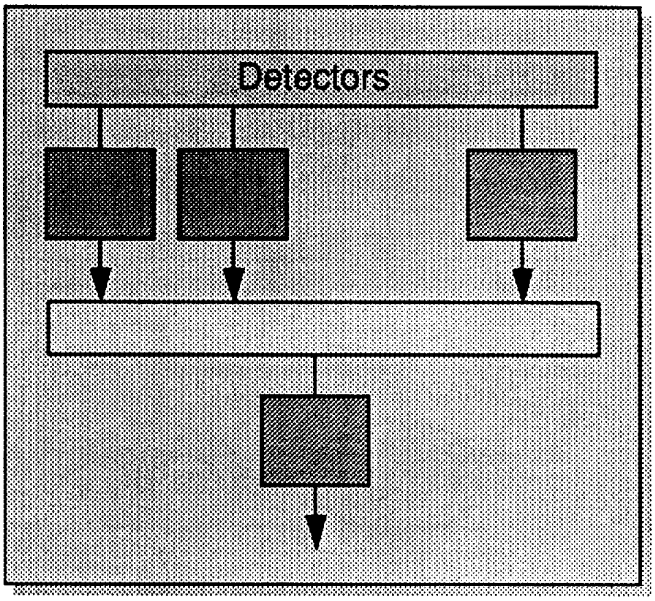


Multiple events



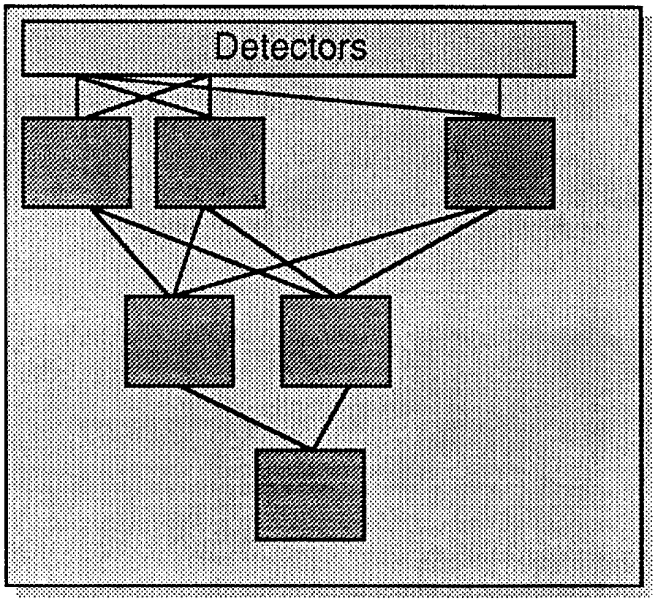
DAQ architecture

Partition & tree



CAMAC
VME
FASTBUS
(Collider, LEP...)

Dynamic routing



VME
Transputers
(HERA, ZEUS...)

High parallelism and multilevels

Trigger Rate

Basic building blocks:

e μ jet $p_{t\ miss}$ signatures

Basic selection:

rough particle id. and E_t thresholds

INCLUSIVE RATES

Muons

full rate (12 λ Pb)	10^5 - 10^6 Hz
$p_t > 20$ GeV	$2 \cdot 10^3$ Hz
$p_t^{1,2} > 20$ GeV	25 Hz

Electrons

$p_t > 20$ GeV (10^2 rej.)	10^5 Hz
($p_t^{\pi 0} > 20$ GeV: $2 \cdot 10^4$ Hz)	
$p_t^{1,2} > 20$ GeV	10^3 Hz
(but x10 MC uncert. for $p_t^{jet} \approx 20$ GeV)	

Jets

$p_t^{1,2} > 180$ GeV (or $m_{1,2} > 400$)	10^4 Hz
$p_t^{1,2} > 300$ GeV (or $m_{1,2} > 800$)	10^3 Hz

Missing p_t

$p_t > 50$ GeV (cracks, 3-jets only)	10^3 Hz
(but increase > x10 from 2-jets)	

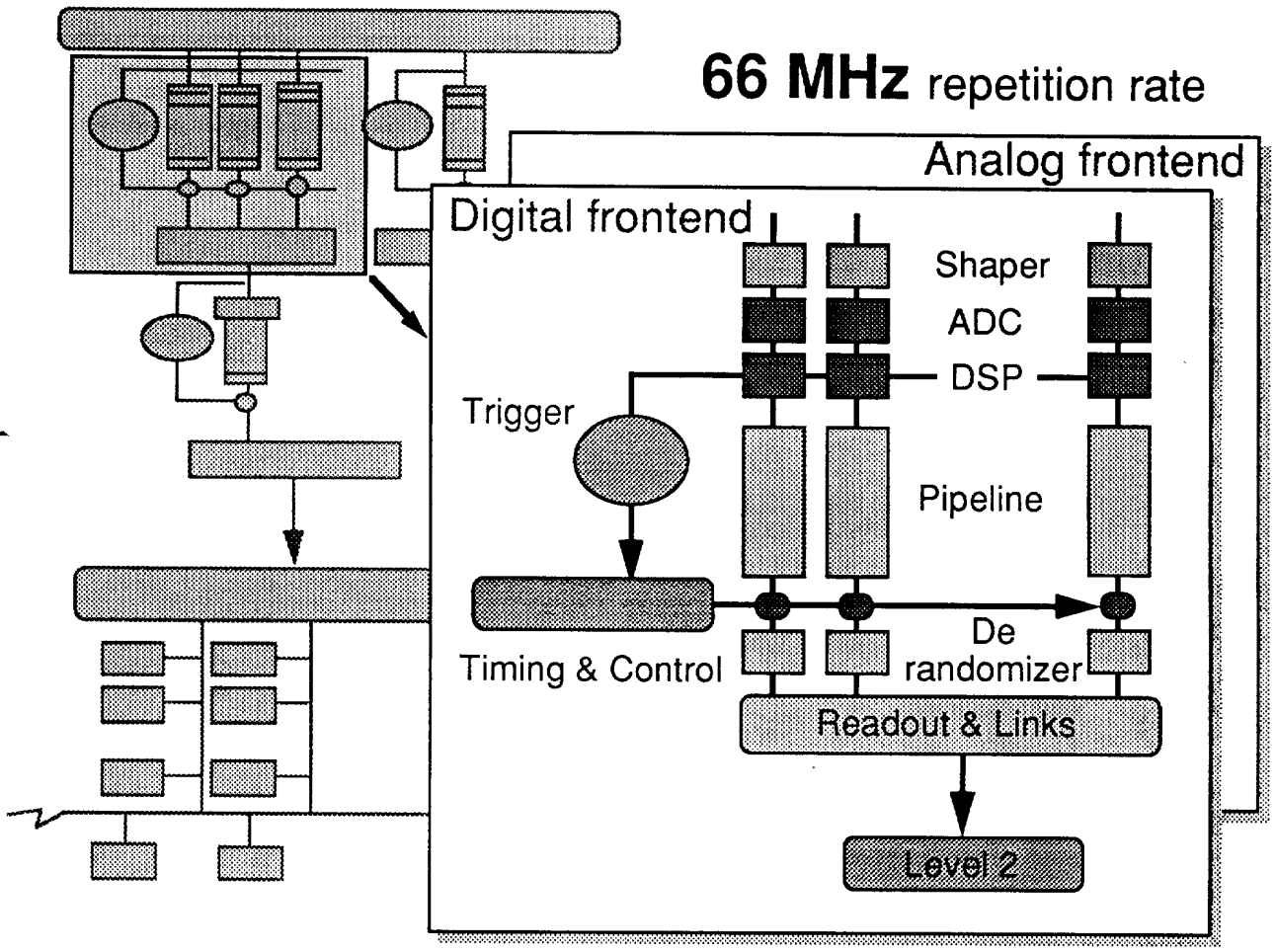
Trigger Rate

Rates from examples of physics channels.

Top		
l + jets	$p_t^{\mu} > 40$ GeV	200 Hz
	$p_t^{e} > 40$ GeV	$5 \cdot 10^4$ Hz
e + μ	$p_t^{\mu} > 50$ GeV	100 Hz
	$p_t^{e} > 50$ GeV	400 Hz
Higgs		
4 l	$p_t^{2\mu} > 20$ GeV	25 Hz
	$p_t^{2e} > 20$ GeV	10^3 Hz
e ν j j	$p_t^{e} > 100$ GeV	15 Hz
SUSY		
p_t^{m}+jets	$p_t^{3j} > 200$ GeV	500 Hz
4 l +jets	$p_t^{2\mu} > 30$ GeV	10 Hz
	$p_t^{2e} > 30$ GeV	10^2 Hz

LVL-1 rate 10^4 - 10^5 Hz

Frontend

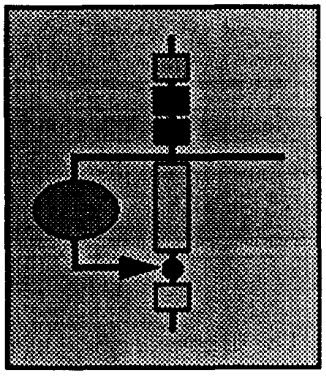


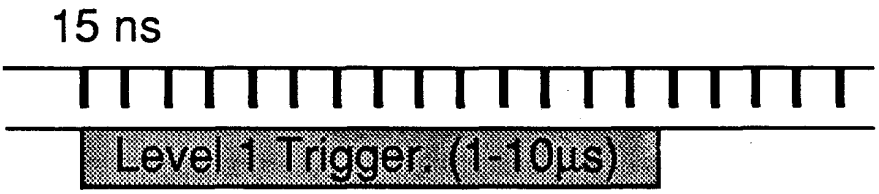
Frontend main challenges :

- Analog to Digital Converters
- Pipelined readout structures (Analog/Digital)
- Digital Signal Processing
- Systolic trigger and data flow processor systems
- Data access, Control and Calibration

- Power, radhard, cabling, packaging

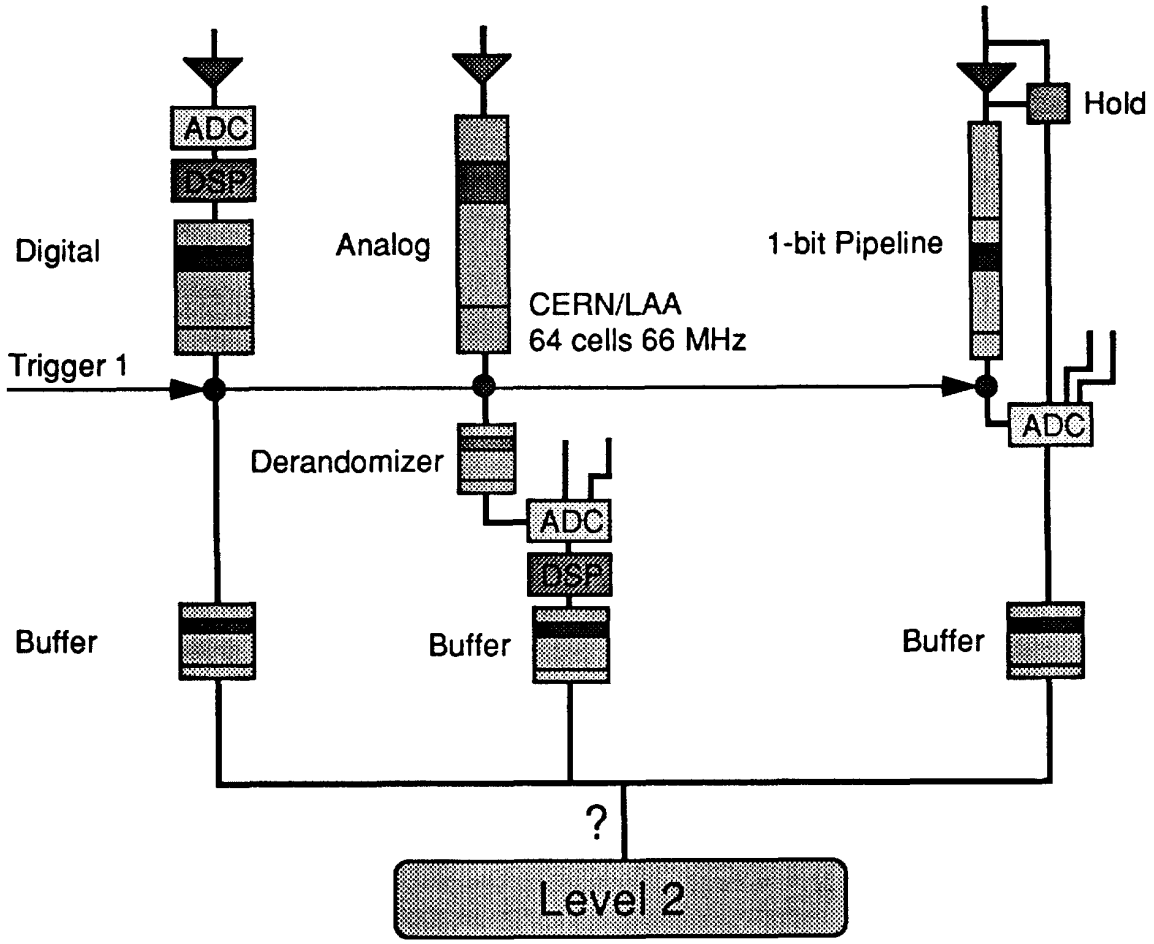
Pipelines





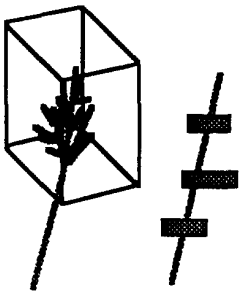
- Long pulse (> 15ns)
- Large dynamic range
- High (≤12 bits) resolution

- Fast pulses (<15ns)
- Low occupancy detecto
  (N•Occ <<1)



LHC Trigger Levels

Level 1. Particle identification & energy cuts



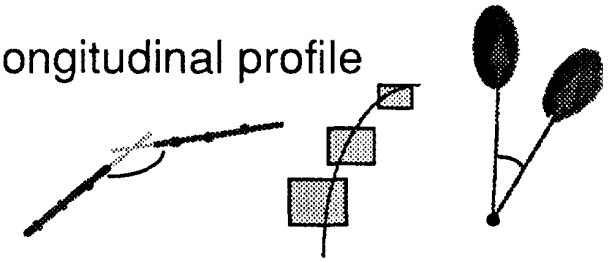
- High p_T electron, muon, (jets), (and missing E_T)
- Energy sums and cuts
- Local pattern recognition and energy evaluation on prompt macro-granular information

Reduction $\approx 10^{-5}$

1, 2 e, Jets..	$\approx 10^4$ - 10^5 H:
Top/Higgs/SUSY	$\approx 10^4$ - 10^5 H:
Muons	$\approx 10^5$ Hz

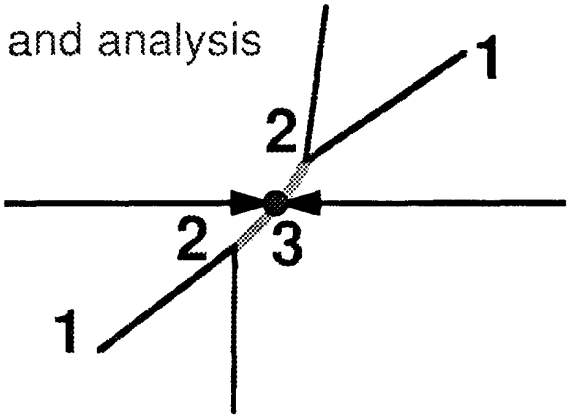
Level 2. Clean particle & kinematics signature

- Finer granularity transversal and longitudinal profile
- Kinematics cuts
- Track reconstruction
- Detector matching and topology



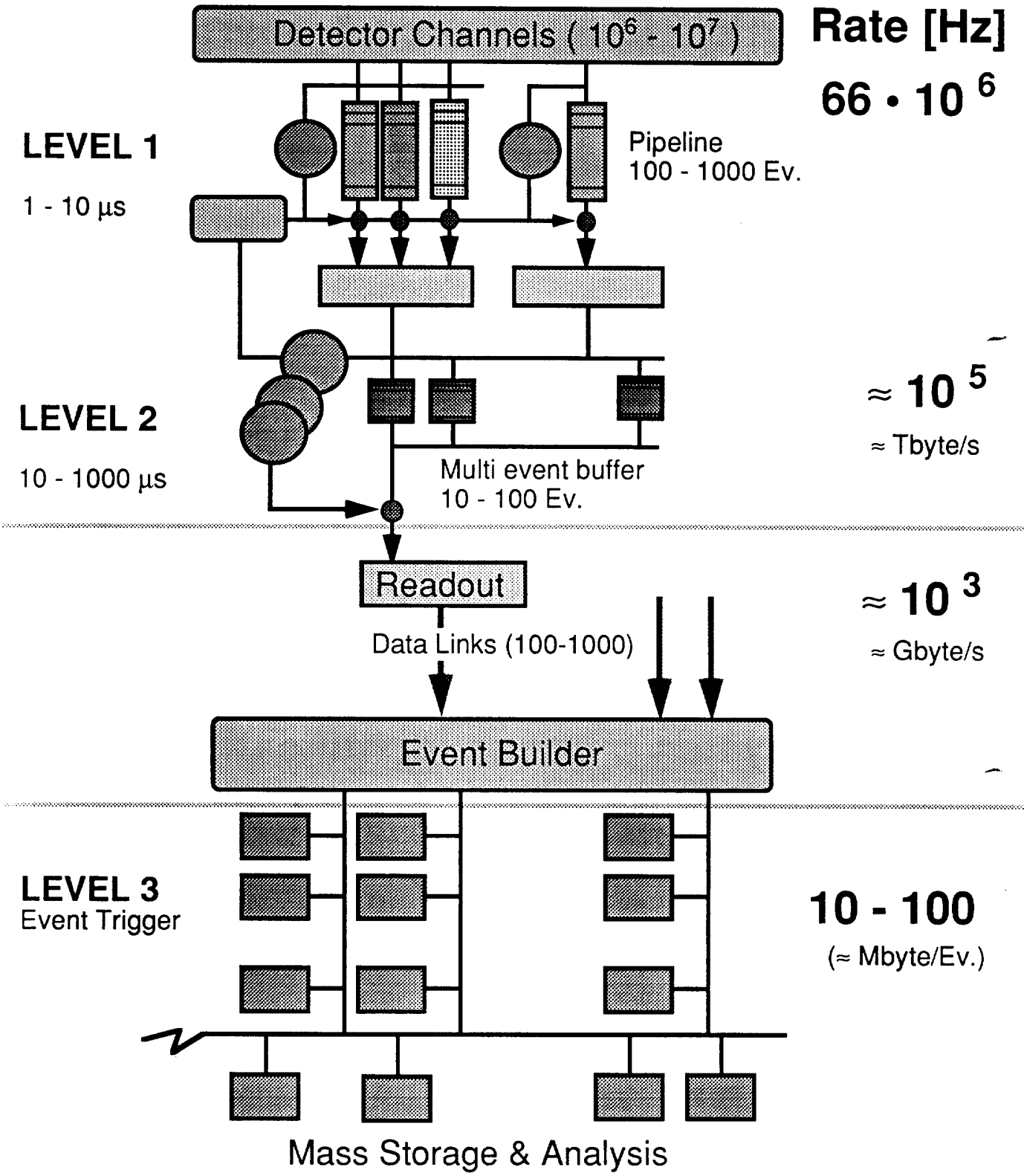
Level 3. Physics process identification

- Event reconstruction and analysis

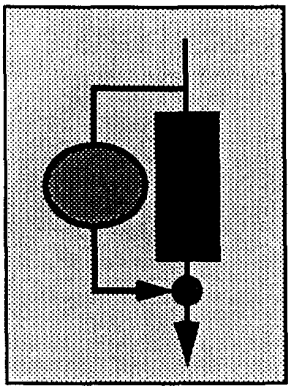


The data acquisition system is modeled by the trigger strategy

LHC General-Purpose DAQ

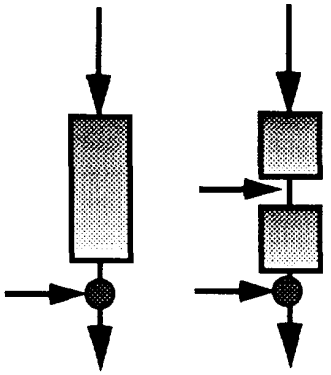


Pipeline



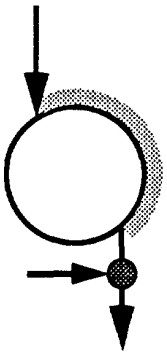
In order to have a zero-deadtime trigger all channel information must be buffered during the decision time (1 - 10μs) each 15 ns
- Charge, Amplitude (multi crossings)
- Hit tag
- Time
- Digital data

Delay line

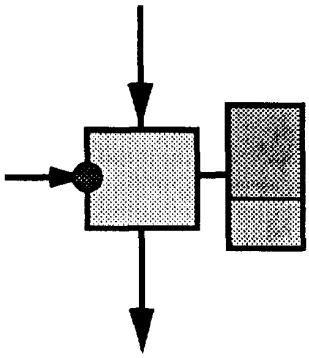


Fixed latency
Synchronous output

Ring Buffer



File system



Variable latency trigger
Asynchronous output

- **Analog or Digital ?**
- **Delay line or random access ?**

Architecture study

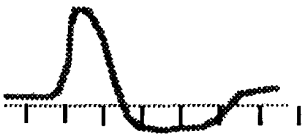
to identify the basic components and confine to a minimum the detector dependent area.

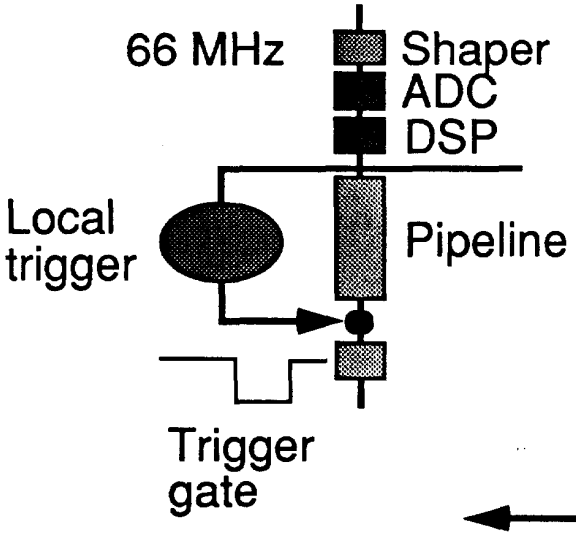
- CERN-LAA HARP project
  3 μm CMOS 64 cells pipeline
- Zeus Calorimeter. 64 Cells 10MHz
- Acoustic Charge Transport delay line..

Today's Pipelines

The frontend of a drift time detector (e.g. Icarus) readout has several aspects in common with an LHC calorimeter channel. Both systems need signal conversion and pipeline. Signal processing and zero-skipping are common as well although the timing and synchronization are tighter for LHC.

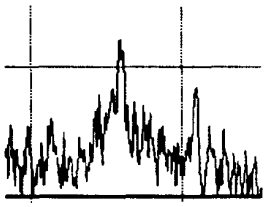
LHC calorimeter

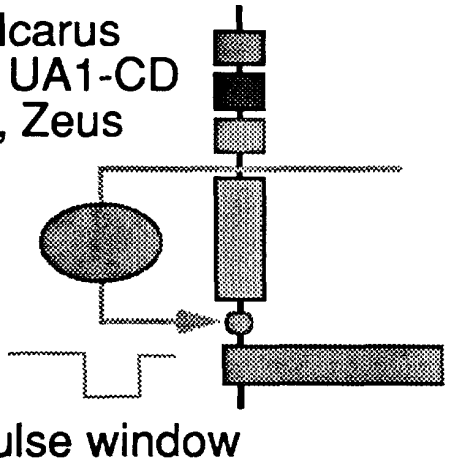




- Bunch crossing (66 MHz)
- Pipeline
- Digital signal processing
- Systolic local prompt trigger

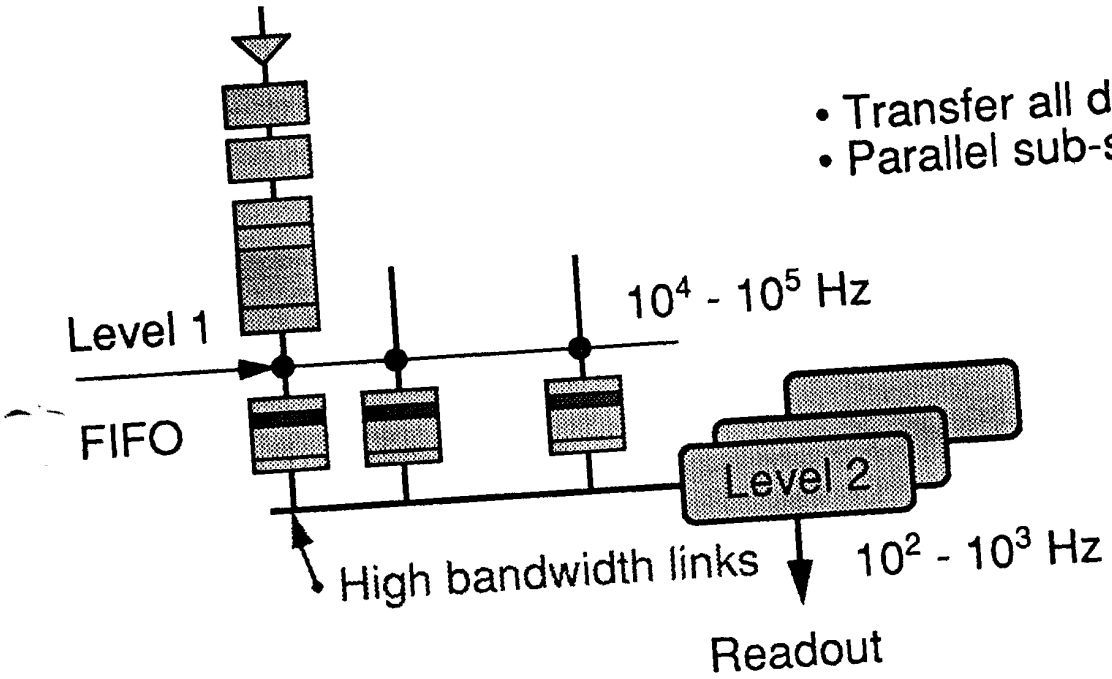
Drift time pulse

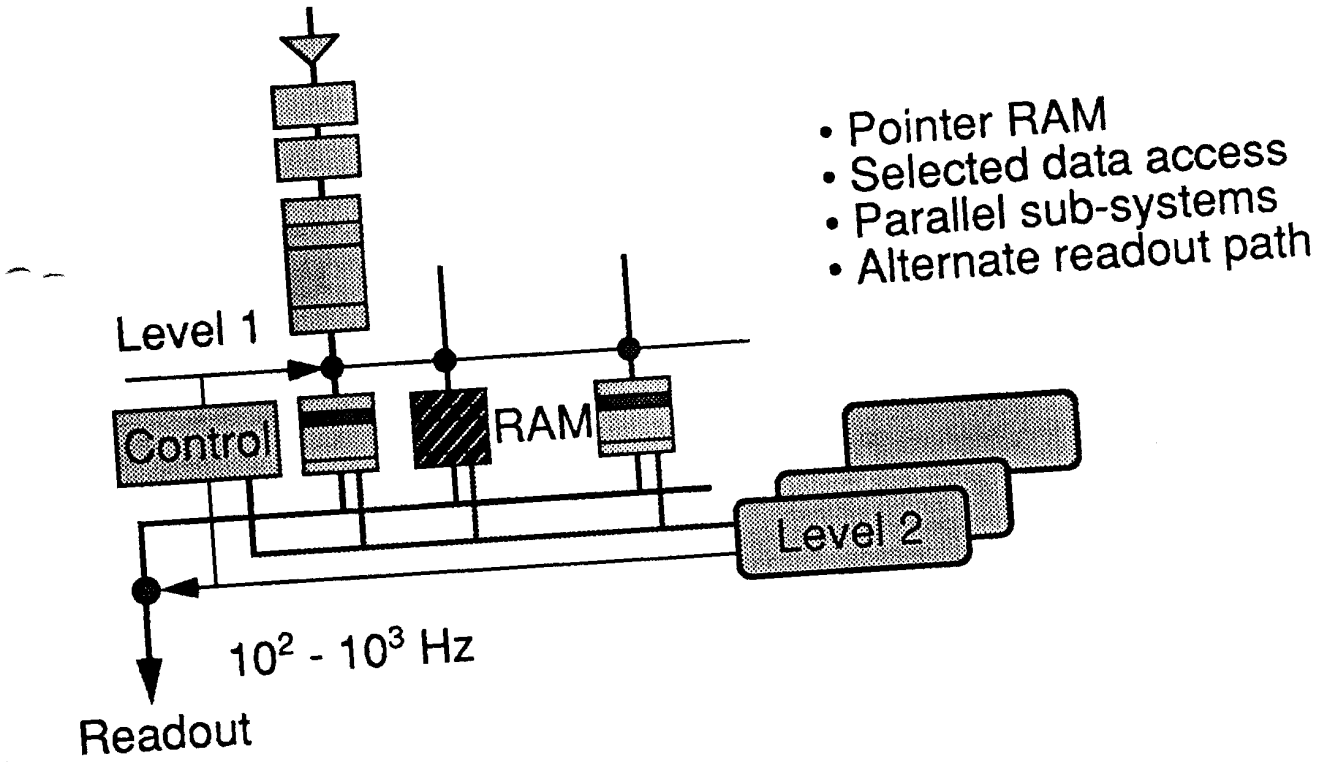




- Sampling rate
- Image readout
- Hit processing
- Track segment finding

Level 2 Data Access



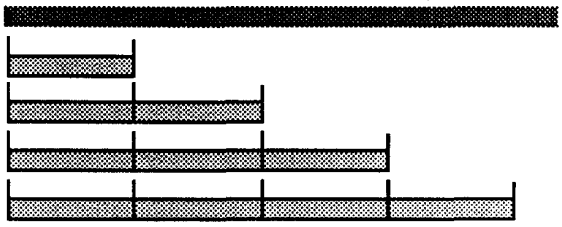


Digital Conversion

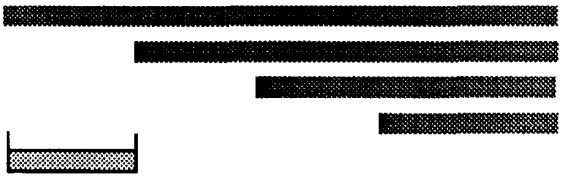
Digitizing means measuring something (charge, amplitude, time..) that is compare it with a reference unit.

Entity to be measured

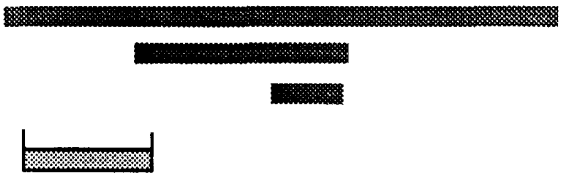
Ruler unit



Compare entity with a series of rulers in sequence (standard ADC, counting)
or in parallel (FADC, decoding)

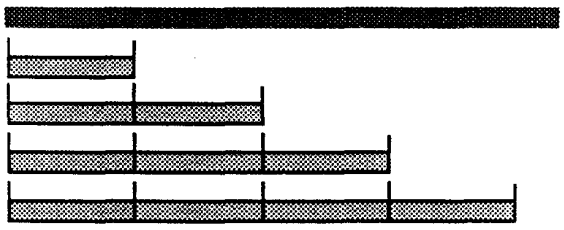


Compare entity with a ruler, subtract ruler from entity (Sigma Delta ADC)



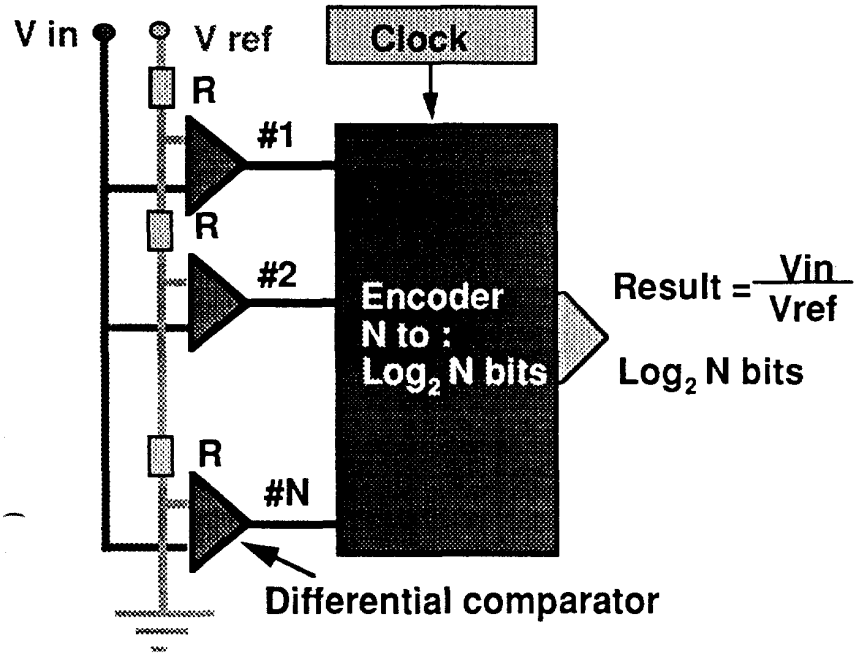
Compare entity with a ruler then subtract ruler from entity and halve the result (HARP pipeline ADC)

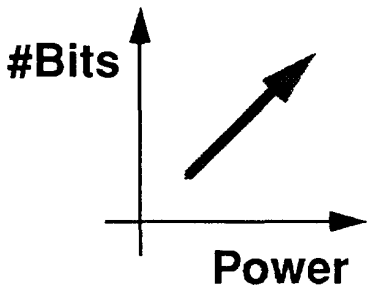
Flash ADC



Compare entity with a series of rulers in sequence (standard ADC, counting)
or in parallel (FADC, decoding)

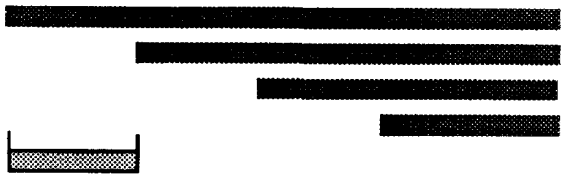
Flash ADC





Dynamic range	critical for	Calorimeter (15-16 bits)
Resolution	"	Calorimeter (9-10 bits)
Power consumption	"	Inner detectors
Speed	"	All (n• 67MHz n≥1)

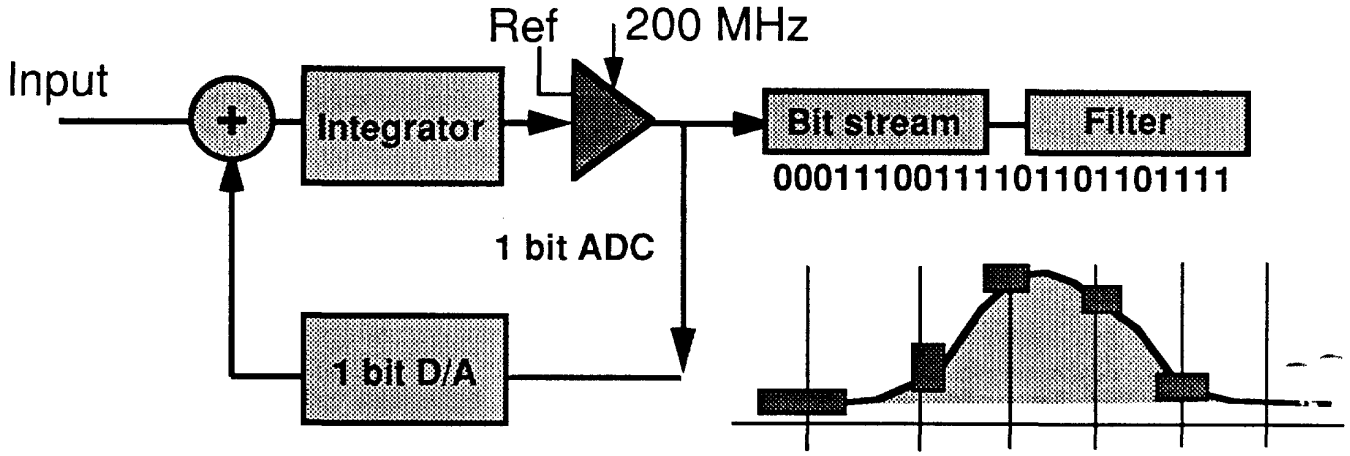
Sigma Delta ADC

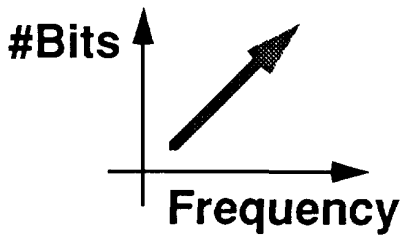


Compare entity with a ruler,
subtract ruler from entity
(Sigma Delta ADC)

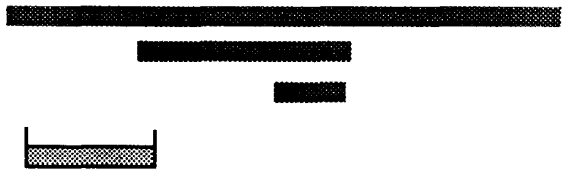
Sigma Delta ADC

(CERN-LeCroy) 9-14bit ≈ MHz



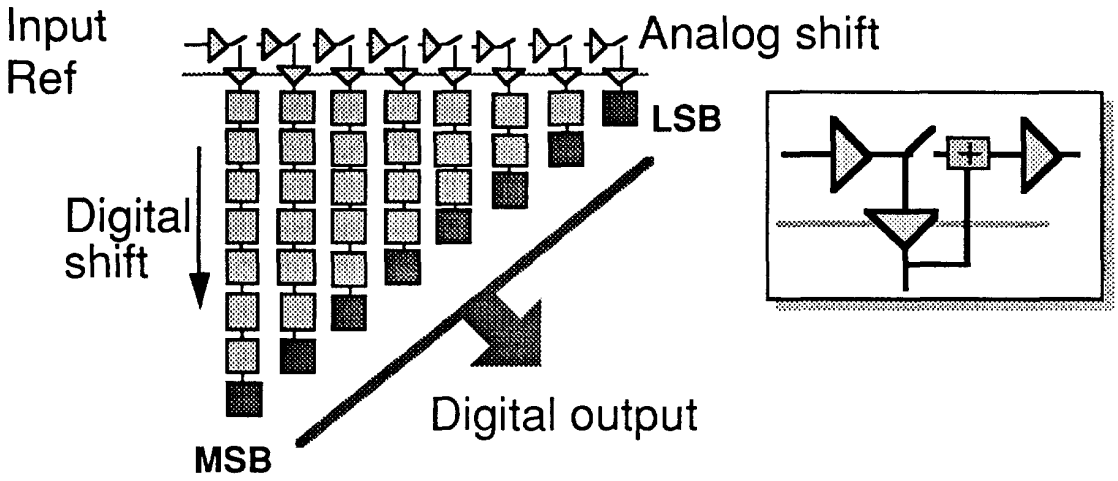


Pipeline Conversion

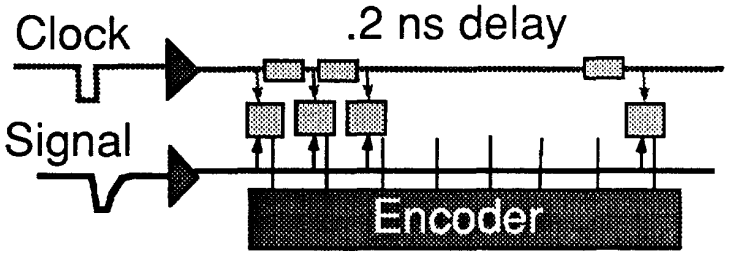


Compare entity with a ruler
then subtract ruler from entity
and halve the result
(HARP pipeline ADC)

ADC pipeline (CERN-LAA HARP) 12 Bits 1MHz

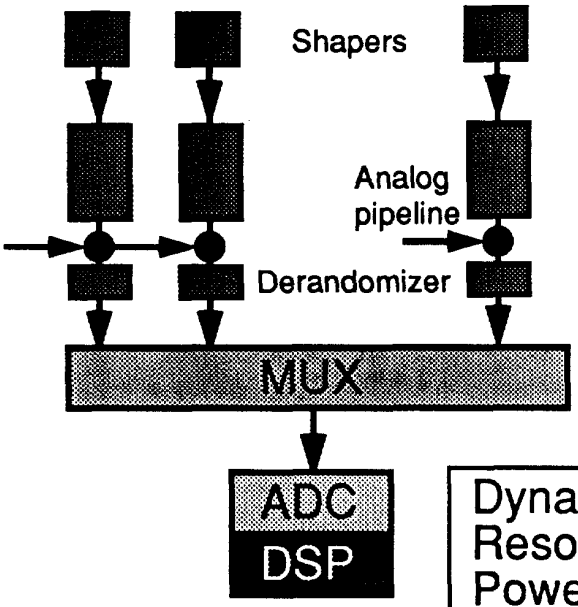


Time Memory Cell (KEK/Hiroshima/NTT)



Digital output

Frontend Configuration



Shape/Analog Store/Digitize

- Power dissipation
- Packaging

- Dynamic range
- Clock driven
- Calibration & Timing
- Radiation hardness

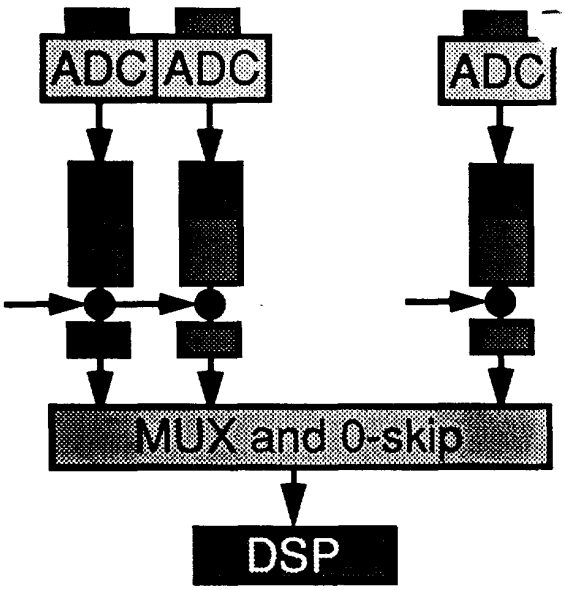
Dynamic range	Cal. (15-16 bits)
Resolution	Cal. (9-10 bits)
Power consumption	Inner detectors
Speed	All (n• 67MHz n≥1)

Digitize/Digital Buffer/Process

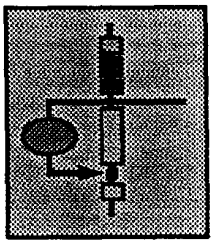
- Digital signal analysis
- Timing and synchronization
- Data driven
- Radiation hardness

- Power dissipation
- Cabling

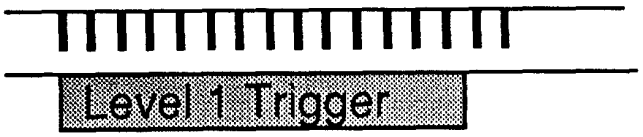
Design of electronics is related to the engineering of the detectors



Trigger Architectures



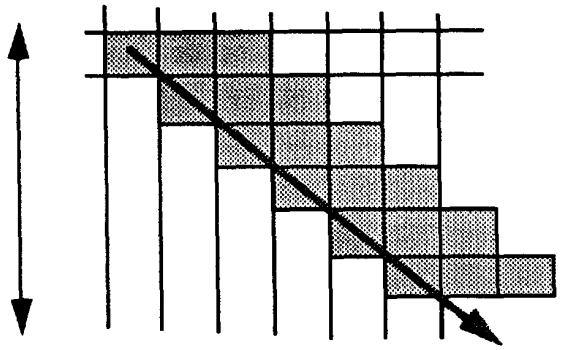
Level 1 trigger.



Scope
- Segment finding
- Energy clustering
- Energy Sums

Techniques
- Analog processors
- Systolic processor arrays
- Associative memories
- Data driven processors

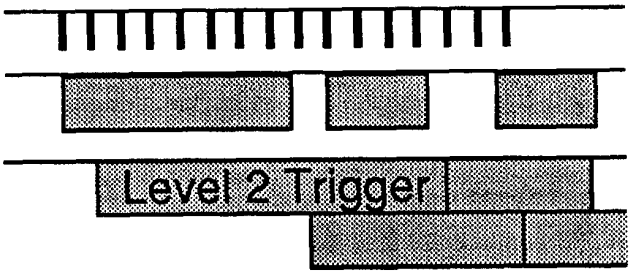
Full pipeline. Step = 15 ns



1 - 10μ Trigger latency One ev

Level 2 trigger

Asynchronous processor systems

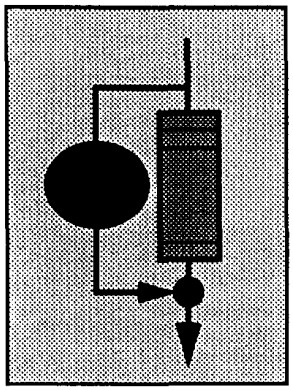


- Pixel processors
- Neural nets
- μP farms
- Data flow architectures

- Full calorimetry
- Track reconstruction
- Kinematics
- Detector matching

Level 1 Trigger

66 MHz



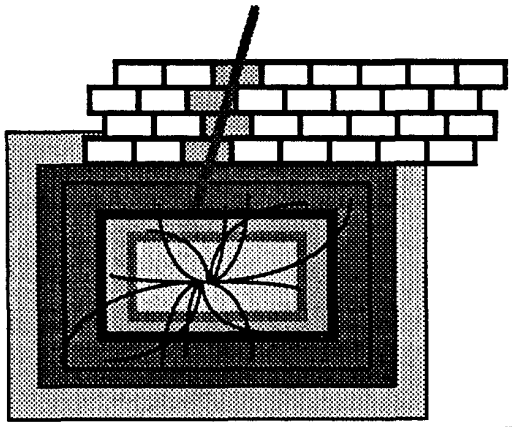
≈100 kHz

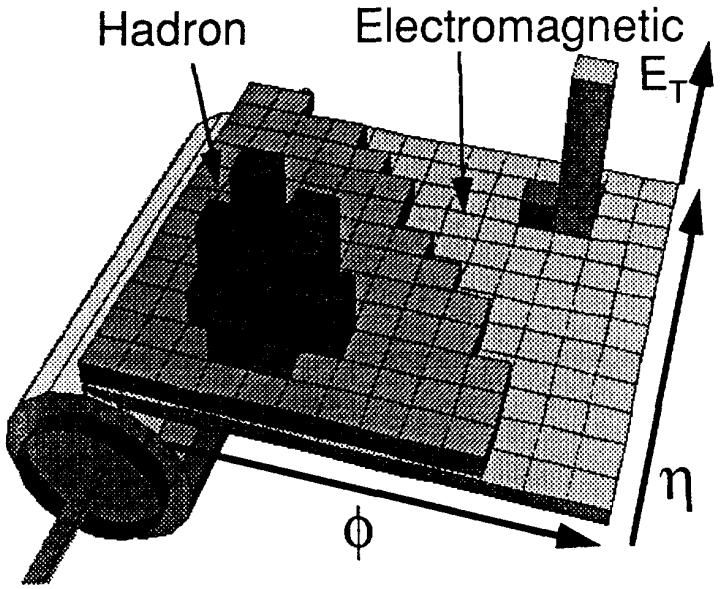
Particle signatures :

- Electron, muon, jets identification
- Energy clusters and sums
- Missing p_T

- 66 MHz
- ≈ 1 - 10 μs latency
- ≈ 10-4 reduction ratio

Track segment recognition
Prompt hits from fast detectors:
(scintillators, TRD, Tubes..)



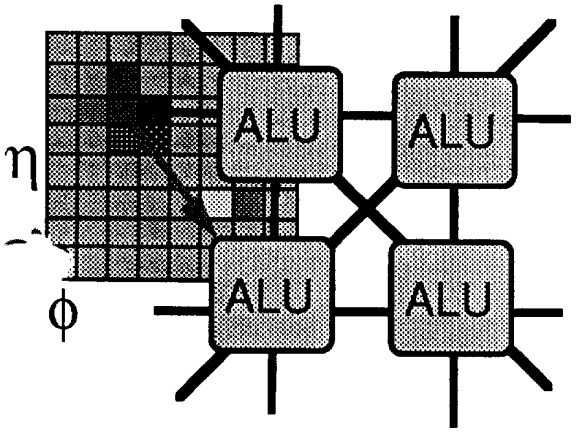


Cluster finding & Energy cuts
on pseudo-rapidity/azimuth
'Lego' plots made of calorimete
2-D e/h segments of suitable
granularity .

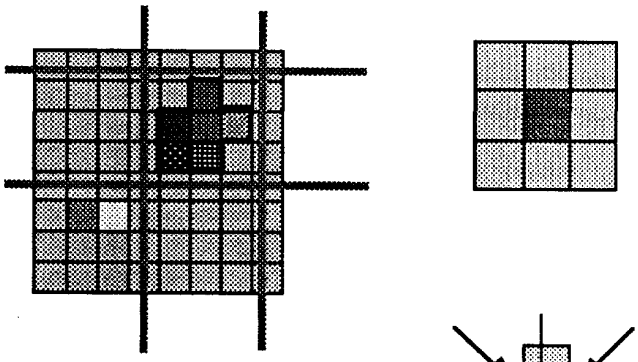
Calorimetry

Clustering in the η/ϕ 'Lego' plot.

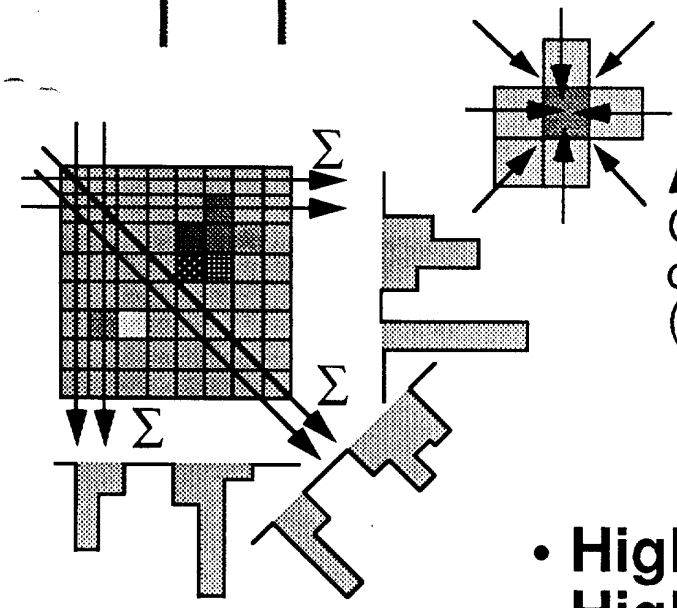
- EM showers, Jets, Energy sums, missing p_T



Processor net mapped onto data plot. Clustering and energy sums done by parallel/pipelined logical and arithmetical units
(Id. UA1. N. Ellis, J. Garvey)



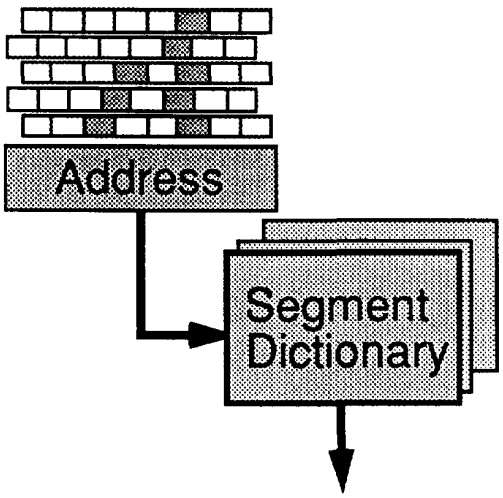
Pixel processor applied in a defined region.
(CERN-LAA MaxVideo)



Analog automata
Clustering by energy sums or by contiguity rules.
(Preshower em. id., R. Bonino)

- **High parallel processing**
- **High connectivity**
- **Applied Specific IC. ASIC**

Tracking



Lookup table

The hit pattern is used as address.
Simple control, but large memory size
(UA1. Muon cone finding ≈2μs)

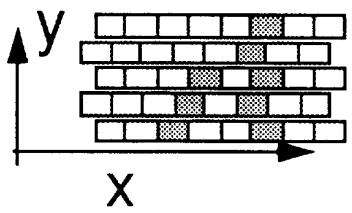
Associative memory

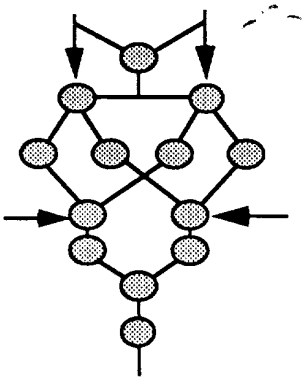
Memory is addressed by its contents.
Large control, limited memory size
(CDF. Segment & track finding 1-10μs
ASP massive digital parallel processors)

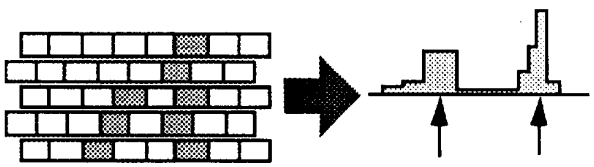
Data Driven

- Flexible structure
- Natural pipeline

Track following algorithms are translated by subsequent steps of arithmetical units driven by the availability of the operands.





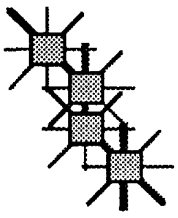


(x,y) Transforms

Hough- parameter, polar coordinates
Trackfinding by (x,y) mapping into an
appropriate coordinate system.
(CERN-LAA. MaxVideo)

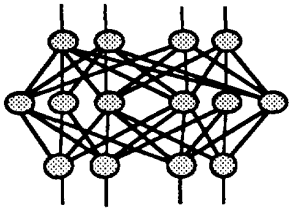
Analog/Digital automata

Find pattern via elementary rules describing the interaction (logical/analog) of contiguous cells



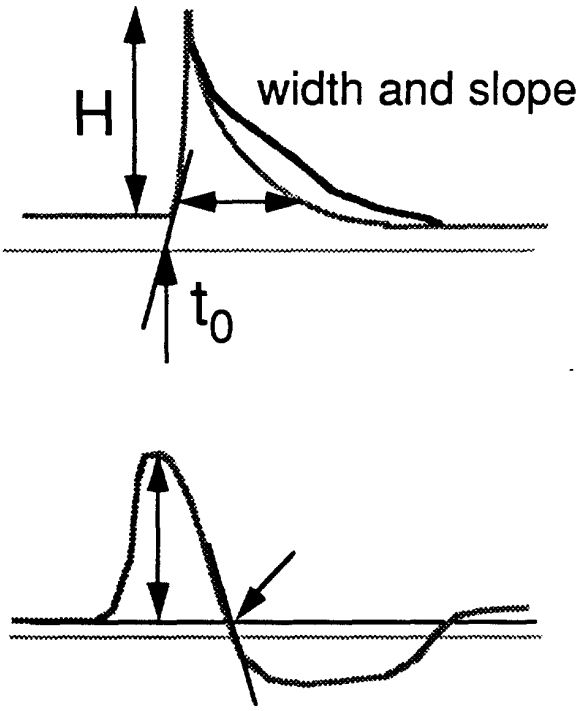
Neural networks

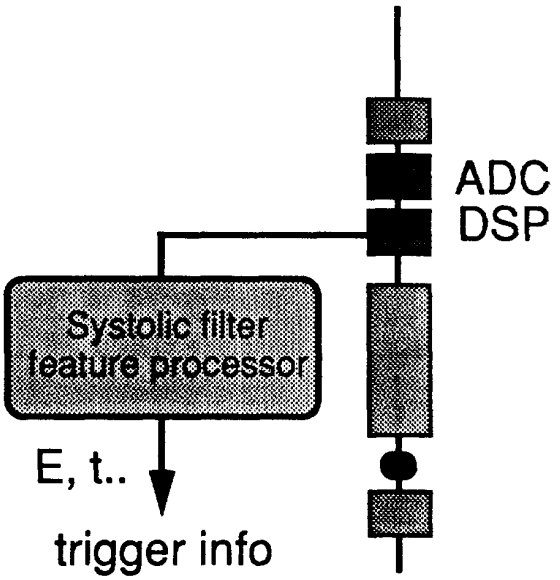
Not algorithmic analog processors trained to classify patterns.
(CDF. Analog INTEL ETANN ≈ 1μs)



Digital Signal Processing

The signals generated by an LHC calorimeter cell will be diffused over more than one bunch crossing. A digital channel with programmable filter capability is needed to extract the physical information and to associate events within bunch crossings.
In addition, for those detectors where the particle (e/π) can be identified by the signal shape in a single channel, the digital analysis can perform the first step of the trigger process.
Apart from considerations of power consumption, electronics packaging and radiation hardness, it seems very attractive to go digital immediately after the preamplifiers, complementing the analog shaping with a **pipelined digital signal processor**.





Basic filter operation : $\sum \mathbf{x_i} \bullet \mathbf{W}$

Trigger Level 1

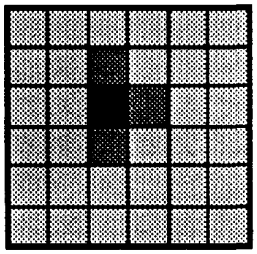
Level 1.

Local object identification and cut on energy sums. (e, μ, jets, track segments)

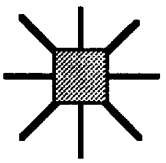
Each trigger subsystem is local to a part of the detector and it will be limited to flag events by cuts on the sums of energy over contiguous calorimeter cells or by recognition of a track segment in a binary matrix.

For a deadtimeless first level trigger, the trigger processor must itself operate as a **pipeline** at the 66 MHz bunch crossing rate (eg. **systolic processor**).

Multilevel matrix

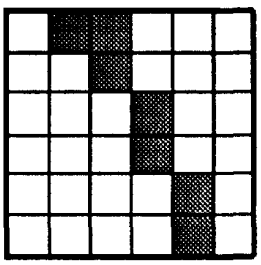


- Cluster pattern recognition
- Multiply / Add
- Cell / processor mapping

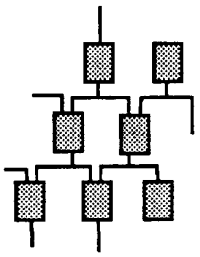


$$\sum x_i \cdot w_i$$

Binary matrix



- Model matching
- Contiguity rules
- High connectivity

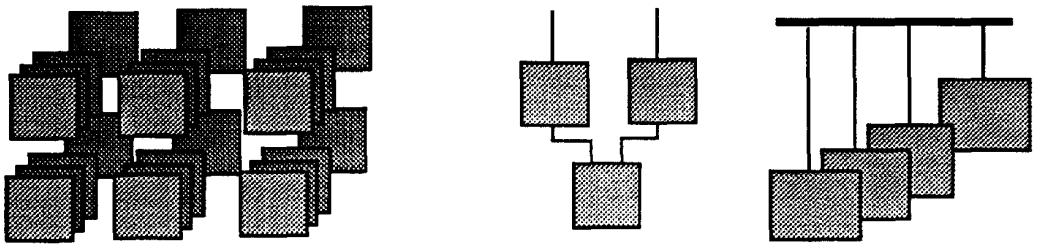


Trigger Level 2

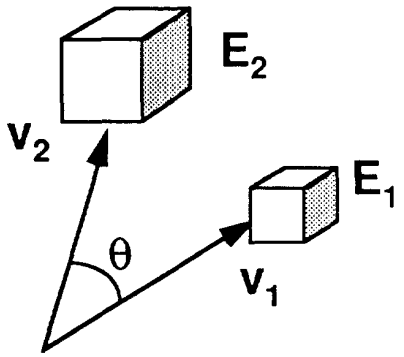
Level 2.

Full measurement and cuts on the kinematics parameters.
Pattern recognition may be still needed (if fine granularity tracking detectors are used)

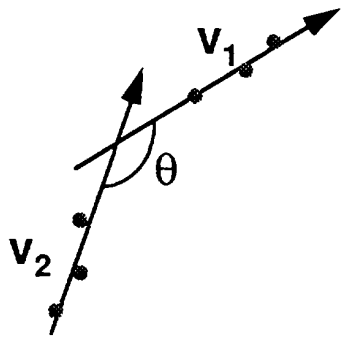
At this level data are locally buffered and the data flow can proceed asynchronously.
The processor architecture can be either **massive parallel** (with asynchronous units) or **data flow** or **farm** based.
(according to amount of data and the data collection architecture)



When the selection is made on kinematical cuts then the basic operation to perform is a 3(4) dimensions scalar product.

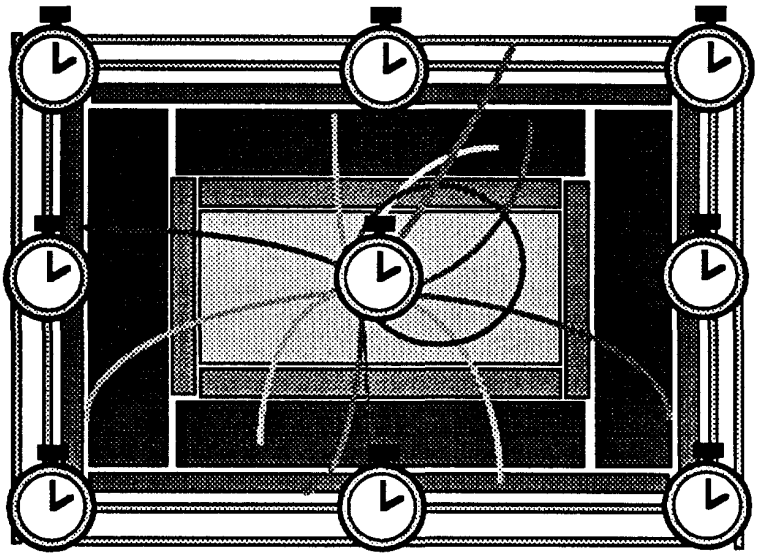


$v_1 \cdot v_2 \rightarrow \sum x_i \cdot y_i$



Sparse data collection and data flow computers

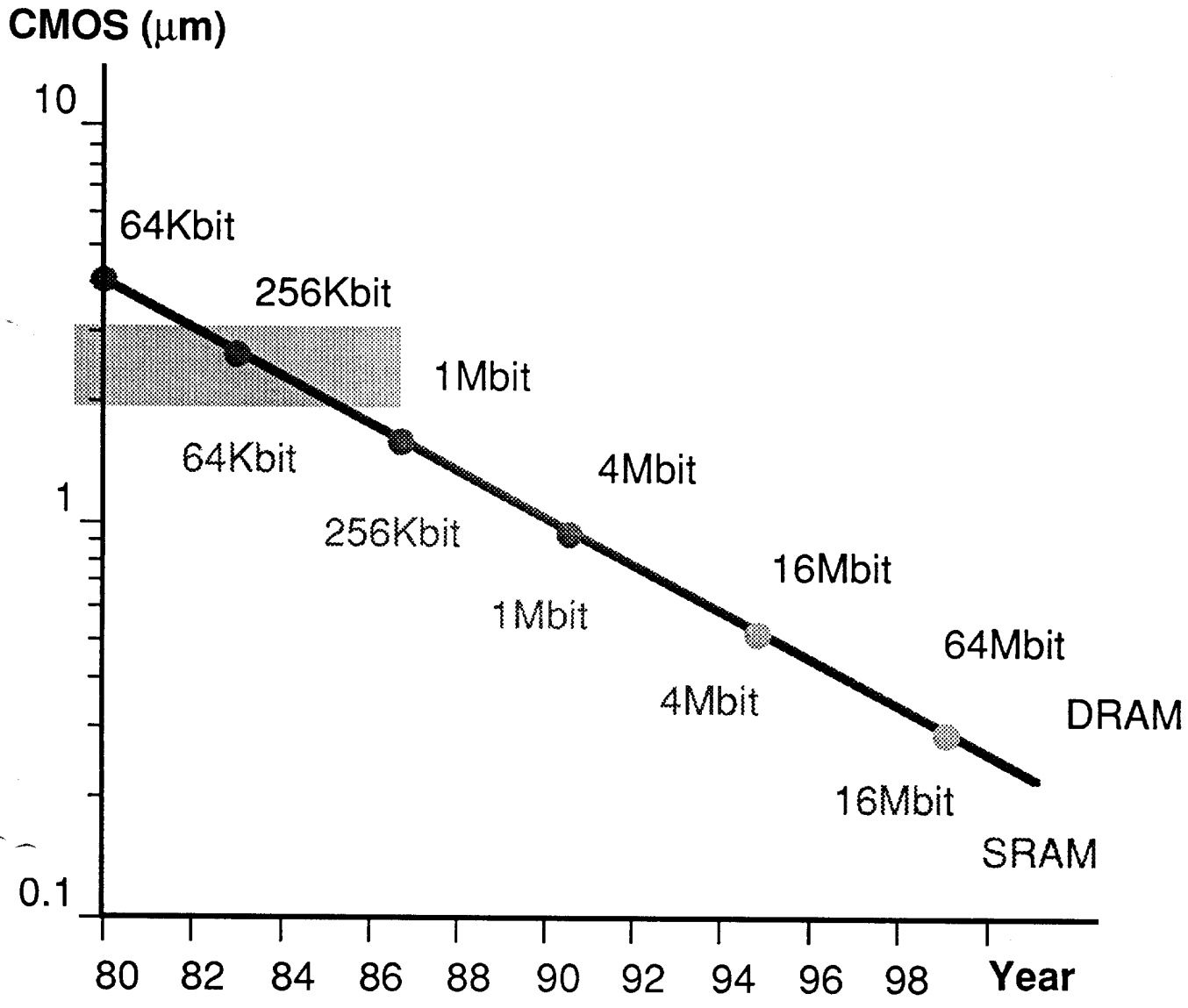
Timing



Bunch crossing timing must be distributed around the detectors.

- **Is this sufficient to identify the data belonging to the same event?**
- **Event identification based on an absolute time tagging (e.g. T_0 from stiff tracks. Mean time measurements...)?**
- **Data driven flow with time info lists ?**

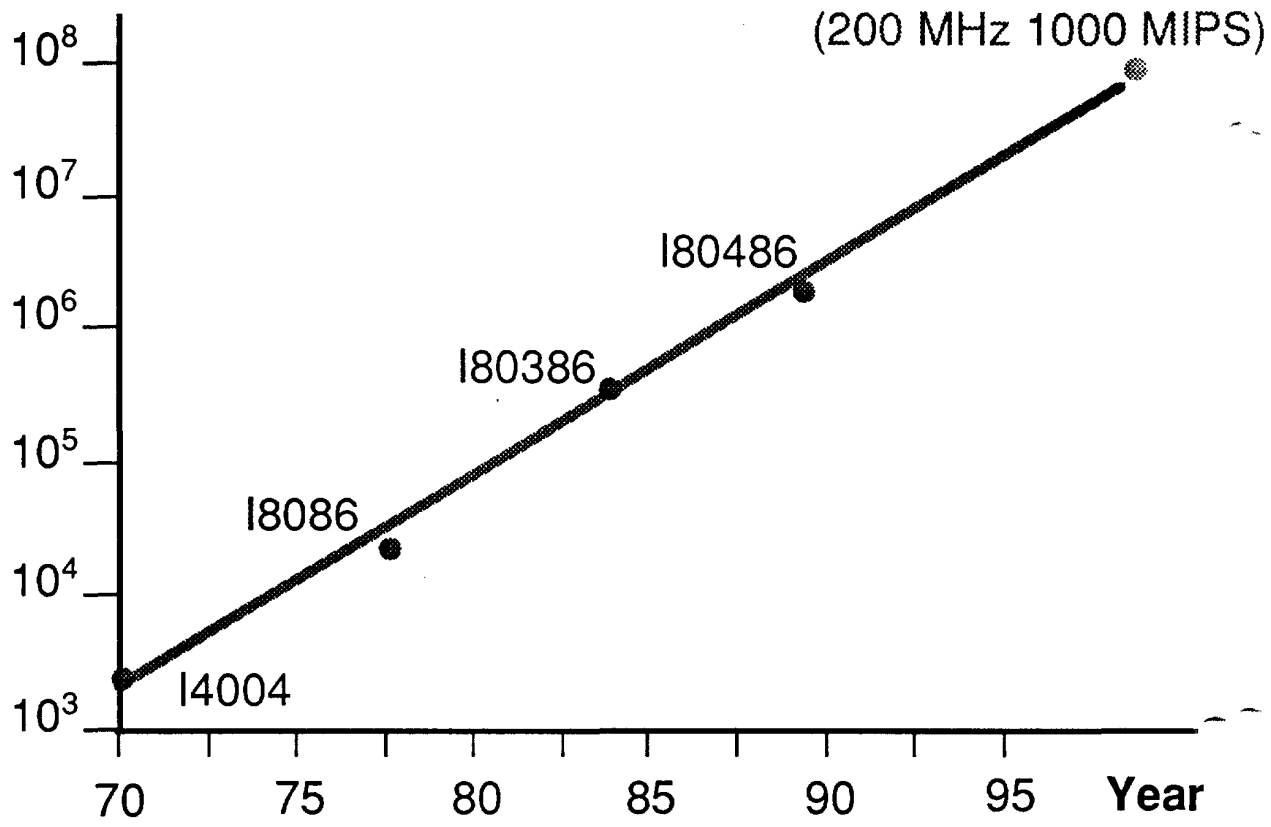
Memory Evolution



Collider/LEP
≈ 10^5 channels
≈ 10^5 byte/ event
≈ 10^5 Hz rate

LHC
≈ 10^7 channels
≈ 10^6 byte/ event
≈ 10^7 Hz rate

No. of Transistors

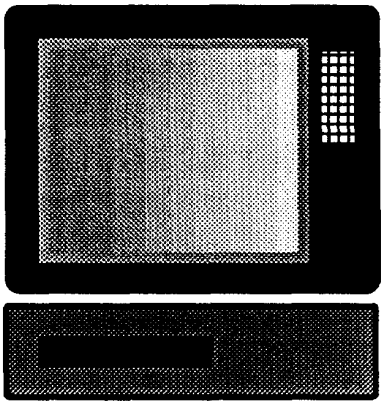


BiCMOS prediction and no assumption of :

- technological changes (GaAs)
- new architectures (massive parallel, neural net)
- new technology
  optical computers, quantum effect electronics

Industry

In the last 20 years, the requirements of to telecommunication and in particular to television have strongly contributed to the development of standard technology (CMOS, BiCMOS) and mass production by industry.
Together with other fields, the high energy physics experiments have exploited these developments extensively.



Flash ADC
Analog memory
Personal computers
Helical scan recording
Data compression
Image processing
Cheap MFlops
for image synthesis

In recent years the world television industry has undertaken a new challenge :

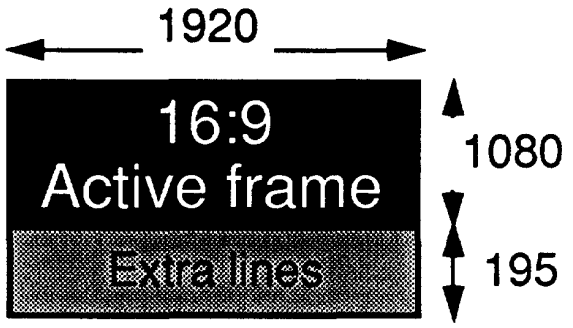
the High Definition TeleVision (HDTV).

This represents a tremendous effort of research and development in the field of standard technology.
In Europe it is organized under the project EUREKA 95.

Eureka 95

Eureka HDTV project EU95

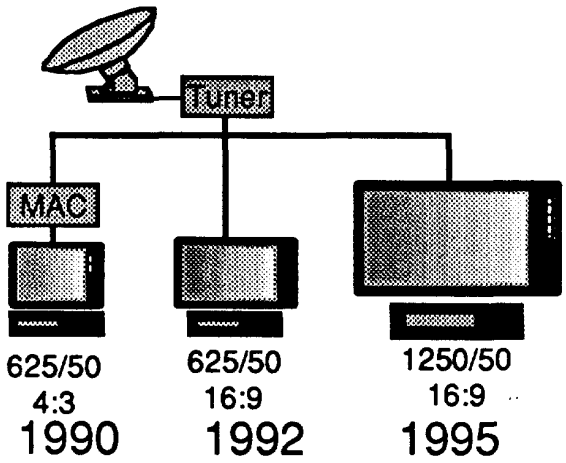
Directorate : Bosch, Nokia, Philips, Thomson
+ 20 firms, universities and national centres
1986 estimated development cost $1 billion
1990 spent $350 million



(8 digital audio channels encoded)

- **50Hz ≈ 1.7 Gbit/s**

Camera sampling rates :
144MHz (36MHz)
luminance(colour)

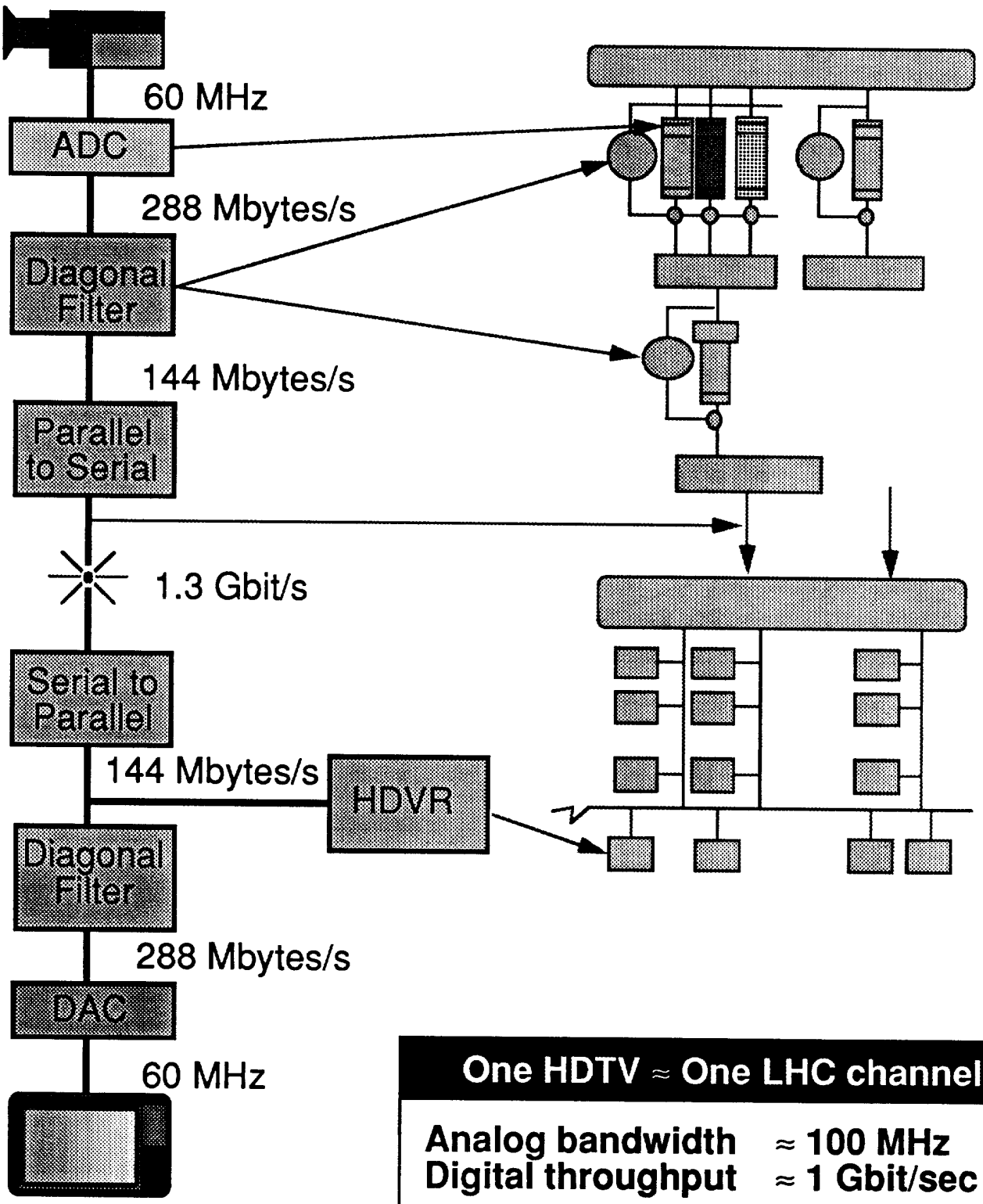


MAC (Multiplexed Analog Components) transmission system. MAC is raster-compatible with PAL/SECAM. A MAC decoder allows the satellite reception on existing B/W and colour sets.

Main areas :

Origination	Production	Transmission	Display	Replay
Fast ADC Pixel proc.	Mass storage CDV	Optical fibres Data compr. TDM time division multipl.	ADC Pipeline Dig. filters	CDV

HDTV chain



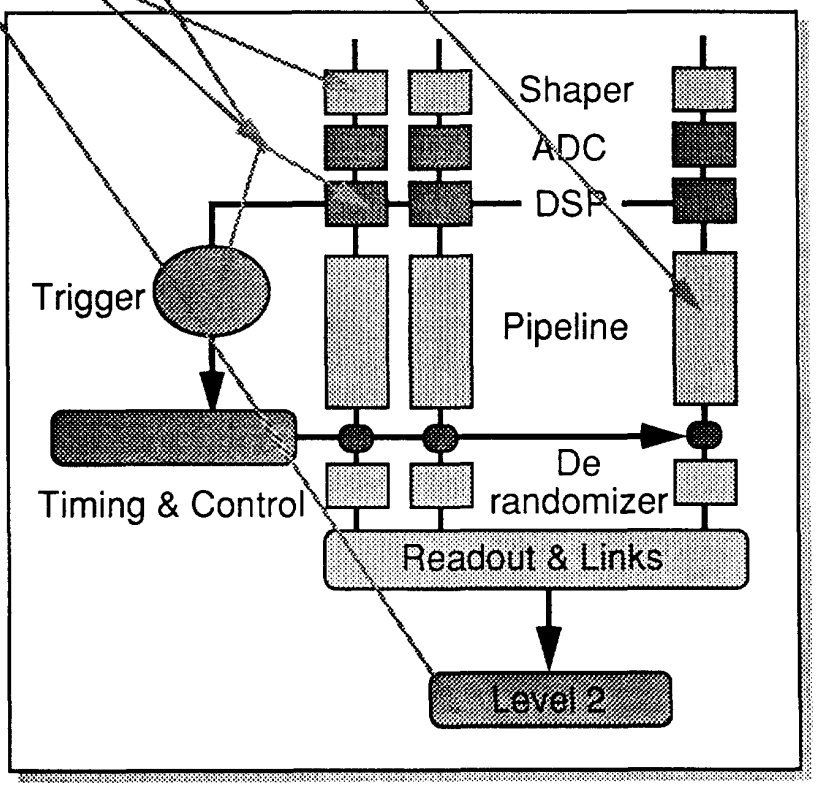
One HDTV ≈ One LHC channel

Analog bandwidth	**≈ 100 MHz**
Digital throughput	**≈ 1 Gbit/sec**

+ more : DSP, Links, Storage .....

HDTV Spin-off

- LRV 16K. Memory delay line. 2048 Bytes 72MHz FIFO
- MULAC8. Transversal filter processor.
  54MHz Systolic array of 8 multiplier/adder 18ns pipeline for real time digital image processing and filtering.
  XOUT(30bits) = Σ XIN(i)•W(i) [10bit•12bit, i=1-8]
  IC prototypes designed and developed by CNET (Centre National d'Etudes des Telecomunictions) in Grenoble in the framework of the HDTV project :
- Dataware ITT. Programmable video signal processor.
  (Σ XIN(i)•W(i)) 4 Giga-OPs. ITT West Germany
- High speed Flash ADC. ...

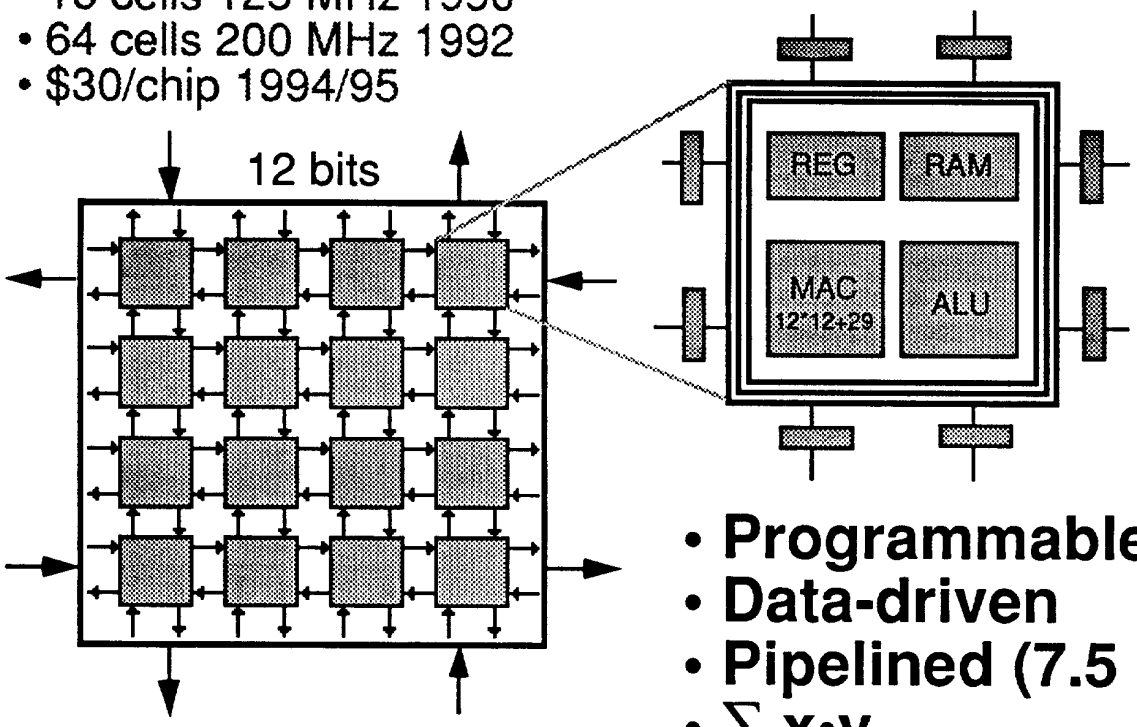


\+ Gbit/s optical links, data compression and mass storage

VSP (DAVIS)

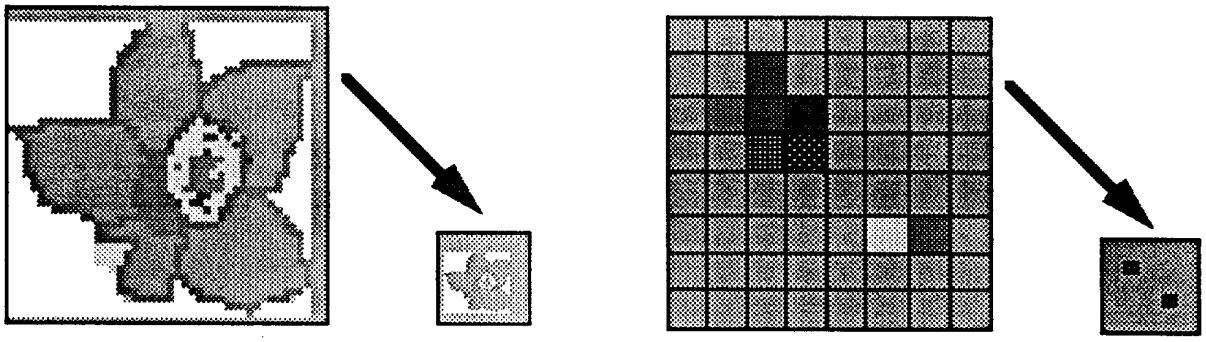
Data Driven Video Signal Processor

- 16 cells 125 MHz 1990
- 64 cells 200 MHz 1992
- $30/chip 1994/95

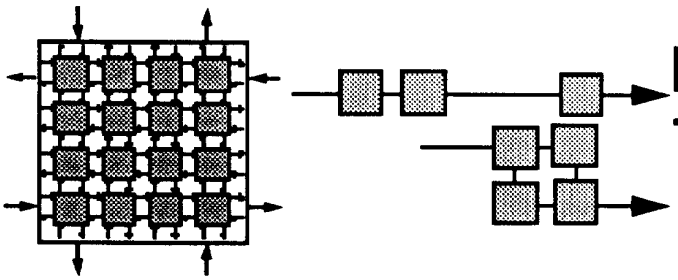


- **Programmable**
- **Data-driven**
- **Pipelined (7.5 ns)**
- **$\sum$ x•y**

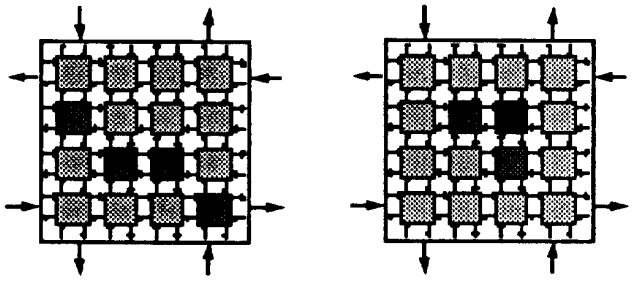
- **1D/2D digital filters and Convolution**
- **Frequency decimation**



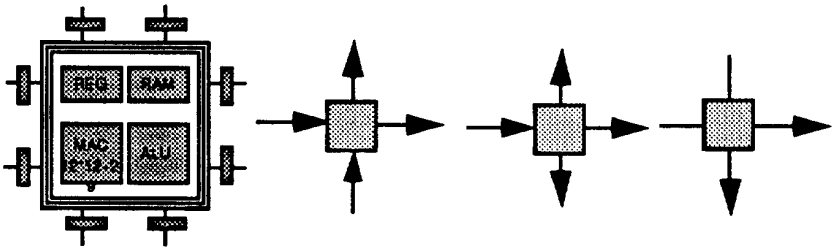
DAVIS



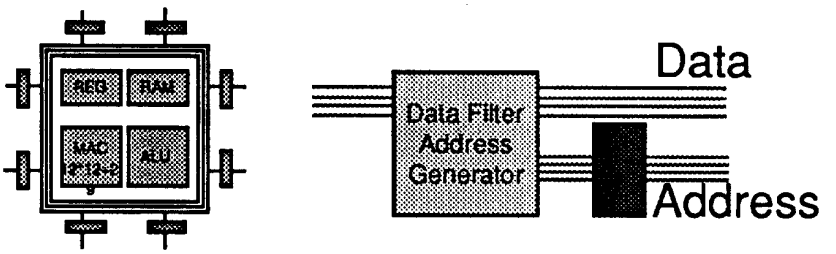
Data Driven processor
1D-2D Digital filters



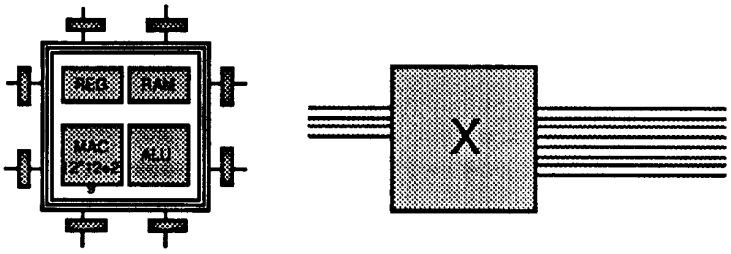
Contiguity Machin
7.5 ns cycle



Bus switch
750 MByte/s peak



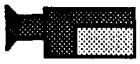
DMA Controller
375 MByte/s

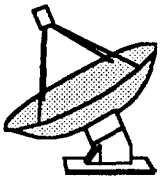


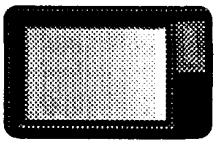
Intelligent
LookUp Table

HDTV

HDTV



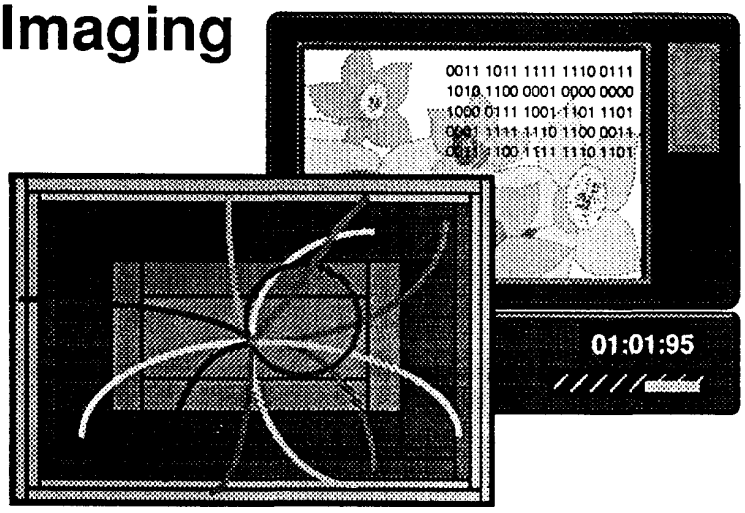




Transmission encoding — 144 MHz, 10bit
Receivers — 16-30 MHz, 10bit

- High speed ADCs
- Mass storage
- Image processors
- Data communications

High Performance Imaging



- Digital filters
- Delay lines
- High speed ADC/DAC

High Energy Physics Multi-Tev calorimetry

60-150	MHz
15 bit	dynamic range
10 bit	linearity
10^{5-6}	channels

A tremendous effort :
Developed by European industry
Exploiting the standard technology

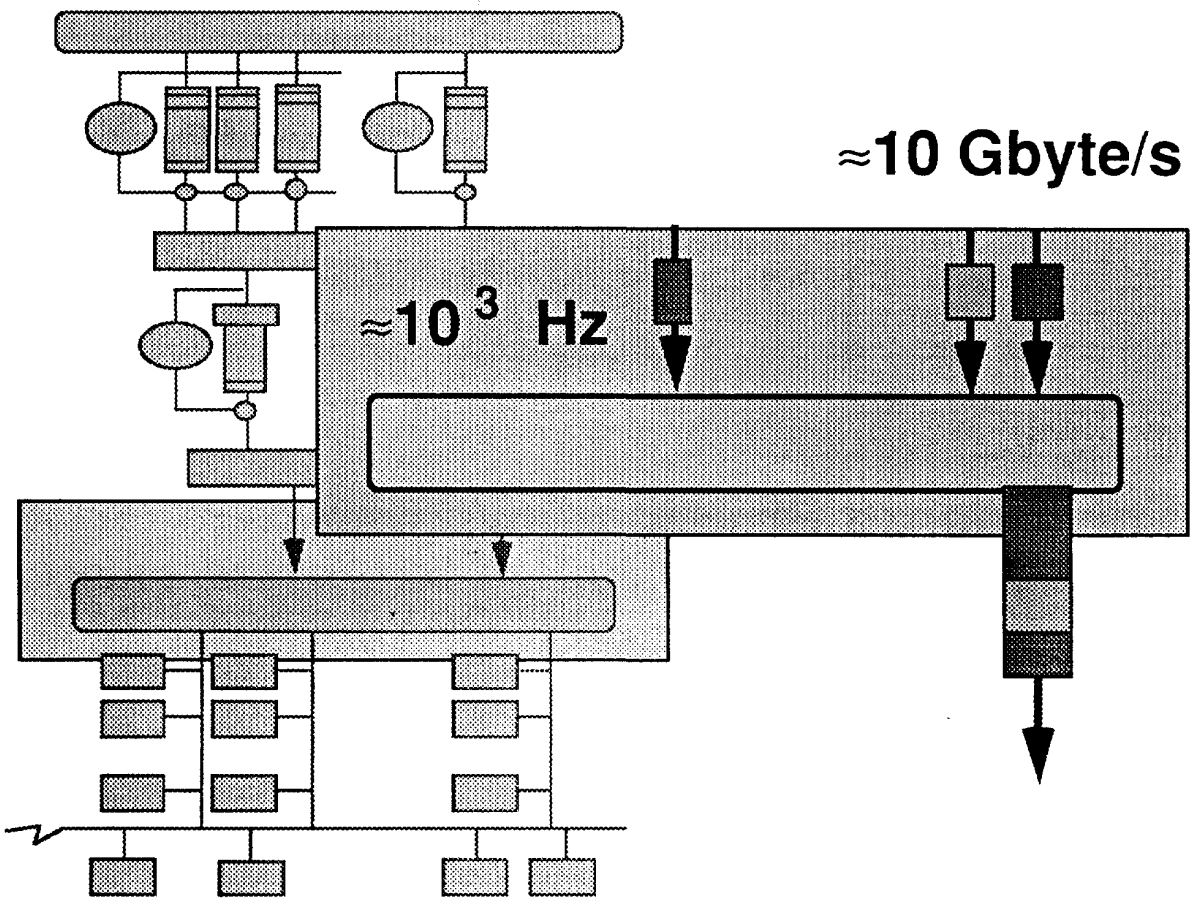
Event Builder

- **Event builder**

It has to perform the merging of multiple sub-detector data streams into a single detector/event data stream in order to be processed by a subsequent trigger level.

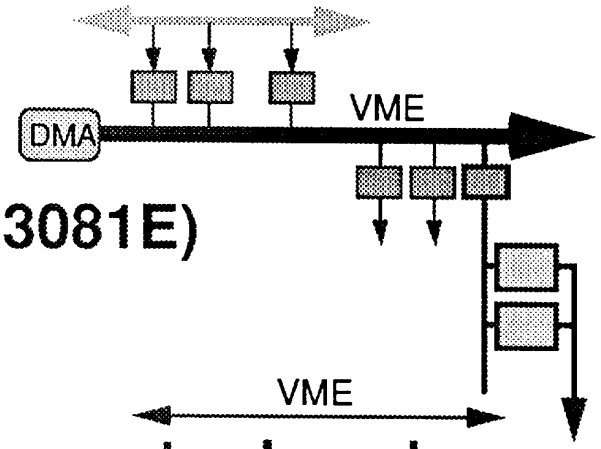
- **Data links & Connectivity**

100-1000 data sources. Optical links

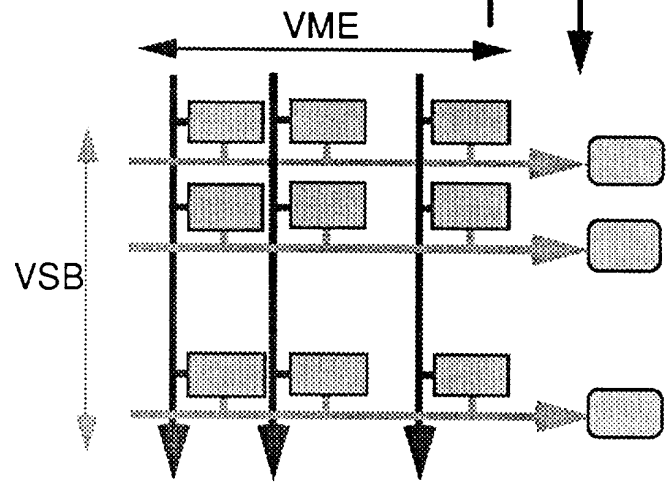


VME-FastBus Event Builders

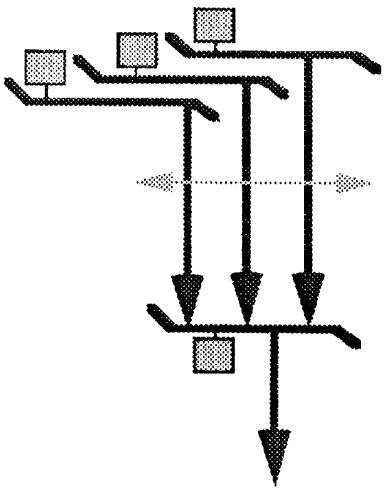
UA1
(CAMAC, VME and 3081E)

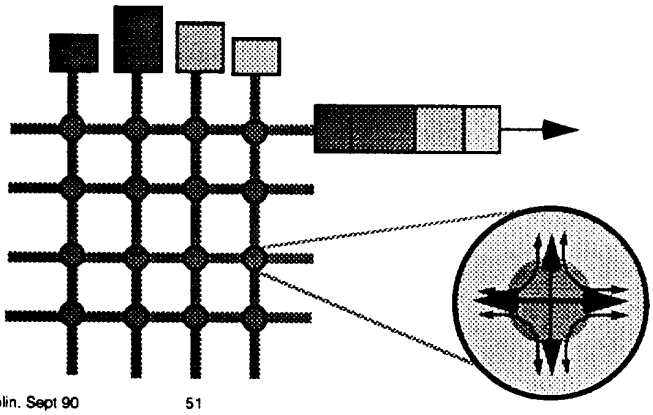


OPAL matrix
(VME/VSB)



ALEPH event mover
(FASTBUS)

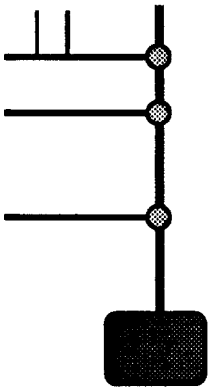




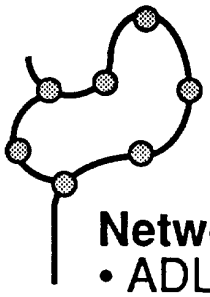
Barrel switch

Bus matrix switch node

Buses

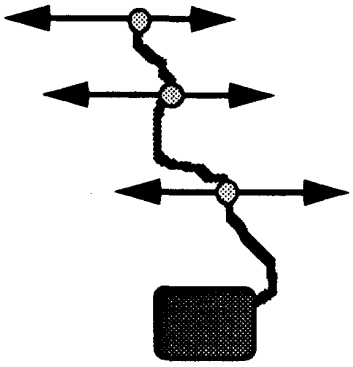


CAMAC/REMUS
- Geographic addressing
- Built in block transfers
- Hierarchical structure

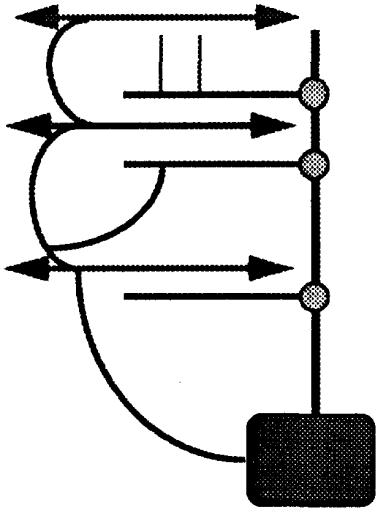


Networks
- ADLC lans
- Token ring
- Ethernet
- FDDI

....



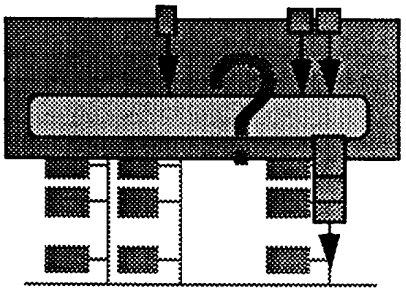
VMEbus, Fastbus
- Multi processor system
- Master/slave
- Logical addressing

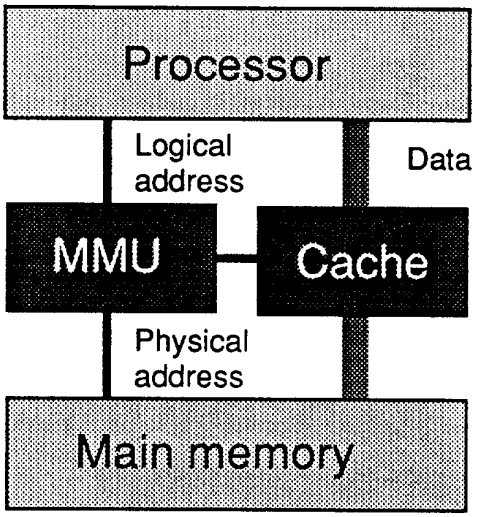


- Preprogrammed data path and auto block movers
- General purpose buses for control and monitoring
- Redundant access

VME 64/256.. VXI
Futurebus
SCI, HIPPI...
(standard protocols and point to point)

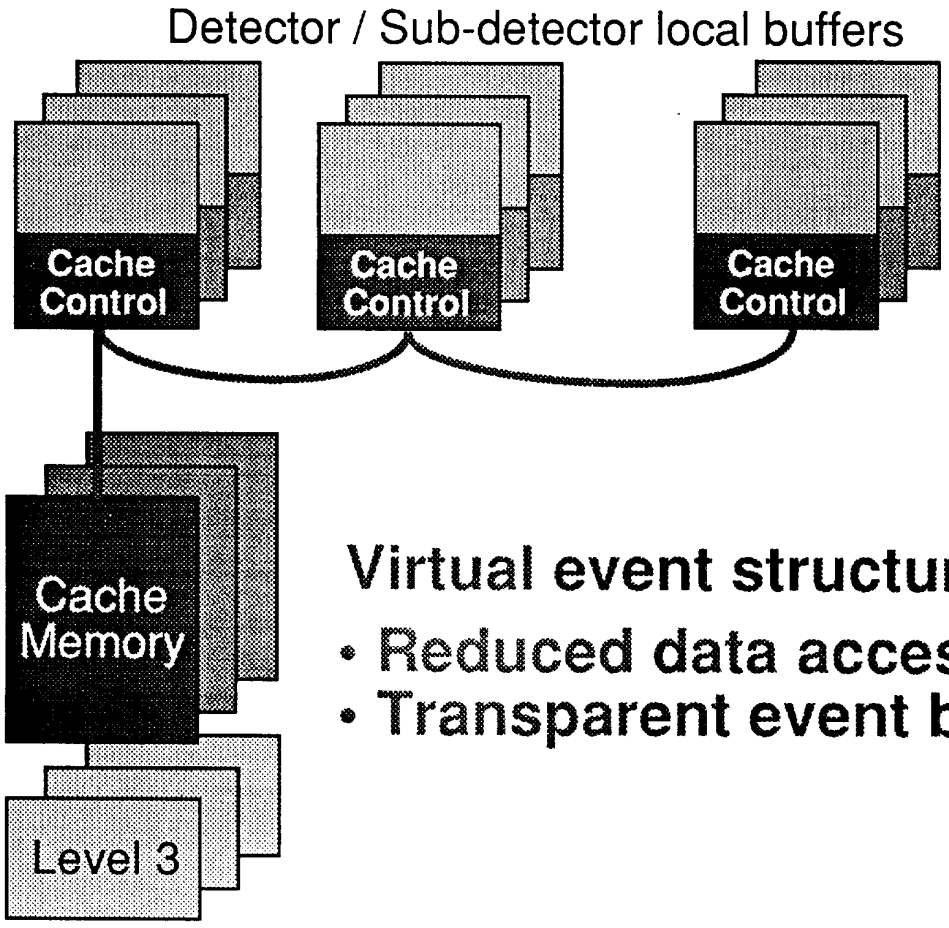
Virtual Event & Cache Readout





MMU ⟷ Event Selection

Cache ⟷ Event Builder



Virtual event structure

- Reduced data access
- Transparent event building

Experiment Computer Center

- **Event filter & Data reduction**

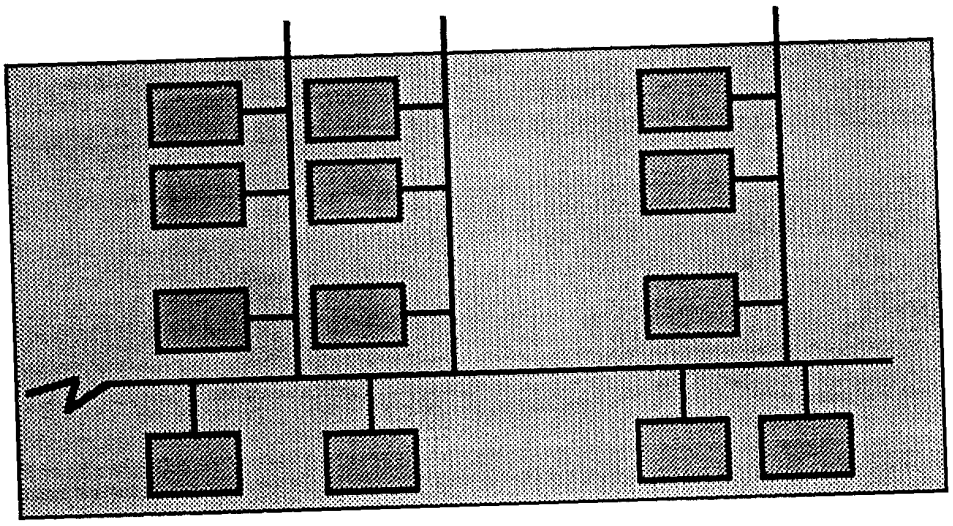
The event filter constitutes the final selection step based on global event physics analysis.
A distributed multi-stack of Power servers integrated in the event builder system with standard hardware access and development tools.

- **Distributed Computing**

Offline production, Data base, Calibration, Control&Simulation

- **Laboratory & World interconnection**
- **Mass storage**

100Mbyte/s. Tbyte/day. Event server facilities



10^3 Hz

≈ MB/event

10-100 Hz

10-100 MB/s

1 event 1 sec	Event Filter	Analysis
UA/LEP	10 MIPS	400 MIPS
LHC	10^4 MIPS	10^6 MIPS

Computing

RISC Workstations & Power Servers (1990)

- **Silicon Graphics.** (Mips3000 33 MHz)

Parallel CPUs 160 MIPS (600 MIPS next)

- HPPI (200 MB/sec)
- FDDI (100 Mbit/s)....

- **Dolphin, Nord Data.** (M88000 25 MHz)

Parallel CPU structure 120 MIPS (1000 MIPS next)

- SCI (1 GB/sec)

- **IBM 6000** (IBM RISC processor)

Ranging from 15-50 MIPS

- Hyper channel (40 MB/sec)

Array Processor & Parallel Computing

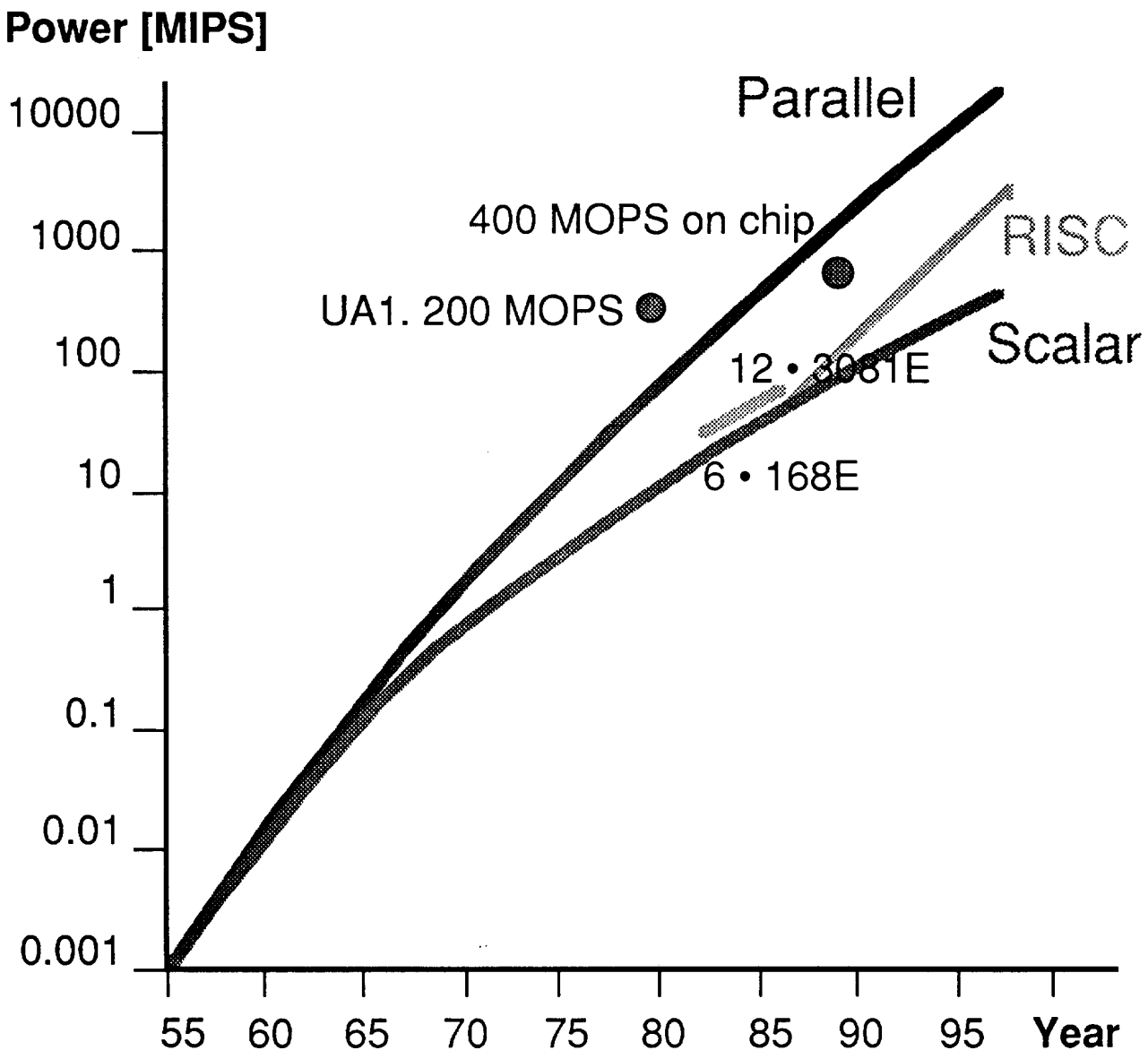
- **INTEL** parallel computers 64K nodes

2D-3D topology 100Mb/s bandwidth, 10^6 MIPS

- **Transputer** net (H1-100MIPS/node. 1991..)

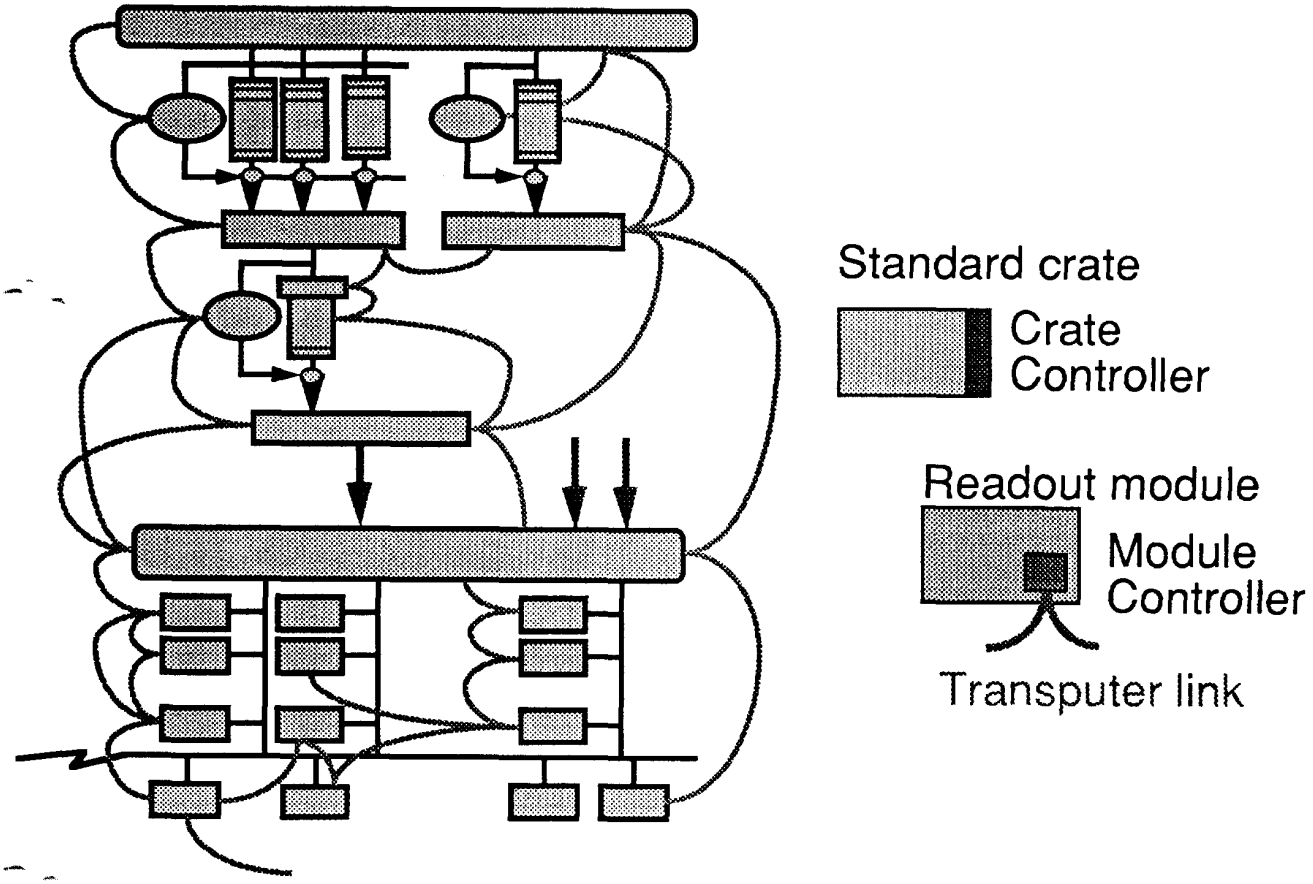
.....

Processor Evolution



Control & Calibration

Multi-access control network for :



- **Standard networks ?**

- **Transputers (H1) as general interface for distributed intelligent control ?**

  - Transputer-Workstation interface
  - Transputers as standard electronic system controller

Software Methods

Architecture Modelling & Simulation

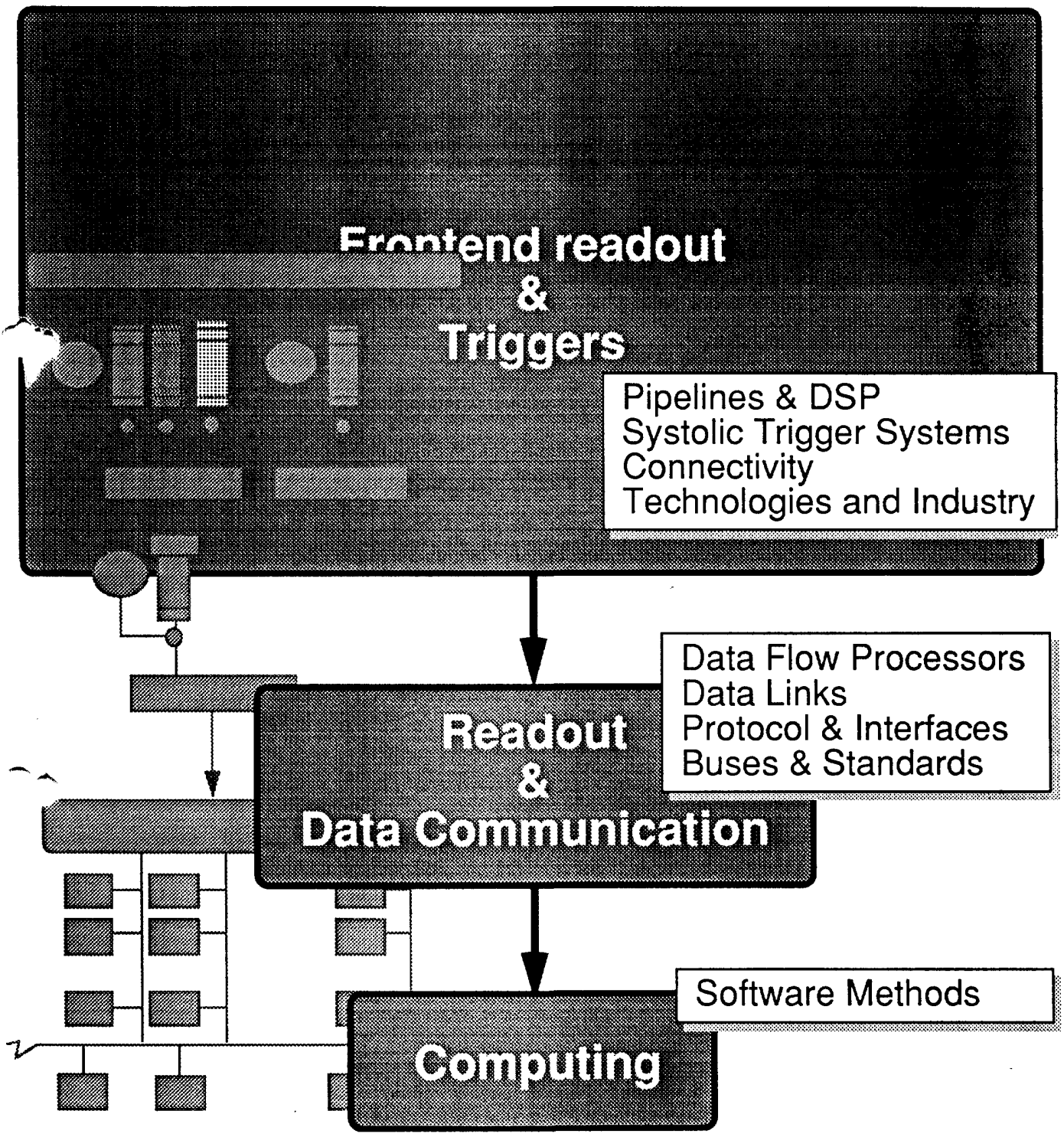
- **Hardware description language**
- **System modelling** (from gate to complex)
  - Behavioural simulation and animation
  - Timing and statistics analysis

Methods for :

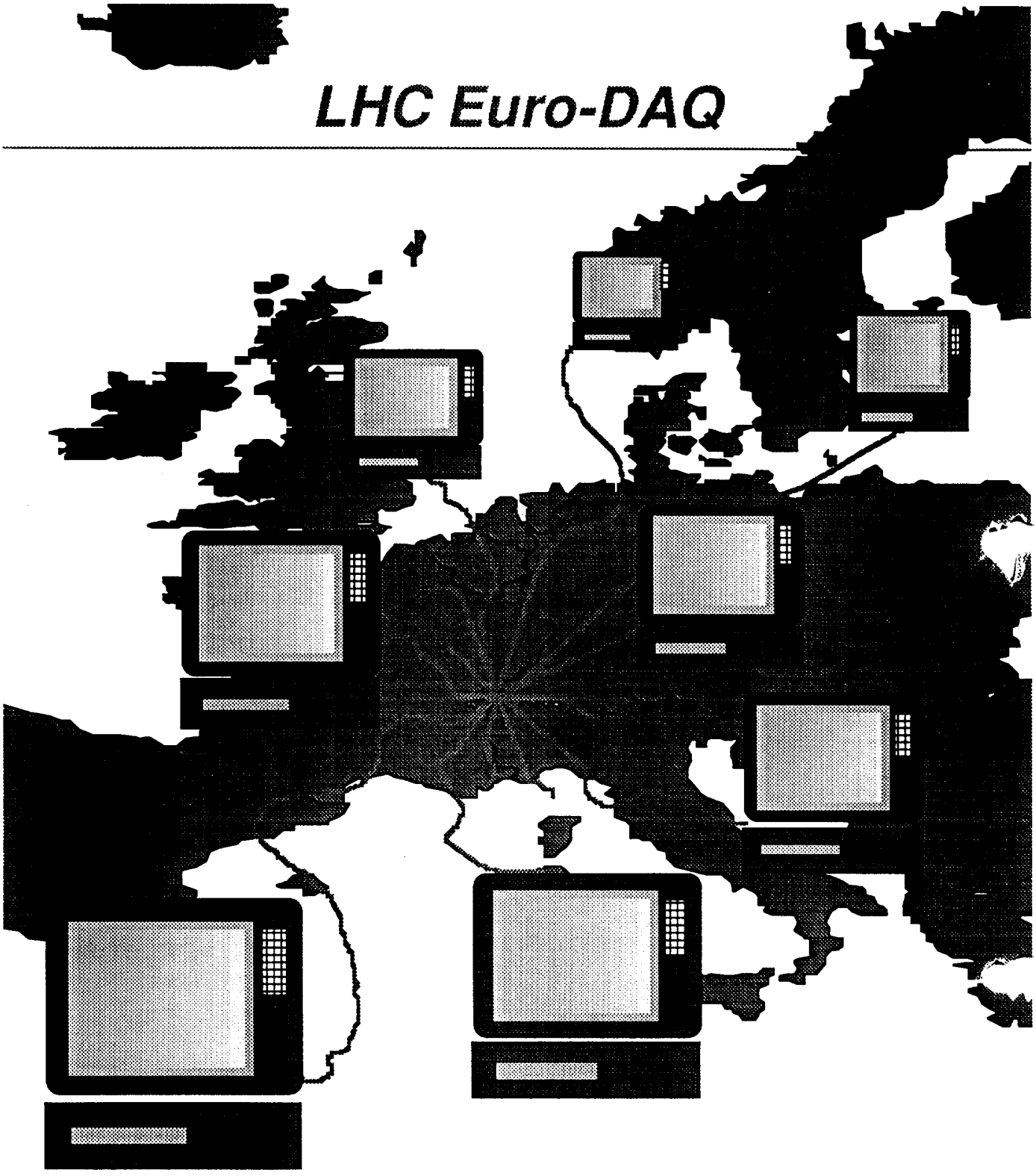
- **Specification and Description Language**
  - Graphical and textual system description language
  - Tools for complete system design and code generation
- **Object programming (**FORTRAN and C).
- **Operating system & development**
  - UNIX (hidden UNIX) ...
- **User interface. Virtual reality**
- **Data base. Multimedia**
- **Expert Systems**
  - Maintenance / debugging / documentation.

Software must be reusable !

The Problem View



LHC Euro-DAQ



1 LHC channel ≈ 1 TV channel
LHC DAQ ≈ 10M home HDTV systems