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A PROPOSAL FOR A NUMERICAL ACCELERATOR PROJECT

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This paper proposes a pilot project to study the feasibility of a numerical accelerator installation at CERN with a long term target (LHC startup time frame) of real-time performance. The rapid evolution of microprocessors based on RISC architectures, the ever increasing system integration level and the associated compiler technology now provides the opportunity to imagine a numerical accelerator. In the next few years, the increased speed of microprocessors and the computer systems as a whole, as indicated by technology road maps from various manufacturers should enable the real time simulation of large machines such as the LHC.

Keywords: Computer simulation; dynamic aperture.

1 INTRODUCTION AND PROJECT SUMMARY

A modest pilot project to explore the possibilities of real-time accelerator simulation in the LHC startup time frame is proposed. If the assumptions of the pilot project are confirmed we estimate that a fully-fledged simulator or numerical accelerator is not only feasible but also economically realistic.

The pilot project will establish, what performance improvement can be achieved (a factor 2–4 is expected) when simulating a circulating particle pair in SIXTRACK on a symmetrical multiprocessing system (SMP). The current version of the program is single threaded and built for single cpu systems with display output generated after the simulation is finished. The time estimated for remodelling the code into a multi-threaded version, to thoroughly verify the correctness and to adapt the current post-processing display to a first version of a real-time display is 18–24 months with a manpower of two fulltime equivalents.

If the improvement factor can indeed be reached, it seems reasonable, from technology projections and past computer performance improvements, to state that in 10 years time real-time simulation is indeed within grasp. The cost of the pilot project is $\approx$ 0.5 MCHF which covers the cost of a 6–8 cpu SMP system and two high performance graphic workstations (in a joint project environment).

To simulate the beam in the LHC a minimum of 10 particle pairs are needed; the corresponding number of SMP systems would in the final simulator cost $\approx$ 4–5 MCHF at today's price. However, the price/performance evolution of computing systems has become very favourable with the microprocessor revolution and no change in that trend can be seen today. More powerful machines will be available for less cost as more system functionality is integrated onto a single silicon chip and more processors are put into a single system environment further reducing the price of an individual system.

Assuming a very conservative improvement of 20% per year in price/performance, this would give a cost of the order of 1.5 MCHF in the year 2000 and less than 1 MCHF at LHC start-up. Our plan, if the pilot project succeeds, is to gradually build up the simulator, by a continuous upgrading of the installed cpu's to improve single system performance and by continuously adding systems, to improve the integrated simulator performance.

Setting up this project as a joint project with one or several computer manufacturers will, in addition to favourable price conditions, also give access to the latest developments and possibly extra manpower.

1.1 Background

Since a number of years special processors have been thought of in the accelerator community to study non-linear single particle dynamics. At DESY a heroic pioneer project[1] was undertaken to build such a dedicated computer. The idea had been to tailor the computer to the RACETRACK code,[2] a predecessor of the SIXTRACK code.[3] Originally no divisions were required in the code and very little memory space for data storage was needed. Unfortunately, during the project it became apparent that the code had to be changed, dictated by new physics insight. As a result a sizable number of divide operations had to be included and large memory became necessary to store tracking data for post-processing.

Already in the late 80's an alternative was used instead: a farm (6 units) of 370E emulators.[4] Massive tracking simulation were performed with this

cluster of computers without limitations due to a special purpose design while achieving a reasonable computing speed (some 25% of a IBM 3081 D).

In the meantime supercomputers had become fashionable and have been heavily used (CRAY Y-MP) by the SSC design team[5] and also at CERN (CRAY X-MP) for the first round of LHC tracking studies.[6]

The next step was the advent of RISC stations: the SSC design team have used a Hyper-Cube[7] while CERN invested into a farm of IBM-RISC stations, the PaRC cluster.[8] It is interesting to compare the performance of the IBM RISC station with respect to the 370E back in 1985. The speed-up factor is roughly 110 for a pair of particles, derived by simply scaling the results from the HERA machine to the LHC. In this factor the gain in speed by vectorisation of about 2 has been disregarded.

Even in the early 80's people were dreaming of real-time performance of such dedicated machines.[9] In reality, 10 years later we are still short by some factor of 180 (see Section 2 for details). This factor is however not too far from what has been gained in the last 10 years which lets us hope to achieve a similar factor in about the same time given a determined and steady effort.

Obviously we are not planning a remake of a DESY-like project. This is not only unrealistic due to lack of manpower and financial resources, but the technological progress is so fast that by the time the project will be finished it is more than likely that there will be a faster, cheaper and more reliable commercial product available.

There are examples of large scale cooperations between teams of physicists and prominent computer firms in the US. One team in Los Alamos is using clusters of CRAY computers[10] to study non-linear space charge forces. In the framework of CERN and the LHC machine studies such a project is both economically and technically unrealistic.

In this project we will make a more reasonable approach. We will try to induce computer vendors, interested to work with CERN, to help us achieve our ambitious goal within the next 10 years. The idea is to use off-the-shelf technology, upgrade it continuously and, together with the vendors experts, permanently work to adapt and optimise the code with all present and future tools available (see APPENDIX A). We thus want to assemble a powerful computing facility with an ever increasing computing performance at a reasonable price (see Section 4). This steady improvement is desperately needed in the design phase of the LHC but it will also serve to assist in the commissioning and optimisation phase with its real-time response.

In addition to the high performance computers, systems for visual display of the data generated are a necessity and finally have become affordable.[11]

A typical example of output with a stable particle from SIXTRACK is shown in Figure 1. This file corresponds to 3 Mbytes of data and 10^4 turns of one circulating particle with 4 phase space coordinates.

The next figure, Figure 2 shows a chaotic particle which will be eventually lost. This loss, however, could take place after millions of turns or minutes of storage time. Despite decades of research there is still no tool or technique available to predict this loss time, not even approximately. Hence, the only reliable approach is brute-force tracking with a dedicated computer such as proposed here.

Of course, once an easy-to-use graphical tool together with mass storage and fast data transfer speeds is available more sophisticated graphical post-processing will be demanded by the users, such as: on-line graphical control of simulation runs, cuts and rotations of 100 K samples, application of various on- and off-line data processing techniques, interaction between graphical surface and computing facility.

A very nice example of what can be done in visual display techniques is the SSC Particle Visualisation System, see Ref. 12.

2 ACCELERATOR SIMULATION PROGRAMS

At CERN several computer codes have been developed for both design work and simulation. One of the programs used for LHC simulations is the SIXTRACK program, mentioned above. This program provides estimates of the stability of particles in the machine and is thus a very valuable tool for the understanding of the machine behaviour under various conditions. In particular it is used to study the dynamic aperture of the machine, see Ref. 13.

Currently a simulation of 100 turns with 20 particles requires 16 seconds of cpu time on a single cpu IBM SP2 node. In order to study the beam instabilities at injection energy in the machine, about 100,000 turns are estimated necessary. In one second the beam makes about 10,000 turns ($T_{\text{rev}} = 88.924$ μsecs).[14] This has to be compared with 16 msecs for one turn and one particle in the computer, neglecting a factor of 2 due to the vectorisation. The level of improvement required in the computing performance to reach the real time goal is daunting, a factor of 180 must be gained, but this does not look insurmountable any more.

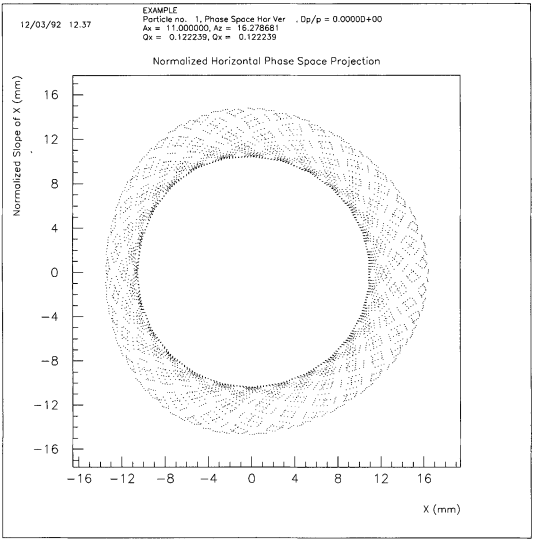

FIGURE 1 SIXTRACK output, stable conditions.

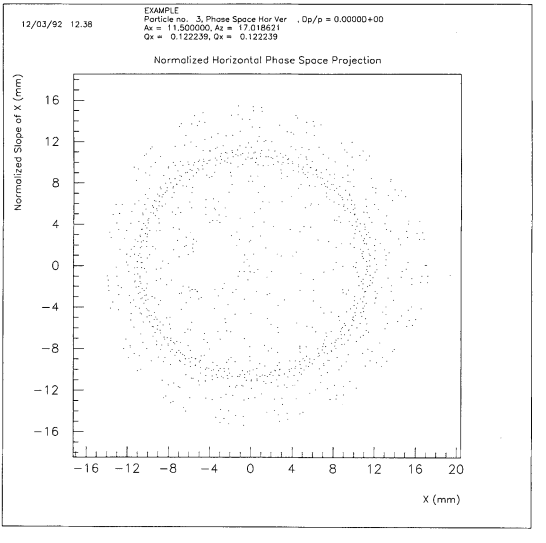

FIGURE 2 SIXTRACK output, unstable conditions.

3 PILOT PROJECT

The pilot project's aims are to study the SIXTRACK programs implementation, behaviour and performance constraints as well as the output data visual presentation in order to:

- Investigate any possible improvements/alternatives to the method currently used to solve the machine physics problem.
- Investigate multi-threading and algorithmic improvements.
- Investigate the scaling properties of the selected platform.
- Investigate means of data representation in real time.

The reason for pursuing multiple avenues of performance improvements simultaneously is simple; the improvement expected in pure hardware performance due to clock frequency increases over the next 10 years is of the order of a factor of 4–6, improvement expected due to architecture features such as multiple instruction issue and bigger on-chip caches is of the order of 3–5; and finally compiler/operating system development is expected to give a factor 2–4. Over the next 10 years the expected improvement factor can be estimated to be in the range of 24–120, an admittedly wide range with a very conservative lower limit!

It is worthwhile to note that the improvement actually achieved over the last three years by several vendors is already of the order of 4.[15] For more details on these estimates, see APPENDIX F.

Any other improvements in the overall performance must then come from either improvements in the SIXTRACK algorithms or from a multiprocessing approach or from both.

As indicated in Section 2, a 20 particle simulation requires a speed-up factor of 180; SIXTRACK's elementary unit of processing is a particle pair, using many processors in parallel could reduce the speed-up factor to 100 which does, in the LHC time frame, look attainable.

The visualisation aspect is important since the amount of data generated is huge. Inspecting the data files with a text editor is not meaningful and we will investigate what tools are available in this area for our purpose. The CERN developed PAW/PIAF tools are heavily oriented towards statistics and histogram displays and not appropriate to this application. The Application Visualisation System (AVS) in this context is very interesting[16] and also a de facto industry standard.

It should be emphasised here, that the use of SIXTRACK for the numerical accelerator pilot project, does not indicate an exclusion of any of the other codes that are widely used, such as MAD.[17] If the pilot project is successful, we strongly wish to provide the other codes on the simulator. SIXTRACK has only been selected for the pilot project due to our intimate knowledge of the code. The current, frozen, version of SIXTRACK will be used as reference version against which all modifications will be compared as regards correctness of the output results.

4 TOTAL COST OF A NUMERICAL ACCELERATOR

This proposal only covers the cost of the pilot project, see next section. If the conclusions of the pilot project are positive, showing that in fact scaling does apply to this type of problem, the cost of installing a complete real-time numerical accelerator at CERN in the time frame considered (8 years), is hard to predict, but an upper limit is given in the project summary section. The price/performance of systems change every 3–6 months within a very competitive market. What can be guaranteed is that it will in any case be far below what would be required today to reach the required performance. An example of the price/performance evolution of computing systems in the last 5–8 years is enlightening; the price ratio of the IBM 9000/900 to the DEC Alpha 8400 server with similar configurations is about 25 to 1; the performance ratio is approximately 1 to 10.

This is due to a microprocessor technology revolution and it should be remarked here that it is unlikely to be repeated once more during this projects lifetime.

Permanent manpower requirements for the final installation should not exceed the pilot projects requirements.

5 PILOT PROJECT REQUIREMENTS AND EVALUATION

The material requirements for the pilot project are limited: A typical small SMP system with 6–8 processors, network interconnect, ample memory and disk amounts to approximately 300–400 kCHF and two high performance graphics workstations with FDDI connections to approximately 70 kCHF. The manpower is estimated to one full-time equivalent person from the

CN division, one full-time equivalent person from the SL/AP group (possibly a fellow) and (potentially) one half-time person from the system supplier(s). Our current planning is to launch this project as a joint project between CERN and the appropriate computer manufacturers. The reason for this is threefold:

- A joint project will give us better access to the latest developments from the vendor's engineering departments.
- A joint project will permit us to get high performance hardware with a good discount.
- A joint project will provide us with invaluable operating system and compiler expertise[a] for RISC processors.

The aim of the pilot project is to verify the scaling assumptions made, that in the LHC startup time frame, we should be able to build a numerical accelerator with real time performance, i.e. running a simulated machine setup should take about the same time on the computer as in real life. If the performance improvement we can achieve during the pilot project scales as expected then we will conclude:

- The numerical accelerator will have acceptable performance.
- The total price of such an installation will be acceptable.

The time frame for the pilot project is estimated to 18–24 months.

APPENDIX A IMPROVEMENT AREAS OF CURRENT VERSION

The SIXTRACK code itself will be investigated in depth for loop unrolling, data structure definitions as required by the selected hardware for maximum performance and other general performance improvement techniques. The High Performance FORTRAN Forum and the development of the FORTRAN 90 language are evidently of interest in the general performance area where code adaption/rewrites may be necessary. However, to reach the real time goal, a multi-threaded version of the program will most certainly be required. SIXTRACK spends a majority of the execution time in a matrix multiplication loop and a Horner scheme, sweeping through the memory. The analysis tools available give an in depth analysis of where the program spends its time,

[a] RISC = Reduced Instruction Set Computer or Relegate Important Stuff to the Compiler.

including first and second level cache misses, pipe line stalls etc. The way loops are ordered has a major impact on the performance of the application, making large strides through memory without attention to how the cache memory is structured may cause the cpu to be in permanent wait for data if every cache access generates a miss!

The loop ordering areas in SIXTRACK will require particular attention but it may be necessary to also study other mathematical/numerical methods for solving the equations than those currently used in order to increase the performance significantly.

APPENDIX B SIXTRACK ON VARIOUS PROCESSORS

This section shows the results of the SIXTRACK benchmarks on the more interesting of the various processors that we have or have had access to.

TABLE I SIXTRACK performance on various RISC processors and older machines

System	*Time (secs)*	*Comment*
Alpha300 Mhz – EV5	8.3	EV5, Latest ALPHA implementation
Alpha275 Mhz – EV45	14.0 (est.)	Intermediate ALPHA implementation
Alpha150 Mhz – EV4	39.43	First released ALPHA implementation
CRAY X–MP/48	21.3	Vectorized version
HP 755	45.5	
IBM SP2 "Fat node"	15.5	
IBM SP2 "Thin node"	18.4	
IBM SP1	28.1	
IBM 9000/900	42.2	Vectorized version
DEC VAX 9000	221	

APPENDIX C NEW ARCHITECTURE IMPLEMENTATIONS

The notion of architecture vs silicon implementation will become more and more important as the chip density grows. With a growing number of transistors on-chip, many of the functions that currently are off-chip will be moved on-chip, increasing the overall performance. However, although the

application software will be binary compatible, only a program compiled with the new processor as target, may be able to fully benefit from the added processor features.

APPENDIX D NEXT GENERATION PROCESSOR PERFORMANCE ESTIMATES

This section gives an overview of the next generation of processors, see Ref. 18. As can be seen from the "Volume Ship" row, most of these processors are already expected to ship this year!

TABLE II Performances of the next generation

	Alpha 21164+	*MIPS R10000*	*HP PA 8000*	*PowerPC 620*	*SUN UltraSPARC*
Clock (MHz)	366	200	200	133	167
SPECint92	400	300	350	225	250
SPECfp92	600	500	550	300	360
Volume Ship	4Q 1995	4Q 1995	1Q 1996	3Q 1995	3Q 1995

APPENDIX E SEMICONDUCTOR PROCESS PROJECTIONS

The various semiconductor manufacturers have published long-range (5–7 years) projections of the future implementation technology in terms of chip density, feature sizes and clock frequencies. IBM expects a 1000 SPECint92 performance in 1998 while DEC is somewhat less aggressive projecting this to happen in 2000.

TABLE III IBM VLSI CMOS semiconductor process evolution[19]

	1992	1995	1998	2001
Memory	16 Mb	64 Mb	256 Mb	1 Gb
Min feature (μm)	0.7/0.5	0.5/035	0.35/0.25	0.25/0.18
Maximum chip size	200	300	400	
Power Supply (V)	5–3.5	3.3–2.5	2.5	1.8
Performance (SpecInts)	62	250	1000	

TABLE IV DIGITAL Equipment CMOS microprocessor road map[20]

Wafer size	5"		6"			8"	
Mfg year	1985	1987	1991	1993	1996	1999	2002
Rel. gate speed	1	1.3	2.2	2.9	3.7	4.8	6.3
Min. feature (μm)	2.0	1.50	0.75	0.5	0.35	0.25	0.18
Clock rate – MHz	12	37	150–200	225–350	400–500	500–750	750–1000
Transistor count (M)	0.2	0.4	1.5	9	30	100	250
SpecInts			74.6	277–341			

It is interesting to note that the two tables coincide fairly well as regards feature size and density. The future process developments seems to be already defined for the next 5–7 years.

APPENDIX F EXPECTED MICROPROCESSOR PROGRESS

This appendix details some of the expected performance improvements in microprocessor technology that computer vendors and industry analysts have published as road maps of future processors and future semiconductor processes. As can be clearly seen the raw performance increases delivered so far is expected to continue unabated for at least the next 8–10 years. In a longer perspective the way to improve the performance will become multidimensional; not only the clock frequency will be increased, the amount of work done per clock cycle will increase as implementations with multiple instruction issue appear. The estimates of the factors of improvement that can be expected in these two dimensions over the next 10–15 years are, see Ref. 21:

- Expect clock frequency to increase by a factor of 10.
- Expect multiple instruction issue to give a factor of 10, but perhaps after a decade of compiler research.

A factor of perhaps 100 might be expected over the next 10–15 years, any further improvements beyond that must come from a multiprocessing approach. The reported improvement[15] of a factor 4 per three year period would, if continued, give a factor of 16 already in the year 2001. The estimates

made in Ref. 22, that a factor of 12 improvement in the year 2000 time frame could be expected, thus seems somewhat conservative.

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