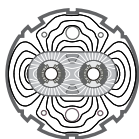


EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
European Laboratory for Particle Physics



Large Hadron Collider Project

LHC Project Report 57

Solid State Switch Application for the LHC Extraction Kicker Pulse Generator

E. Carlier, L. Ducimetière, U. Jansson, M. Schlaug, G. Schröder, E. Vossenberg

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The switch is made of 10 modified 4.5 kV, 66 mm symmetric GTO's (also called FHCT-Fast High Current Thyristor), connected in series. It holds off a d.c. voltage of 30 kV and conducts a 5 μ s half-sine wave current of 20 kA with an initial di/dt of 10 kA/ μ s. Major advantages of the switch are the extremely low self-firing hazard, no power consumption during the ready-to-go status, instantaneous availability, simple condition control, very low noise emission during soft turn-on switching and easy maintenance. However, the inherent soft, relatively slow turn-on time is a non negligible part of the required rise time and this involves adaptation of generator components. A dynamic current range of 16 is achieved with variations in rise time, which stay within acceptable limits.

Important generator improvements have been made with the series diodes and freewheel diodes. A more efficient droop compensation circuit is being studied. It is directly connected in series with the freewheel diode stack and maintains an acceptable flattop variation of 5% of the magnet current during 90 μ s. This paper presents the complete generator, in particular the solid state switch and discusses related electrical measurements.

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Introduction

CERN, the European Laboratory for Particle Physics, is designing a Large Hadron Collider to be installed in the existing LEP tunnel of 27 km circumference. The LHC will accelerate in opposite directions two beams of 3×10^{14} protons each and will collide them at a centre of mass energy of 14 TeV. The stored energy of up to 334 MJ per beam has to be disposed by a dumping system safely at the end of a physics run when a refill becomes necessary. The dumping system will also be used frequently during setting-up and machine studies, and must always be ready in case of equipment malfunction or abnormal beam behaviour at all beam energies. The beam dump system uses 14 fast kicker magnets per beam to extract the

particles in one revolution of the collider and to dispose them on external absorbers.

Pulse Generator

Each magnet is powered by its own pulse generator. The basic electrical circuit employing a switch with negligible turn-on and conduction losses is shown in Fig. 1. Calculated waveforms of the switch and magnet current are given in Fig. 2. The circuit consists of a discharge capacitor in series with a power switch, that produces in combination with a free-wheel diode stack, in parallel to the magnet, a current pulse of 3 μ s rise time and about 2 ms fall time, of which only about 90 μ s will be used. The current droop is compensated by a low voltage, high current capacitor discharge that produces the flat top required for extraction. The main switch conducts only during the first 12 μ s.

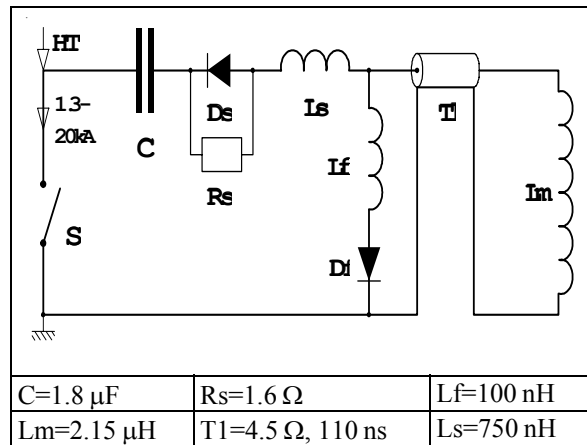


Fig. 1 Basic circuit diagram

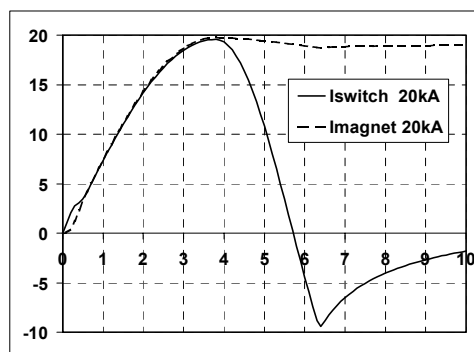


Fig. 2 Switch and magnet current at 20 kA (Hor. scale 1 μ s/div., Vert. scale 5 kA/div.) (Turn-on and conduction losses neglected)

The magnet current needs to be proportional to the beam momentum over a wide dynamic range, from injection at 0.45 TeV/c, corresponding to 1285 A, to top momentum of 7 TeV/c, corresponding to 20 kA. During a collider run of e.g. 10h the pulsers are continuously under the voltage corresponding to a discharge current of 20 kA. A more detailed description of the pulser is given in [1] and [2].

Switch Requirements

D.c.voltage range	1.7/27	kV
Peak current	+20/-10	kA
Current rate of rise	~10	kA/ μ s
Current conduction time	12	μ s
Charge transfer pos./neg.	70/20	mC
Repetition time minimum	30	s
typical	5-10	h
Lifetime at peak current	10^5	pulses
Spontaneous conduction rate	$< 10^{-4}$	

Table 1: Switch requirements

The basic requirements of the switch are listed in Table 1 in which negligible turn-on and conduction losses are assumed, as are normally obtained in gas tubes, like thyratrons or pseudospark switches. Until recently, semiconductor power switches were not capable to switch with the required rate of current rise of ~ 10 kA/ μ s. In 1993 preliminary tests were done at CERN with a standard high power GTO thyristor that was slightly doped. With this device a rate of rise of 16 kA/ μ s for a 6 μ s half sine wave with 32 kA peak current were obtained [2], making solid state switches a promising candidate for this application. Compared to gas switches they are in particular not plagued by a limited operation voltage range and by spontaneous conduction. It was therefore decided in 1994 to construct a full scale semiconductor switch for this application.

30kV Switch Assembly

Fig. 3 shows the switch assembly consisting of 10 in series connected FHCT's. This system has been tested with 70.000 discharges at a peak current of 30 kA.

The individual components are assembled in an isolated coaxial fixture without heatsinks compressed with a force of 35 kN. This fixture has a "cage" structure composed of 9 stainless steel rods equidistantly distributed around the FHCT to carry the return current and limit the switch stray inductance to about 200 nH.

The following components are mounted outside the cage:

- The anti-parallel diode, type WESTCODE, SM45CXC604

- A static voltage divider of 5 M Ω metal film resistors, type METALLUX, 968.2
- A 50 Ω gate-cathode resistor
- Over-voltage protection capacitor of 250 nF, 4.7 kV, type NCL, GT2134
- A 10:1 step-down trigger pulse transformer.

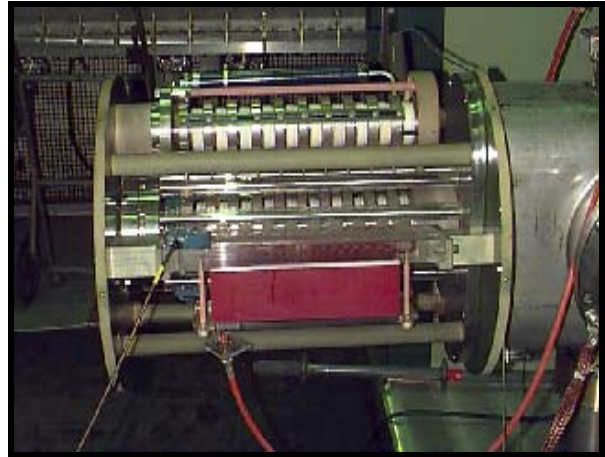


Fig. 3 The switch

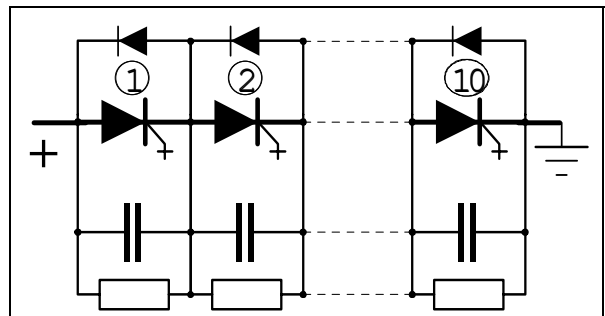


Fig. 4 String of 10 FHCT's

Fig. 4 shows the basic circuit diagram of the switch. Differences in switching speeds and turn-on delays of the FHCT's are accommodated by the parallel over-voltage protection capacitors. The measured difference in turn-on delays is smaller than 100 ns.

The 10:1 step-down pulse trigger transformer, manufactured by STANGENES is insulated at 40 kV and consists of one primary and 10 secondary windings. The primary voltage is 3 kV and each secondary voltage is 300 V at 250 A, obtained by a R-C peaking circuit. The primary leakage inductance is 5 μ H. The actual pulse generator is equipped with a 1.52 μ F capacitor and the total risetime inductance is 3.1 μ H.

Fig. 5 shows the gate and main switch currents with the minimum and maximum amplitude of 1.3 kA and 20 kA during the first 9 μ s. Both main currents are displayed with the same amplitude to show the non-

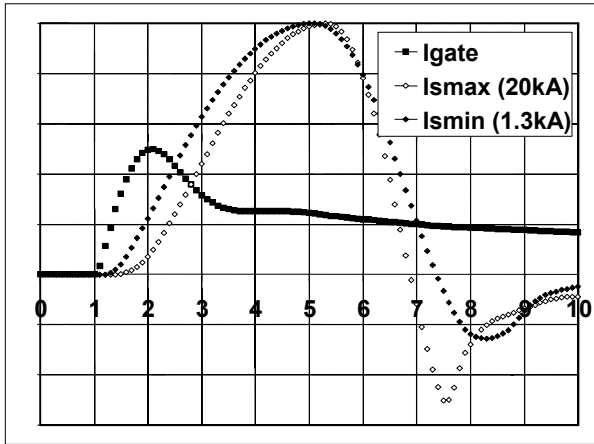


Fig. 5 Gate current and maximum and minimum switch current
(Hor. scale 1 μ s/div., Vert. scale Igate 100 A/div., Ismax 4 kA/div., Ismin 0.26 kA/div.)

linear turn-on behaviour of the FHCT.

For this application the FHCT must be considered as a comparably slow switch with soft turn-on, whose characteristics influence considerably the circuit layout. The capacitor value must be decreased to 1.3 μ F to meet the required risetime. The initial pulser voltage will increase to 33 kV, which means a difference of about 25% with respect to the maximum voltage in case of a loss free switch. Fig. 6 and 7 show the measured turn-on voltage of the switch and magnet current at maximum energy and at injection energy respectively. The initial fallback of the magnet current is mainly determined by the stray-inductance of the freewheel diode stack composed of 5 extra thin 4.2 kV diodes, type WESTCODE, SM42CXC15C. For beam optics reasons the magnet current overshoot must be limited to 5%. This will be achieved by installing 2

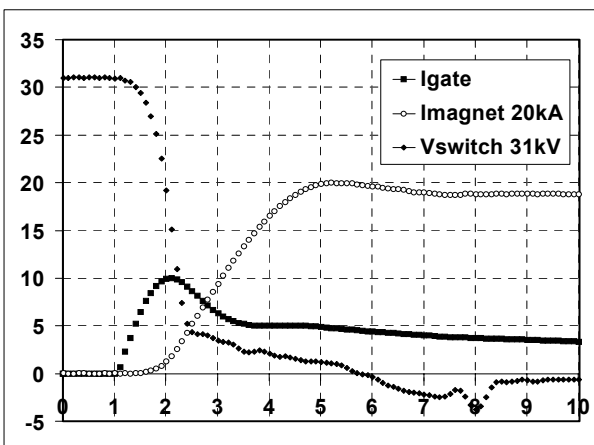


Fig. 6 Switch voltage, gate and magnet current at full energy
(Hor. scale 1 μ s/div., Vert. scale 5 kA/div., 5 kV/div.,

Igate Vert. scale 125 A/div.)

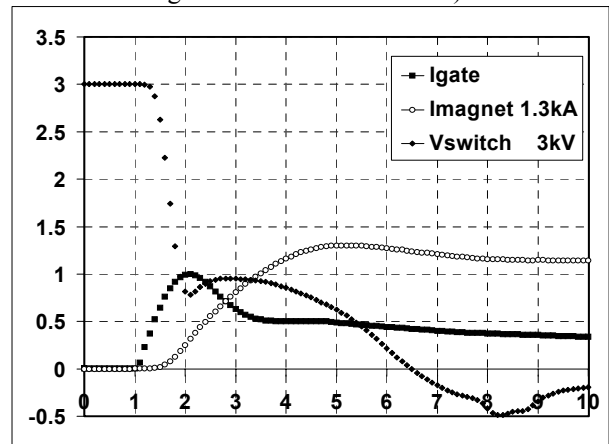


Fig. 7 Switch voltage and magnet current at minimum energy
(Hor. scale 1 μ s/div., Vert. scale 500 A/div., 500 V/div., Igate Vert. scale 125 A/div.)

diode stacks in parallel.

Fig. 7 shows at injection energy corresponding to 3 kV the voltage waveform over the FHCT switch and the magnet current. The turn-on losses at low voltage are relatively high, requiring 3 kV for a magnet current of only 1.3 kA. This corresponds to a dynamic voltage range of about 11 for a required magnet current range of 16.

Fig. 8 shows the measured normalised maximum and minimum magnet currents. The difference in turn-on behaviour is quite pronounced and requires of the main capacitor value to 1.3 μ F to assure a correct risetime.

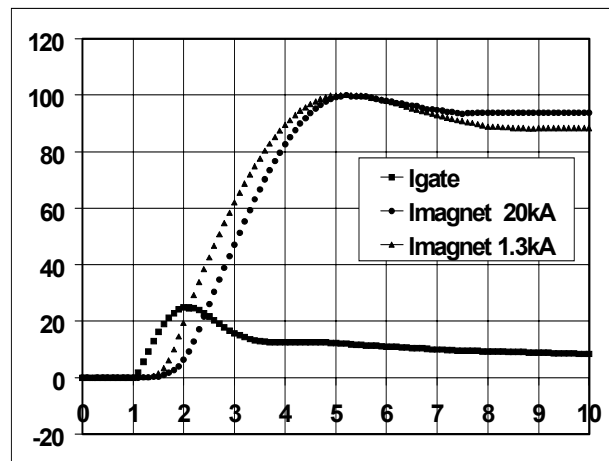


Fig. 8 Magnet current at full and injection energy
(Hor. scale 1 μ s/div., Igate Vert. scale 200 A/div.)

The current fallback after the maximum of 20 kA is 6.5% and increases to 11.5% at 1.3 kA. This difference is caused by the dynamic turn-on behaviour of the freewheel diode stack. Tests with different diode types, like the 12 kV ABB multi-chip freewheel diode, type

DSA 1508-12000, are in progress to improve the initial fallback at low magnet current. First tests show an improvement at minimum current of 30%.

Series Diodes

Substantial progress has been made with the novel series diode stack Ds, type WESTCODE, SM45CXC604. These diodes have an extremely low recovery charge and interrupt the negative switch current at less than 50% of the positive amplitude. The stack consists of 7 devices paralleled by a resistor of $1.6\ \Omega$, constructed from a 0.6 mm diameter stainless steel welding wire. This multi-function resistor allows d.c. charging of the main capacitor, improves the turn-on behaviour of the series diode and determines at blocking of the negative switch current the voltage amplitude and distribution over the diode stack. Finally it takes the stored charge away from the diodes and attenuates the negative switch current.

Flattop Compensation

The first attempt to compensate for flattop current droop was done with a circuit in parallel to the freewheel branch [1], the parallel compensation circuit. The disadvantage of such a circuit is the need of a costly blocking diode stack, designed for full voltage and low inductance. A further drawback is the relatively slow take over of the magnet current by the compensation circuit due to the fact that only a low voltage capacitor of 500 V can be employed. The new compensation circuit is mounted in series with the freewheel diode stack. Two variants are being tested (see Fig. 9).

In the compensation circuit A a capacitor of 4 mF with low stray inductance, charged to -500 V for full energy is connected in series with a FHCT switch. This assembly is branched in parallel to the last diode D

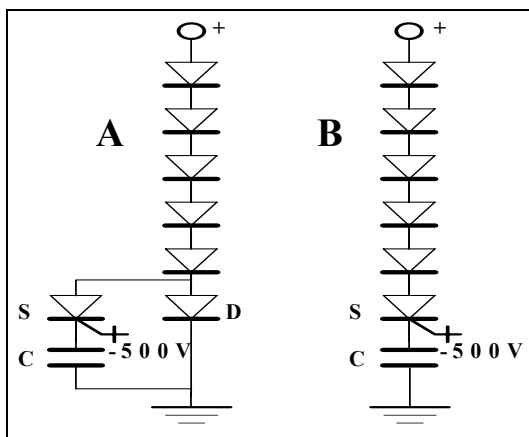


Fig. 9 Flattop current droop compensation circuits

of the freewheel stack. Initially the magnet current flows through the freewheel stack. Immediately after having

reached its maximum, switch S is closed and the current in diode D is commutated. The capacitor C is now connected in series with the magnet inductance and oscillates with a superimposed half-sine wave of $200\ \mu\text{s}$. The initial capacitor voltage is determined such that it compensates the resistive losses of the magnet current. Measurements showed that the commutation process of diode D takes about $10\text{-}15\ \mu\text{s}$ during which the magnet current continues to drop by an unacceptable amount. The novel compensation circuit B avoids the diode commutation. The magnet current will be freewheeled and compensated simultaneously. The total stray inductance of this circuit must be kept low. A further advantage is a shortening of the duration of the decaying magnet current to about $500\ \mu\text{s}$ since the compensating capacitor remains in series with the magnet. In the original circuit the magnet current decay lasts 2 ms which is more difficult to support for the current carrying contacts.

Outlook

The FHCT is still a “youngster” in the semiconductor family and despite the substantial progress made has still a high potential for future improvements. We expect to benefit from new semiconductor materials, like silicon carbide (SiC) for which the turn-on and conduction losses will be significantly lower due to the nearly 10 fold increase in permissible field strength, which will reduce considerably the thickness of the pn junction. An improvement is furthermore expected from buffer-layer structures which will also reduce the silicon waver thickness.

Acknowledgements

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