A LOW POWER, LARGE DYNAMIC RANGE, CMOS AMPLIFIER AND ANALOG MEMORY FOR CAPACITIVE SENSORS

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I. Abstract

This paper has been written to announce the design of a CMOS charge to voltage amplifier and it's integration within an analog memory. Together they provide the necessary front end electronics for the CMS electromagnetic calorimeter (ECAL) preshower detector system in the LHC experiment foreseen at the CERN particle physics laboratory.

The design and measurements of the amplifier realised in a $1.5\mu m$ bulk CMOS process as a *16* channel prototype chip are presented. Results show the mean gain and peaking time of $<peak\_voltage> = 1.74mV/mip$, $<peak\_time> = 18ns$ with channel to channel variations; $\sigma_{(peak\_voltage)} = 8\%$ and $\sigma_{(peak\_time)} = 6.5\%$. The dynamic range is shown to be linear over $400mips$ with an integral non linearity $(INL)=0.05mV$ as expressed in terms of sigma from the mean gain over the $400mip$ range. The measured noise of the amplifier was $ENC=1800+41e/pF$ with a power consumption of $2.4mW/channel$. The amplifier can support extreme levels of leakage current. The gain remains constant for up to $200\mu A$ of leakage current.

The integration of this amplifier within a *32* channel, *128* cell analog memory chip "DYN_{LDR}" is then demonstrated. The DYN_{LDR} offers sampling at $40MHz$ with a storage time of up to $3.2\mu s$. It provides continuous Write/Read access with no dead time. Triggered data is protected within the memory until requested for readout which is performed at $2.5MHz$. The memory is designed to have a steerable dc level enabling maximum dynamic range performance. Measurements of the DYN_{LDR} are presented confirming the original amplifier performance. The memory itself has a very low pedestal non uniformity $(\sigma_{(ped)})$ of $0.9mV$ and a gain of $10mV/mip$.

[i]II. Introduction

The preshower detector consists of two planes of silicon detectors and sits respectively after *2* and *3* X_0 of lead before the ECAL endcaps. It consists of 176000 $60x2mm^2$ silicon strips which present an input capacitance per electronic channel of $40pF$. The fine granularity of the preshower detector improves the separation of single photon electromagnetic showers from those induced by two close photons produced in the decay of a neutral pion. The measurement of the charge released in the silicon is used to

measure the shower barycenter and to correct for the energy deposited in the lead radiator. It can also be used to improve electron-pion separation. The charge produced by *300μm* thick silicon detectors can be from *4fC* to *1600fC* corresponding to *1* to *400* minimum ionising particles (mip) .

The FCICON has been designed to act as the front end interface to the preshower detectors. It produces a charge to voltage conversion with linear characteristics from *4fC* to *1600fC*, it is robust against leakage current and operates with a large capacitive loading on the input. The amplifier is a symmetric ICON (current conveyer) structure with a folded cascode stage offering very low input impedance and high output impedance. This enables the amplifier to be directly connected to the detector reducing considerably cross coupling problems between detectors. The amplifier has a leakage current compensation system which enables the amplifier to work perfectly with many tens of micro amperes of dark current produced by the detectors.

III. The FCICON design

The FCICON shown in Figure 1, is based on the current conveyer principle [1]. It is a symmetric structure with common gate input transistors Mni and Mpi offering a very low impedance at the input node. The signal then passes symmetrically through the cascode transistors Mnc and Mpc before being transferred to two output branches through current mirrors Mp2 and Mn2. Transistors Mp1 and Mn1 are the current sources controlling I_{total} and the cascode transistors are biased in such a way as to control I_{bm}. The two input transistors therefore receive a dc current of I_{total} - I_{bm}. Transistors Mn3,4 and Mp3,4 are the current sources for the output branches each having dc current I_{bm}.

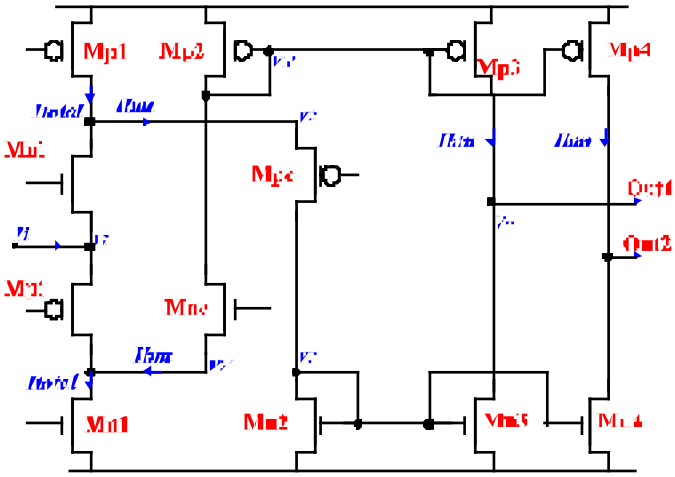

Figure 1, The FCICON

In the frequency region of interest the noise in the amplifier is dominated by thermal white noise as opposed to 1/f noise. In order to optimise for thermal noise behaviour the input transistors have been sized such that C_i / C_{det} = *1/3* [2][3] defining an input capacitance of *13pF*. With *200μA* of drain current the transistors are working in strong inversion with their source transconductance (*gms*) as given in (1) [4].

$$gms = n\sqrt{\frac{2\mu \cdot C_{ox} I_d \cdot W}{nL}} \qquad (1)$$

where n is the weak inversion slope, μ is mobility, C_{ox} the capacitance of the silicon dioxide under the gate, W the

transistor channel width and L the transistor channel length.

The small signal model of the circuit is shown below in Figure 2.

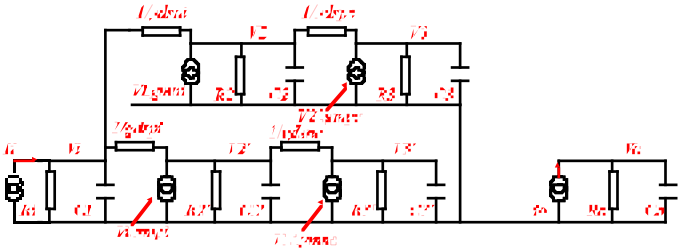

Figure 2 FCICON small signal model

The common gate structure of the input devices together with their large W/L ratios offers a very low input impedance in the region of 124Ω as given by (2) . This together with C_i (3) produces the fast input time constant (τ) of $1.6ns$.

$$R_i = \frac{1}{gms_{in} + gms_{ip}} \qquad (2)$$

$$C_i = Cgs_{ni} + Cgs_{pi} \qquad (3)$$

In contrast the output impedance (4) is designed to be extremely high at $2.8M\Omega$.

$$R_o = \frac{1}{gds_{p3} + gds_{n3}} \qquad (4)$$

Where gds is the drain to source conductance. The load impedance then defines the voltage gain of the amplifier (5)

$$\frac{V_o}{V_i} = \left(\frac{gms_{ni} \cdot gm_{n3}}{gm_{n2}} + \frac{gms_{pi} \cdot gm_{p3}}{gm_{p2}} \right) R_o \qquad (5)$$

Noise analysis has been done on order to show the equivalent noise charge (ENC) [5] in terms of equivalent series $(e_n{}^2{}_s)$ (6) and parallel $(i_n{}^2{}_p)$ (7) noise sources at the input [6].

$$e_n{}^2{}_s = \frac{8kT \cdot \Gamma}{3(gms_{ni} + gms_{pi})} \qquad (6)$$

$$i_n{}^2{}_p = \frac{6kT}{\Gamma} \left(\sum_{x=1}^{x=3} gm_{n(x)} + \sum_{x=1}^{x=3} gm_{p(x)} \right) \qquad (7)$$

Where k is the Boltsman factor, T the temperature and Γ the technology dependant excess noise coefficient.

The series component of the ENC is dominated by the channel thermal noise of the two input transistors and is shown in (8).

$$ENC^2{}_s = \frac{e_n{}^2{}_s \cdot C_i{}^2}{t_m} \qquad (8)$$

Where t_m is the rise time after an external filter which sets a sampling window of $25ns$.

The parallel component is shown in (9) and is dominated by the noise of the current sources.

$$ENC^2{}_p = \frac{i_n{}^2{}_p \cdot t_m}{3} \qquad (9)$$

IV. The LDR amplifier chip.

The LDR amplifier chip consists of 16 identical channels, each one as shown in Figure 3.

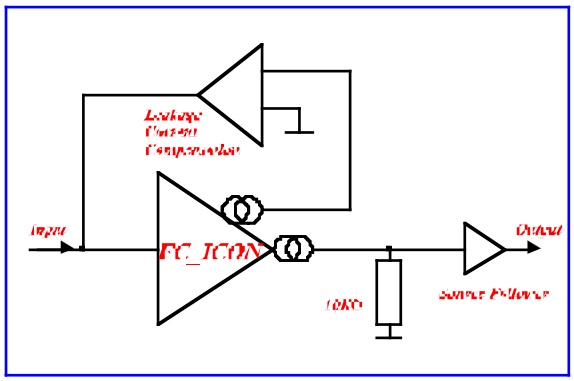

Figure 3 LDR amplifier channel

One output from the FC_ICON is fed to a leakage current compensation unit and it's output is then connected to the FC_ICON input. This enables a dc connection directly to the detector since any leakage current from the detector causes a small change in the output voltage level. This is sensed by the leakage current compensation unit and the leakage current is then diverted into the feedback device. Extremely low frequency behaviour of the feedback amplifier means that the signal current remains unaffected.

The second output from the FC_ICON is connected to a physical resistance to ground. The value of the terminating resistance has been chosen such that the integrating node at the output is completely suppressed and the voltage pulse shape follows directly the form of the detector current pulse. The gain is then determined using equation (5) with the terminating resistance (R_L) in parallel with R_o. This voltage pulse is then transferred off the chip by the voltage buffer.

V. LDR_amp Measured Results

The amplifier was biased with $I_{total} = 250\mu A$, $I_{bm} = 50\mu A$ and a $6V$ power supply. The overall power consumption was $2.4mW$ per channel.

The signal response to a $4fC$ input signal is shown in Figure 4. This is equivalent to the charge produced when 1 mip passes through $300\mu m$ of silicon.

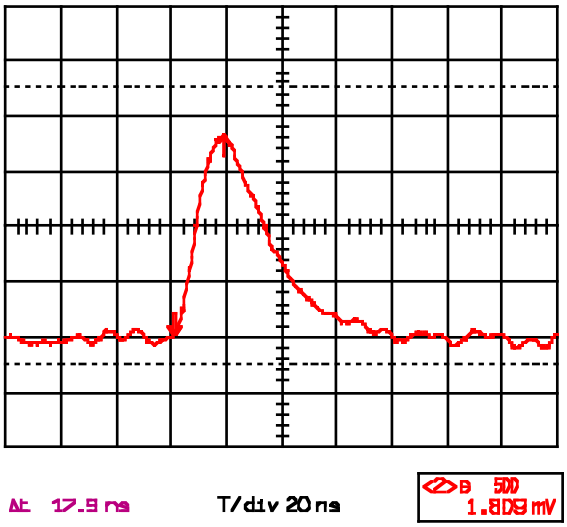

Figure 4 Signal response to 1 mip

The peak of the pulse is reached after18ns whilst the tail takes approximately $75ns$ to clear completely. The value of the voltage gain is $1.8mV/mip$.

The signal response is linear from -$800fC$ to $800fC$ $(400mips)$ of input charge and is shown in Figure 5. It has an integral non linearity (INL) of $0.05mV$ as expressed in terms of sigma from the mean gain over the $400mip$ range.

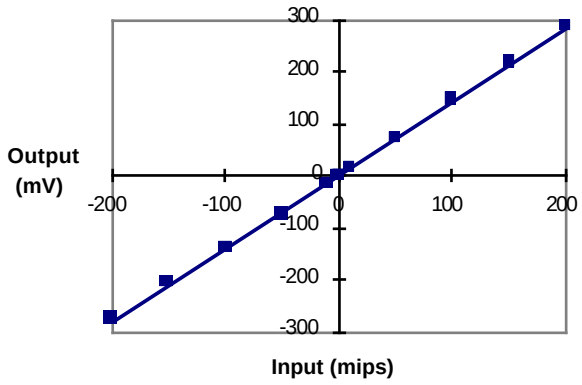

Figure 5 Linearity

The robustness to leakage current is shown in Figure 6 which shows the normalised voltage gain as a function of leakage current.

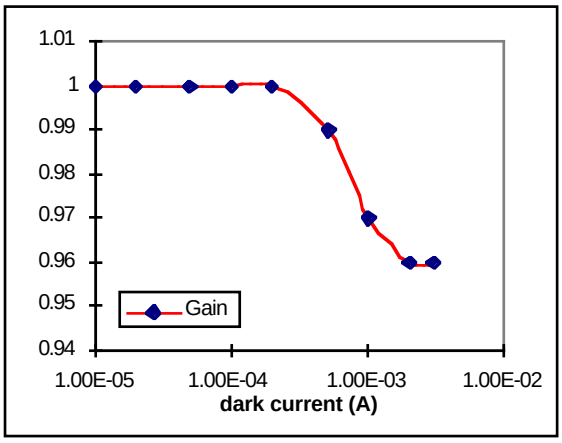

Figure 6 Signal response against leakage current

There is no apparent deteriation in signal response up to a value of *200µA* of detector leakage current with less than 5% loss after 1mA. The dc output level remains constant up to *1mA* with a noise increase of approximately *1e/µA*.

The leakage current expected for 1.2cm^2 silicon strips is 25µA after *10Mrads(Si)* of irradiation.

The noise behaviour is shown in Figure 7. The series noise can be seen to be *41e/pF*, *(1.04nV(Hz)$^{-1/2}$)*.
The parallel noise is *1800e* if one assumes a linear fit to the measured data and approximately *8pF* of load capacitance due to bonding, packaging and parasitic board capacitance on the inputs.

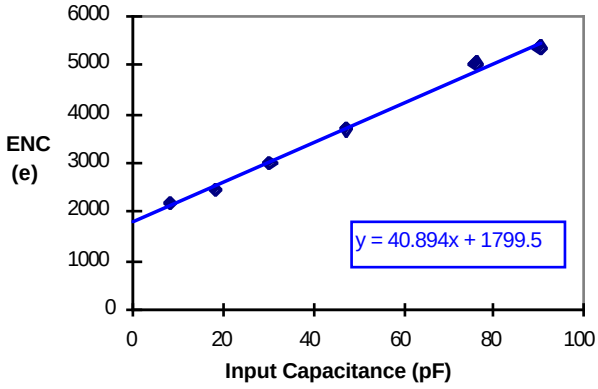

Figure 7 Measured Noise of the FCICON

The standard deviation of the measured values across the 16 channels of the chip was $\sigma_{(peak\_voltage)} = 8\%$ and $\sigma_{(peak\_time)} = 6.5\%$.

VI. The DYN$_{LDR}$

The DYN$_{LDR}$ is a large dynamic range analog memory based on the architecture of the DYN1 analog memory chip [7]. The block diagram of the chip is shown in Figure 8

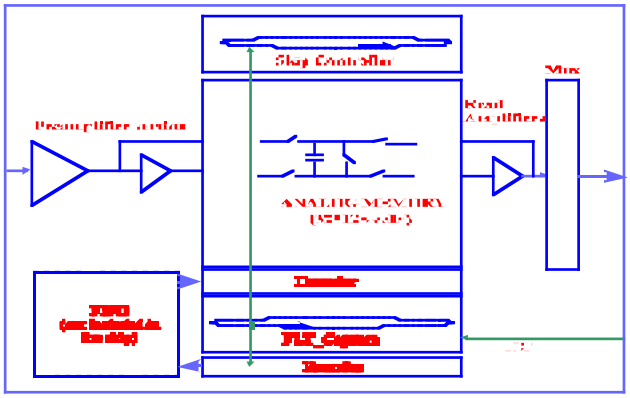

Figure 8 DYN_LDR architecture

It is capable of sampling 32 channels of sensor analog data at the full LHC

bunch crossing frequency of *40MHz*. *100%* of the data is stored for a minimum of *3.2μs* and triggered data can be stored for an indefinite time awaiting readout. Readout is performed at the lower frequency of *2.5MHz* and takes the form of an analog stream of *32* multiplexed channels from a triggered time slot. The operation is continuous Write/Read and triggers with no dead time.

The chip (photograph in Figure 9) has a total area of $55mm^2$.

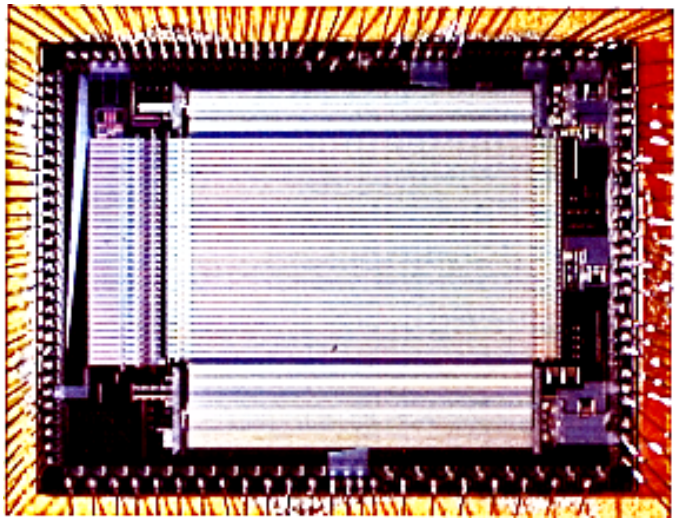

Figure 9 DYN_{LDR} photograph

The analog signal path through the memory is shown in Figure 10.

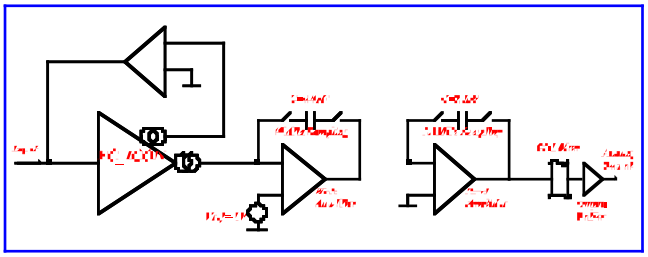

Figure 10 DYN_LDR analog signal path

A single channel consists of a FCICON preamp with a leakage current compensation feedback amplifier. The current produced is then integrated directly onto a memory capacitor by the Write amplifier. The Write amplifier itself is designed to serve both as an integrator and to control the dc level into the memory in order to obtain the maximum dynamic range. The dynamic range is determined by the virtual impedance looking into the switched capacitor memory which forms R_L for the FCICON and the linear sampling range of the switched capacitor matrix. The virtual impedance is a function of the capacitor value and switching frequency whilst the usable range is from the minimum V_{ref} setting of the Write amplifier up to the power rail minus the threshold voltage of the n_type switch transistors. The Read cycle samples the triggered capacitors and the voltage is then multiplexed and buffered out.

A data acquisition system digitises the analog data at 2.5MHz and also controls the latency of the trigger. In this way the memory can be scanned to produce a map of systematic offsets in the array . Part of this map is shown in Figure 11.

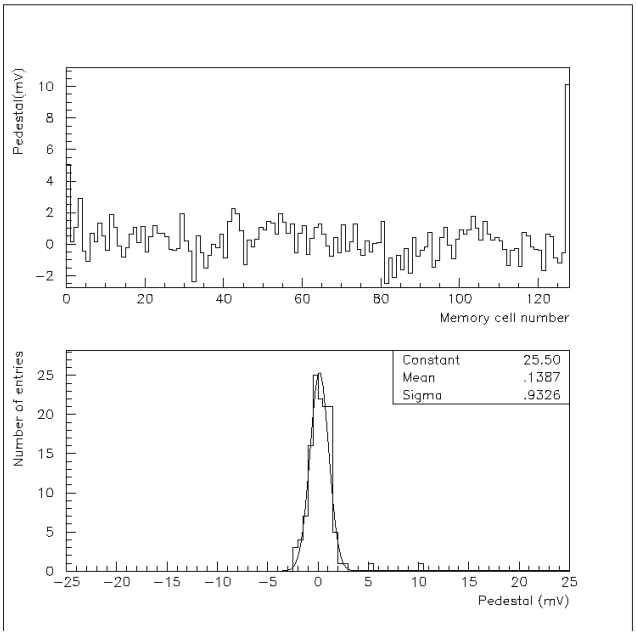

Figure 11 Pedestal variation in one channel.

The top trace shows the pedestal values of 128 cells in one channel as sampled by the ADC. There are peaks at the edge of the memory where there is a break in the symmetry of the structure. A variation in the processing at this point could play a part as could a change in dynamic parasitic pickup. The bottom trace shows the distribution of the samples. The σ_{ped} is 0.9mV. These measurements have been performed without the use of common mode baseline subtraction.

The dynamic range is shown in Figure 12. It shows a gain of 9.7mV/mip with an INL of 0.37mV (3.8%) over a 400mip linear range.

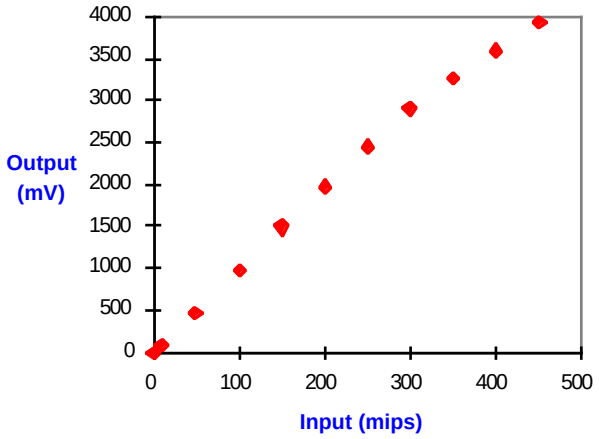

Figure 12 DYN_LDR dynamic range

VII. Summary

The design and measurements of a large dynamic range amplifier and it's integration into an analog memory have been presented. The design is optimised for performance with a 40pF detector such as is foreseen for the CMS preshower development. The performance of the chip is compatible with the specifications for a linear front end system for the CMS ECAL preshower detector. The main results are condensed in Tables 1 and 2.

LDR_amp	
Linearity	400mips
Integral Non Linearity (INL)	0.05mV
Level of input leakage current compensation	200µA
ENC	1800e+41e/pF

Table 1

DYN_LDR	
σ_{ped}	0.9mV
Signal gain	9.7mV/mip
Linearity and INL	400mips (INL 0.37mV)

Table 2

VIII. References

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