CERN - DD/DA/67/5
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March 1967

IBM 1800 - CDC 6600 Data-Link Preliminary Specifications

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1. INTRODUCTION

This link is used in order to transfer to the 6600 blocks of checked raw data collected by the 1800 during each accelerator burst. Complete calculations are performed in the 6600 and results are sent back to the 1800 via the link.

2. OUTLINE OF THE SYSTEM

2.1 The CDC 6600

The data link is connected to channel 11 (octal) of the 6600 via a data channel adapter for high speed data/status exchanges. There is also a connection to subchannel 6 of the multiplexer for slow rate status input to the 6600.

2.2 The IBM 1800

The data link is connected to digital groups with address 00 (data output) and with address 01 (status output).
It is also connected to digital group 64 (data input) and to three interrupt levels with decimal addresses 20,21,22 (future reassignment of interrupt levels is foreseen). Interrupts on levels 20 and 21 are entered as single bits. Interrupt on level 22 corresponds to process interrupt status word of 4 bits.

2.3 Data link

The data link consists of two items :

a) Data link control unit (DLC) located in the proximity of the 6600.

b) Transmission equipment consisting of cables, transmitters, receivers and special interface circuits. Eight cables of the type described in CERN report 65-5, section 2.1, are employed and therefore a total of 80 signal lines is available.

The cables are laid out in three sections, one from the 6600 area to the East compressor building, another from the East compressor building to the South Hall, the last one from the East compressor building to the East Hall (fig. 1).

A junction box in the East compressor building is used in order to link the 6600 area to either the East Hall or the South Hall area, depending on the location of the 1800.

Part of the electronics of the DLC unit is common to the existing SDS 920 data link (CERN report 65-40 and internal DD report DD/DA/66/10).

The common parts are : 6600 control, data conversion register, or to DCA, MUX interface, power control.
Parts which are not in common are :

- 920 control, O/P flags, gates to 920, parity circuit. 920 input flags - for one link.
- 1800 control, O/P flags, gates to 1800, 1800 input flags - for the other link.

3. OPERATION

3.1 Status information from the 1800 to the 6600.

Status information is transferred to a register of the DL control (input flag register) when an XIO instruction is executed which specifies one word in memory having the following characteristics :

- Bit 2^{15} always present
- Bits 2^{0}-2^{5} variable, they express the value of the status transmitted.

The address of the digital output used is 01 and this code is either contained in the data word specified by the IOCC or in the second word of the table depending on whether direct programme control or data channel control are used. Bits 2^{0}-2^{5} are stored in the input flag register, which can be interrogated by the 6600 P.P. by means of a status request function followed by a 1 word input. Bits 2^{0}-2^{5} of the latter word represent the same original 1800 bits.
The register is reset to zero only when the 1800 executes a transfer with bit 2^{15} equal to 1 and bits 2^{0}-2^{5} equal to zero.
Bit 2^{7} of the 6600 status input word is set by the data link control, whenever the data link is operational which implies that :

a) Data link II operational push button is on.

b) Power is on.

c) DLC to DCA connections are made.

Table of fig. 2 shows a list of input flags with their conventional meaning.

Note : Output digital group 01 of the 1800 is used by other devices connected to the 1800 (e.g. Display). When this device is connected, the above-mentioned output works in request/acknowledge mode, which means that :

a) Write mode control signal is kept at "0" level.

b) Write request is continuously provided by the display system.

c) Write acknowledge and write pulse are sent out with the status word.

When the display is not connected the conditions are the following :

a) Write mode control signal is kept at "1" level.

b) Write pulse is sent out with the status word.

In both cases the status output is initialized by the 1800 performing an Initialize Write Single Address (Area=01100, Function=101, Modifier=01000000).

3.2 Status/control information from 6600 to the 1800

A control/status word of 6 bits (2^0-2^5) is transferred from a 6600 peripheral processor to a register of the DL control (output flag register) when a function instruction is executed.

The function word has the following characteristics. Bit 2^9 (synchroniser address) always present. Bit 2^6 (data link address) always present. Bits 2^0-2^5 variable according to the control 02 the status which is transmitted. Table of fig. 3 shows a list of output flags with their conventional meaning. OF2-4, OF2-5, OF2-6 are commands which prepare the data link electronics, they do not affect in any way the 1800. OF2-1 and OF2-2 cause single 1800 interrupts respectively on level 10 (decimal address 20) and on level 11 (decimal address 21). OF2-7 to OF2-10 have the following characteristics : Bits 2^9, 2^6, 2^1, 2^0 are always present. Bits 2^2, 2^3, 2^4, 2^5 can be selected to give any of 16 possible status words, which will cause an 1800 interrupt on level 12 (decimal address 22). As soon as this interrupt request is recognized its PISW word can be read into the A register of the 1800 and this makes possible to determine which combination of the four bits has caused the interrupt.

Note : Only pulses or level changes from "0" to "1" are recognized by the 1800 as interrupts. This carries two consequences :

a) 6600 programs should provide reset of the output flags by executing a function with function word equal to 1100 whenever two subsequent identical flag combinations are set. This precaution is not necessary for OF2-4, OF2-5 and OF2-6 which are only used by the data link control.

b) "Link operational" being a static condition cannot be easily recognized by interrupt on level 12. Suggestion is made that the 1800 should interrogate the 6600 by means of an input flag to find out whether the link is operational. The 6600 will then set an output flag to specify this condition.

3.3 Data transfer from the 1800 to the 6600

Blocks of 16 bit words are transferred from the 1800 via digital address 00.

An XIO instruction is executed with an IOCC containing the following information :

- Address of a data table
- Area = 01100
- Function = 101 (initialize write)
- Modifier = 01000000 corresponding to "write single address" mode.

The table should contain

Word no. 1 - Scan control = 00 (single scan of table and stop with an interrupt) or scan control = 01 (no interrupt and test if channel is busy).

- Word count = n+1 (n = number of 16 bit words in the table)

Word no. 2 - Address of digital output e.g. 00

Following words - Block to be transferred.

The transfer of words will be executed in a request/acknowledge mode in the following way :

a) Write mode control level is at "0" level

b) Write acknowledge signal is set to "1" by the 1800 when write is initialized together with the "write" pulse, while the first output word is sent out on the data lines.

c) The data link answers not earlier than 8 µs from the time when the write pulse is sent out with a write request which causes the write acknowledge to be reset to zero.

d) A second word is sent out with a write pulse while write acknowledge is set to one again.

e) Every word of the block is transferred this way.

The end of the block is recognized by an interrupt as specified by the scan control.

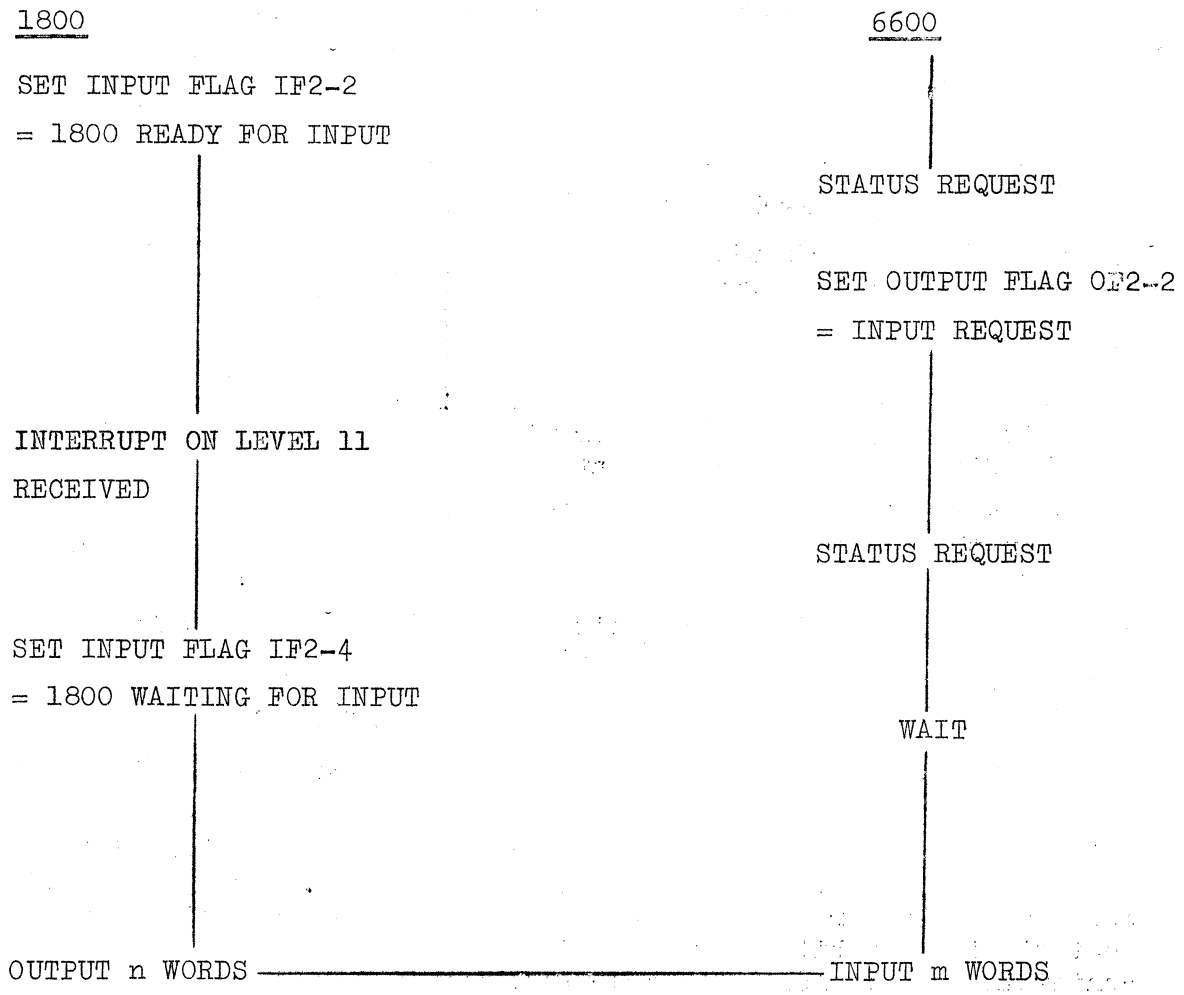
Write pulses cause the accompanying 16 bit word to be stored in the conversion register of the data link control. From there two words are transferred to the 6600 PP, the first containing the 4 most significant bits of the original 16 bit word, the second containing the 12 least significant bits.

The following sequence of instructions is necessary at the PP end :

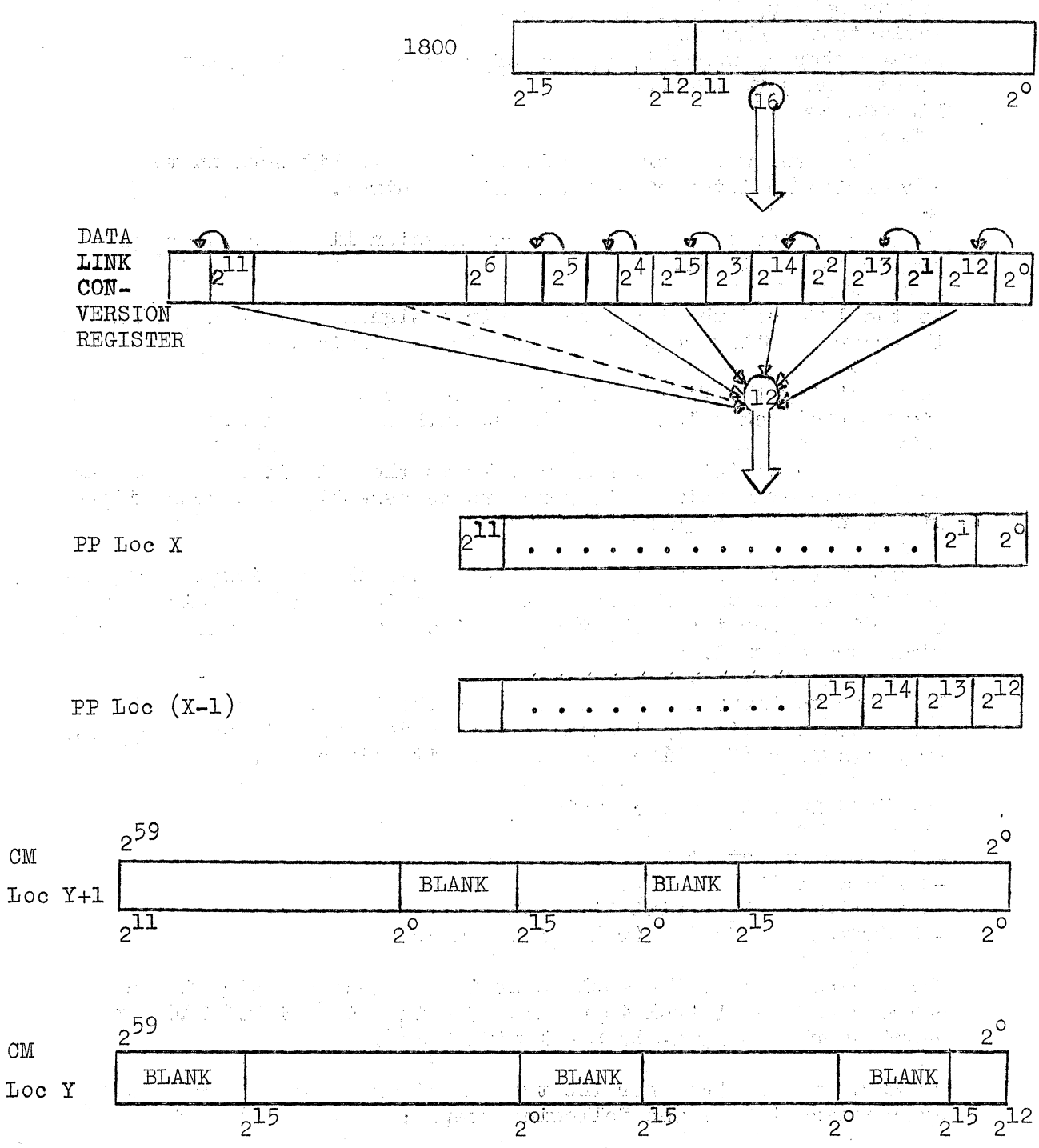
Input select
Activate channel
Load number of words = m into A register ($m \geqslant 2$ n)
Input (IAM)
Wait for disconnect

Absence of write acknowledge signals from the 1800 for a period of about 100 µs will cause a disconnect to the 6600 and the latter will terminate the transfer independently from the amount of words transferred.

Previous to the transfer the two computers should be brought into synchronisation by the following steps :



The following sketch shows the disassembling and assembling of words from the 1800 to the 6600 central memory :



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3.4 Data transfer from 6600 to 1800

The PP programme executes the following sequence of instructions :

Output select
Activate the channel
Load number of words to be transferred = m into A register
Output (OAM)
Disconnect

The first two words are assembled into a 16 bit word in the conversion register of the data link control.

The word is sent out onto the transmission lines together with a read request signal.

At the 1800 end the Read Mode Control signal must be at "0" level in order to allow request/acknowledge operation.

On receiving the first word with a read request the 1800 answers with a read acknowledge signal and with a read pulse.

The read acknowledge signal travels to the data link control and causes a second pair of PP words to be assembled and transmitted with a new read request.

If the interval of time between read acknowledge signals from the 1800 is longer than 100 µs a disconnect is generated which causes the 6600 to terminate the transfer independently of the number of words transferred.

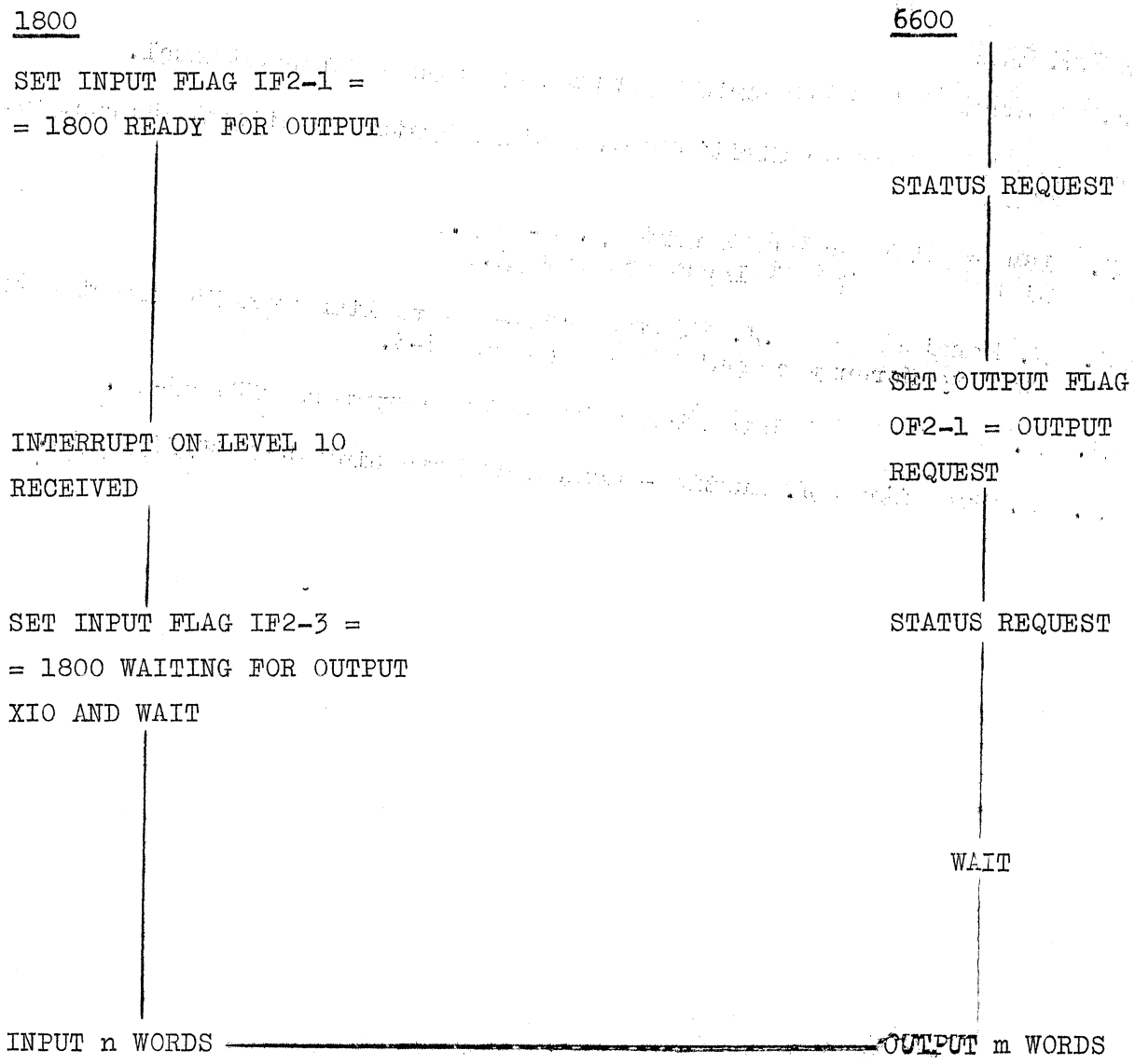
In order to input the block of words the 1800 executes an XIO instruction similarly to what has been described in paragraph 3.3 from transfer of 0 block in the opposite direction.

The IOCC in this case contains

- Address of data table
- Area = 01011
- Function = 110 (initialize read)
- Modifier = 01000000 (read single address)

The second word of the table contains 64 decimal which is the address of the digital input used for the data link. The word count should be equal to $n + 1$ with $n = \frac{m}{2}$.

Previous to the transfer the two computers should be brought into synchronization by the following steps :


1800
SET INPUT FLAG IF2-1 =
= 1800 READY FOR OUTPUT
INTERRUPT ON LEVEL 10
RECEIVED
SET INPUT FLAG IF2-3 =
= 1800 WAITING FOR OUTPUT
XIO AND WAIT
INPUT n WORDS
6600
STATUS REQUEST
SET OUTPUT FLAG
OF2-1 = OUTPUT
REQUEST
STATUS REQUEST
WAIT
OUTPUT m WORDS

References

1. Control Data 6600 Series Computer Systems Reference Manual.

2. IBM 1800 Data Acquisition and Control System Functional Characteristics.

3. IBM Special Feature Report No. 2-0016.
High Speed Digital Input and Output.

4. F. Marciano and H.J. Slettenhaar - A data link from PS experimental area to Mercury computer CERN report 65-5.

5. F. Marciano - A data link between two computers CERN 65-40.

6. S. Bunodière, J. Austin - Manuel du Data Link CERN DD/DA/66/16.

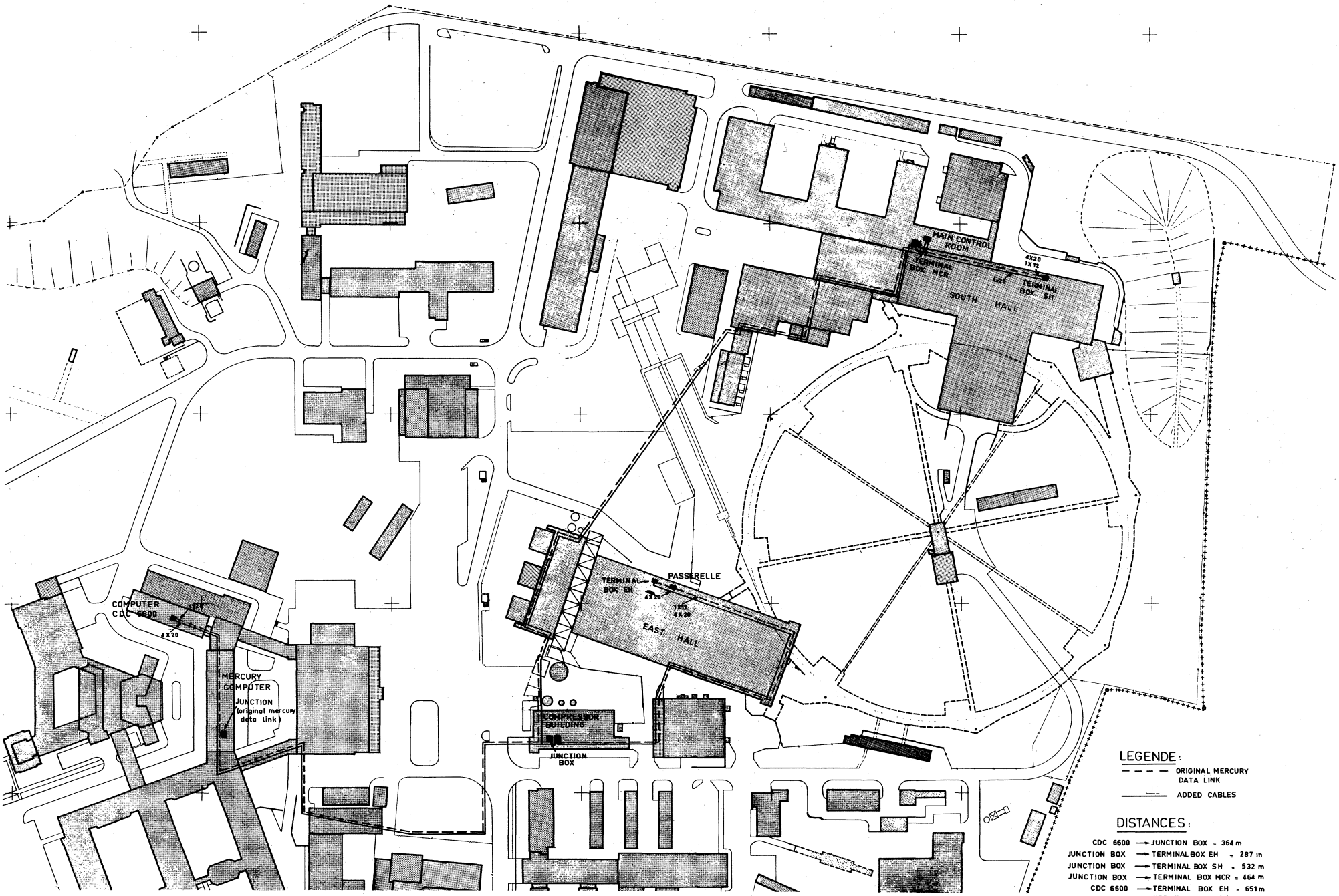

MAIN CONTROL ROOM
TERMINAL BOX MCR
4X20
1X12
TERMINAL BOX SH
SOUTH HALL
PASSERELLE
TERMINAL BOX EH
4X20
1X16
4X20
EAST HALL
COMPUTER CDC 6600
4X20
MERCURY COMPUTER
JUNCTION (original mercury data link)
COMPRESSOR BUILDING
JUNCTION BOX
LEGENDE:
ORIGINAL MERCURY DATA LINK
ADDED CABLES
DISTANCES:
CDC 6600 → JUNCTION BOX = 364 m
JUNCTION BOX → TERMINAL BOX EH = 287 m
JUNCTION BOX → TERMINAL BOX SH = 532 m
JUNCTION BOX → TERMINAL BOX MCR = 464 m
CDC 6600 → TERMINAL BOX EH = 651 m
CDC 6600 → TERMINAL BOX SH = 896 m

Fig. 1

INPUT FLAGS

NAME	MEANING	SET BY 1800 O/P STATUS WORD BIT	TESTED BY MUX, DCA	DCA BITS	DCA STATUS RESPONSE	MUX BITS
IF2-1	1800 READY FOR O/P	2^0	MUX DCA	2^0	1	2
IF2-2	1800 READY FOR I/P	2^1	MUX DCA	2^1	2	3
IF2-3	1800 WAITING FOR O/P	2^2	DCA	2^2	4	
IF2-4	1800 WAITING FOR 1/P	2^3	DCA	2^3	10B	
IF2-5	ANY STATUS	2^4	MUX DCA	2^4	20B	5
IF2-6	ANY STATUS	2^5	DCA	2^5	40B	
IF2-8	LINK OPERATIONAL	SET BY DLC	MUX DCA	2^7	200B	6

Fig. 2

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OUTPUT FLAGS

NAME	MEANING	SET BY	FUNCTION CODE	CAUSES	INTERRUPT LEVEL STATUS WORD BITS
OF2-1	6600 REQUESTS O/P	DCA	1101 B	INTERRUPT LEVEL 9	
OF2-2	6600 REQUESTS I/P	DCA	1102 B	INTERRUPT LEVEL 10	
OF2-3	STATUS AVAILABLE	DCA	11X3 B (*)	INTERRUPT LEVEL 11	
OF2-4	O/P SELECT	DCA	1104 B	DATA LINK SELECTION	
OF2-5	I/P SELECT	DCA	1110 B	DATA LINK SELECTION	
OF2-6	STATUS REQUEST	DCA	1114 B	DATA LINK SELECTION	
OF2-7	ANY STATUS	DCA	1107 B	INTERRUPT LEVEL 11	2^0
OF2-8		DCA	1113 B	INTERRUPT LEVEL 11	2^1
OF2-9		DCA	1123 B	INTERRUPT LEVEL 11	2^2
OF2-10		DCA	1143 B	INTERRUPT LEVEL 11	2^3

(*) BITS 2^0, 2^1, 2^6, 2^9 always present, BITS 2^2, 2^3, 2^4, 2^5 represent a variable code $\neq 0$

INTERRUPT	INTERRUPT LEVEL	DECIMAL ADDRESS	HEXADECIMAL ADDRESS
9	10	20	14
10	11	21	15
11	12	22	16

Fig. 3