CERN BIBLIOTHEQUE
SCP
CERN-DRDC 93-5
93-5
Add. 5

Nuclear Instruments and Methods in Physics Research 00 (1992) NIM00151
North-Holland

GALLEY PROOFS
NIM. IN PRESS

S

CERN-DRDC 93-5, ADD 5
PROPOSAL P48
8/ 1/ 93

A fast integrated readout system for a cathode pad photon detector

M. French and M. Lovell
Rutherford Appleton Laboratory, Chilton, UK

E. Chesi and A. Racz *
CERN, Geneva, Switzerland

J. Séguinot and T. Ypsilantis
College de France, Paris, France

R. Arnold and J.L. Guyonnet
CRN / Louis Pasteur University, Strasbourg, France

J. Egger and K. Gabathuler
Paul Scherrer Institute, Villigen, Switzerland

CERN LIBRARIES, GENEVA
SC00000160

Received 20 July 1992

A fast integrated electronic chain is presented to read out the cathode pad array of a multiwire photon detector for a fast RICH counter. Two VLSI circuits have been designed and produced. An analog eight-channel, low-noise, fast, bi-polar current preamplifier–amplifier and discriminator chip serves as the front-end detection electronics. It has an rms equivalent noise current of 10 nA, 50 MHz bandwidth with 10 mW of power consumption per channel. Two analog chips are coupled to a digital sixteen-channel CMOS readout chip, operating at 20 MHz with a power consumption of 6 mW per channel. Readout of a 4000 pad sector requires 2–3 μs, depending on the number of hit pads. The full RICH counter is made up of many such sectors, read out in parallel. The minimum time needed to separate successive hits on the same pad is 70 ns. The conception of the digital chip and its properties are fully presented in this report. The analog chip is described in less detail since it will be fully covered in a forthcoming paper.

1. Introduction

Particle identifying RICH (ring imaging Cherenkov) counters at high-luminosity hadron colliders (Tevatron, LHC, SSC, Eloisatron) will require fast, pixel photon detectors sensitive to UV light and capable of operation in a high multiplicity environment at interaction rates up to 100 MHz. The presently available gaseous photosensors are vapours of the organic molecules TEA, TMA or TMAE mixed with a transparent amplifying carrier gas such as methane, ethane or isobutane [1]. Newly demonstrated alternate photosensors are the reflective photocathodes of CsI or CsI/TMAE (a CsI film with an adsorbed layer of TMAE) made by vacuum deposition onto a cathode pad pixel array [2]. Since the produced photoelectrons are reflectively injected back into the atmospheric pressure carrier gas, the same amplifying structures used for gaseous tracking detectors (MWPC or PPAC) can also be used to detect single electrons from photocathodes.

These photodetectors are fast with small time dispersion ($\sigma_t \approx 10$–20 ns for TEA or TMA, $\sigma_t \approx 1$ ns for CsI or CsI/TMAE) but they require a large number of pixels (electronic channels) to uniquely determine the photoconversion points. They are well suited for use at high-luminosity hadron colliders (or at electron–positron B factories) because the fast timing avoids mixing events from successive beam crossings. Interaction rates up to 100 MHz are expected at LHC but data acquisition must be kept ≤ 10 kHz hence, to obtain 90% live time, readout must be effected in ≤ 10 μs. This will require that subsectors of the detector be

* ① Also from Paul Scherrer Institute, Villigen, Switzerland.

0168-9002/92/$05.00 © 1992 – Elsevier Science Publishers B.V. All rights reserved

214406

read out in parallel. To limit the number of readout and control lines, detection and readout electronics will be implanted on the detector. To achieve these goals, we fabricate application specific integrated circuits (ASICs) using the very large scale integration (VLSI) technique.

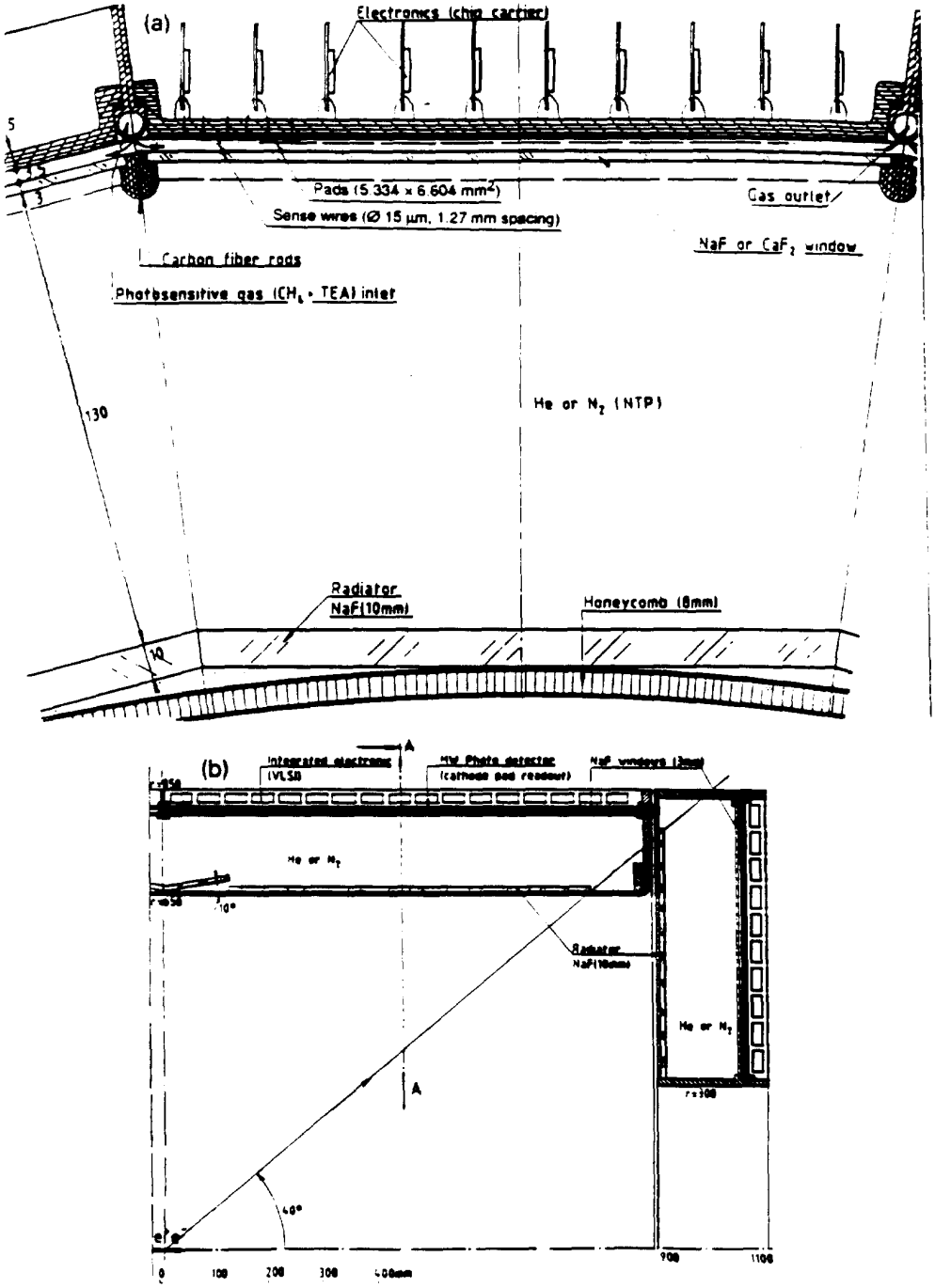


Fig. 1. The RICH counter for a B-meson factory: (a) transverse and (b) longitudinal views. The essential elements shown are the crystal radiator, the photodetector and the readout electronics.

At Rutherford Appleton Laboratory, we have developed two custom ASICs for fast readout (a few microseconds) of a RICH photodetector designed originally as part of the Universal Research Instrument (URI) for a proposed B-meson factory project in Switzerland [3]. The front-end analog chip is an eight-channel, low-noise, fast, bi-polar current preamplifier–amplifier and discriminator delivering a digital current output into a sixteen-channel CMOS digital readout chip. The characteristics of the analog chip are partly given here and will be discussed more completely in a later paper [4]. The chip can detect induced pad currents with threshold variable between 10 nA (noise) and 160 nA, adjustable by a 4-bit DAC sited on the digital chip.

The design and operation of the digital CMOS chip is fully presented in this paper. These chips are connected to form a two-dimensional array of 3840 channels per sector. They are read out with zero suppression in several microseconds, depending on the number of hit pixels. Many such sectors, which comprise the full RICH counter, will be read out in parallel. This same electronics can also be used for fast digital readout of pixel elements from any sort of tracking detector, i.e. silicon, gas microstrip or MWPC, and even a liquid xenon vector calorimeter [5].

After a short description of the Fast RICH Project, which motivated this development, we give the basic characteristics of the photodetector. The mounting and connections of the readout electronics are also discussed in order to give an overall view of the electronic problems and their solutions. A general outline of the electronic architecture is given and operation of the digital chip is described in detail. Tests of the readout chain are then reported followed by a summary and conclusions.

2. The fast RICH detector

2.1. Mechanical conception of the detector

The fast-cathode pad photodetector of a RICH counter (fig. 1) has been extensively tested and simulated as reported in ref. [1]. This counter was designed to give π/K identification up to ≈ 2.5 GeV/c (3σ standard deviations) with TEA as the gaseous photosensor and NaF as the proximity focused radiator [6]. The lever-arm distance between detector and radiator is 130 mm and the crystal radiator is 10 mm thick. Other crystals, such as MgF_2 or LiF in the same geometry, have since been shown to give π/K discrimination up to 3 to 4 GeV/c with gaseous TEA and 4 to 5 GeV/c with gaseous TMAE or solid CsI/TMAE photosensors [6].

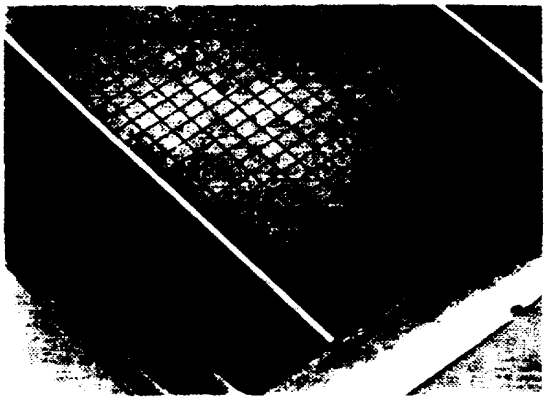
This RICH counter, which extends between cylindrical radii of 0.65 and 0.85 m, is made of polygonal sectors (0.9 m long half-barrel staves) subtending 12° of azimuth. The barrel is closed at both extremities by end-cap counters of the same design. Tight interfacing of the barrel and end-cap radiators ensures that no images are lost in this region. These modular photodetectors have detection and readout electronics at the outer radius. A charged particle passing through the radiator crystal produces many Cherenkov photons which propagate through the transparent lever-arm region (N_2 gas) and are absorbed in the photodetector gas. The detected photons form a parabola-like image (not a ring) containing 10–20 image points (photoelectrons). The radiator thickness (≈ 10 mm) is fixed by the needed number of image points and the lever-arm distance (≈ 130 mm) by the needed Cherenkov angle resolution σ_θ.

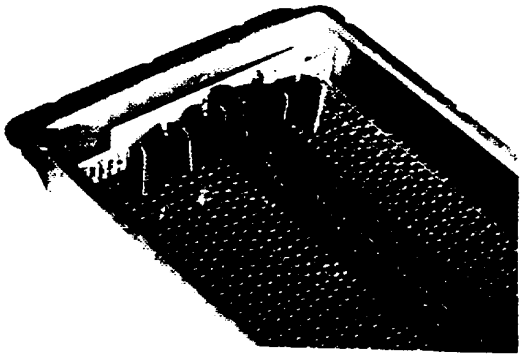
The RICH counter photodetectors (fig. 1) are asymmetric MWPCs with an exterior pad array of 30 columns (constant x) and 128 rows (constant y) totalling 3840 independent pads per sector, individually read out to define the image points.

The pad sizes ($\Delta x = 5.33$ mm, $\Delta y = 6.60$ mm) are chosen so that the detection point (x, y) contribution to σ_θ is less than the emission point (z_e) error due to the radiator thickness [i.e. $\sigma_\theta(x)$, $\sigma_\theta(y) \leq \sigma_\theta(z_e)$] and to give approximately equal space-point resolutions ($\sigma_x \approx \sigma_y \approx$ 1 mm) [1]. The detector operates in a mixture of methane saturated with TEA at 14°C ($p \approx 40$ Torr, $l_{ph} \approx 0.5$ mm). Its 3 mm gas thickness absorbs 99.8% of the Cherenkov photons in the TEA response region of 140–165 nm, and causes a dispersion of photoelectron arrival (drift) times of $\sigma_t = l_{ph}/v_d \approx 10$–20 ns.

Gold-plated tungsten anode wires, 15 μm in diameter, are strung along the barrel axis (y) with a pitch of 1.27 mm at a distance $d = 0.5$ mm from the pad plane so as to maximize the induced pad signal [1]. The wire spacing is a (1/4) sub-multiple of the pad width (Δx), thus wire positions scale for each pad column, ensuring similar pad response over the full sector surface. The wires are glued to 0.5 mm thick insulating ceramic spacers at 10 cm intervals (16 pad lengths) to guarantee good accuracy on wire position (wire–wire and wire–cathode) and mechanical stability hence more uniform gas gain along the wire since electrostatic deflection is minimized.

The photodetector is separated from the lever-arm region by a CaF_2 window (five 18 cm long segments, 3.5 mm thick with 80% transparency in the TEA response region) glued onto a rigid aluminium frame fixed to, but electrically insulated from, the main support structure. The clear window areas of the aluminium frame represent 88% of the sector surface. This construction allows detector replacement without disturbing the gas in the lever-arm region and provides mechanical rigidity. The inner surface of the CaF_2





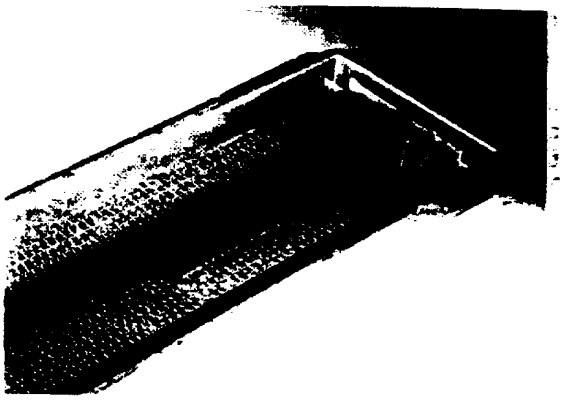


Fig. 2. (Top) View of the detector side of the cathode pad array and (bottom) the rear side of the array.

Fig. 4. The readout columns seen from: (top) the analog chip side, and (bottom) the digital chip side.

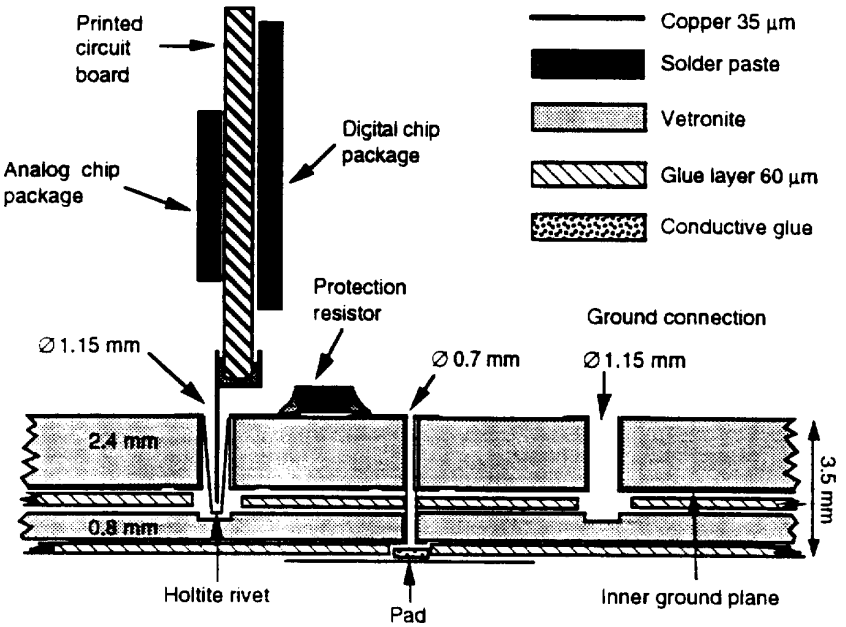


Fig. 3. A side view of the cathode pad plane with feedthroughs, inner ground plane and pads.

windows (facing the MWPC wires) is coated with 100 μm wide silver traces, running along the x direction, with 1.5 mm pitch (93% transparency). These traces are set at potential U_w (via the aluminum frame) and define, along with the anode wire potential U_a and the cathode pad potential U_k, the electrostatic field of the MWPC unit cell. An outer aluminium tray-like structure supports the cathode pad array and houses the gas inlets and outlets.

2.2. The cathode pad rear plane and implantation of the electronics

The cathode pads are etched onto the front side of the photodetector back plane (figs. 2 and 3). Connections from pads to electronics pass through a ground plane built into a vetronite sandwich (fig. 3). Pad electronics is mounted vertically inside the aluminium tray, on multilayer printed-circuit boards (PCBs) which transmit power supply, control and data lines.

As the density of electronic channels is still modest (5.33×6.60 mm^2), the chips are housed in standard PLCC packages (44 and 68 pins for analog and digital chips, respectively) mounted on multilayer PCBs using the SMD technique. Interchangeable cards of 64 channels (4 digital chips) are plugged on the back side of the back plane in 15 columns per sector. Each column thus contains four daisy-chained cards comprising 256 channels which are symmetrically connected to two adjacent columns of 128 pads each.

The back plane is a composite of two vetronite sheets (0.8 and 2.4 mm thick) sandwiching a thin copper foil (35 μm thick) and glued onto the rigid 1 mm thick aluminium tray (fig. 4). The tray, made by forming and soldering, has excellent planarity with measured variation of the wire to cathode distance $\sigma_d < 20$ μm. The perimeter of the Cu foil is connected to the grounded tray with conducting silver glue to provide electrostatic shielding of the pad array and an excellent ground for the sensitive fast analog preamplifiers. The tray itself is grounded by metal-to-metal contact with the main support structure. The connection between a pad and its analog preamplifier is effected through metallized holes which pass through the grounded copper foil (fig. 3).

Pad fabrication is finally achieved by gluing a 35 μm thick copper foil onto the front vetronite surface and locally connecting the metallized holes to the foil with conductive glue (deposited by serigraphy), followed by chemical etching of the pad boundaries (fig. 3).

3. A general description of the electronic architecture

The RICH counter for the B-meson factory project requires such a large number of electronic channels (3.4×10^5) that the need for custom designed ASICs is

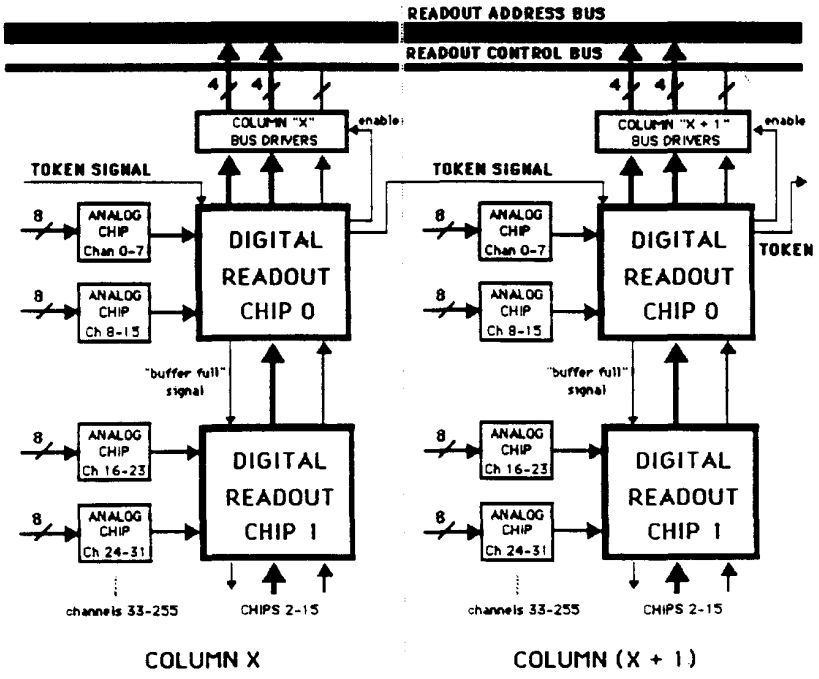


Fig. 5. A schematic of the electronic readout architecture.

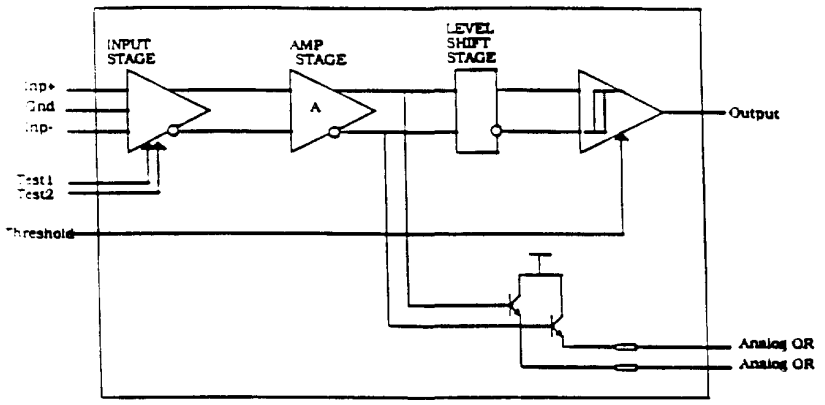


Fig. 6. One-channel block diagram of the analog chip.

obvious. Two circuits have been designed using the VLSI technique:

(a) An analog 8-channel, fast, bi-polar, current preamplifier-amplifier and discriminator chip.

(b) A digital 16-channel, fast readout CMOS chip.

A schematic diagram of the electronic architecture is shown in fig. 5.

The complex functions of the digital chip require relatively large silicon surface area hence, to keep power consumption low, CMOS technology is preferred. However, to attain fast response in the analog chain, bi-polar technology is indicated. Although integration of CMOS and bi-polar technologies on the same chip is now possible (it was not so when the project started), this option is rejected because coupling (possibly large) between the low-level input of the fast analog chain with the readout TTL clock signals could lead to an unacceptable loss of input sensitivity.

Each digital CMOS chip forms a chip set with two analog bi-polar chips, placed oppositely on the PCBs (figs. 3 and 4). These cards have eight layers to carry the voltage supplies, data bus and control lines. Two of these layers carry return currents from analog and digital chips to ground to suppress crosstalk between the low-level analog input and the digital chip TTL clock lines. Each of the 15 columns have 16 chained digital chips (four daisy-chained cards) forming an array of 240 digital readout chips per sector. They are connected to a common output (top bus) via drivers located at the top of each column. Individual pads are

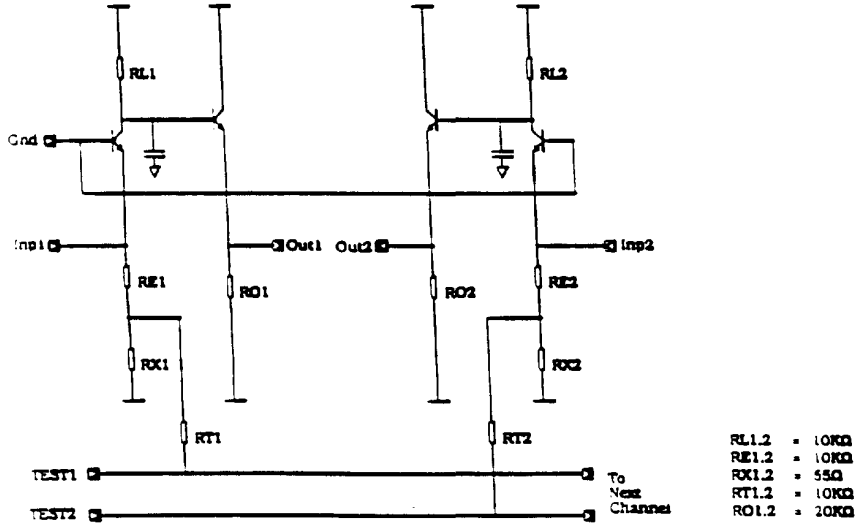


Fig. 7. The analog chip differential common base input stage with test inputs.

connected to the input of the analog chip with a 270 Ω resistor in series for protection against detector sparking (fig. 3).

4. The analog chip

4.1. General description and characteristics

An analog eight-channel, low-noise, bi-polar current preamplifier, amplifier and discriminator IC was designed with the bandwidth limited to 50 MHz. This limit optimizes the signal-to-noise ratio relative to the response time of the detector while keeping the power dissipation to ~ 10 mW/channel.

The chip design is based on a differential architecture and works in common mode noise rejection so as to overcome stability problems inherent in low input-level circuits. Each channel has a differential input and amplification stage, a shift-level stage and a differential discriminator stage output. Each chip also has biasing networks to set the discriminator threshold and to control the internal bias. A schematic diagram of one channel is shown in fig. 6. Each input stage has positive and negative connections to allow its use with either pad or wire signals (fig. 7). To minimize crosstalk, a separate ground connection is made for each channel. The input stage consists of a differential pair of npn transistors connected in a common base configuration with an input impedance of ~ 100 Ω and a transresistance of 10 kΩ (defined by the collector resistors). Emitter followers are used between the input stage and the amplification stage to keep the collector stray capacitance low (≤ 1 pF), thus enhancing gain and time response. A dc noise current $\sigma_n \approx 10$ nA is measured, which, for an RC response time of $\tau = (10\ \text{k}\Omega)\ (1\ \text{pF}) = 10$ ns, corresponds to an equivalent rms input noise charge of 0.1 fC (625 e) for input pulse widths $\geq 3\tau$.

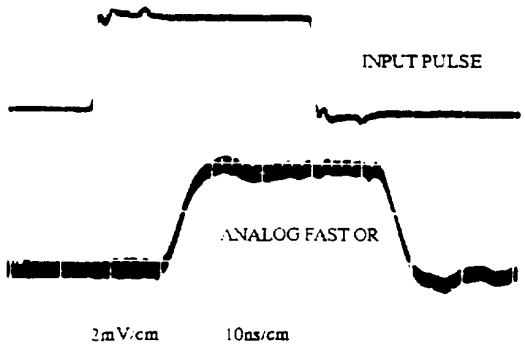


Fig. 8. The analog chip input current and the output fast-or (on 50 ω) showing 7 ns rise time.

Positive and negative inputs, common to the eight channels of the chip, have been built-in for test purposes. From HSPICE simulation, the total gain of the differential amplification chain (to the discriminator) is 1.37 mV/nA (62 dB). The chip is fabricated by Plessey Electronics.

After the amplification stage, the signals pass through a level-shift circuit to the output discriminator controlled by a single threshold level, common to the 16 channels of the chip set. The discriminator is designed to cancel the dc offset inherent to any differential circuit and to compensate long-tailed signals from the detector. A small amount of hysteresis is included to obtain clean switching of the output, thus enhancing operational stability.

To prevent feed-back crosstalk with the input stage the discriminator delivers a current output signal rising from 100 to 300 MA, for a digital input impedance of 550 Ω. Also to reduce crosstalk, the analog stages and discriminators have separate voltage supply and ground lines.

The discriminator threshold is fixed by an input current I_{th}, adjusted by the 4-bit DAC register common to the 16 channels of the chip set. This register is integrated in the digital chip and set by the data acquisition (DAQ) computer during system initialization (section 5.7.2). The input current threshold is adjustable from 1 to 16 times the base threshold current (e.g. 12.5 μA), thus allowing large flexibility to optimize signal-to-noise and to cope with detector hot spots or noisy chips.

An additional feature of the chip is the availability of an analog fast-or output common to the eight channels of the chip.

4.2. Characteristic test results

A detailed description of this chip with all test data will be given in a later paper [4]; however, here we give essential results needed to understand the chip function. A typical input pulse with the analog fast-or output is shown in fig. 8. The rise time of the analog fast or is ~ 7 ns, in agreement with the 50 MHz measured bandwidth of the amplification stage. Discrimination curves for the 8 channels of a chip (mounted on a test board not connected to the detector pads) are shown in fig. 9. The detection efficiency is plotted versus the input current for a fixed discriminator threshold. The derivative of each curve is a Gaussian whose mean current is the threshold (50% efficiency point) and whose rms width is the input noise current. The equivalent input current threshold and dispersion for 100 chips (800 channels) is $I_{in} = 147 \pm 20$ nA (fig. 10). The input noise current and dispersion is $\sigma_n = 9.3 \pm 1.8$ nA, also for 800 channels (fig. 11). A linear variation of the noise current σ_n with detector

capacitance is shown for a single channel in fig. 12. Its intercept and slope are 10 nA (625 e) and 0.20 nA/pF (12.5 e/pF), respectively. During detector operation the threshold will be set to a level $\geq 3\sigma_n$.

Once an input signal I_{in} passes threshold, the output current of the analog chip switches from 100 to 300 μA. This threshold is set by a DAC value which digitally fixes the threshold current (i.e. $I_{th} = 12.5$ μA

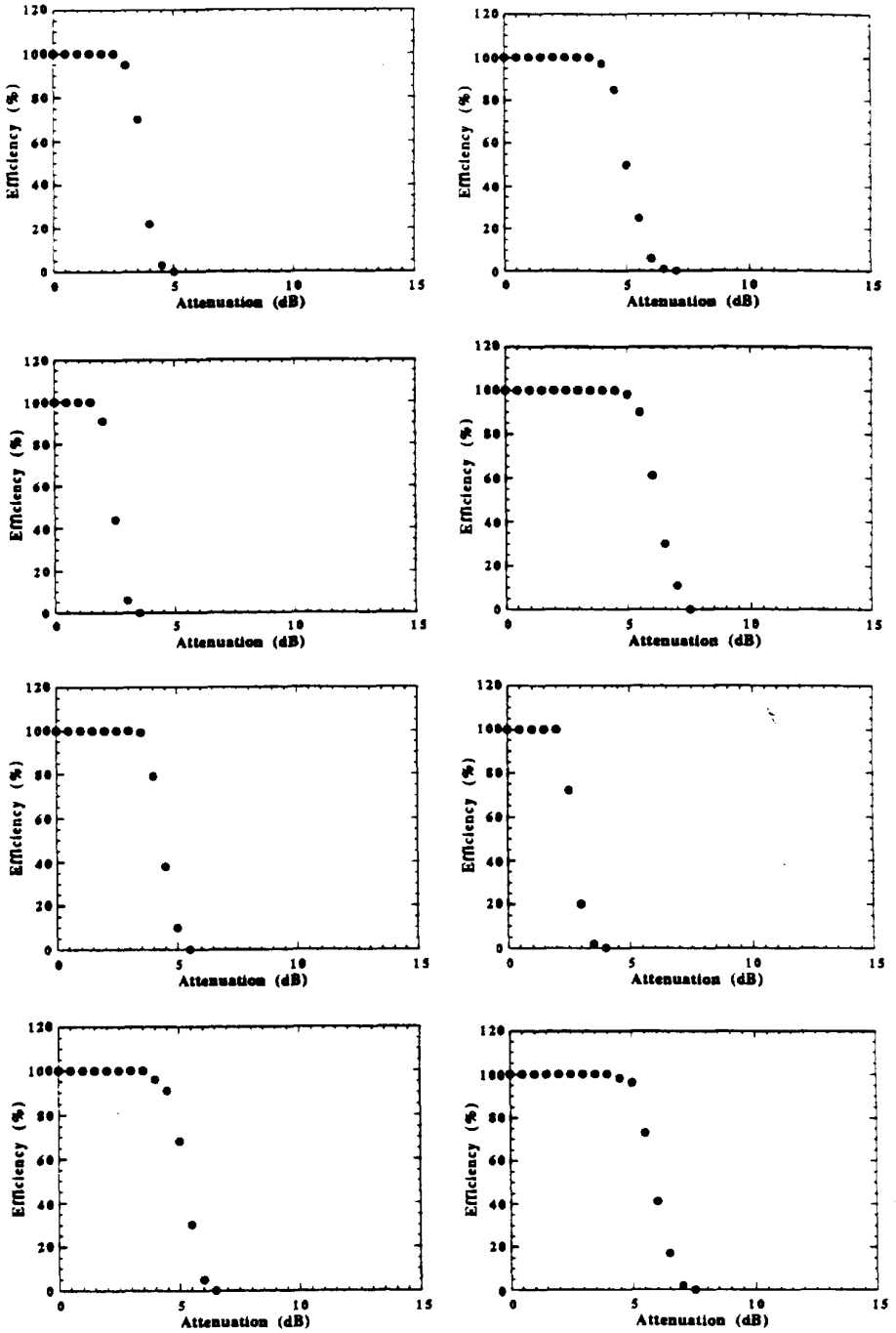


Fig. 9. The discriminator efficiency versus input current for 8 channels of an analog chip. The unattenuated input current was 378 nA with a width of 150 ns. The threshold current set for the analog chip was $I_{th} = 125$ μA ($I_{in} = 200$ nA, DAC = 10).

× DAC), which, in turn, analogically fixes the I_{in} threshold. As example, in fig. 10, a DAC value of 7 corresponds to $I_{in} = 147$ nA. Due to amplifier variations, I_{in} may vary from channel to channel but I_{th} is fixed by the DAC value (for all channels of the chip set).

5. The digital cmos chip and the readout principle

The digital CMOS chip was designed for fast readout of sparse data appearing on the detector when a good event is selected by the first-level trigger (time delay ≤ 1.32 μs). A schematic of the readout chain is shown in fig. 13. The chip was fabricated by European Silicon Structures using a 1.5 μ CMOS process.

5.1. Data acquisition

Since the image quality of a RICH counter (hence its particle identification power) depends on its ability to reject background (i.e. non-coincident events, electronic noise and detector noise), data are accepted for readout only during the time duration of strobe generated by the triggered event. Here and below, CAPITALIZED words will indicate the functional units of the chip and **bold** words represent signals or flags. Strobe width (Δt) is adjusted to accept the full spread of photoelectron arrival times ($\Delta t > 3\sigma_t = 30$–$60$ ns). Since **trigger** for a good event is derived (after logical treatment) from signals from other detector components, it arrives much later than the digital current output of the analog chips. To compensate this delay, the input data are pipelined in a 64-element asynchronous 50 MHz SHIFT REGISTER (fig. 13). These constantly shifting registers are loaded only once per input pulse by a 20 ns wide TTL pulse formed by shaping the digital output current of the analog chip synchronized to the 50 MHz CLOCK. Each chip either has its own 50 MHz oscillator driven by its own external quartz or an external clock signal is distributed to each of the 4 chips of a card. In either case, the pipeline delay is $(64 + 2) \times 20$ ns = 1320 ns, the two added clock pulses are needed to generate the 20 ns input pulses.

For each channel which has received **end pulse** from SHIFT REGISTER during strobe, the chip latches a logical value into the input memory of PRIORITY ENCODER. Asynchrony between the 50 MHz CLOCK and the input data causes an rms time dispersion $\sigma_a = 20$ ns$/\sqrt{12} = 6$ ns, comparable with the TEA time dispersion $\sigma_t \geq 10$ ns. At this point data acquisition is terminated, i.e. selected data from all channels have been memorized.

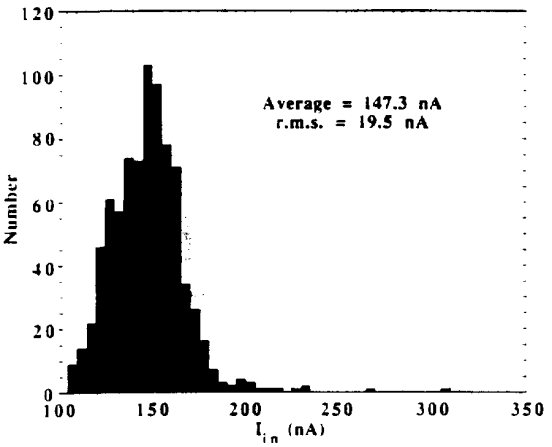


Fig. 10. The equivalent input current threshold I_{in} and dispersion for 800 analog channels.

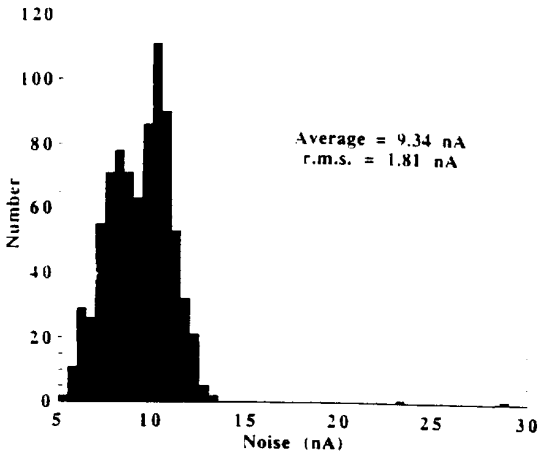


Fig. 11. The input current noise I_{in} and dispersion for 800 analog channels.

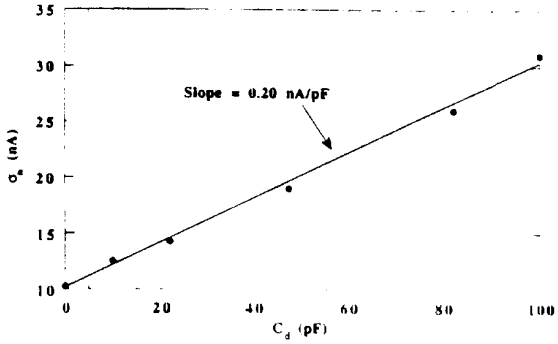


Fig. 12. The input noise current σ_n versus detector capacitance C_d for a single analog channel.

Each digital chip has a **fast-or** which may be wire-ored to the other digital chips to define a **sector-fast-or.**

5.2. Address generation – the "live mode" of the chip

The layout of the chip array is shown in fig. 13 and the architecture of a single chip in fig. 14. The readout phase is initiated by an external **readout signal** which causes PRIORITY ENCODER to encode (at 20 MHz) the addresses of channels with valid data (hits) according to an order of priority (channel 15 – first, channel 0 – last). The resultant addresses are then loaded (also at 20 MHz) by OUTPUT MULTIPLEXER into a 16-word FIFO located on the chip above (same column). Since PRIORITY ENCODER suppresses zeros, only one clock cycle is needed per hit channel. Also, ENCODER and FIFO can operate concurrently (i.e. data can be entered into the FIFO while the EN-

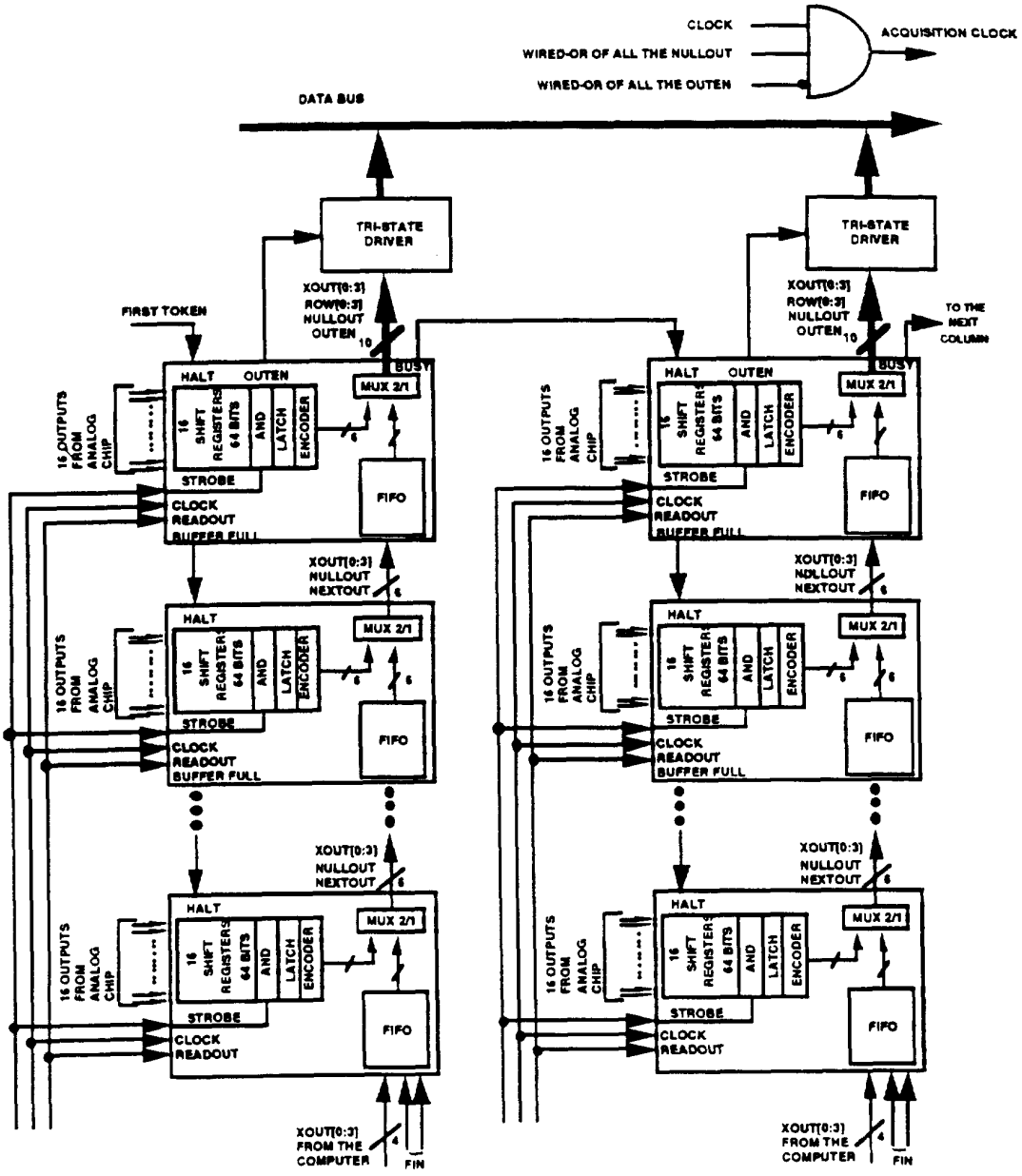


Fig. 13. The digital chip array with functional elements and flags indicated.

CODER is outputting data via its OUTPUT MULTIPLEXER), thus significantly reducing the readout time. To reduce crosstalk with the analog chip, the 20 MHz readout clock is activated only after the **readout** is received.

The encoding process generates two flags, **next row**

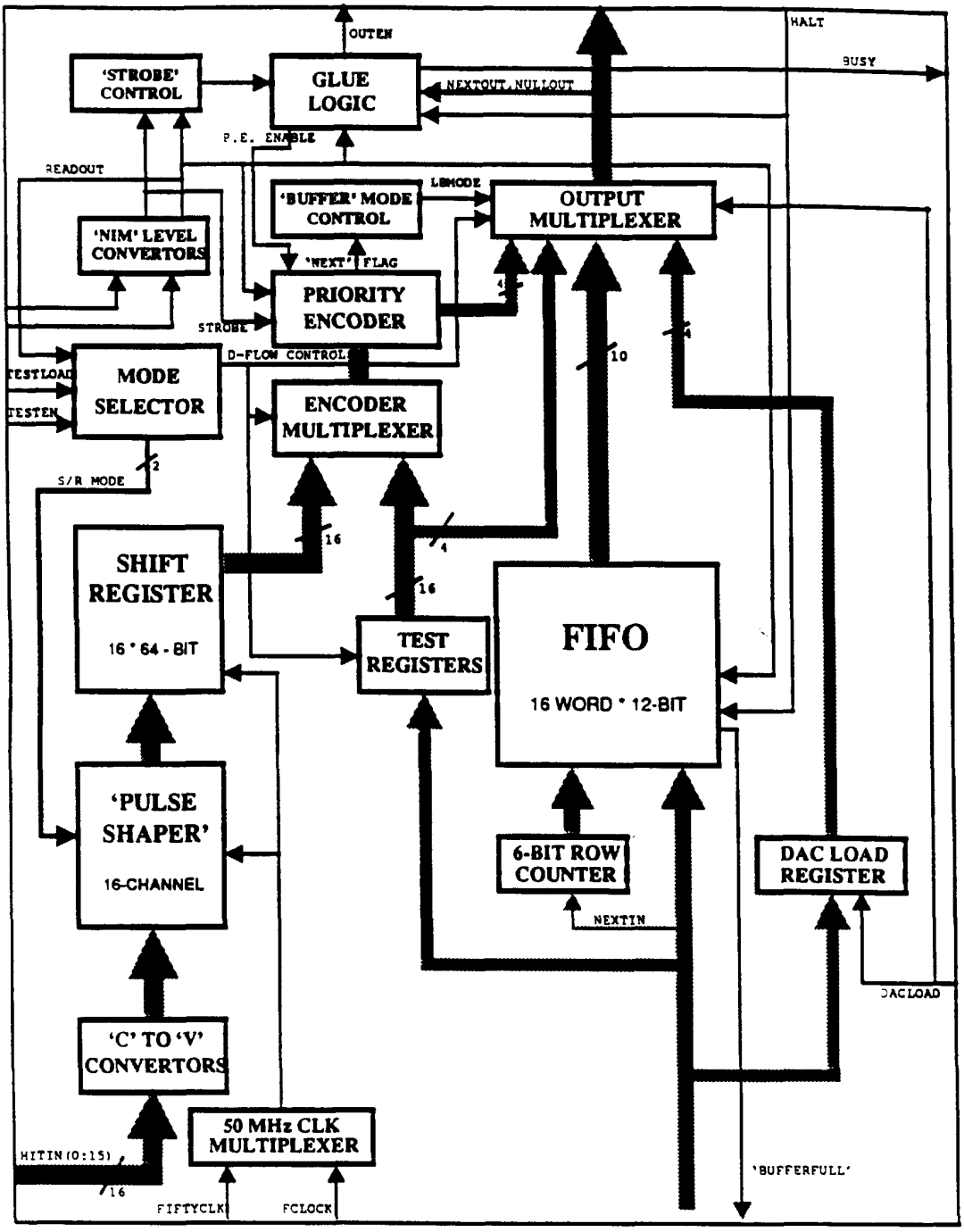


Fig. 14. The architecture of a single digital chip.

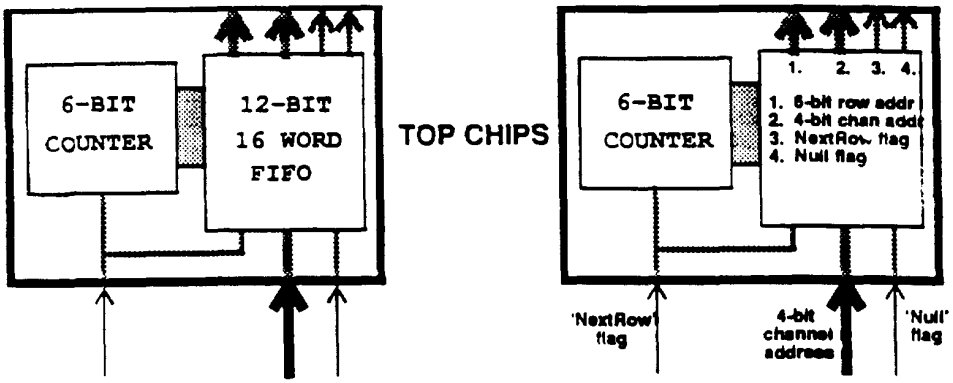


Fig. 15. Row address reconstruction in the buffer mode.

and **null**, which are stored along with each encoded address to indicate their status when reconstructing the row address. When there are no more hits in the chip to be encoded, **next row** true is generated. When there are no hits in the chip to be encoded, **next row** and **null** true are simultaneously generated, hence, each chip always produces at least one address.

5.3. Buffer mode operation

During the above sequence, a chip in a column will have been simultaneously transmitting data to the chip above and receiving data into its FIFO memory from PRIORITY ENCODER of the chip below. Once all the data have been encoded, each chip will automatically start reading out its stored FIFO data into the free FIFO memory of the chip above. This is called the "buffer mode" of the readout process. The FIFO memory of each chip in a column effectively combines to form one large memory. Successive readout clock cycles progressively move all data to the top of this large memory for readout onto the top bus. If at any time a chip FIFO memory becomes full of data (i.e. 16 words) then **buffer full** true flag is generated to stop the chip immediately lower down the column from passing up its data and overwriting valid hit addresses.

5.4. Row address reconstruction and data expansion

As data arrive at the top chip it undergoes "expansion". This is the process of reconstructing row addresses and removing the unwanted **null** flags. Row addresses are obtained from the ROW COUNTER of the top chip of each column (fig. 15). The counter will increment on every clock cycle that contains a **next row** true from the chip below (here **null** can be either true or false). True **null** or **next row** flags are not required for readout as these merely indicate that a chip in the

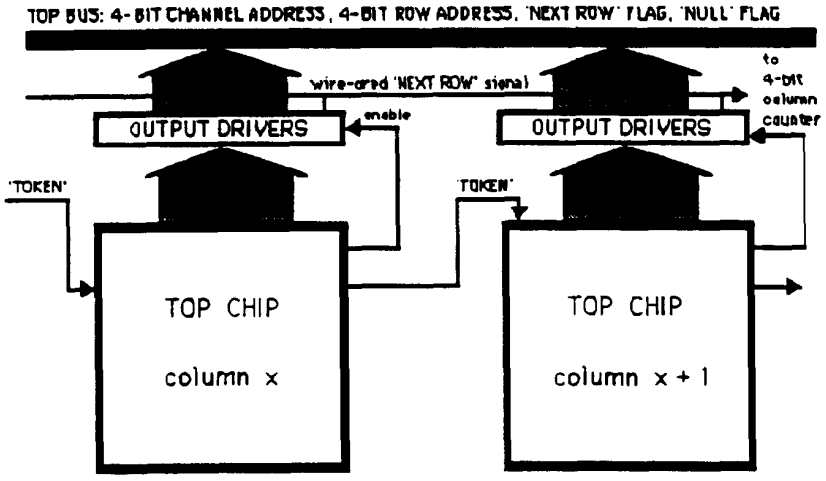


Fig. 16. The column readout logic with token passing indicated.

column received no its during data acquisition. In this case the counter is incremented as if **next row** is true, but loading the top chip FIFO is inhibited. Hence, **null** events are not stored in the top chip but the ROW COUNTER is correctly incremented.

A unique combination of **next row** false and **null**

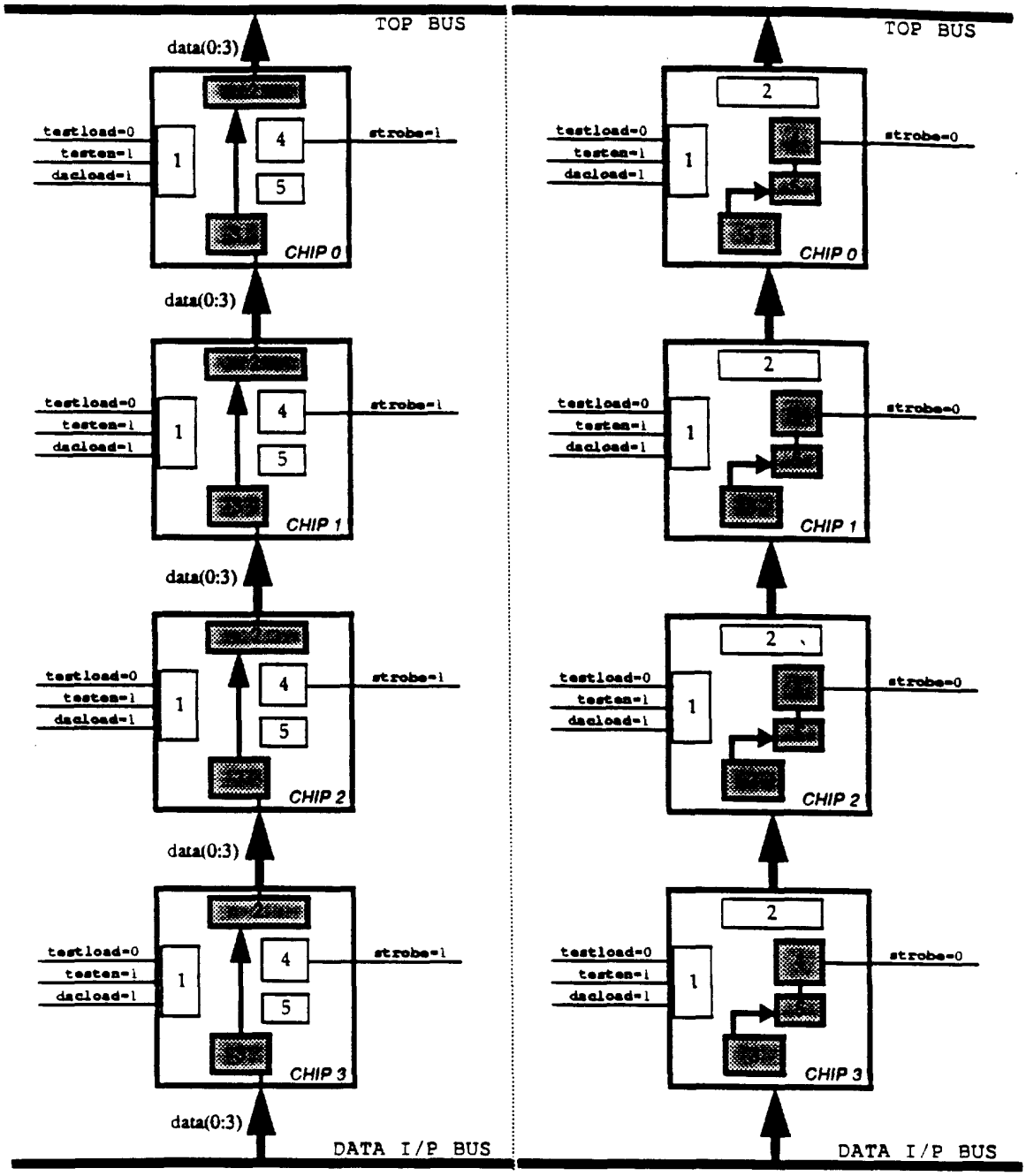


Fig. 17. Mode 3: testing of the priority encoder. Active states are shown by the darkened blocks, which represent: 1 = mode selector, 2 = output multiplexer, 3 = test registers, 4 = priority encoders, 5 = priority encoder input multiplexer; (a) data passes upward via 3 and 2; (b) test data is latched into 3,4 and 5 by the **strobe** signal.

true flags is hardware loaded into the FIFO in the bottom chip of each column. Throughout each readout cycle it forms a **fin** flag when combined with an address. When the system enters the buffer mode, **fin** propagates up through the column of FIFOs, immediately following the last encoded hit. This logical combination, when detected by the top chip, signifies that the column has no more data, therefore control of the top bus (the token) will be passed to the next column.

5.5. Data readout – top bus output

In order to reconstruct a column address for each hit without using multiple buses and control lines, a token passing bus arbitration system is used. This system uses a single flag called **token** to enable/disable control of the column TOP BUS DRIVER (fig. 16).

A token line is serially chained between the top chips of each column (0 to 14) of the sector. Only the column with the token can read out data. At the start of the readout cycle, column (0) has the token (hard wired) and therefore can immediately begin outputting data. When the **fin** flag reaches the top chip, all the data of column (0) will have been read, hence **fin** signifies **next column**. This enables the current top chip to pass the token to the next column and disable its external tristate buffer by switching to high impedance. Then the **outen** (out enable) and **busy** flags from the top chip become inactive (output high). The **busy** output of a column (n) is connected to the **halt** input of the top chip of the adjacent column ($n+1$). After a delay of one clock cycle the **outen** of this chip goes active (output low) and the column acquires the **bus start** to transfer data. This process repeats until the entire sector array has been read out.

To reconstruct the column address the **outen** outputs of the top chips are wire-ored and connected to a separate and external 4-bit counter. The column address 0 to 14 is appended to the hit row addresses as data are taken into the readout computer.

5.6. Data readout time

For all top chip encoders in the array, a **null** true flag cannot be removed as data do not pass through the FIFO control logic. This also applies to all **null** true flags generated in the rest of the column, if the top chip has no data. Thus, in an array of 15 columns, if all columns are empty it will take 16 clock cycles to propagate the **fin** flag from the bottom to the top chip (while 16 **nulls** will have been read by the top bus) and another 14 clocks to propagate the token to the last column, and one added clock to end the readout. Hence, the readout time $t_{ro} \geq (16 + 15) \times 50$ ns or 1.55 μs plus one clock cycle per hit, i.e. $t_{ro} = (1.55 + 0.05N_h)$ μs, where N_h is the number of hits. Since it is expected that $N_h \leq 20$, the average readout time will be $\equiv 2.5$ μs.

5.7. Test structures and DAC loading

Changing of the discriminator thresholds in any location of the sector array is accomplished by DAC loading via the computer console interface.

The digital chip has built-in features which permit testing of its readout functions. There are 4×4 bit internal registers in each chip which can be serially loaded through the four data bus inputs to the chip **xin[0:3]**. The mode SELECTOR, integrated on the chip (fig. 14), is used to select a data path through the chip according to the operation mode via the three external inputs to the chip (**dacload, testload, testen**). Mode selection is obtained according to the truth table (T = true = 0 V,F = false = +5 V) (table 1). In mode

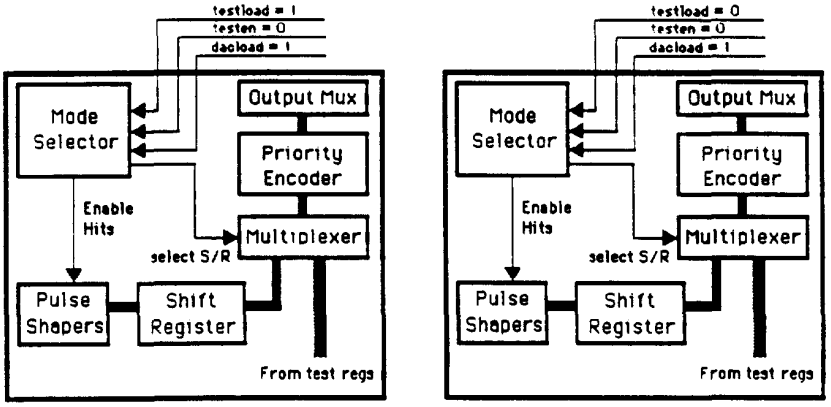


Fig. 18. Modes 4 and 5

3, the TEST REGISTERS are used to apply any pattern of 16 bits to the PRIORITY ENCODER data latches. Alternately, loading of hits in all/none of the 16 shift registers is obtained via mode 4/mode 5.

5.7.1. Test modes

For normal readout SELECTOR is set to mode 1. In mode 3 the test data passes through the 16 chips of a column via the data bus, the TEST REGISTER (16 bits) and the OUTPUT MULTIPLEXER of each chip. The data flows from bottom to top of the column at the frequency of the control computer (fig. 17a). A total of 16×4 clocks are therefore needed to load a column of 16 chips. Next, the PRIORITY ENCODER of each chip is loaded through a multiplexer (normally commuted to the shift register in modes 1, 4 and 5) by applying a **strobe** signal (fig. 17b). Mode 3 thus allows PRIORITY ENCODER to be tested independently of SHIFT REGISTER and is also useful for testing the readout process and its speed.

Modes 4 and 5 (fig. 18) allow SHIFT REGISTER to be tested independently of the PULSE SHAPER and CURRENT-TO-VOLTAGE CONVERTER. Mode SELECTOR is used to force the outputs of PULSE SHAPERS to a logical value corresponding to a hit or no hit. The SHIFT REGISTER will then pass these data to the MULTIPLEXER input of PRIORITY ENCODER, where it can be strobed and read out (mode 1) to verify that all channels of the shift register work correctly. The test registers are not reset by the **reset** signal.

5.7.2. DAC Loading (mode 2)

The digital chip has four output pins **dacout[0:3]** connected through 4 resistors to the current inputs (I_{th}) of the analog chips which control the discriminator thresholds [4]. The four **dacout** lines are connected to zero or to a fixed voltage level by a 4-bit register dedicated to loading DAC. Hence, an appropriate choice of the four resistors allows sixteen different values of I_{th}, linearly incremented. Mode 2 allows each DAC register to be loaded with different codes, as shown in fig. 19. As in mode 3, DAC threshold data from the **xin** data bus at the bottom of a column are shifted once per control computer cycle to the top of the column. Each chips output **dacout[0:3]** will then set the desired threshold to their associated analog chip pair. These values are stored in the DAC prior to normal data acquisition and readout. The DAC registers are not reset by the **reset** signal.

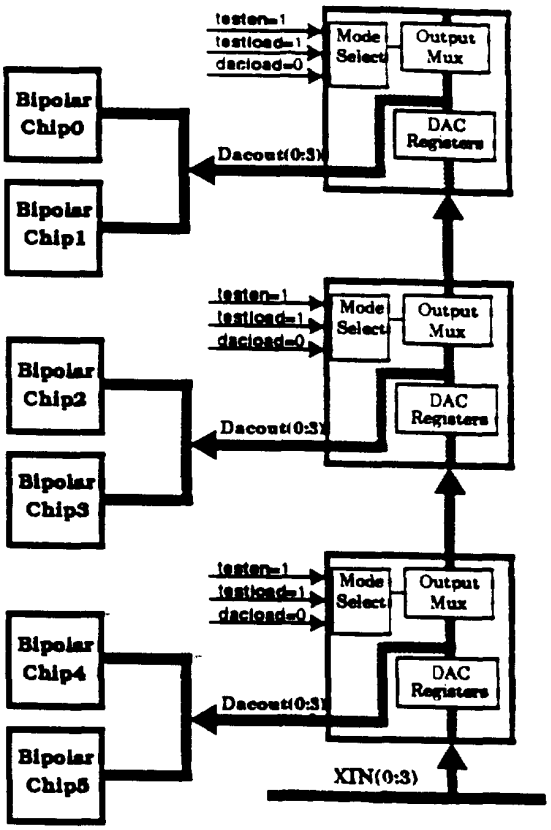


Fig. 19. DAC loading a column (mode 2).

5.8. Readout initialization

An external input signal called **reset** is sent to the chip between readout cycles to clear all on-chip storage elements (except for the TEST and DAC registers). This avoids spurious data being encoded and read out. The input signal **readout** enables the readout process (section 5.2) and is active during the live and buffer modes. If a spurious trigger signal is received during this phase, the priority encoder would immediately latch new data and begin encoding. Any previous unencoded data would be lost and invalid addresses would be outputted. To prevent this, the **readout** flag disables the **strobe** signal.

Table 1
Test structure codes

Mode number	Type	**testload**	**testen**	**dacload**
1	normal	F	F	F
2	dacload	F	F	T
3	test reg. load	T	F	F
4	shift reg. all hits	F	T	F
5	shift reg. no hits	T	T	F

5.9. The chip clocks

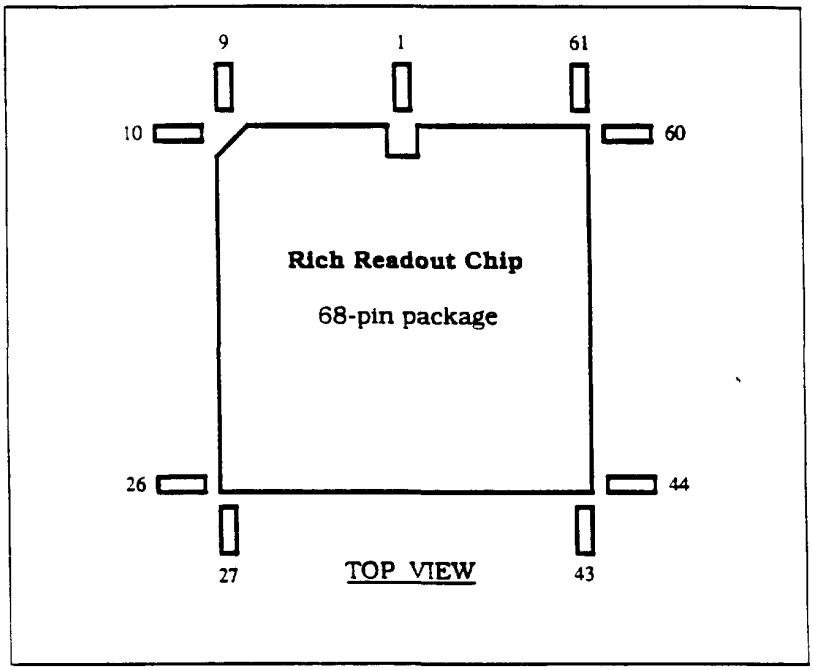
The input PULSE SHAPER (synchronizer) and SHIFT REGISTER are controlled by the 50 MHz CLOCK which can be produced either by an on-chip oscillator (individually controlled by an off-chip quartz) or by a single external clock signal delivered by an oscillator common to the 64-channel PCB. An **excken** input selects one of these clock sources. In either case, crosstalk between the TTL clock signals and the low-level inputs of the analog chip (via the PCB common ground) must be avoided. Crosstalk due to the 20 MHz readout clock is not a problem since it is only enabled after data acquisition. The 20 MHz clock is automatically synchronous over the entire sector array, whereas the 50 MHz clocks are synchronous (in a 64-channel card) only if the external clock option is implemented.

5.10. Pin diagram of the digital chip

The signals into and out of the digital chip and its geometry are shown in fig. 20. The power consumption is 96 mW per chip or 6 mW per channel mostly due to the shift register. In addition, the analog chip consumes 10 mW/channel (section 4.1) hence the total power consumption is 16 mW/channel or 5 kW for the full B-factory RICH counter.

5.11. Tests of the digital chip

Here, we summarize the tests needed for chip use. These include the measurement of the input threshold, the shift register delay and the overall readout performance. The detection efficiency of the circuit versus



Pin Key

1	VDD	18	NEXTOUT	35	DACOUT(2)	52	NEXTIN
2	IN(8)	19	DGND	36	DACOUT(3)	53	NULLIN
3	IN(9)	20	VDD	37	READOUT	54	FCLOCK
4	IN(10)	21	XOUT(0)	38	TESTEN	55	RESET
5	IN(11)	22	XOUT(1)	39	TESTLOAD	56	VDD
6	IN(12)	23	XOUT(2)	40	unused	57	DGND
7	IN(13)	24	XOUT(3)	41	unused	58	XTAL2
8	IN(14)	25	HALT	42	VDD	59	XTAL1
9	IN(15)	26	DGND	43	DGND	60	IN(0)
10	DGND	27	BUSY	44	DACLOAD	61	IN(1)
11	ROWOUT(0)	28	TOPROW	45	BUFFUL	62	IN(2)
12	ROWOUT(1)	29	OUTEN	46	XIN(3)	63	IN(3)
13	ROWOUT(2)	30	unused	47	XIN(2)	64	IN(4)
14	ROWOUT(3)	31	READCLK	48	XIN(1)	65	IN(5)
15	ROWOUT(4)	32	STROBE	49	XIN(0)	66	IN(6)
16	ROWOUT(5)	33	DACOUT(0)	50	unused	67	IN(7)
17	NULLOUT	34	DACOUT(1)	51	EXCKEN	68	DGND

Fig. 20. Pin connections to the digital chip.

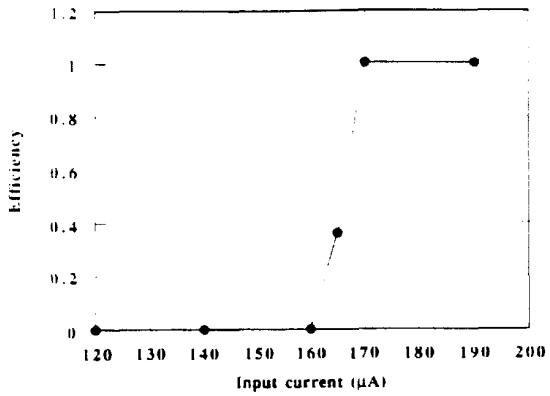


Fig. 21. The detection efficiency of the digital chip versus input current.

input current is shown in fig. 21. The transition from low to high efficiency (0 to 1) is very rapid at 160 μA, comfortably less than the 300 μA delivered by the analog chip discriminator. The SHIFT REGISTER was tested by measuring the readout detection efficiency for a strobe width of 10 ns (fig. 22a) and 40 ns (fig. 22b) versus the delay relative to the rising part of the input pulse. The shift register clock frequency is 50 MHz. One may note from fig. 22a that full efficiency is observed for a delay of 1320 ns (66 clock cycles of 20 ns). This is as expected for a 64-element SHIFT REGISTER since two clock cycles are needed to latch the data. The response width and shape are as expected from convolution of the input pulse with the clock waveform and give an rms time dispersion $\sigma_a = (20$

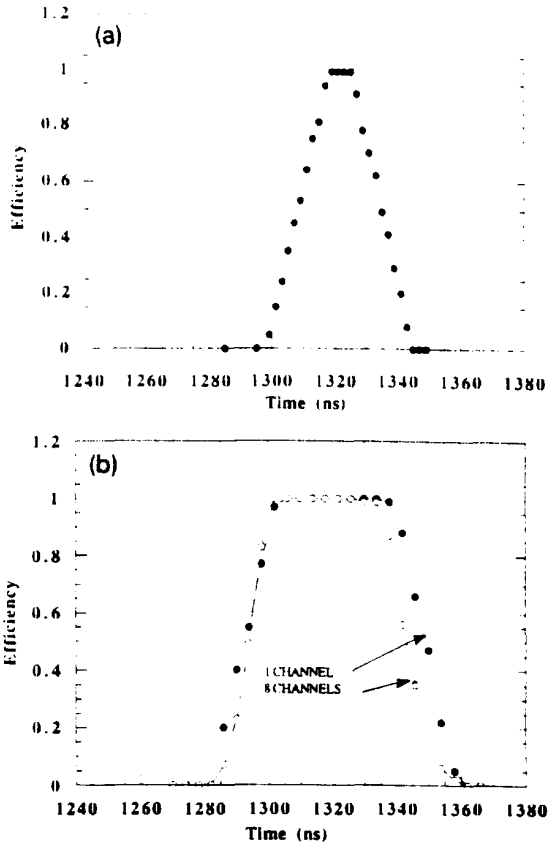


Fig. 22. Readout detection efficiency for a strobe width of (a) 10 and (b) 40 ns versus delay relative to the rising part of the input pulse. The SHIFT REGISTER clock frequency is 50 MHz.

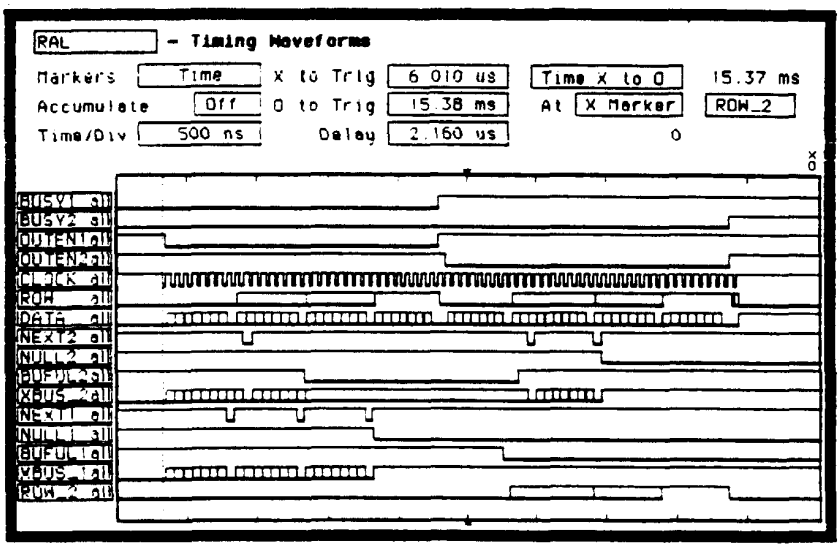


Fig. 23. The logic signals generated in readout of a 64×2 matrix (4 digital chips in 2 columns).

ns/$\sqrt{12}$) = 6 ns, quite comparable to the TEA detector time dispersion σ_t = 10–20 ns.

The logic signals generated during the readout of a 64 × 2 matrix (4 digital chips in 2 columns) are shown in fig. 23 (all signals are active low). It shows typical readout signals recorded versus time with a Hewlett-Packard logic analyzer. Each chip contains 8 hits except the second chip of the second column which contains 10 hits. The signals shown are:

- **busy1** and **busy2** are the busy outputs of columns 1 and 2;
- **outen1** and **outen2** are the **outen** outputs of columns 1 and 2;
- **clock** is applied (NIM level) to all chips at the **clock** input;
- **row** shows **row[0:5]** on the top bus;
- **data** shows **xout[0:3]** on the top bus;
- **next2, null2, bufull2, xbus2** are the signals entering the top chip of the 2nd column;
- **next1, null1, bufull1, xbus1** are the signals entering the top chip of the 1st column;
- **row2** shows **row[0:5]** in the 2nd column before the column driver.

From the **busy** and **outen** lines, the token passing and management of the column driver are visible. During readout of column 1, its driver is enabled by **outen1**, and **busy1** is true in order to prevent column 2 from emitting conflicting data onto the top bus.

Once column 1 data are read out, **busy1** goes false along with **outen1**. At this time the top bus is in its high-impedance state until the next clock cycle. Then, the second column driver is enabled so that this column can emit data onto the top bus. Readout end is signalled by the true-to-false transition of the **busy** line on the last column of the sector (here the 2nd, but in full scale the 15th).

We now consider the traffic within a column just at the entry to the top chip. In the 1st column, the **next1** true flag is generated with the last valid hit of the previous chip. Here, **bufull1** is never true since the top bus is immediately available. This allows the FIFO to read out an address at the same rate as receiving an address from the adjacent chip down the column. For this situation the top chip FIFO can never become full (unless the top chip PRIORITY ENCODER contains 16 hits) therefore, **bufull1** remains false. Readout of the 2nd column must await top bus access, hence **bufull2** becomes true on the 17th clock cycle. Once it is read out, true **null** and **next** flags indicate a **fin** flag.

To read out 66 hits, in this example, requires 68 clock cycles, one per datum and one for each token pass. The eagle-eyed observer will note that there are 69 cycles in fig. 23, the extra cycle is needed to disable the READOUT CLOCK with the **busy2** flag.

The non-valid cycles (i.e. token passing or null data not suppressed at the top chip) are suppressed on-line by filtering the clock used for the acquisition system [i.e. **clock(system) = clock** (readout) & **null** & **outengen**], where **outengen** is the wire-or of all the **outen** lines after the column drivers. This signal is also used to count the columns in order to have a unique and complete address per hit. With this test setup, a maximum data readout rate of 19 MHz was attained (20 MHz was the target) with on-line suppression of non-valid cycles.

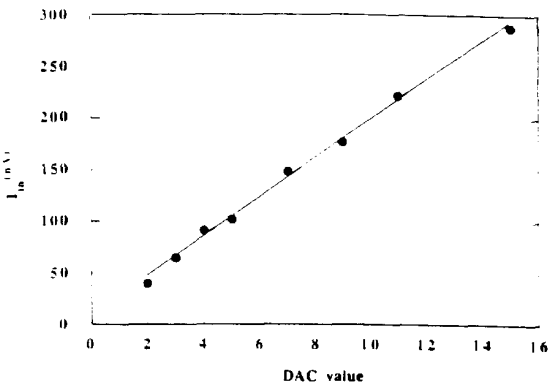


Fig. 24. The analog input current I_{in} to obtain 50% detection efficiency versus the DAC value. The corresponding digital chip threshold current is I_{th} = (12.5 μA) × DAC.

6. Tests of the readout chain on the detector

In this section we give the test results obtained with the prototype chips mounted on the RICH detector. The complete readout chain (analog and digital) was tested under normal detector operating conditions with the top chip of the top card connected to the top data

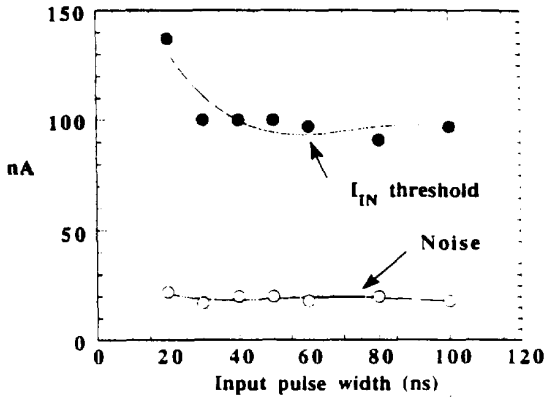


Fig. 25. The equivalent input current threshold I_{in} and channel noise versus input pulse width. The settings were DAC = 4 (i.e. I_{in} = 90 nA) with an injected current pulse of 205 nA.

bus (carried on the vetronite back plane). Each card had a single common oscillator. The shift register was tested at the design frequency of 50 MHz. The 4-bit DAC outputs (driven at +5 V) were connected to the 1th inputs of the 16 coupled discriminators with serial resistors of 200, 100, 50 and 25 kΩ; the least to most

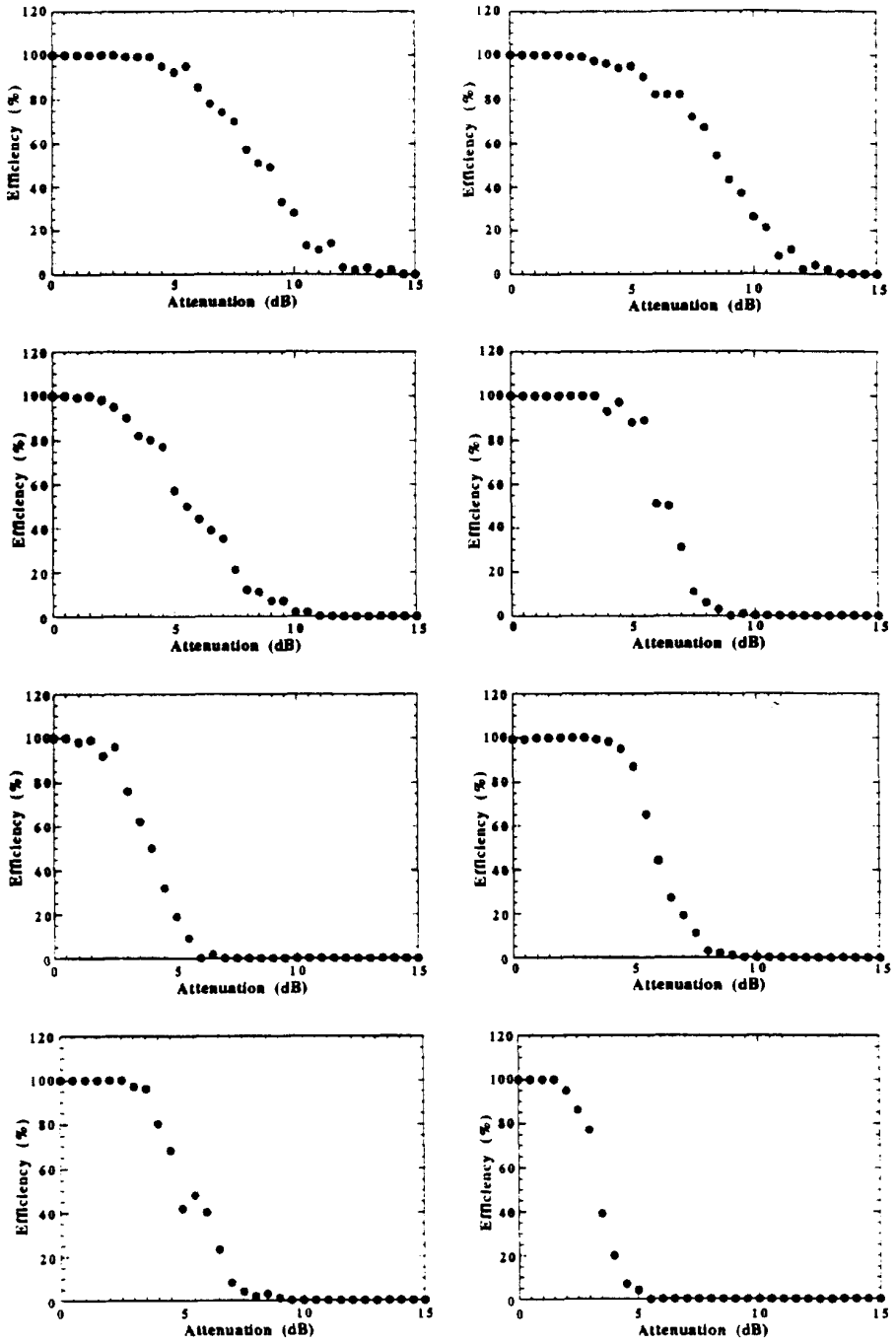


Fig. 26. Detection efficiency (DAC = 3) versus input current for the eight channels of an analog chip mounted on a card connected to detector pads. The unattenuated input current was I_{in} = 378 nA.

significant bit, respectively. These tests were conducted with a standard VME data acquisition system interfaced to the detector via a CAMAC module for translation from TTL to MECL levels and for distribution of control lines. A Valet Plus microcomputer was used as input–output to the VME system and a Macintosh SE30 minicomputer served as host.

6.1. Noise measurement versus threshold level

The calibration curve of a single representative discriminator is shown in fig. 24 as a function of the 4-bit DAC pattern. The input current threshold I_{in} is determined by the DAC value from $I_{th} = (12.5\ \mu A) \times$ (DAC). The input current pulse had 100 ns width and gave 50% detection efficiency at the indicated DAC level.

A flat variation of I_{in} at threshold (50% detection efficiency) with the input pulse width is shown in fig. 25. It shows that the preamplifier is sensitive to current (and not to charge) for input pulse widths > 25 ns. This pulse width is defined by the time constant of the input stage and, as expected, the measured equivalent input noise is independent of the pulse width. Here, the cards are mounted on the detector which was outside its shielded structure, hence the input noise (for this channel) is twice the previous average (see fig. 11 and comments below).

Discrimination curves for 8 channels of a chip are displayed in fig. 26. An input current pulse of 378 nA was injected onto the cathode pads. Comparison with earlier results (fig. 9) shows that input noise has almost doubled in passing from an isolated test setup to a card mounted on an unshielded detector, with a mean value between 15 and 20 nA and unchanged dispersion.

A more practical noise measurement is given in fig. 27, which shows the variation of the pad hit probability versus the DAC pattern. This result was obtained with a 50 ns wide strobe signal applied randomly to the 64 channels of a card. For the RICH counter with a crystal radiator we expect 10 to 20 real photon hits per image distributed over a 200 pad surface. At a DAC = 3 threshold the single channel noise count probability is 10^{-3}, hence for 200 pads the noise count will be 0.2 whereas 10–20 real photon hits are expected. This represents an excellent signal-to-noise ratio of 50–100. This ratio decreases by a factor 30 at DAC = 2 or increases by a factor 10 at DAC = 4.

6.2. Time resolution and two-hit separation

The variation of detection efficiency with strobe delay is shown in fig. 28 for an input current pulse of 335 nA (injected directly onto the pad) and a 50 ns strobe width. The equivalent input threshold setting was $I_{in} = 200$ nA (i.e. DAC = 10). The rise and fall of

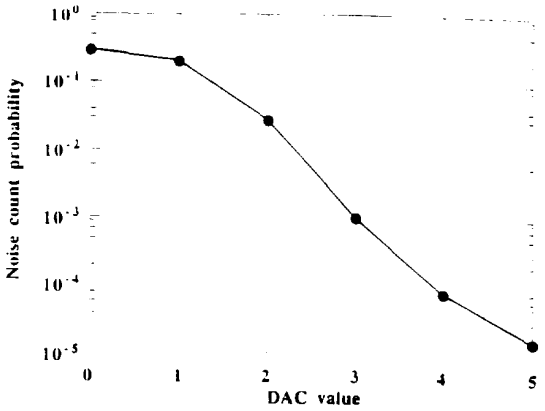


Fig. 27. A single-pad channel noise count probability versus discriminator DAC value.

the coincidence curve corresponds, as expected, to the clock period (20 ns) and the plateau with the strobe width. The centre delay (1315 ns) corresponds closely to (64 + 2) clock cycles of 50 MHz. The coincidence onset is amplitude-dependent because of the limited bandwidth of the analog chain. This is illustrated in fig. 29, which shows 15 ns time slewing between two input signals (335 and 3350 nA), twice the value expected from the rise time of the fast-or signal (fig. 8). This degradation is due to the level shifter interface between amplifier and discriminator.

Finally, in fig. 30 we show the dead time of a single channel to successive hits. A pulse of amplitude A was injected at $t \approx 0$ followed by a threshold signal T at a later time. As A is increased, the time needed to detect T (50% efficiency) also increased as shown in fig. 30. When both pulses are threshold, a minimum time separation of 70 ns is needed to detect both pulses.

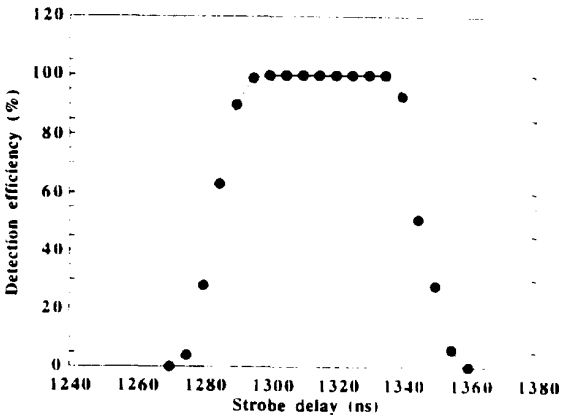


Fig. 28. Pad detection efficiency versus strobe delay for 50 ns strobe width and DAC = 10.

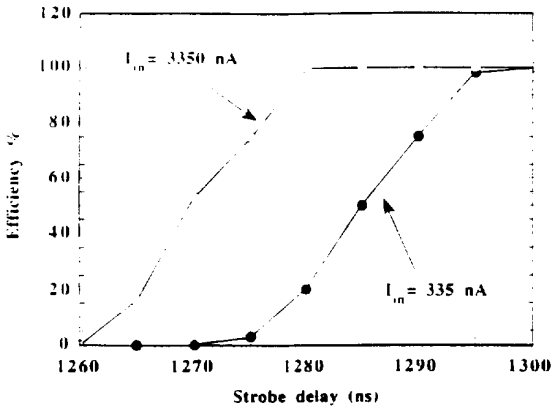


Fig. 29. Time slewing for input signals of 335 and 3350 nA. The threshold set was DAC = 10.

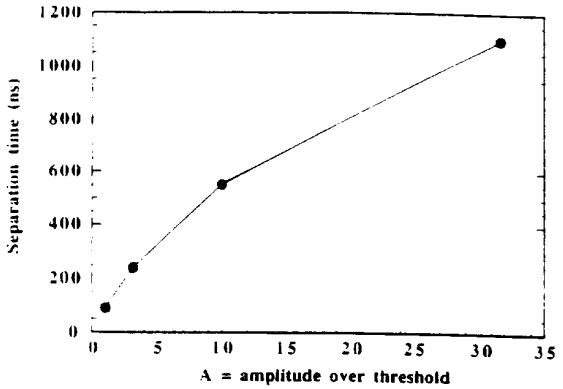


Fig. 30. The time separation needed (for 50% detection efficiency) between a threshold (T) signal and an earlier signal of amplitude A/T.

7. Single photoelectron detection efficiency

In this section we present single photoelectron response measurements made with the prototype fast RICH photon detector. A schematic drawing of the setup is shown in fig. 31. The pulsed UV light source has been previously described [1]. This self-triggered H_2 filled flash lamp produces, after collimation, a spot

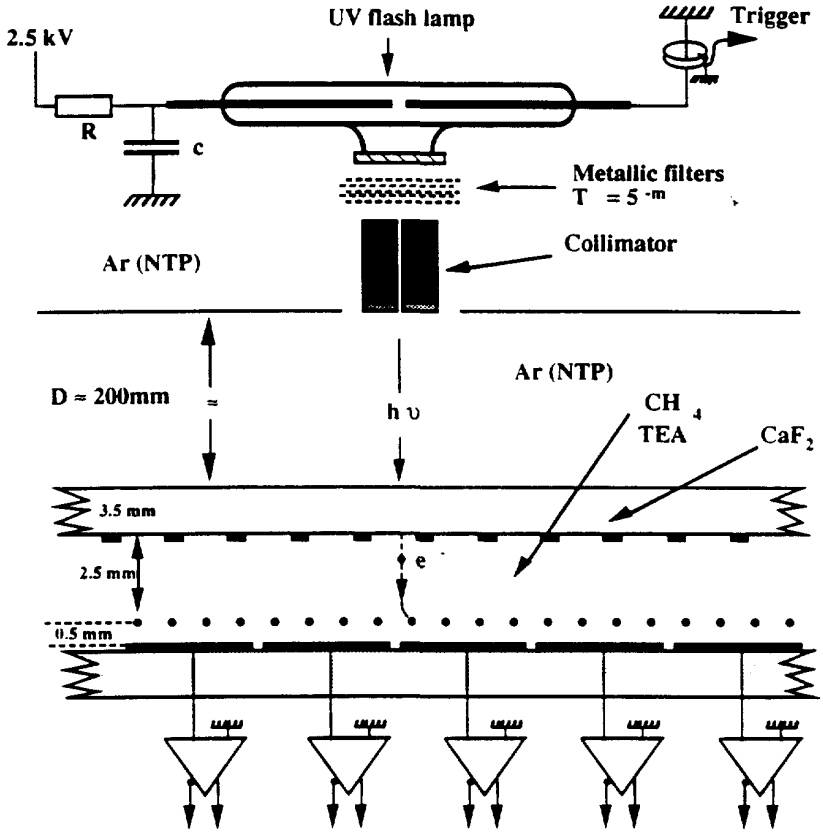


Fig. 31. The setup of the pulsed UV lamp to measure single photoelecton efficiency in the fast RICH counter equipped with the full electronic chain. The beam transmission (T) is reduced by adding (m) metallic filters.

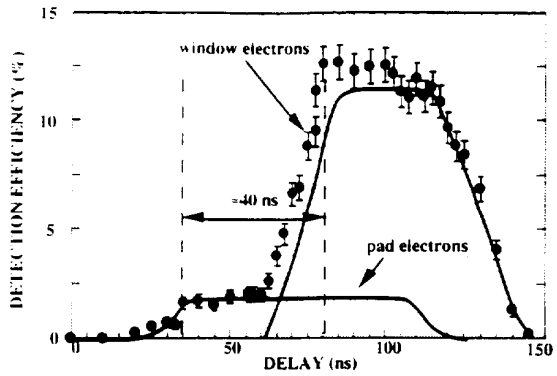


Fig. 32. The delay curve observed in pure methane from photoelectrons produced on the window strips or the cathode pads. The 40 ns delay for the 2 mm drift path difference determines the drift velocity $v_d \approx 4.4$ cm/μs. The peak detection efficiency of ≈ 10% means that ≈ 5% of the pulses have two photoelectrons.

of ≈ 1 mm ∅ on the photodetector window. Photoelectrons are produced at the boundary surfaces (i.e. the cathode pad metal surface or the metallized strips of the CaF_2 window) when the detector is flushed with pure methane or in the detector gas when it is flushed with methane + TEA (15°C). In either case the light intensity is adjusted by means of metallic filters so that only ≈ 10% of the pulses are detected. From a Poisson distribution we calculate that the probability of detecting two photoelectrons in an event is ≈ 5%, hence the measured distribution is dominantly of single photoelectrons. The current pulse (which flows to ground through the ferrite core when the UV lamp fires) provides a trigger for the readout chain. The light flash pulse duration is ≈ 10 ns (FWHM) and the trigger rate is ≈ 50 Hz.

7.1. Tests in pure methane

The tests with pure methane are interesting because they establish the timing properties of the detector and electronics without contribution of feedback photelectrons. These timing properties are illustrated in fig. 32, which shows the variation of single pe detection efficiency with the strobe delay (40 ns strobe width). The curve is well reproduced by the superposition of two delay curves. Photoelectrons from the cathode pads arrive first and then, ≈ 45 ns later, photoelectrons from the edges of the cathode metal strips arrive. Since the drift path difference is 2 mm we find $v_d = 4.4$ cm/μs. The 20 ns rise and fall time of these curves corresponds to the shift register clock frequency, indicating that any additional time dispersion (≥ 10 ns) will be detectable. Thus, for a CsI photocathode, the response time will be limited only by the readout electronics.

The variation of detection efficiency with anode wire potential U_a (i.e. detector gain) is shown in fig. 33a for fixed DAC = 4 threshold, $U_w = -1.55$ kV. A short plateau is observed with rapid increase of sparking above 1.5 kV. This curve is only slightly dependent on the voltage applied to the window strips U_w. The onset and knee of this curve remained unchanged when the light intensity was increased by a factor of 4, thus confirming that the two-photoelectron contribution is small.

The single pe detection efficiency versus DAC threshold is shown in fig. 33b for fixed $U_a = 1.4$ kV and $U_w = -1.5$ kV. Below DAC = 2 the detector noise increases strongly and dominates. These results confirm

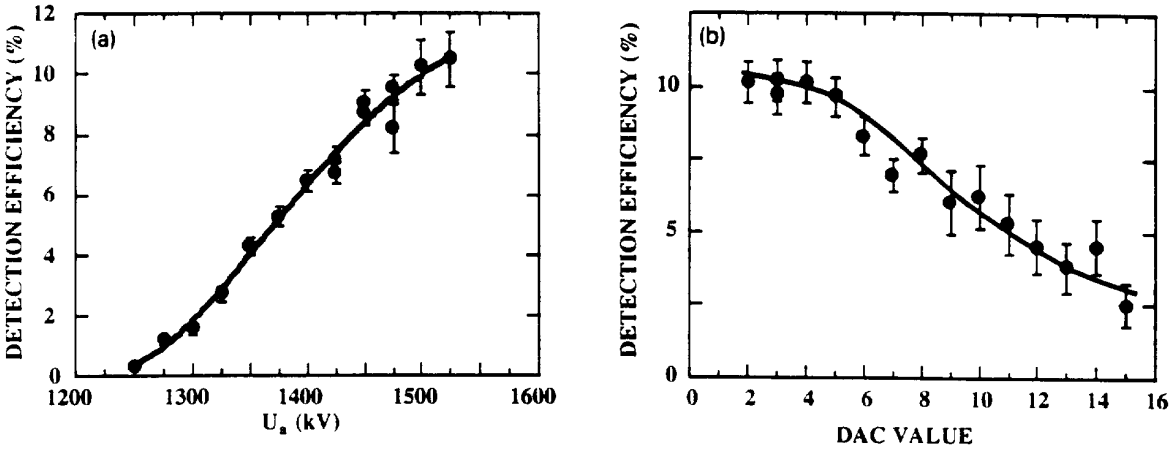


Fig. 33. (a) The pure methane single pe detection efficiency vs anode voltage U_a. (b) The detection efficiency vs DAC value shows a plateau for DAC ≤ 5.

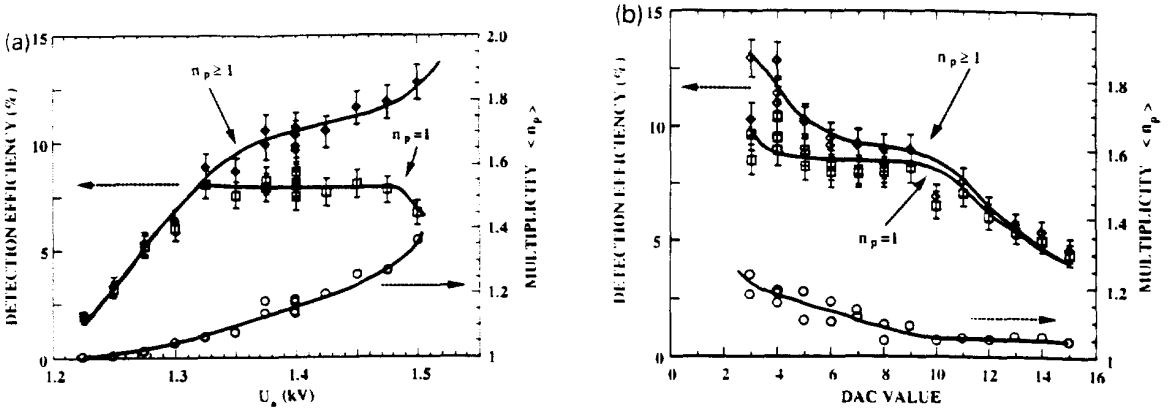


Fig. 34. (a) The methane+TEA (15°C) single pe detection efficiency vs anode voltage U_a for all events ($n_p > 1$) and single pad events ($n_p = 1$). Also shown is the the average multiplicity $\langle n_p \rangle$ with the right-hand scale. (b) The detection efficiency vs DAC value shows a plateau for $3 \leq AC \leq 10$ and $n_p = 1$. Also shown is the average multiplicity $\langle n_p \rangle$ with the right-hand scale.

the good single photoelectron detection efficiency in pure methane even for DAC = 4 (input current threshold of 90 nA), largely improving the noise count probability to $\leq 10^{-4}$ (see fig. 27).

7.2. *Tests in methane with TEA*

These last tests were performed in normal conditions of operation with methane saturated by TEA vapor at 15°C ($l_{ph} \approx 0.8$ mm). These data show how the detector response is affected by feedback photoelectrons. The single photoelectron detection efficiency is shown in fig. 34a versus U_a for events with one pad hit per cluster ($n_p = 1$) and all events ($n_p \geq 1$). The light spot position on the pad is not known with accuracy; therefore, the interpretation of these results is qualitative. From ref. [1] we know that the radius of the detectable induced charge spot is ≈ 1 mm. Thus, the selection $n_p = 1$ should correspond to an induced charge spot fully contained on a pad. On the contrary, the variation for $n_p > 1$ (equivalent to the difference between curves) corresponds to induced charge spots distributed over adjacent pads. The long 150 V plateau observed when the induced charge is confined to one pad ($n_p = 1$) becomes gain dependent for $n_p > 1$ events because only a fraction of the charge is induced on the measured adjacent pads. The fall of detection efficiency for $n_p = 1$ above 1.47 kV (complementary to the rise for $p_p > 1$) is explained by the onset of feedback photoelectron production. The large increase of the plateau for $n_p = 1$ relative to the previous measurements (fig. 33a) is the result of secondary photoelectrons being collected on the same wire near the primary avalanche, thus increasing the mean avalanche charge and also the induced pad current.

This interpretation is well confirmed by observation of the discriminator curve, shown in fig. 34b, which exhibits the integral of the current distribution at the preamplifier input, for $U_a = 1.4$ kV. It is clearly visible that the differential distribution is peaked with a maximum at DAC = 10. This extremely good result proves that a higher DAC threshold (> 4) can be used with small loss of detection efficiency. This will increase enormously the signal to noise ratio with a concomitant gain in image reconstruction fidelity.

The measurement of detection efficiency versus strobe delay showed that the rise and fall time of this curve increased from 20 ns (shift register period) to ≈ 40 ns due to the time dispersion of the collected photoelectrons. The quadrature difference ($\delta \approx 35$ ns) must be equal to some number (α) times the conversion point time dispersion, i.e $\delta \approx \alpha\sigma_t = \alpha l_{ph}/v_d = \alpha$ (0.8 mm/4.4 cm/μs) hence we obtain $\alpha = 2$.

We conclude from all the tests performed with the photon detector that the design of the electronic readout is very well suited to the requirements of a fast RICH counter.

8. Summary and conclusions

We have developed a system to readout the pad array of a fast photon detector and have now produced 24 000 channels, of which 11 520 will be installed for test in the prototype Fast RICH counter. The readout chain is implemented on the rear plane of the detector in such a way that only 8 control and 10 data lines are needed (per sector of 3840 pads) to relay the data to the DAQ computer. Two VLSI circuits have been designed (in the micro-electronics group of the Rutherford Appleton Laboratory) as the basic units for detection and readout.

Fast induced pad signals are detected in the 8-channel bi-polar analog chip. Each channel has a fast, low-noise, current preamplifier-amplifier and discriminator. The measured equivalent rms input noise current is 10 nA (or 625 e) for 50 MHz bandwidth with 10 mW per channel power consumption. The discriminator threshold, common to the 8 channels of the chip, is set by a 4-bit DAC addressable from the console of the data acquisition system via the data bus.

The basic architectual element of the readout is the 16-channel digital chip (1.5 μm CMOS) which forms a chip set with two 8-channel analog chips. The digital chips are daisy-chained in columns (15 for the present application) of 256 elements successively connected (at the top of each column) to a data bus via drivers. The power consumption of the digital chip is 6 mW per channel. This chip contains the DAC register which controls the threshold of the chip set. The output registers of the discriminators are asynchronously delayed by shift registers of 64 elements running at 50 MHz [delay = $(64 + 2) \times 20$ ns = 1.32 μs]. The end pulses of the shift registers are latched for readout only during the width of a strobe signal ($\geq$ 20 ns) generated by an external trigger. Once the readout process is initiated, a 20 MHz readout clock train is generated and synchronously distributed to the chip array. Addresses of detected hits in the 16 channels of a chip set are encoded by a 4-bit priority encoder and loaded into a FIFO memory (16 words deep) located in each digital chip. Data transfer from the first chip column is then enabled while, in parallel, data compression is effected in the remaining columns. When the first column is emptied (this requires at least 16 clock cycles) then data transfer from the second column is started but, because of the parallel data compression, this requires only one clock cycle per hit. This process continues until the last chip column is emptied. Addresses of the row and column positions are encoded by counters and associated to the hit readout data.

Tests show that a detector with $15 \times 256 = 3840$ pixel elements operated with discriminators set for 50 nA ($\approx 5 \times$ input noise) will have between 1.5 and 2 noise hits per sector readout. Hence, the total readout time will be mostly defined by the number of real image points (50 ns per hit with 1.55 μs for initialization). The digital chip contains various facilities to check the correct operation of the readout chain by loading programmable hit patterns at different levels of the chip structure.

We have developed a low-cost, fully integrated fast readout chain capable of operation at the next generation of high-luminosity hadron colliders (LHC/SSC) as well as at asymmetric e^+e^- B-factories.

Acknowledgements

We warmly thank Professor J. Haissinski of IN2P3 (Paris, France), whose initial and continuous support of the Fast RICH concept made possible this development. We are, of course, heavily indebted (morally as well as financially) to Professor P. Sharp of RAL Micro-Electronics group for his enthusiastic support of this program. The support of Professor A. Zichichi of CERN-LAA was highly appreciated. The aid of P.G. Innocenti of the CERN/ECP division has also facilitated this work.

The major part of the Fast RICH development has been financed by IN2P3, the CERN/LAA project, Rutherford Appleton Laboratory and the Paul Scherrer Institute. More recently, we have received additional support from the CERN/ECP division.

We wish also to acknowledge the contributions of M. Bramhall and P. Murray in various stages of the chip design and to E. Christoffel of CRN Strasbourg for his suggestions during discussions on readout concepts and circuitry. We wish also to thank J.P. Jobez of the Collège de France for his excellent mechanical design work in all phases of the Fast RICH project.

The difficult technical development required for the fabrication of cathode pads was ably carried out by A. Gandi and D. Berthet of the CERN/MT division.

References

[1] R. Arnold, Y. Giomataris, J.L. Guyonnet, A. Racz, J. Seguinot and T. Ypsilantis, Nucl. Instr. and Meth. A314 (1992) 465.

[2] J. Séguinot, G. Charpak, Y. Giomataris, V. Peskov, J. Tischhauser and T. Ypsilantis, Nucl. Instr. and Meth. A297 (1990) 133.

[3] Proposal for an electron–positron collider for heavy flavour particle physics and synchrotron radiation, Paul Scherrer Institute, CH-5234 Villigen, Switzerland, PR-88-09 July (1988).

[4] M. French, M. Lovell, E. Chesi, A. Racz, J. Séguinot and T. Ypsilantis. A fast bi-polar preamplifier–amplifier and discriminator chip, paper in preparation. please update ●●●.

[5] J. Séguinot, G. Passardi, J. Tischhauser and T. Ypsilantis, Liquid xenon ionization and scintillation, studies for a totally active-vector-electromagnetic calorimeter, CERN/LAA/PC/92-004 (10/6/92); Submitted for publication in Nucl. Instr. and Meth. please update ●●●.

[6] J. Seguinot and T. Ypsilantis, ICFA review article on ring imaging Cherenkov counters, in preparation; to be published in Nucl. Instr. and Meth. A, part 1; now available as a preprint CERN/LAA/PI/91-004 (31/3/91). please update ●●●.