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SC00000176

CERN/DRDC/90-64

DRDC/P16

1 November 1990

CERN DRDC

90-64

## A SCALABLE DATA TAKING SYSTEM

### AT A TEST BEAM FOR LHC

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project, additional participation is expected.*

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## **Abstract**

We propose the installation of a data taking system at a test beam for the simultaneous test of LHC detectors, trigger and readout electronics, together with the development of the supporting architecture in a multiprocessor environment. A strong emphasis is put on a highly modular design, such that new hardware and software developments can be conveniently introduced for training and evaluation. One of the main thrusts of the project will be the modelling and system integration of different readout architectures, which are meant to provide a valuable training ground for new techniques. To address these aspects in a realistic manner, we propose to collaborate with two detector R+D projects.

## A SCALABLE DATA TAKING SYSTEM AT A TEST BEAM FOR LHC

### Introduction

The Large Hadron Collider (LHC) will produce 16 TeV proton-proton collisions at luminosities ranging between  $10^{33}$  and  $4 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ . For the predicted inelastic cross section of 60 mb, interactions will occur at rates from  $6 \cdot 10^7$  to  $2 \cdot 10^9$  Hz. Given the bunch structure of the machine, with bunch spacing of 15 ns, the collision rate will be 67 MHz. There will be an average of between 1 and 40 overlapping events every bunch crossing.

In order to cope with the high particle rate and maintain the required identification power, detectors will have high granularities and a general purpose detector could have as many as  $10^7$  to  $10^8$  electronic channels. Present estimates indicate prompt trigger rates of the order of  $10^4$  to  $10^5$  Hz, implying data acquisition bandwidths of the order of GBytes/sec [1].

Such machine and detector parameters impose severe demands on the performance of the front end electronics, trigger and data acquisition systems, which will have to deal with unprecedented event rates and data volumes. Research and development work for LHC detectors has already started. After active investigation, first in the SSC community and more recently in Europe, the need has been recognized for a major effort in the field of electronics, triggering and data acquisition. While initial work in the areas of detectors, fast read-out, triggering and data acquisition can be done independently, the stringent time scale and the size of the problems suggest the need to proceed quickly to more realistic, fully integrated test conditions.

### Project overview

A necessary step in the development of an experiment of the complexity expected for LHC is the integration in a working system of all its components, from particle detection to the final storage of valid data. Such a system will need to scale both with the requirement of the experiments and with the appearance of new techniques.

We propose, therefore, to implement a test beam setup for the simultaneous testing of LHC detector prototypes, read-out electronics, trigger architectures and algorithms, and data acquisition software.

The proposal intends to achieve four main objectives:

- create a *realistic environment* for the study of architecture prototypes and their gradual integration into a general system
- develop as an *integrated component* of the general LHC R+D effort
- provide an ideal *learning ground* for new techniques and methodologies
- pursue *R+D activities* related to the design of a modular and scalable architecture, the evaluation of computing technologies for front end applications and the exploitation of the system for trigger and data acquisition developments.

### *Realistic environment*

The basic feature of providing a real life environment for tests and integration assumes, as a pre-requisite, close collaboration with detector R+D projects. While the test beam setup should evolve to include several detectors constituting a future experiment, practical considerations limit the initial configuration to two. In order to optimize the conditions for realistic tests of trigger techniques the two should consist of a calorimeter and a complementary detector for electron or muon identification.

Further practical considerations have led us to seek and find collaboration, for the initial stage, with SPACAL [2], the fibre electromagnetic and hadronic calorimeter, and with SITP [3], the silicon tracking and preshower detector. Both projects, in the configuration approved by the CERN Research Board last October following recommendations of the DRDC, have asked to use the UA2 (H2) test beam. The existing DAQ system at H2 will be adequate for the initial phases of test beam measurements by these detectors and can be maintained by members of this project, until the proposed new system becomes operational. At that moment the opportunity of collaboration with other detector R+D programs will also be considered.

Needless to say, such a collaboration will be beneficial to and involve responsibilities from both parties. The detector projects, while finding a modular read out and DAQ environment designed to scale with their developments of fast front end electronics, must allow the implementation and testing of the necessary modular and scalable system. The project proposed here will benefit from the real life environment and must provide adequate means for data taking by the detector prototypes, respecting their beam time schedules.

### *Integrated component*

The proposed project, while self contained, is not meant to develop in isolation. We consider it as a part of the overall R+D effort for LHC and we foresee close cooperation with other related hardware and software projects. In particular, we expect to be tightly linked, from the start and in a complementary way, to the proposed project for the development of 'Readout System Test Benches' [4].

### *Learning ground*

To meet the challenge represented by read out, triggering and data acquisition at LHC, the High Energy Physics community will need to employ the best commercially available technology and possibly, beyond some technological threshold, to off-load functionality to specialized hardware. Therefore, we do see the need for environments where the most recent technology, be it commercially available from industry or a specialized hardware or software component, can be immediately put into a real application and its potential evaluated and mastered.

### *R+D Activities*

One of the aims of the project is to identify areas where a concentrated R+D effort is needed. Hence the emphasis of the R+D activities proper will shift as the project evolves. We have identified two initial lines to pursue.

The first concerns the aim of providing an evolving environment. Methods and techniques to design a modular, open, scalable architecture have to be understood and put into practice. The major implications of such a system are the *interchangeability* and, to a lesser extent, the *interoperability* of hardware and software modules. The interchangeability allows the easy replacement and the truly independent development of the system components. The interoperability permits the recombination of a number of existing components for the solution of a different problem. These concepts and their implications are better understood when applied to hardware; a bus is an example of an architecture providing these features. Conversely these concepts have only recently been addressed in the case of software components. For the design and development of software, Object Oriented Programming and Design [5] are promising techniques which have become applicable to real life problems. In this context we also mention the Software Bus initiative [6] which explicitly addresses some of these questions.

Our second line of enquiry concerns the feasibility of extending the use of UNIX to front-end applications. Because of its generic architecture, UNIX has emerged as the best candidate for a common operating system. We have to evaluate the feasibility of its use in the VME environment. Depending on the task assigned to the embedded processor, the required real time response and the processor configuration (memory size etc.), alternatives such as UNIX-like real time kernels may be more appropriate. This is a line of research we intend to follow in cooperation with the project of ref. [4].

### **Project Organisation**

As a preamble to the description of the overall organization of the proposed project, the following points have to be stressed.

The collaborating detectors will need stable data taking conditions very early in the project. We should therefore aim at a first system which will provide the minimal functionality compatible with easy and reliable data taking.

Although it is too early to develop a generic data acquisition system for LHC, this project is a step towards its realisation. Hence we will initially invest as little as possible in system development and concentrate on the design and implementation of an open, scalable and modular architecture capable of smoothly evolving with the overall R+D effort for LHC.

Consequently we have envisaged a two phase schedule.

A first phase aiming at

- designing a modular and scalable system
- implementing the minimal functionality necessary for reliable data taking by the detectors
- studying and understanding the front end processor software environment
- providing support for the early 1991 data taking periods of the two detector prototypes. Such a commitment clearly rests on the assumption that this will take place in the H2 test beam, where the existing facilities could be used with a minimal investment. Should this not be the case, the question of early data taking would have to be reconsidered and rediscussed with the detector collaborations.

A second phase characterized by

- the widening of the system functionality via the exploitation of the scalable architecture developed during the first phase with the implementation of new trigger and DAQ hardware and software
- the development of tight links with other areas, such as front end hardware (ADCs, analog [7] and digital [8] pipelines, etc.), read out and trigger processors [9] and architectures [10], data acquisition software modules, etc.

To effectively achieve the proposed goals we envisage setting up and running two parallel online systems:

- A *development system* for study, development and early integration tests, outside the critical path of the detector data taking.
- A *production system*, providing a stable data acquisition environment to the test beam detectors. New elements of the trigger and data acquisition hardware and software, once tested and stable, would be ported from the development to the production system.

The proposed system is intended to grow both in size and complexity with the integration of new developments and the addition of new features. We cannot overemphasize the importance of the evaluation of well engineered solutions to the system integration task. This will be done by developing, maintaining and refining models of the system at the required levels of abstraction. The modelling activity will be performed by using suitable commercial tools, such as SIMSCRIPT and Verilog already available in the laboratory.

### System Configuration

For the initial stage of the project we have made some basic choices, based on our assessment of current technologies and on discussions with relevant experts. The major choices, with implications for our requests, are:

- *VME as the system integration bus.* VME is by now the most widely spread industry standard bus for which a variety of modules is available. In particular, a wide variety of processor cards is commercially available, as well as adaptors to other buses, such as the HEP popular buses CAMAC and Fastbus.

• *RISC based computing.* The entering of RISC architectures in the computer market has boosted in an unprecedented way the price to performance ratio for minicomputers and workstations. It is now in the range of 1k\$ per MIPS. There are clear signs that the technological limits have not yet been reached and that the trend will continue for some time. All major minicomputer and workstation manufacturers now propose RISC based systems in a market which is highly competitive, thus giving even more scope for improvement of prices and performance. VME processor cards based on RISC computers are also appearing on the market.

• *UNIX as the basic operating system.* The advent of RISC computing has accelerated the trend towards standardization on UNIX-like operating systems. Both large computer manufacturer consortiums, such as Unix International (UI) and the Open Software Foundation (OSF), and standardization bodies, such as the IEEE POSIX initiative, are actively working towards operating system environments independent of a particular (and proprietary) computer architecture. Both UI and OSF guarantee compliance with the POSIX standard.

Such choices translate into the basic high level architecture shown in fig.1, representing the minimal system on which we intend to develop the program of phase one. The system will then consist of a RISC server machine as host, running the UNIX operating system and interfaced to VME. The initial scheme foresees at least one front end processor residing in VME and running UNIX (or the kernel which we will have selected). Data recording, initially on IBM 3480 compatible cartridges, can be done either directly from the front end processor or via the host. A feature of such a design is the possibility of migrating data acquisition functions from the host to the front end processor and vice versa. In one configuration the host function is limited to monitoring and control. In the other the front end processor acts as a slave for high level processing.

For the second phase of the project we envisage an expanded system, which will provide a large number of additional functions. The addition of a second RISC computer and a second VME system including a front end processor will enable us to:

- maintain two completely separate systems, one for developments and the other for production (fig.2)
- evaluate read out architectures. Event building techniques, where the different front end processors can simulate a high level processor farm (fig. 3a) is one example
- test high level trigger techniques (fig. 3b).

The architecture described here is in our opinion well suited to achieve the goals of the two phases of the project. The hardware configuration is kept to



a minimum in order to optimize the trade off between the present investment and future improvements.

We do not underestimate the impact on the work schedule of the managing and support of the operating system environment, both in the host and in the front end processors, although the task might be easier if the common choice of UNIX is feasible.

### Software overview

We have performed a first analysis of the software requirements resulting in the following classifications.

- *Data Acquisition Toolkit*, including read out libraries, drivers, event management and distribution, event recording.
- *Framework for Monitoring*, supporting tools and development techniques for easy production of programs which use the data acquisition system for monitoring, calibration and control purposes.
- *Control* of the data taking process (run control) and of ancillary equipment (slow controls).
- *Information Management*, providing a unified way to manage all the data in the online system: calibration data, detector description, data acquisition description and status, user program description, histograms and analysis results, etc.
- *Support Software*, such as libraries and tools of general use for both the host and the front end processors. For example User Interface Management Systems (UIMS), access to the information data base, data modelling, software engineering, methods and tools.

We intend to make use of commercially available software products as much as possible. While this applies particularly to the software running on the host, the uniform use of the UNIX operating system throughout all the processors would allow extending the use of commercial software to the front end. UIMS, controls and data bases are examples of application areas in which commercial products could be used. Given the wide scope of the software aspects, encompassing all of the application areas listed above, we intend to profit as much as possible from the outcome of related studies. We also expect to establish close collaboration with other projects and groups involved in software developments, both inside and outside CERN.

## Schedule

We expect to fulfil the aim of the project according to the following schedule.

- Upgrade of the existing H2 test beam for early data taking	<i>Spring 1991</i>
- Completion of phase one, with hardware and software acquisition and system integration	<i>End 1991</i>
- Detector data taking with system completed in phase one	<i>Spring 1992</i>
- Implementation of phase two, with the exploitation of the scalable architecture and the integration of detector read out developments	<i>1992</i>
- Definition of a possible third phase, based on the evaluation of the achievements of the first two phases	<i>1992 - 1993</i>

## Resources

In order to fully exploit the potential of the proposed setup, additional expertise is needed in areas such as the development of specialised software, in particular for the front end, the choice and application of programming techniques and methods, and the evaluation of commercial products. This could be provided both by direct involvement and through collaboration with other projects and groups. In this context we have initiated discussions with the CERN groups ECP/DS and ECP/PT, as well as with other institutions, to agree on the form of their participation.

The proposed project provides an ideal opportunity to gain experience in all aspects of data acquisition systems. We therefore consider the participation of young physicists and computer scientists an essential part of the project.

We expect that general purpose products for software developments and system modelling are provided at the laboratory level. Access to basic hardware diagnostics tools, such as a digital oscilloscope and a logic state analyser, will be needed. Apart from a modest contribution to the electronics pool, we have not foreseen such entries in the budget, on the assumption that a satisfactory arrangement can be made.

**Budget**

1991	
	kSF
Host server and workstations	175
VME equipment	80
Front end processor	15
Software: licences, contribution to tools, host and front end environment	70
	TOTAL 340
CERN share (70%)	240
CERN Travel and training	50
	CERN TOTAL 290
 (Travel and training budget for Pavia is not included in this request)	
1992	
A precise request will only be possible after evaluation of the 1991 activity. A second host server for development, additional workstations, two extra processors in the front end amount to approximately	
	200
Costs for new VME equipment including fast modules, software and training are much more difficult to estimate. An investment similar to the one of 1991 would amount to approximately	
	250

We assume that the SUMMIT cartridge unit (of the value of 40 kSF) of the current UA2 setup will become part of the proposed new system.

It is also assumed that electronics and equipment specific to the detector tests will be responsibility of the detector R+D collaborations.

## Conclusions

An R+D project such as we are proposing responds to a need in the HEP community involved in LHC activities. We believe that a number of different and complementary areas will benefit from it.

- *Technology.* The challenge represented by read out, triggering and data acquisition at LHC is such that HEP will need to use the best commercially available electronics and computing technology. The understanding, mastering and the continuous monitoring of industry advances is a step that the HEP community will have to take. The proposed project will contribute with an environment where learning and evaluation will be possible in real life conditions.
- *System Integration.* R+D efforts in detector, read out, triggering and data acquisition can proceed independently, yet they will all need realistic test conditions. We propose a setup where all components of a future experiment will be integrated in an experiment-like environment.
- *Software.* In this open and modular system, specialised software will be developed and evaluated in realistic conditions.
- *Detectors.* Data taking will be possible in a modern way which will scale with the evolution of read out electronics and triggering techniques.

## References

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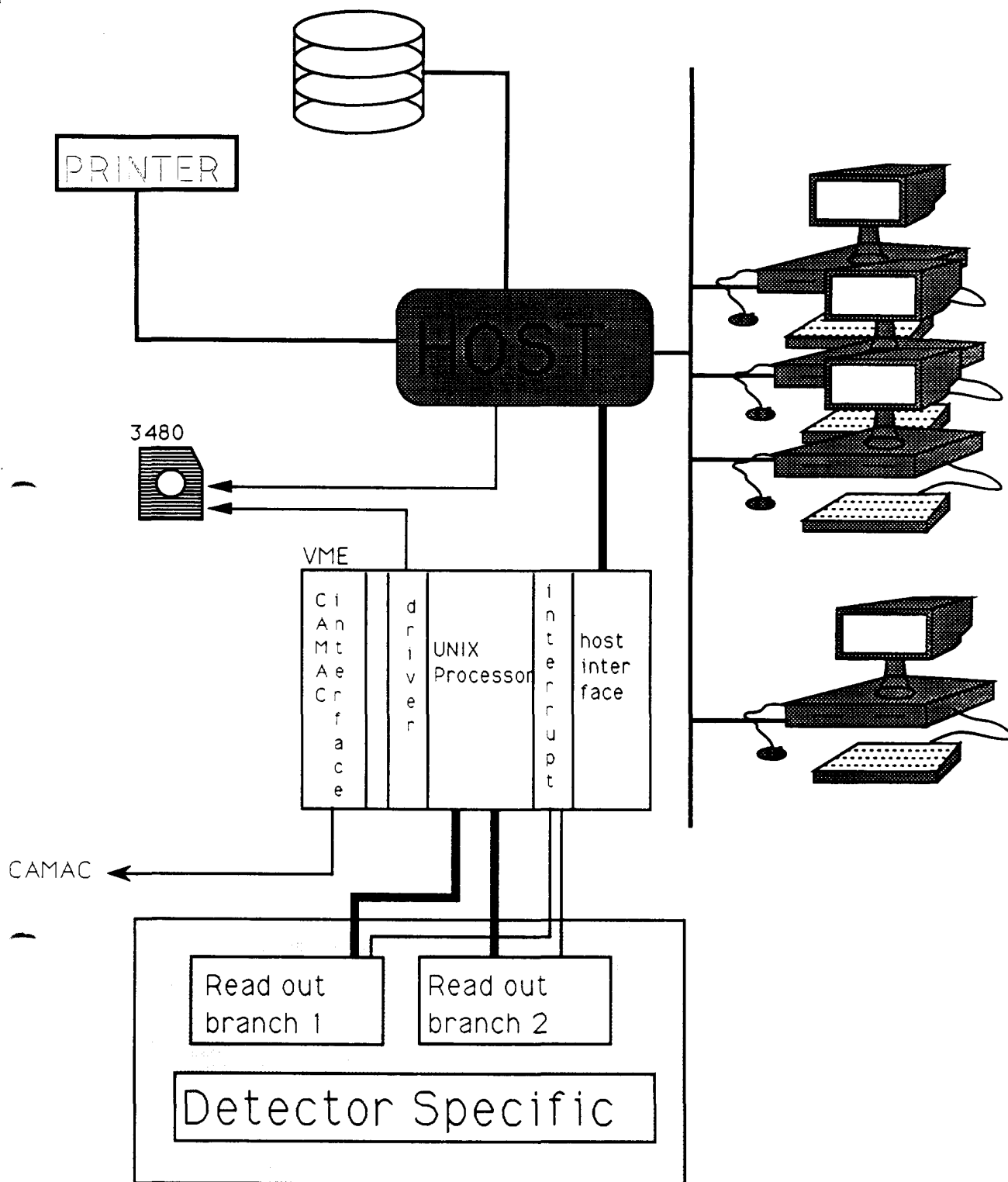


Fig. 1: Configuration for phase 1

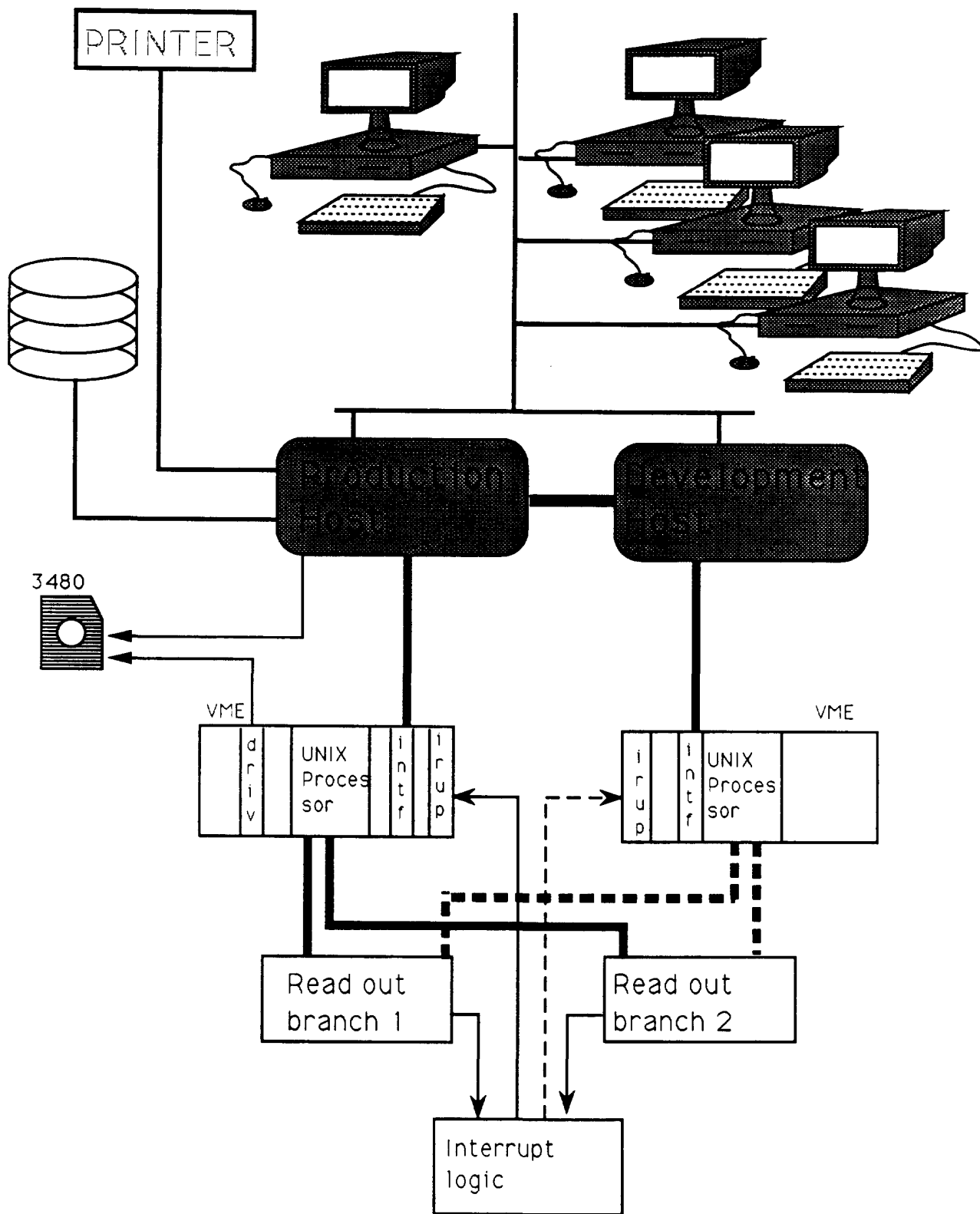
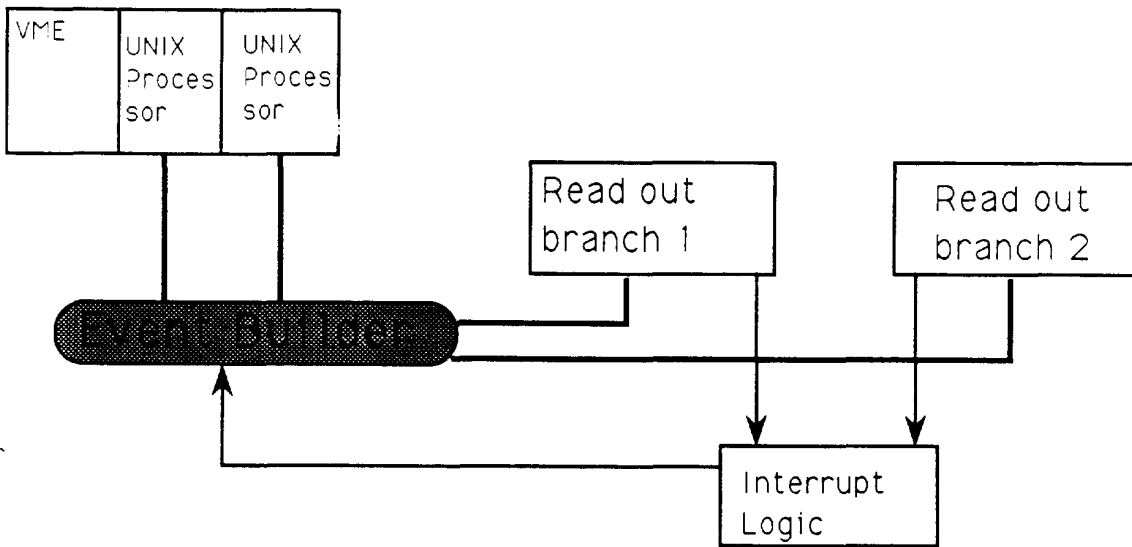


Fig. 2: Separate Read-Out Streams in Phase 2



a)



b)

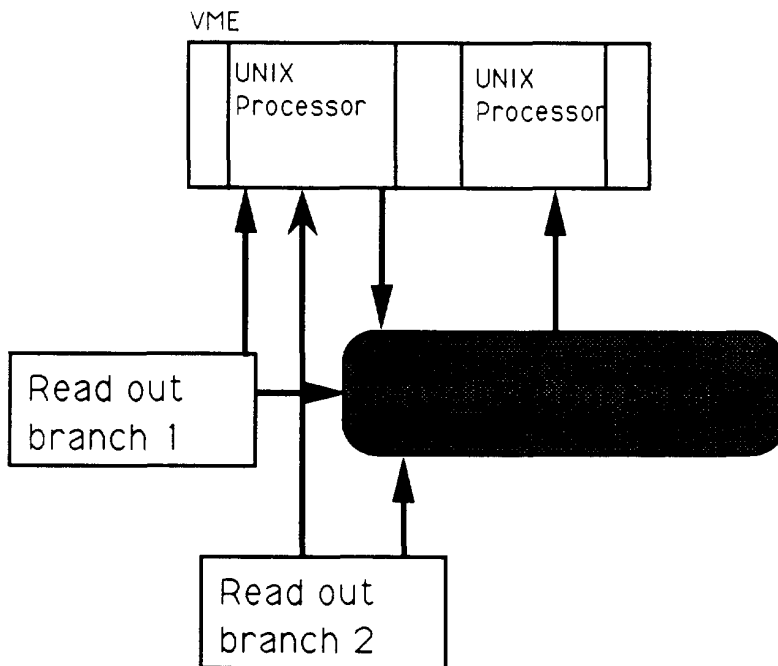


Fig. 3: Phase 2 Applications

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