# Hyper-Systolic Parallel Computing 

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#### Abstract

A new class of parallel algorithms is introduced that can achieve a complexity of $O\left(n^{\frac{3}{2}}\right)$ with respect to the interprocessor communication, in the exact computation of systems with pairwise mutual interactions of all elements. Hitherto, conventional methods exhibit a communicational complexity of $O\left(n^{2}\right)$. The amount of computation operations is not altered for the new algorithm which can be formulated as a kind of $h$-range problem, known from the mathematical field of Additive Number Theory. We will demonstrate the reduction in communicational expense by comparing the standard-systolic algorithm and the new algorithm on the connection machine CM5 and the CRAY T3D. The parallel method can be useful in various scientific and engineering fields like exact n-body dynamics with long range forces, polymer chains, protein folding or signal processing.


## 1 Introduction

Within many scientific and engineering applications one is faced with the intermediate computation of bilocal objects, $f\left(x_{i}, x_{j}\right)$, on a given set of numbers $x_{i}, i=1, \ldots, n$. Think for example of the exact treatment of 2-body forces in n-body molecular dynamics [1] as employed in astrophysics or thermodynamics of instable systems, convolutions in signal processing [2], autocorrelations in statistically generated time series [3], n-point polymer chains with long-range interactions, proteinfolding [4] or fully coupled chaotic maps [5, 6].

In the case of bilocal objects, symmetric in $i$ and $j$, the entire computation of all $f\left(x_{i}, x_{j}\right)$ requires $n(n-1) / 2$ combinations of elements. In the spirit of truly parallel processing, the $O\left(n^{2}\right)$ complexity can in principle be reduced to $O(n)$ per parallel processor if the number of processors is increased as $n$, the number of bilocal objects.

On such massively parallel computers with distributed memory, the elements $x_{i}$ of the array $\mathbf{x}$ are spread out over many processing elements, i.e. local memories. For this reason such computations in general require considerable interprocessor communication. Any progress in reducing the ensuing communication overhead is therefore welcome ${ }^{1}$.

Various methods have been devised in the past to exactly solve the computational problem; we mention two generic parallel approaches ${ }^{2}$ :

- The replicated data method [1] deals with $n$ identical copies ${ }^{3}$ of the entire array $\mathbf{x}$ that are to be placed within each processor in advance. On these arrays, the computation is performed such that each processor $i$ calculates the elements $f\left(x_{i}, x_{j}\right)$ for $j=$

[^0]$1, \ldots, n$.

- The parallel organization of the evaluation in form of a systolic array computation $[1,9,10,11]$ proceeds with one moving and one fixed array, that are distributed across the processing elements. In each systolic ${ }^{4}$ step the moving array is shifted by one position along the processing elements and subsequently, the computations are performed. After $n-1$ steps, all pairs $f\left(x_{i}, x_{j}\right)$ have been generated.

Various procedures which combine features of both above mentioned methods are known in the literature. Common to all such approaches is that both the computational complexity and the complexity of the interprocessor communication is $O\left(n^{2}\right)$.

In this work, we introduce a parallel computing concept that, to a certain extent, can be regarded as a generalization of systolic array computations with 'pulse' and 'circular movement'. We will point out that a formulation of the computational problem in the context of Additive Number Theory-leading to a kind of $h$-range problem [14]defines a new class of algorithms. Choosing the base of the $h$-range problem suitably, one can recover the classical systolic realization of the computational problem. In addition, various other bases can be contrived that allow to diminish the complexity of the interprocessor communication. We will present a selection of extremal (shortest) bases and a 'regular' base that both reduce the complexity of the interprocessor communication to $O\left(n^{\frac{3}{2}}\right)$. The regular base is nearly optimal and well suited for massively parallel machines.

The new method, further denoted as 'hyper-systolic', has in common with the standard-systolic array computation that only one array is moving in each step in a regular communication pattern. Therefore, it is well suited for SIMD and MIMD machines as is the case with standard-systolic computations. The distinctive feature as compared to the standard-systolic concept, however, lies in the fact that storing of shifted arrays is required ${ }^{5}$, similar to the replicated data method. But in contrast to the latter where the required storage goes with $n^{2}$,

[^1]a significant reduction in interprocessor communication is achieved while only a moderate additional amount of storage space is needed. To achieve the optimal hyper-systolic speed-up, the required storage goes with $n^{\frac{3}{2}}$. We will demonstrate that, in view of the state-of-the-art problem sizes mentioned in footnote 1 , our method can be of considerable practical importance.

In section 2 , we present the generic form of the computational problem to solve, in section 3 , we review the standard-systolic concept. In order to provide a graphical illustration, we will deal with systolic automata models [10, 15]. A suitable generalization of the latter which gives us the means to graphically represent the hyper-systolic parallel computing structure is worked out in section 4 . In section 5 , we discuss implementation issues concerning the hyper-systolic method on parallel machines and we compare standard-systolic computations on the Connection Machine CM5 with their hyper-systolic counterpart. Furthermore we present results from measurements on the Cray T3D. Finally, we summarize and give an outlook.

## 2 The Computational Problem

The generic computational task we deal with in the following is the calculation of

$$
\begin{equation*}
y_{i}:=\sum_{j=1}^{n} f\left(x_{i}, x_{j}\right), \quad i=1,2,3, \ldots, n, \quad i \neq j \tag{1}
\end{equation*}
$$

with the input array (sequence)

$$
\begin{equation*}
\mathbf{x}=\left(x_{1}, x_{2}, x_{3}, \ldots, x_{n}\right) \tag{2}
\end{equation*}
$$

and the resulting array

$$
\begin{equation*}
\mathbf{y}=\left(y_{1}, y_{2}, y_{3}, \ldots, y_{n}\right) \tag{3}
\end{equation*}
$$

space.

The number of combinations $\left\{x_{i}, x_{j}\right\}$ required for the computation of all $f\left(x_{i}, x_{j}\right)$ symmetric in $i$ and $j$ is

$$
\begin{equation*}
\binom{n}{2}=\frac{n(n-1)}{2}, \tag{4}
\end{equation*}
$$

i.e., the computational complexity inherent to Eq. 1 is $O\left(n^{2}\right)$.

In molecular dynamics terms, the sequence $\mathbf{x}$ can $e . g$. be thought of as the coordinates of $n$ particles, where the sequence $\mathbf{y}$ describes the potential (or equivalently a component of the force) which particle \# $i$ is subject to in the presence of all the other particles.

## 3 Standard-Systolic Computation

We first review the systolic realization of Eq. 1 from which our further considerations start. We use the concept of systolic automata models to illustrate parallel computing structures [10, 15].

A systolic automaton consists of cells with data transfer and processing units, see Fig. 1, that are arranged in a regular grid. The cells are coupled to each other in a uniform next-neighbour wiring pattern as depicted in Fig. 2. The processing elements (pe) are drawn as open triangles. They realize functions of equal load between consecutive communication events. The data transfer elements are drawn as black squares. They are delay elements (de) that represent abstractions for memory locations in which data is shifted in and out in regular clock steps $^{6}$. Data processing and transfer are completely pipelined ${ }^{7}$.

The graphical structural counterpart of Eq. 1 is given in Fig. 2. The cells are consecutively arranged in a linear order. Each cell is connected with its left and right next neighbours. Note that the systolic computation of Eq. 1 leads to a toroidal topology of the linear array.

[^2]

Figure 1: Processing element (open triangle) and delay element (black square), arranged in a systolic automaton cell (large dotted square). The element $x_{i}$ resides stationary in the processing element. In each clock step the delay element delivers another data element $\hat{x}_{j}$ of the moving array. The function $f\left(x_{i}, x_{j}\right)$ is computed and successively added to $y_{i}$ that is resident in the processing element as well.

At clock step 0 , a sequence $\mathbf{x}$ of $n$ data elements is distributed over $n$ processing elements. This sequence will stay fixed in the following process. Initially a copy $\hat{\mathbf{x}}$ of the array $\mathbf{x}$ is made. The array $\hat{\mathbf{x}}$ is shifted and the processing on all cells is performed subsequently clock step by clock step. In Fig. 2, the situation is shown for the first clock step. Fig. 3 illustrates the state of the systolic computation after 3 clock steps.

The small black boxes stand for the de's, the function of which is to shift the data element $\hat{x}_{i}$ in one clock step from cell \# $i$ to cell $\#$ $(i+1)$. Subsequently, the pe's perform the numerical computation of the function $f$, i.e., they link the elements of the fixed array $\mathbf{x}$ with the elements of the shifted array $\hat{\mathbf{x}}$. The result in the $i$-th cell is added to the resulting data element $y_{i}$ of the array $\mathbf{y}$ such that after $n-1$ steps, the resulting data elements are distributed over all processing elements ${ }^{8}$.

[^3]

Figure 2: Systolic array of abstract automaton cells with uniform next neighbour connections in toroidal topology.


Figure 3: Data location of the systolic array after the third clock step.

The mapping of the abstract automaton model onto a real parallel computer is straightforward: the pe's are identified with the processors of the parallel machine, the de's symbolize registers or memory locations exchanging data via the interprocessor communication network. Of course, for the parallel machine a communication network is required that allows to realize the above considered particular communication pattern with a toroidal topology efficiently. This is the case for the most SIMD and MIMD parallel machines, see the implementation of the hyper-systolic algorithm described in section 5 .

The complexity of the systolic computation of Eq. 1 is of order $n^{2}$ for both the data transfer operations and the processing operations, i. e. exactly $n(n-1)$ processing operations and communication events were required if the method would be applied to the full array with $n$ elements. One can improve on the scaling of the systolic realization taking into account the symmetries. The computations can be reduced to $n(n-1) / 2$ processing operations but now $n(n+1)$ communication
events have to be performed, since also the result array has to be shifted $n / 2$ times and finally one reverse shift must be carried out. This method, called 'Half-Orrery' algorithm, has been introduced in a recent paper by Scholl and Alimi [13]. The limiting behaviour of $O\left(n^{2}\right)$, however, is the same as before, for both communication and CPU operations.

## 4 The Hyper-Systolic Algorithm

The main message of this paper is that the total time expenditure for the interprocessor communication in the computation of Eq. 1 can be reduced considerably as it is possible to achieve a complexity of $O\left(n^{\frac{3}{2}}\right)$ by a suitable re-organization of the data-movement for the communicational part of Eq. 1, at a moderate expense of storage space. The amount of processing operations is not altered.

### 4.1 Motivation

Consider the matrix $C$ which explicitly enumerates the data elements of the shift-array $\hat{\mathbf{x}}_{t}$ for the clock steps $t=0,1,2, \ldots, n-1$, as delivered successively in the systolic implementation of section 3:

$$
C=\left(\begin{array}{cccccc}
1 & 2 & 3 & \ldots & & n  \tag{5}\\
n & 1 & 2 & \ldots & n-2 & n-1 \\
n-1 & n & 1 & \ldots & n-3 & n-2 \\
\cdot & & & & & \cdot \\
\cdot & & & & & \cdot \\
\cdot & & & & & \mathrm{t}=0 \\
\mathrm{t}=1 \\
\mathrm{t}=2 \\
\mathrm{t}=3 \\
& 3 & 4 & \ldots & n & 1
\end{array}\right) \begin{gathered}
\mathrm{t}=\mathrm{n}-1 .
\end{gathered}
$$

We observe in (5) that all combinations of different elements actually occur $n$ times, if every shifted array $\hat{\mathbf{x}}_{t}$ is stored for $t=0,1,2, \ldots, n-1$ and combinations between all the rows are allowed. Note that storing the shifted arrays is in contrast to the systolic concept where only one fixed and one moving array came into play. Here, as time proceeds, an
increasing number of 'resident' arrays is needed, with only one array in movement.

The matrix $C$ shows that an $n$-fold redundancy of pairings is encountered if all shifted arrays are stored. It appears natural to reduce this redundancy of pairings and optimize by storing a few arrays $\hat{\mathbf{x}}_{t}$ only, for a suitably selected subset of time steps $t$.

To illustrate the idea, let us consider a simple example for $n=16$; from matrix $C$ in Eq. 5 we take five rows:

$$
C^{\prime}=\left(\begin{array}{llllllllllllllll}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 & 16  \tag{6}\\
16 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
14 & 15 & 16 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 \\
12 & 13 & 14 & 15 & 16 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 \\
8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 & 16 & 1 & 2 & 3 & 4 & 5 & 6 & 7
\end{array}\right) .
$$

It suffices to discuss in $C^{\prime}$ combinations with element $\# 1$ only, because of the toroidal topology of the systolic array. In the first column the combinations $\{1,16\},\{1,14\},\{1,12\}$ and $\{1,8\}$ can be found, in the second column $\{1,2\},\{1,15\}$, $\{1,13\}$ and $\{1,9\}$ occur, in the fourth column we have $\{1,3\},\{1,4\}$ and $\{1,11\}$, in the sixth column we have $\{1,5\}$ and $\{1,6\}$ and in the tenth column the yet missing combinations $\{1,10\}$ and $\{1,7\}$ are present.

Thus, in order to generate all pairs for $n=16$ only 5 stored arrays are required.

We note further that to realize Eq. 1, we cannot just add the outcome of the computations to one resulting array: for every row $\hat{\mathbf{x}}_{t}$ to be stored, a separate resulting array $\hat{\mathbf{y}}_{t}$ is required. These arrays have to be shifted back in steps inverse to the foregoing. Then they can be added to give the final resulting array $\mathbf{y}$.

Therefore, for this small example, in total 8 shift-operations are required. In the standard systolic process 15 shifts of the moving array must be carried out. Using the symmetry in $i$ and $j$, in total, 17 shifts are to be performed (Half-Orrery algorithm [13]), because in this case the result array must be transported too, and finally shifted back. The array length 4 represents the cross-over between standard-systolic and the new way to compute Eq. 1 concerning the number of array shifts.

Going to larger arrays, the new algorithm becomes more and more advantageous.

### 4.2 The algorithm

We now give a general prescription to compute Eq. 1 according to the ideas exposed in the last section. The new algorithm is called hyper-systolic, the name referring to the topological features of the underlying communicational structure:

1. For a given array $\mathbf{x}$ of length $n, k$ copies $\hat{\mathbf{x}}_{t}$ are generated by shifting the original array $\mathbf{x} k$ times by a stride $a_{t}$ and storing the resulting arrays as $\hat{\mathbf{x}}_{t}, 1 \leq t \leq k$. The variable stride $a_{t}$ of the shifts must be chosen such that
(a) all pairings of data elements occur at least once,
(b) the number of equal pairings is minimized,
(c) the number of shifts $k$ is minimized,
(d) the number of different strides $a_{t}$ is minimized.
2. The required $n(n-1) / 2$ results $y_{i}$ according to Eq. 1 are successively computed and are added to $k$ resulting arrays $\hat{\mathbf{y}}_{t}$.
3. Finally, applying the inverse shift sequence, the arrays $\hat{\mathbf{y}}_{t}$ are shifted back and corresponding entries are summed up to build the elements of the final array $\mathbf{y}$.

In the above defined hyper-systolic parallel computing structure, in general, $2 k$ intermediate arrays are required. Later, we will come to special realizations that work with less intermediate arrays.

### 4.3 Graphical representation

The concept of systolic automata models can be transferred to the hyper-systolic parallel computing structure. For the graphical representation we use the objects introduced in section 3. Fig. 4 shows the $i$-th hyper-systolic cell unit. The de's again represent input and


Figure 4: Processing element (open triangle), delay element (black square) and store elements (se) (open squares), arranged in a hyper-systolic automaton cell (large dotted square). The element $\hat{x}_{i}$ resides stationary in the storing element. First, in each clock step $t$, the delay element delivers a new data element $\hat{x}_{i+a_{t}}$ that is both stored in the local se and transmitted further. Subsequently the computing is performed on the relevant combinations of yet stored elements. The results are stored in the corresponding memory locations $\hat{y}_{i+a_{t}}$. Note that each de is equipped with $r$ connectors to account for the $r$ different strides $a_{t}$. Second, the results $\hat{y}_{i+a_{t}}$ have to be successively shifted back, using a stride sequence inverse to the above, and added up to yield the final result.
output. Additionally we use open rectangles to symbolize the memory locations for the stored data elements $\hat{x}_{i+a_{t}}$ and $\hat{y}_{i+a_{t}}, 1 \leq t \leq k$, $1 \leq i \leq n$. Thus we account for the original systolic functionality of the de's acting on transient data elements only ${ }^{9}$. The de's now possess 1 input and $r$ output connectors, one separate connector for each required shift width $a_{t}$. In general, the number of connectors $r$ is not equal to $k$. It depends on the chosen hyper-systolic scheme.

Again the cells are arranged in a uniform grid; in addition to the next-neighbour wiring, the new connections between the processors are drawn in Fig. 5. They correspond to the shifts of data elements

[^4]

Figure 5: 3 abstract automaton cells as part of a hyper-systolic array with $r=2$ uniform next neighbour connections and toroidal topology. In this simplified case, the two strides are of length 1 and 2.
by strides $a_{t}$. According to the number $r$ of different strides $a_{t}, r$ direct connections would be optimal. From the point of view of the original one-dimensional systolic array structure - due to these additional communication connections - the (one-dimensional) space of processing elements has acquired topologically non-trivial interconnections. Fast interprocessor data transfer to distant cells can be achieved in one clock step via these interconnections that are used as shortcuts. Thus the characterization of our new algorithm as hyper-systolic.

The pe's now don't realize functions of equal load between consecutive communication events. The amount of processing operations $g(t)$ increases with an increasing number $t$ of stored arrays $\hat{\mathbf{y}}_{t^{\prime}}, 1 \leq t^{\prime} \leq t$. We emphasize again that hyper-systolic data movement and storing extends the standard-systolic concept.

Fig. 5 indicates the graphical structural counterpart of Eq. 1 for the hyper-systolic algorithm; we have plotted the situation for $t=1$. At clock step $t=0$, a sequence $\mathbf{x}$ of $n$ data elements is distributed over $n$ processing elements. In every clock step $t=0,1,2, \ldots, k$, a copy $\hat{\mathbf{x}}_{t}$ of the array $\hat{\mathbf{x}}_{t-1}$ is generated and, in the next clock step, the array is shifted by a stride $a_{t}$. Subsequently, the new array $\hat{\mathbf{x}}_{t}$ is stored in the se's. Then the processing can be done by the pe's involving ever more of the stored arrays for increasing $t$. Fig. 6 shows the situation after 2 clock steps. Note however that only one array is moving as is the case in the standard-systolic computation.


Figure 6: Data location on a part of the hyper-systolic array after the second clock step.

In clock step $t$, the $g(t)$ results in the $i$-th cell are added to the corresponding elements $y_{i+a_{t^{\prime}}}, 1 \leq t^{\prime} \leq t$. Finally, when $n(n-1) / 2$ processing operations have been performed, the $k$ resulting arrays $\hat{\mathbf{y}}_{t}$ are shifted back by strides inverse to the above sequence and successively added up to the result array $\mathbf{y}$.

### 4.4 Additive Number Theory and hyper-systolic parallel processing

As explained in section 4.2, our task is to construct a sequence of strides $A_{k}=\left\{a_{0}=0, a_{1}, a_{2}, a_{3}, \ldots, a_{k}\right\}$ that-in the course of the hyper-systolic process-provides us with $k+1$ sequences $\hat{\mathbf{x}}_{t}, t=$ $0,1,2, \ldots, k$, represented as a rectangular matrix $C^{\prime 10}$ :

$$
C^{\prime}=\left(\begin{array}{ccccc}
x_{1+a_{0}} & x_{2+a_{0}} & x_{3+a_{0}} & \cdots & x_{n+a_{0}}  \tag{7}\\
x_{1+a_{1}} & x_{2+a_{1}} & x_{3+a_{1}} & \cdots & x_{n+a_{1}} \\
\cdot & & & & \cdot \\
\cdot & & & & \cdot \\
\cdot & & & & \cdot \\
x_{1+a_{k}} & x_{2+a_{k}} & x_{3+a_{k}} & \cdots & x_{n+a_{k}}
\end{array}\right) .
$$

As mentioned above, in $C^{\prime}$ all indices are understood as $\bmod \left(i+a_{1}-\right.$ $1, n)+1$. It is required that all combinations of elements from 1 to

[^5]$n$ can be constructed along the columns of $C^{\prime}$. The integer $k$ is to be chosen as small as possible. $a_{t}$ is the stride by which $\hat{\mathbf{x}}_{t-1}$ is cyclically shifted to render $\hat{\mathbf{x}}_{t}$.

We formulate the algorithmic problem in terms of Additive Number Theory:

Let $I$ be the set of integers $m=\{0,1,2 \ldots, n-1\} \in{ }_{0}^{n}, n \in$. Find the ordered set $A_{k}=\left(a_{0}=0, a_{1}, a_{2}, a_{3}, \ldots, a_{k}\right) \in{ }_{0}^{k+1}$ of $k+1$ integers, with $k$ minimal, where each $m \in I,(0 \leq m \leq n-1)$, can be represented at least once as the ordered partial sum

$$
\begin{equation*}
m=a_{i}+a_{i+1}+\ldots+a_{i+j} \tag{8}
\end{equation*}
$$

or as

$$
\begin{equation*}
m=n-\left(a_{i}+a_{i+1}+\ldots+a_{i+j}\right) \tag{9}
\end{equation*}
$$

with

$$
\begin{equation*}
0 \leq i+j \leq k, \quad i, j \in_{0} . \tag{10}
\end{equation*}
$$

This formulation with the extremal base $A_{k}$ is reminiscent of the 'postage stamp problem', a famous problem in Additive Number Theory $[14,17]$. In contrast to the original postage stamp problem, here we deal with sequences $A_{k}$ instead of sets and with ordered partial sums. In these terms we are looking for the $h$-range $n\left(h, A_{h}\right)$ of the extremal basis $A_{h}$ with only ordered partial sums of the elements of $A_{h}$ allowed as given by Eqs. 8, 9 and 10.

Unfortunately, our problem is just as little solvable in general as the postage stamp problem. Nevertheless, later we will propose an approximate solution that carries optimal asymptotic scaling properties and is very well suited for the hyper-systolic realization on parallel SIMD and MIMD machines.

The formulation in terms of an $h$-range problem appears to provide a quite general framework covering a whole class of algorithms: any chosen base $A$ induces its specific new algorithm.

The realization of $A_{k}$ with $k=n-1$ brings us back to the standardsystolic algorithm with the base

$$
\begin{equation*}
A_{n-1}=\left\{0, a_{1}, \ldots, a_{n-1}\right\}, \quad a_{i}=1 \quad \forall i=1, \ldots, n-1, \tag{11}
\end{equation*}
$$

that features a communicational complexity of $O\left(n^{2}\right)$.
The realization

$$
\begin{equation*}
A_{\frac{n}{2}}=\left\{0, a_{1}, \ldots, a_{\frac{n}{2}}\right\}, \quad a_{i}=1 \quad \forall i=1, \ldots, \frac{n}{2}, \tag{12}
\end{equation*}
$$

leads to the Half-Orrery algorithm if the result array is moved too.
A lower bound on the minimal possible $k$, with optimal complexity, can be derived by the following consideration:

The total number of combinations required is $n(n-1) / 2$. Let the matrix $C^{\prime}$ of Eq. 7 be realized by $k$ shifts, $i . e$. by $k+1$ arrays. The number of possible combinations between the elements of a given column of $C^{\prime}$ follows as $\binom{k+1}{2}$. Thus, the following unequality holds:

$$
\begin{equation*}
\frac{n(n-1)}{2} \leq\binom{ k+1}{2} n, \tag{13}
\end{equation*}
$$

therefore,

$$
\begin{equation*}
k \geq-\frac{1}{2}+\sqrt{n-\frac{3}{4}} . \tag{14}
\end{equation*}
$$

with $k$ integer. Obviously, a sequence $A_{k}$ with less than $k_{\text {min }}$ elements cannot solve the h-range problem presented above. In other words, the complexity for the interprocessor communication of any hyper-systolic algorithm can at best be $n \sqrt{n}$.

### 4.5 Regular bases

In choosing a suitable base for the hyper-systolic algorithm, we better make use of the fastest links of our parallel architecture. So we have to meet a constraint: in general, from each processor there is a limited number $r$ of fast connections to $r$ other processors. This is, however, very much dependent on the particular parallel machine. On (hyper)cubic interconnection networks, e.g., $r$ relates to the dimension of the hypercube. We should prefer shift sequences that are restricted to exploit the $r$ fast interprocessor connections available, in
the actual implementation of the hyper-systolic method on a parallel machine. To a certain extent, the network can provide shortcuts or 'wormholes' through higher dimensions that allow to accelerate the standard-systolic movement along the one-dimensional array.

In the case of the standard-systolic array, $r=1$, because only next neighbour wiring is requested in the systolic process. This amounts to take local trains only for long-distance traveling.

The next simple step would be a mix of intercity and local connections for the long-distance journey. In fact, a nearly optimal choice of a suitable sequence, leading to a very efficient implementation of the hyper-systolic ideas and requiring $r=2$ interprocessor connections only, is given by:

$$
A_{k=2 K-1}=(\underbrace{1,1, \ldots, 1}_{K}, \underbrace{, K, \ldots, K)}_{K-1}, \quad K=\sqrt{\frac{n}{2}},
$$

with $K$ shifts by 1 and $K-1$ shifts by $K$. The length of the base is $k=2 K+1$. It can easily be shown that such a base leads to an h-range of $n$ with respect to Eqs. 8 and 9 . The communicational complexity of the hyper-systolic method using the regular shift sequence with shift constant $K$, i.e. strides $a_{t}=1$ for $t \leq K$ and $a_{t}=K$ for $t>K$, turns out to be $2 n(2 \sqrt{n / 2}-1)$. Note that we have included an additional factor 2 . This is due to the fact that the number of required reverse shifts the result arrays are subject to also is given by $2 \sqrt{n / 2}-1$.

In order to illustrate the hyper-systolic array generated by the regular base let us plot an example where $n=32$ and $K=\sqrt{\frac{n}{2}}=4$ in Fig. 7:


Figure 7: Matrix C' for $n=32$ using the regular base $A_{7}=(1111444)$.

Building combinations along the columns, all pairings of the numbers

1 to 32 between the different rows can be found at least once. Note that the last row requires a separate treatment as, only in that case, the pairs occur twice.

Obviously, $K=\sqrt{\frac{n}{2}}$ makes only sense for integer values $K$. Therefore, $\frac{n}{2}$ should be a square number. However, if this is not possible, one can switch over to a suitable neighbouring integer value $K \sqrt{\frac{n}{2}}$ as shift constant.

### 4.6 Shortest bases

The regular bases just introduced are well suited for massively-parallel machines with a large number of processors.

Let us consider the ratio $R$ between standard- and hyper-systolic communicational complexity, the "gain-factor",

$$
\begin{equation*}
R=\frac{n+1}{2\left(2 \sqrt{\frac{n}{2}}-1\right)} \approx \sqrt{\frac{n}{8}} \tag{16}
\end{equation*}
$$

On a machine with 32 processors, e.g., we can gain a factor of 2 in interprocessor communication events between standard-systolic and hyper-systolic computations. This ratio is increasing rapidly going to machines with larger numbers of processors and e.g. becomes 11 for 1024 processors.

On coarser grained computers with \# of processors $\leq 64$, other bases than the regular type might be more advantageous.

In absence of analytical solutions, for various numbers of processors $p$ from 4 to 64 we have constructed well suited extremal bases by straightforward computation. We tried to prefer bases with elements being a power of 2 , as these strides might lead to fastest interprocessor communication on most parallel machine's networks.

Table 1 collects our selection of extremal bases. On a 32 node parallel machine, e.g., we can theoretically gain a factor $R=2.75$ compared to $R=2$ using the regular base.

| $p$ | $k$ | $A_{k}$ | $p$ | $k$ | $A_{k}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4 | 2 | 11 | 5 | 2 | 11 |
| 6 | 2 | 12 | 7 | 2 | 12 |
| 8 | 3 | 112 | 9 | 3 | 112 |
| 10 | 3 | 122 | 11 | 3 | 122 |
| 12 | 3 | 124 | 13 | 3 | 214 |
| 14 | 4 | 1114 | 15 | 4 | 1114 |
| 16 | 4 | 1224 | 17 | 4 | 1128 |
| 18 | 4 | 2184 | 19 | 4 | 3684 |
| 20 | 5 | 11144 | 21 | 4 | 31025 |
| 22 | 5 | 11144 | 23 | 5 | 11144 |
| 24 | 5 | 11148 | 25 | 5 | 11288 |
| 26 | 5 | 12344 | 27 | 5 | 12288 |
| 28 | 6 | 111444 | 29 | 6 | 111444 |
| 30 | 6 | 111444 | 31 | 6 | 111444 |
| 32 | 6 | 111448 | 36 | 6 | 3618412 |
| 48 | 7 | 311171644 | 64 | 8 | 11123108204 |

Table 1: Shortest bases for various machine sizes.

For $p>32$ it becomes increasingly difficult to find extremal bases with elements near a power of 2 that would be shorter than the regular base. For $p=64$, however, if we do not require all elements being a power of 2 , the shortest base is only $k=8$ elements in length whereas the regular base needs $k=11$ elements.

Again we illustrate the hyper-systolic algorithm using an extremal base for $n=32$, see Fig. 8:


Figure 8: Matrix C' for $n=32$ using the extremal base $A_{6}=(111448)$.

### 4.7 Coarse grained limit

The number of processors $p$ of a given parallel machine and the number of array elements $n$ can be different. In order to adapt both the standard-systolic and the hyper-systolic concept to this situation, we can partition the array of $n$ elements into $\frac{n}{p}$ subarrays, such that each processor deals with $\frac{n}{p}$ data elements. Each subarray (of $p$ elements) is distributed across the $p$ processors and can be treated by the standardsystolic or hyper-systolic method such that successively all required combinations between all $n$ data elements can be constructed.

To illustrate the situation, the two stored hyper-systolic arrays for $p=16$ and $n=32$ using the extremal base of Table 1 are depicted in Fig. 9.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 16 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 14 | 15 | 16 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| 12 | 13 | 14 | 15 | 16 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 32 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| 30 | 31 | 32 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 |
| 28 | 29 | 30 | 31 | 32 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
| 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |

Figure 9: Two matrices $\mathrm{C}^{\prime}$ for $n=32$ and $p=16$ using the extremal base $A_{4}=(1224)$.

Considering the complexity, in the standard-systolic (Half-Orrery) computation, $n(p+1)$ interprocessor data movements have to be carried out, whereas in the hyper-systolic case the number of interprocessor movements follows as $2 n(2 \sqrt{p / 2}-1)$. The improvement again can be described by the ratio $R$ of Eq. 16,

$$
\begin{equation*}
R \approx \sqrt{\frac{p}{8}} . \tag{17}
\end{equation*}
$$

With $n \gg p$ it becomes important to compare the pure computation
time vs. the interprocessor communication time as the former scales as $O\left(n^{2}\right)$. If we take $n$ very large the parallel machine turns back to a scalar machine, i.e., interprocessor communication becomes irrelevant for both standard-systolic and hyper-systolic computations. Of course there is a limit in cpu-power, and the latter determines the maximal possible $n$ that can be computed in reasonable time. In practice, for that value of $n$, one has to determine the amount of interprocessor communication overhead compared to the pure computation in order to asses a substantial improvement of the hyper-systolic method vs. the standard-systolic method.

## 5 Performance Tests and Results

We will demonstrate in the following section that the hyper-systolic method, applied to the computation of Eq. 1 on massively parallel computers, is indeed superior to standard-systolic implementations in real life applications. In the realistic setting of an exact molecular dynamics simulation with long range forces, we study the performance of standard- hyper-systolic n-body dynamics with mutual gravitational interactions on connection machines CM5 with numbers of nodes in the range of 16 to 1024 and 320 -node Cray T3D.

### 5.1 Molecular dynamics with long-range for-

 cesThe gravitational force $\vec{F}\left(\vec{x}_{i}\right)$ acting on the $i$-th particle within an ensemble of $n$ particles of equal mass $m=1$ reads:

$$
\begin{equation*}
\vec{F}\left(\vec{x}_{i}\right)=\sum_{j=1}^{n} \frac{\vec{x}_{i}-\vec{x}_{j}}{\left|\vec{x}_{i}-\vec{x}_{j}\right|^{3}}, \quad j \neq i \tag{18}
\end{equation*}
$$

where the gravitation constant is set to 1 . The $\vec{f}\left(\vec{x}_{i}, \vec{x}_{j}\right)=\frac{\vec{x}_{i}-\vec{x}_{j}}{\left|\vec{x}_{i}-\vec{x}_{j}\right|^{3}}$ by Eq. 18 belong to the class of symmetric bilocal objects used in Eq. 1. We deal with two dimensions, i.e., $\vec{x}_{i}=\binom{x_{i}^{1}}{x_{i}^{2}}$.

In a molecular dynamics simulation, given a distribution of particles to which coordinates and momenta are assigned at time step $T=l$, the long range forces between the particles are calculated with respect to Eq. 18, and subsequently, the new positions and momenta at time step $T=l+1$ are found using a suitable integration method like, e.g., the leap frog scheme ${ }^{11}$ [18]. The time-consuming part of the simulation is the computation of Eq. 18. In order to improve on the interprocessor communication we have to concentrate on the efficient parallel implementation of the latter. As we here deal with two dimensions, two arrays of coordinates, $\overrightarrow{\mathbf{x}}=\binom{\mathbf{x}^{1}}{\mathbf{x}^{2}}$, describe the position of the given particle. The momenta do not enter the computation of Eq. 18.

### 5.2 Implementation issues

At this stage the individual features of the programming languages and network topologies are discussed.

CM-FORTRAN [19] This parallel language supports the concept of 'virtual' processors. From the user's point of view, it allows to emulate a virtual parallel machine with $n$ virtual processors, whereas the real machine has $p$ real processors. In principle, the user can write programs as if there would be a machine with $n$-processors at hand, and the compiler and the operating system take care of the additional administrative overhead. CM-FORTRAN appears to be well suited for the straightforward implementation of a one-dimensional standard-systolic array. The hyper-systolic method, however, requires explicit control over the data distribution across the $p$ real processors. Therefore, on a machine with $p$ real processors, we cut the array into $n / p$ parts and declare each array of $p$ elements as data-parallel array.

The interprocessor communication network on a connection machine CM5 is based on the fat-tree concept [20]. We expect that communication times to nodes at a 'distance' of more than one processor scale logarithmically with the number of processors. A connection machine

[^6]CM5 meets the requirements of the hyper-systolic concept with regular array shifts: for any available machine sizes ranging from 16 to 1024 processors, the shift of a data element to a location at distance $a_{t}=K=\sqrt{p / 2}$ in the hyper-systolic array, is achieved nearly as fast as the shift to the next array element ( $a_{t}=1$ ) because the latency dominates the communication time.

T3D A message passing parallel programming language, as e.g. PVM implemented on the Cray T3D, does not support virtuality. We set up the array of $n$ data elements on $p$ processors available in the straightforward way discussed above, cutting the array into $n / p$ parts. Note that PVM is not the only way to program message passing on the T3D. We did, however, not employ the fast low-level communication routines that are available.

The T3D's communication network consists of a three-dimensional torus. Unlike the CM5's network, colliding messages are possible on this network. If the T3D application is run on a small partition it cannot use the toroidal structure. However, we expect the latency for exchange of interprocessor messages to dominate the 'node-hopping' time and therefore only little influence of this effect should be observable.

### 5.3 Performance results on CM5 and T3D

On the CM5, we want to avoid any interference of the 'VP-management' with improvements due to the hyper-systolic computation. For our tests, we decided to work with $n=p$ on CM5 and CRAY T3D, i.e., the VP-ratio is 1 on the CM5. Therefore, any gain in performance should theoretically scale as given by Eq. 16. ${ }^{12}$

We had access to the connection machine CM5 at GMD/HLRZ, Germany, with partitions of 16,32 , and 64 nodes and the CM5 at Los Alamos National Laboratories, USA, with 128, 512 and 1024 node

[^7]partitions. Furthermore, we were able to conduct performance measurements on the 320-node Cray T3D at Edinburgh Parallel Computing Centre (EPCC) where we tested our algorithm using partitions of 16, 32, 64, 128 and 256 nodes.

Table 2 gives the hyper-systolic shift constant $K$ as a function of the number of processors and the number of shifts for the moving array x .

| p | 16 | 32 | 64 | 128 | 256 | 512 | 1024 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| K | 2 | 4 | 6 | 8 | 12 | 16 | 24 |
| k | 4 | 7 | 11 | 15 | 23 | 31 | 47 |

Table 2: Shift constants $K$ for the regular shift sequence as function of the number of processors.

We plotted the actual interprocessor communication time (ipc) and the cpu-time for the computation of Eq. 18 in one molecular dynamics step as function of the number of processors $p=n$ in Fig. 10, both for the standard-systolic and the hyper-systolic algorithm. As indicated, the lines connect results from different partitions of one and the same machine. Fig. 11 is a logarithmic replot of Fig. 10 to exhibit scaling behaviour. The figure shows equal scaling of all curves except the curve showing the time for the hyper-systolic communication. We note that the hyper-systolic computation appears to need slightly less cpu-time than the systolic computation. This is probably due to a slightly improved pipelining of the cpu-operations, see footnote 12 on page 22 .

It turns out that the standard-systolic computation-for $p=n$-is dominated by interprocessor communication on both the connection machines CM5 and the CRAY T3D ${ }^{13}$. On the T3D, the effect of the

[^8]

Figure 10: Interprocessor communication time (ipc) and cpu-time for the computation of Eq. 18 in one molecular dynamics step as function of the number of processors $p=n$. The lines connect results from different partitions of one and the same machine.


Figure 11: Same plot as before using a logarithmic y-scale.
hyper-systolic computation being less cpu-time intensive is much pronounced due to the time consuming caching. Most of the time is spent with load and store operations between cache and local memory.

Since both, the CPU-time required and the interprocessor communication time should grow proportional to $n^{2}$, the ratio between both values would be expected to vary only slightly for the standard-systolic method as is the case for the T3D. On the CM5, we have to take into account logarithmic corrections in interprocessor communication as explained later. The result is depicted in Fig. 12. We see that the interprocessor communication will become irrelevant on massively parallel machines, where the hyper-systolic computation of Eq. 18 can show its full power.

In Fig. 13, we present the gain-factor $R$ between the standard-systolic and hyper-systolic interprocessor communication times along with the theoretical prediction. In our particular implementation, we expect a scaling of the gain-factor according to $R=\sqrt{p / 2} / 3$ in contrast to Eq. 16. The dashed curve represents this naive expectation. On the CM5, however, we have to take into account logarithmic corrections to the scaling law. This is due to the fat-tree hierarchy of its communication network: communication times to processors in a 'distance' $r$ increase logarithmically with $r$. Our findings demonstrate that the hyper-systolic algorithm will at any rate be superior to conventional methods: the interprocessor communication expense grows with $n^{\frac{3}{2}}$ as compared to $n^{2}$. The full power of the method can be exploited on big massively parallel machines.

The additional amount of memory needed in hyper-systolic computations is tolerable in view of the present machine's and problem's sizes: even on the largest CM5 with $p=1024$ we only need $2 \times 24 \times 1024$ words of additional memory. Of course, this has to be multiplied by $n / p$ if we go to $n>p$.


Figure 12: Ratio of interprocessor communication time to cpu-time for the standard-systolic and hyper-systolic computation.


Figure 13: Gain-factor $R$ between the standard-systolic and hyper-systolic interprocessor communication times. Two theoretically predicted curves are plotted. On the CM5, we take into account logarithmic corrections to $\sqrt{p / 2} / 3$.

## 6 Discussion

Summary We have presented a new parallel algorithm for the efficient computation of systems of $n$ elements with pairwise mutual interactions among all elements, denoted as hyper-systolic algorithm. We have developed the hyper-systolic array computation by generalizing the ordinary systolic realization of the computational problem. We illustrated the hyper-systolic algorithm in form of the canonical abstract automaton representation as it is known from systolic array computations.

In the context of Additive Number Theory, the hyper-systolic method very naturally can be formulated as an $h$-range problem $n\left(h, A_{h}\right)$. We have discussed a solution of the latter problem which is well suited for the explicit parallel implementation of a hyper-systolic computation on SIMD and MIMD machines and nearly optimal with respect to the efficiency of the interprocessor communication.

We applied our method to the computation of the molecular dynamics evolution of a system of $n$ particles with long range forces. In the practical implementation on 16 up to 1024-node connection machines CM5 and on 16 up to 256 -node partitions of the CRAY T3D we could verify the expected theoretical improvement in interprocessor communication as compared to the standard-systolic realization.

Conclusions The hyper-systolic way of parallel computing can be extended to a variety of parallel computations which are usually done by systolic $n^{2}$-loops. The potential of the method appears of great promise. It might even affect the very architectural issue of parallel machines, as it is efficiently applicable on massively parallel machines with simple (and therefore cheap) toroidal next-neighbour communication networks [21]. As an example, we will implement the hypersystolic array computation on Quadrics (APE 100) machines produced by Alenia Spazio S.p.A. [21]. These machines are equipped with a simple three-dimensional next-neighbour network. We expect the hypersystolic computation to speed-up the Quadrics performance considerably [22]. The full payoff of the idea will be achieved, of course, on
real massively parallel platforms such as described in [23].
We hope that the hyper-systolic approach of tackling $n^{2}$-loop problems will provide an essential improvement for practical simulations.

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[^0]:    ${ }^{1}$ In molecular dynamics applications with long range forces, e.g., exact state-of-the-art calculations are restricted to a number of elements (particles) in the range of $<100.000$. Exact computations are required near locations where physical systems exhibit a phase transition. In such applications, repeated computations of the elements $f\left(x_{i}, x_{j}\right)$ have to be performed with a number of steps in the range of $10^{3}$ to $10^{5}[7]$.
    ${ }^{2}$ Parallel 'linked-cells' algorithms play the major rôle in molecular dynamics with short range forces [8].
    ${ }^{3}$ Here we assume that the numbers of processors, p , and array elements, n , are equal. The case $p<n$ is discussed in section 4.7.

[^1]:    ${ }^{4}$ In molecular dynamics, systolic array computations are known as Orrery-algorithm [12, 13].
    ${ }^{5}$ Complexity in (computer) time is avoided at the expense of complexity in (storage)

[^2]:    ${ }^{6}$ By 'clock step' we denote the clock step of the abstract automaton rather than a physical computer clock step.
    ${ }^{7}$ Precise definitions of systolic arrays and algorithms along with many examples and applications can be found in two monographs by N. Petkov [10, 15]

[^3]:    ${ }^{8}$ In terms of the molecular dynamics example, each particle coordinate is located together with its respective force value in the same processing element.

[^4]:    ${ }^{9}$ We note that the index $i+a_{t}$ is to be taken as $i+a_{t}-n$ for $i+a_{t}>n($ or $\bmod (i+$ $\left.a_{t}-1, n\right)+1$ ) because of the toroidal topology of the hyper-systolic array.

[^5]:    ${ }^{10}$ Note that we have introduced the zero-element.

[^6]:    ${ }^{11}$ The integration is a purely local procedure, therefore no interprocessor communication is required in that step.

[^7]:    ${ }^{12}$ We emphasize that with $n=p$, we don't have the advantage of vectorizing capabilities or communication pipelining.

[^8]:    ${ }^{13}$ Note that we have chosen a realistic setting of the gravitational force, leading to the compute intensive calculation of a square root for every coordinate difference. In our test model, the system is not given a boundary condition, and we have cut off the potential for very small separations of particles, as is necessary in realistic simulations.

