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# A TRANSIMPEDANCE AMPLIFIER USING A NOVEL CURRENT MODE FEEDBACK LOOP

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## Abstract

We present a transimpedance amplifier stage based on a novel current mode feedback topology. This circuit employs NMOS and PMOS transistors exclusively and requires neither capacitor for stabilizing the transimpedance loop nor resistor for the transresistance feedback and transistor loading. This amplifier circuit is fully compatible with submicron digital CMOS processes. The active feedback network consists of two grounded-gate MOS devices which split the output current in both the feedback and output branches. The transresistance and the phase margin are adjustable through external DC signals. The measured rise time of the impulse response of the amplifier implemented in an industrial 0.7 μm CMOS process is 18 ns for a transresistance of 180 kΩ and 30 ns for a transresistance of 560 kΩ. The measured Equivalent Noise Charge (ENC) is 800 rms $e^-$ for an input capacitance of 20 pF with the transresistance adjusted to 560 kΩ.

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## 1 INTRODUCTION

Transimpedance amplifier designs with low-noise and high-speed characteristics are key components in many front-ends, such as optical data-link receivers, smart-pixel-sensor amplifiers and preamplifiers for radiation detectors. The transimpedance configuration circuit is also an attractive approach for fast amplifiers for silicon-drift and -strip detectors at the LHC experiments. Several of the current sensitive preamplifiers for silicon-strip detector applications have been designed in hybrid circuits with bipolar [1] and MOS [2] technologies. More recently, transimpedance preamplifiers have been designed in bipolar, integrated-circuit technologies [3–7].

The main features desired for fast front-end amplifiers are low noise, high gain and excellent frequency stability. Moreover, the developement of front-end systems in radiation-hard CMOS processes [8–10] for the future LHC detectors and advances in deep submicron CMOS technology require design circuit techniques increasingly compatible with digital CMOS processes. The active current feedback circuit principle presented in this paper provides a means of improving the speed performance of a transimpedance amplifier without sacrificing stability or noise, and is fully compatible with digital processes. This novel circuit technique is very compact and enables control of the transresistance gain over a large range (1–10), via an external current, again without affecting amplifier stability. The amplifier architecture can accept a DC input connection with a leaky sensor, such as a silicon-strip detector, without its performance being impared. This circuit does not require any additional passive components such as capacitors or resistors and is therefore compatible with deep submicron CMOS processes. Alternatively, the same circuit can be used to implement a high-value feedback resistor ( > 10 MΩ) for a charge amplifier, by operating the active feedback at very low current.

The active feedback loop circuit principle is presented in Section 2, and is compared with the traditional transresistance feedback structure. In Section 3 the implementation of the active feedback in a transimpedance amplifier in CMOS technology is presented and crucial design issues are discussed. The first experimental results of the active feedback transimpedance amplifier are presented in Section 4, in particular, the noise characteristics. Section 5 concludes the paper with discussion of the future development of this circuit.

## 2 THE ACTIVE FEEDBACK PRINCIPLE

Figure 1 shows a basic circuit diagram for a traditional CMOS or bipolar transimpedance amplifier. Low-noise performance is ultimately determined by the parallel input noise current, inversely proportional to $R_f$. Hence, from the point of view of noise, a high value of $R_f$ is desired — typically above 100 kΩ — to keep the parallel Equivalent Noise Charge (ENC) contribution below 500 rms electrons for a system peaking time of 25 ns to 50 ns. One important consideration is the maintenance of stability under all operating conditions. Major parasitic capacitances affecting the frequency response of the amplifier are shown in Fig. 1. Assuming that the Miller effect of Cm is negligible, the dominant and second poles are given by:

$$\omega_d \approx \frac{A_0}{C_{IN} R_f} \quad \text{and} \quad \omega_N \approx \frac{1}{C_L R_L} \quad , \tag{1}$$

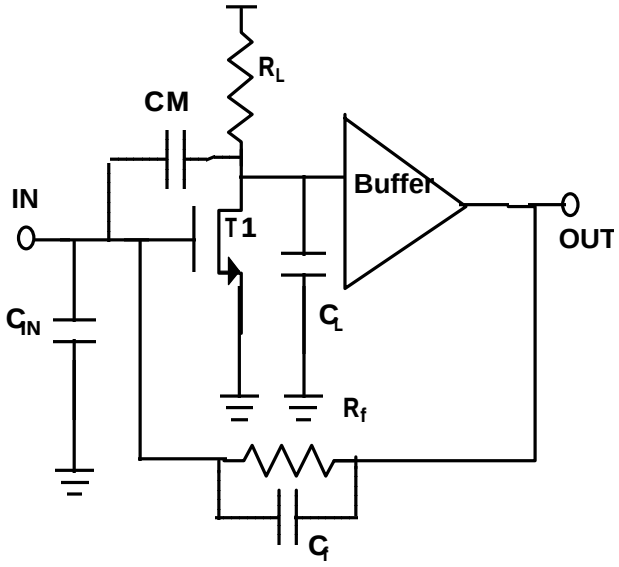


**Fig. 1** Traditional transimpedance amplifier using a feedback resistor. The input device T1, here a MOS transistor, is also in several designs a bipolar transistor. An additional frequency compensation by $C_f$ is commonly used to improve stability, at the expense of a gain-bandwidth reduction.

where $A_0$ is the open loop voltage gain, and $C_{IN}$ represents the detector capacitance, amplifier capacitance and the interconnected parasitic capacitance.

The stability of the amplifier modelled with a two-pole transfer function imposes a minimum phase margin of 58° and an ideal one of more than 76°, requiring $\omega_d$ to be at least 2.7 times larger than $\omega_N$ . In practice, such an amplifier design requires an additional feedback compensation capacitor to add a right-half-plane zero, in order to keep the stability unaffected by the variations of $R_f$ , $R_L$ and $C_{IN}$. The drawback of this compensation is a reduction of the amplifier gain-bandwidth product.

This problem is addressed by using an active feedback network based on two MOS devices, $MP_f$ and $MP_0$, as shown in Fig. 2. The transistor $MP_f$ is placed in the feedback path of the transconductance amplifier, A, where the conventional feedback resistor and transistor $MP_0$ loads the output node OUT*V*. Transistor $MP_f$ is in saturation and is biased close to weak inversion by the current source $MI_f$. Therefore, $MP_f$ acts as a cascode stage across the feedback path so that it replaces the feedback resistor $R_f$ and the load resistor $R_L$, and does not require the buffer depicted in Fig.1. It also maintains adequate biasing conditions for the amplifier A. An additional advantage is that it provides a supplementary current output, OUT*I*.

The transconductance $gms_f$ determines the effective feedback resistor $R_f$ , the effective load resistor $R_L$ and the mid-band gain $A_0$, which can be expressed for weak inversion operation as:

$$R_f = \frac{1}{gms_f}, \quad R_L = \frac{1}{gms_f}, \quad A_0 = \frac{gm_1}{gms_f} \quad \text{with} \quad gms_f = \frac{q}{kT} I_f \quad , \tag{2}$$

where $k$ is the Boltzman constant and $T$ the absolute temperature.

Thus, the dominant and the non-dominant poles become:

$$\omega_d \approx \kappa \frac{A_0 gms_f}{C_{IN}} \quad \text{and} \quad \omega_N = \frac{1}{\kappa}\frac{gms_f}{C_L} \quad , \tag{3}$$

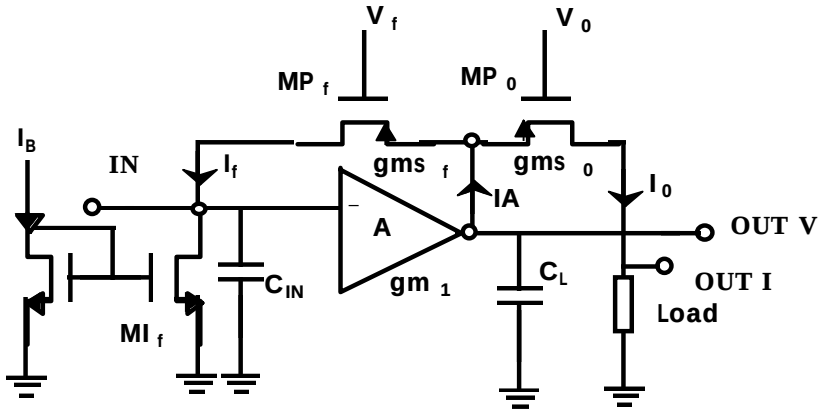


**Fig. 2** Circuit principle of the active feedback loop. MP$_f$ acts as a feedback resistor adjustable via $I_B$. MP$_0$ provides the phase margin adjustment. The amplifier has two outputs: OUT$V$ , with a high transresistance gain and small dynamic range; and OUT$I$ , with a large dynamic range and current gain $gms_0$ / $gms_f$.

where $\kappa = (gms_f)/(gms_f + gms_0)$. One can note that both poles can be controlled by κ. If one assumes that the transistor pair formed by MP$_f$ and MP$_0$ works in weak inversion, the drain currents and κ can be expressed as [8]:

$$\begin{aligned} I_f &= I_{sat}\, e^{-(V_f q/nkT)}[e^{(V_s q/nkT)} - e^{(V_d q/nkT)}], \\ I_0 &= I_{sat}\, e^{-(V_0 q/nkT)}[e^{(V_s q/nkT)} - e^{(V_d q/nkT)}], \end{aligned} \tag{4}$$

with

$$\kappa = \frac{1}{1 + e^{-[(V_0 - V_f)q/nkT]}} \quad ,$$

where $I_{sat}$ is the saturation drain current, $V_s$ the voltage of the output node and $V_d$ the drain voltage of MP$_f$ and MP$_0$.

Therefore, the phase margin controlled by κ can be adjusted by the differential voltage $V_0 - V_f$.

Assuming that the zeros introduced by Miller capacitances and the internal pole of the stage A are negligible, the gain of the transconductance amplifier can be modelled as a second-order system which can be expressed by a two-pole transfer function:

$$G(s) = \frac{V_{out}(s)}{I_{in}} \approx -\frac{1}{gms_f}\,\frac{1}{s^2\frac{C_{IN}C_L}{gm_1 gm_f} + s\frac{1}{\kappa}\frac{C_{IN}}{gm_1} + 1} \quad . \tag{5}$$

For a phase margin between 58° and 76°, the roots of the denominator occur as complex-conjugate pairs. In this condition, the inverse Laplace transform of Eq. (5) for a step response has the following expression:

$$G(t) = -\frac{1}{gms_f}\left[1 - \frac{e^{-(\omega_c t/2\xi)}}{\sqrt{1-(1/4\xi^2)}}\sin\left(\omega_c t\sqrt{1-\frac{1}{4\xi^2}} + \arcsin\sqrt{1-\frac{1}{4\xi^2}}\right)\right] \quad , \tag{6}$$

where $\xi = \kappa \sqrt{(gm_1 C_L / gms_f C_{IN})}$ and $\omega_c = \sqrt{(gm_1 gms_f / C_L C_{IN})}$. The response of the amplifier to an input current impulse obtained by differentiation of Eq. (6) is plotted in Fig. 3 for typical parameters of a 0.7 μm CMOS technology and with an equivalent feedback resistance of 300 kΩ. A peaking time of 15 ns is calculated with a phase margin of 70° for $C_{IN}$ = 20 pF and $gm_1$ = 5 mS.

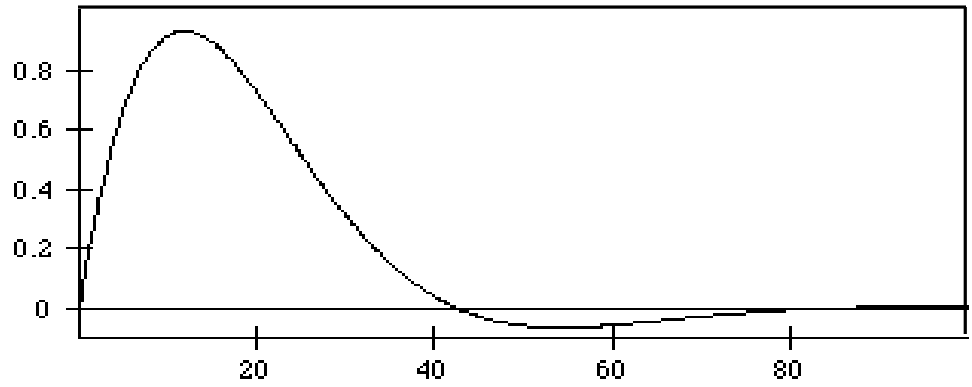


**Fig. 3** Output pulse transient response of the active feedback amplifier shown in Fig. 2. The circuit has been modelled for a 0.7 μm CMOS technology as a simplified second-order system. κ has been adjusted by $V_f - V_0$ to obtain a phase margin of 70°. Time scale is in ns and amplitude is normalized to 1.

## 3 LOW-NOISE TRANSIMPEDANCE PREAMPLIFIER WITH ACTIVE FEEDBACK

The practical implementation of the active current feedback circuit is shown in Fig. 4. It uses the direct cascode configuration built with NMOS or NPN bipolar transistors T1 and T2. In the case of MOS devices, the input transistor T1 is sized to match the sensor capacitance for minimum noise, whereas the aspect ratio of the cascode transistor T2 is chosen to reduce the parasitic capacitance on the output node. In the case of bipolar input, the transistor geometry is sized to keep the base-spreading resistance negligible in comparison with the equivalent noise resistance of the collector shot noise.

Here we study only the MOS version. The active current feedback loop is implemented by the PMOS transistor $MP_f$ and the current source $Mi_f$. With the load transistor $MP_0$, transistor $MP_f$ acts as a cascode stage across the feedback loop and loads the output node with its source resistance $1/gms_f$. $MP_f$ and $MP_0$ sizes are close to the minimum size ($C_L$ minimum), in order to keep $\omega_d$ as high as possible. The adjustable current source $MI_f$ biases $MP_f$ close to weak inversion for a drain current in the 50 nA to 1 μA range. The mid-band input resistance of the active feedback transimpedance amplifier is determined by the ratio $R_f / A_0 = 1/gms_1$, which is not dependent on $R_f$.

The DC operating biasing of the amplifier, shown in Fig. 4, is set by three external voltage sources ($V_{CAS}$ ,$V_f$ and $V_0$) and two external current sources ($I_B$ and $I_D$). Drain voltages of T1 and T2 are entirely set by gate voltages $V_f$ and $V_{CAS}$. The current balance $I_f - I_0$ is set by $V_0$. This biasing scheme enables single-rail, low-supply voltage operation.

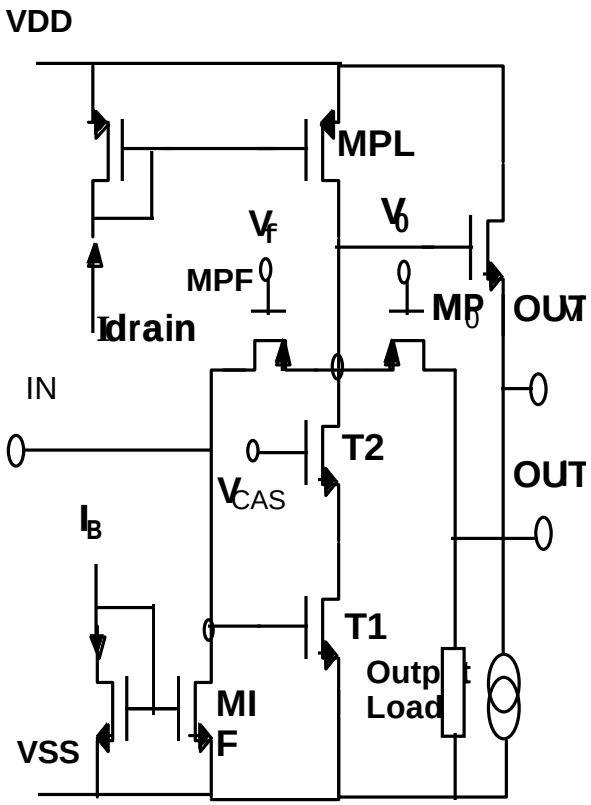


**Fig. 4** Circuit diagram of the active feedback transimpedance amplifier in CMOS technology.

The setting and polarity of the input current source $I_B$ defines three dynamic modes of amplification for the output OUT*V*:

1. **Linear mode:** when the input signal is sufficiently small compared to $I_B$, the amplification is practically linear (if ≥ 300 nA and input charge ≤ 12 fC).
2. **Square root compression:** when the polarity of the input signal is negative and large compared to $I_B$, $gms_f$ varies like the square root of the input current ($MP_f$ in strong inversion). Hence, the amplifier accomplishes a square root compression of the input signal.
3. **Non-linear mode:** when the polarity of the input signal is positive and $I_B$ is sufficiently small (100 nA), the input signal forces the feedback current $I_f$ to 0, switching $MP_f$ off. Then the feedback is opened and the circuit is configured like an open loop transconductance, which enhances the gain considerably (by about a factor of 10). This effect can be used to obtain a non-linear signal processing in such a way that signal and noise level below the switching threshold are dynamically compressed. The technique can be applied to decrease the noise hit rate of readout electronics for a binary or sparse-data-scan-readout system.

The current-output OUT*I* delivers a linear-output signal with a current gain, $I_{out}/I_{IN} = gms_0/gms_f$. This output can be used in current mode with a low impedance load or in integrating mode with a capacitive output node, with the current output OUT*I* working like a charge amplifier output.

SPICE simulation of the circuit produces the transient impulse response shown in Fig. 5. The simulation indicates a more symmetric pulse shape than the calculated result of Fig. 3. Secondary poles and zeros of the direct cascode amplifier not included in the second-order calculation explain this difference.

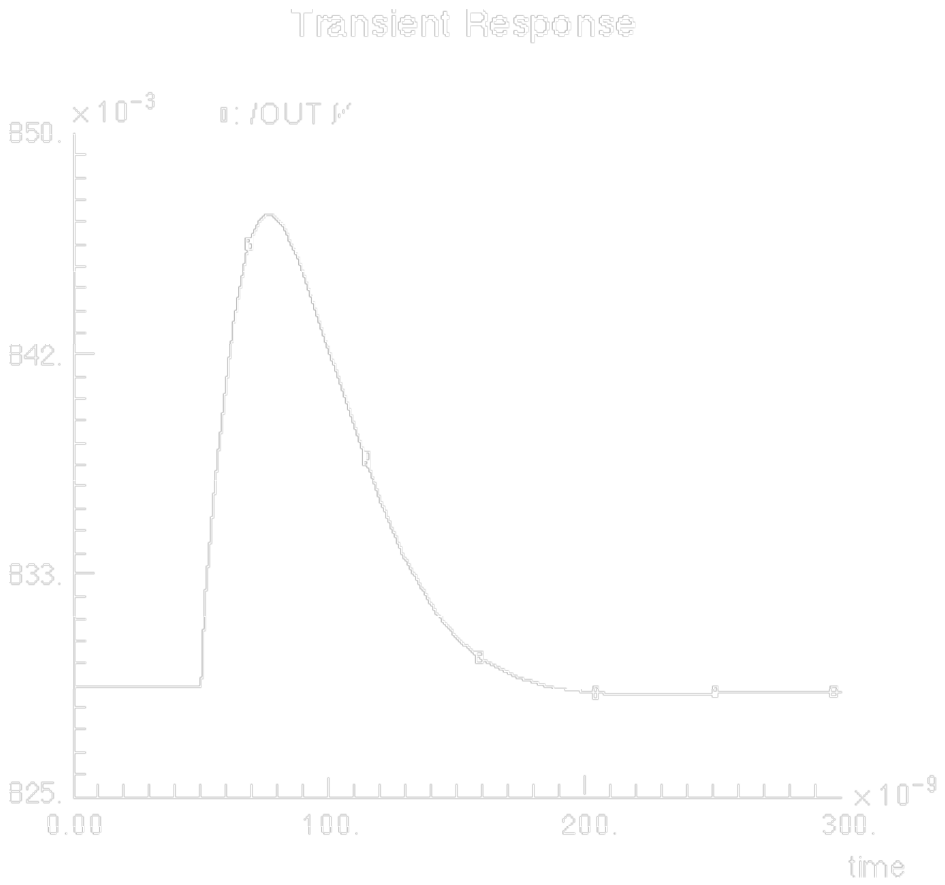


**Fig. 5** SPICE simulation result: transient output pulse response for $I_f$ = 250 nA. The drain current of the cascode amplifier is 400 μA and $C_{IN}$ = 10 pF.

The noise contributions of transistors $MP_f$ and $MP_0$ operating in weak inversion can be expressed from Eq. (2) as the power density of the noise current at the input:

$$\bar{I}n_f^2 = \bar{I}n_I^2 = 4kT\,\frac{1}{2}\,gms_f = \frac{1}{2}\,\frac{4kT}{R_f} \quad . \tag{7}$$

Hence, the total parallel input noise current is

$$\bar{I}n_f^2 + \bar{I}n_I^2 = \frac{4kT}{R_f} \quad , \tag{8}$$

which is equal to the noise of a traditional transimpedance amplifier. If the design could be optimized to operate $MP_f$ and $MP_0$ in strong inversion with $gms_I << gms_f$, the parallel noise would be slightly improved. In this case the total parallel noise current would be:

$$\bar{I}n_f^2 = 4kT\frac{2}{3}gm_f = \frac{2}{3}\frac{4kT}{R_f} \quad . \tag{9}$$

Thus, the parallel noise decreases by 30% when compared to a conventional feedback resistor. Noise analysis is here done assuming that the bulk transconductance associated with the bulk noise resistance of $MP_f$ and $MP_0$ does not contribute to the noise. This assumption is justified because $MP_f$ and $MP_0$ have noise resistance larger than 100 kΩ, which is much higher than the bulk noise contribution of a small geometry transistor.

The series-noise contribution of the active feedback amplifier is essentially identical to the conventional transimpedance or charge amplifier and is mostly determined by the noise characteristics of the input transistor T1. It can be noted that because of its high gain (10 mV/fC), this configuration exhibits a greater robustness against second-stage noise contribution than a fast charge amplifier.

## 4 EXPERIMENTAL RESULTS

The active feedback transimpedance amplifier circuit of Fig. 4 has been designed and fabricated using industrial 0.7 μm CMOS technology[1)]. The T1 input NMOS device has a size of W/L = 2000 μm /1.2 μm and is biased at 400 μA. The $MP_f$ and $MP_0$ transistors have a size of W/L = 2 μm /4 μm. The preliminary measured output pulse shape response for charge input of 1 MIP(4 fC) is shown in Fig. 6. The measurement has been performed with a test board presenting a minimum input capacitance of 10 pF. In these conditions the active feedback circuit shows an excellent stability. The adjustment of the phase margin with the differential voltage $V_f - V_0$ has been verified and works as predicted. The results from experimental output pulse responses shown in Fig. 6 fully agree with SPICE simulations.

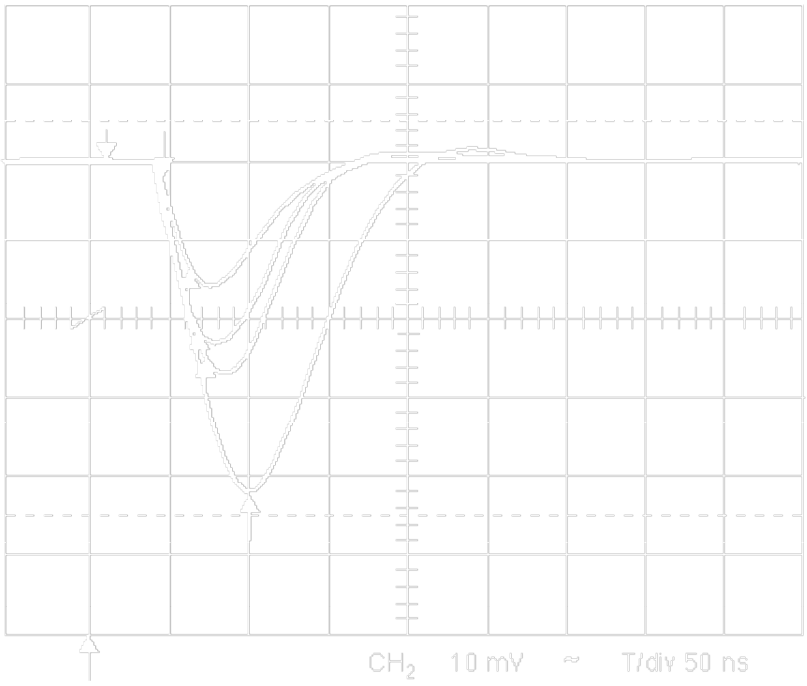


**Fig. 6** Measured output transient pulse response for $I_f$ = 120 nA, 186 nA, 235 nA, 580 nA. The drain current of the cascode amplifier is 400 mA and $C_{IN}$ = 10 pF. Rise time varies from 18 ns to 30 ns.

The transresistance of the active feedback circuit has been measured as shown in Fig. 7. The variation of the transresistance by a factor of 3 from 190–580 kΩ is obtained for an $I_B$ variation of a factor 4.7, from 580–120 nA. This result is slightly different from the calculation of Eq. (2) which predicts a linear dependence. The reason is that the transistor $MP_f$, for $I_B$ above 200 nA, begins to operate in moderate inversion.

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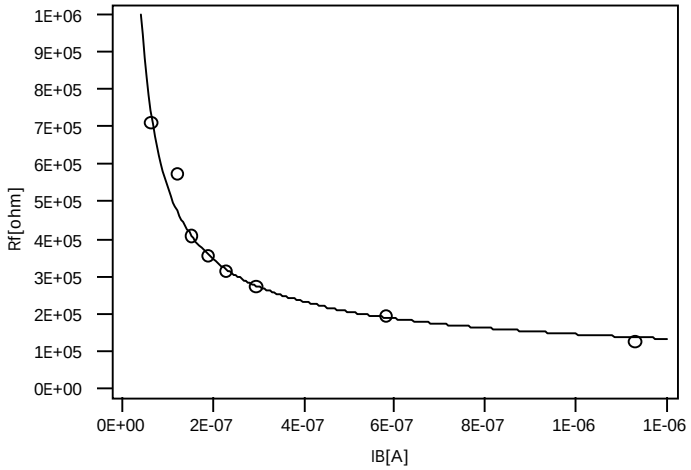


**Fig. 7** Measured transresistance as function $I_f$. Result of the fit indicates that for $I_f$ above 200 nA, $R_f$ is not linear with $I_f$ but is a power function, because $MP_f$ is working in medium inversion.

The ENC, shown in Fig. 8, has been measured as a function of the input capacitance for three different feedback currents and at bias current of the input branch of 400 μA, providing an amplifier transconductance of 7 mS. For $C_{IN}$ = 0, a parallel noise, ENCp = 250 electrons rms, is measured for the higher feedback resistance of 580 kΩ ($I_f$ = 120 nA). The measured noise slope is 30 electrons rms/pF, obtained for a rise time of 45 ns. When the same amplifier parameters are used to make the noise calculation for a charge amplifier followed by a CR–$RC^2$ filter, we obtain a noise slope of 32 electrons rms/pF and a value of ENCp = 200 electrons rms at $C_{IN}$ = 0. The series-noise difference can be explained by the rise-time variation with the input capacitance, which decreases the measured noise slope. The difference between the calculated and measured parallel noise can be explained by the uncertainty as to the absolute value of the total input capacitance, which in our test set-up is 10 pF ± 1.5 pF. Taking into account these effects, experimental results and calculation agree very well.

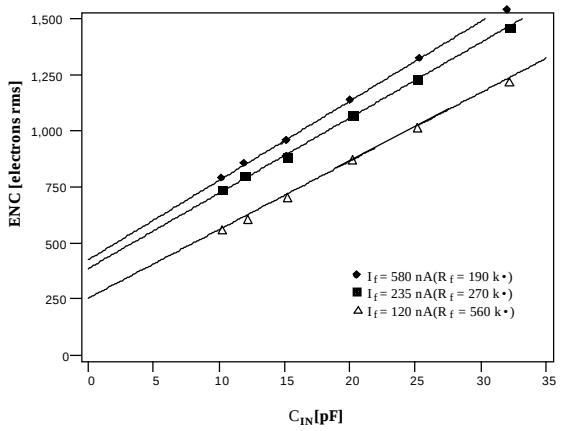


**Fig. 8** Experimental noise measurement of the CMOS active feedback amplifer expressed as ENC as function of $C_{IN}$. The measurement is done for three values of $I_f$. For $I_f$ = 120 nA (560 kΩ), the noise slope is 30 el. rms/pF and ENC = 250 el. rms at $C_{IN}$. = 0 pF.

## 5 CONCLUSIONS

A new active feedback technique for transimpedance amplifiers is presented. A CMOS amplifier circuit based on this novel technique has been designed and tested. This circuit employs n-channel and p-channel devices exclusively. The feedback resistance of the amplifier is adjustable from 150–700 kΩ via a DC current. The phase margin of the amplifier is precisely adjustable via a DC voltage. The measured transimpedance gain is 40 mV for an input charge of 25 000 electrons, with a peaking time of 45 ns for a transresistance of 500 kΩ. In these conditions, a total noise of 800 electron rms is obtained for an input capacitance of 20 pF, making this circuit very promising for low-noise and fast-preamplifier applications. Comparable designs using radiation-hard CMOS and BiCMOS technologies are in development. Preliminary simulations of these versions indicate the same circuit behaviour with a faster rise time.

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