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FAST, LOW POWER, ANALOGUE MULTIPLEXER FOR READOUT OF MULTICHANNEL ELECTRONICS

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ABSTRACT

A dedicated analogue multiplexer chip (AMUX) for the readout of silicon strip detectors was designed and manufactured in 1.2 μm n-well CMOS AMS technology.

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A dedicated analogue multiplexer chip (AMUX) for the readout of silicon strip detectors was designed and manufactured in 1.2µm n-well CMOS AMS technology.

1. INTRODUCTION

Since in a particle physics experiment a very large number of sensors and readout electronics is placed in a small volume, low power consumption at a given speed is a driving issue for the presented design. A huge number of electronic channels placed in a small volume requires the use of low power techniques for building a fast analogue multiplexer. Our goals were to design a 32 channel analogue multiplexer with the following parameters:
– power dissipation less than 50mW for 32 channels,
– readout speed 20MHz,
– dynamic range at the input 0 ÷ 1V, power supply ±2V
–maximum load capacitance 20pF, typical 10pF.

2. THE ARCHITECTURE OF THE AMUX AND READOUT BUFFER

The schematic of the analogue multiplexer is shown on Fig. 1. The multiplexer chip contains 32 input channels with sample-and-hold circuits. In addition to the 32 input channels, one extra channel is used to cancel the offset and the cross-talk from the digital part. The output of this channel is used as a reference for the differential output. Each channel consists of an input switch, a storage capacitor and an input buffer designed as a source follower based on an NMOS transistor biased with 20µA. Because of the n-well technology is used, the gain of this stage is about 0.8. The multiplexing function is implemented as a simple array of 32 NMOS switches controlled by a shift register connected by analogue bus line to the output buffer. The parasitic capacitance of this line is about 4pF for 32 channels (including drain-bulk capacitance of the switches) and therefore it is necessary to adapt the current in the readout channel. We can obtain this in a simple way by adding a pull-up NMOS transistor (working as a resistor) connected to the VSS. The value of this resistor together with the switch resistance limits the output current and speed and also has influence on the linearity of the multiplexer. Assuming that transistors M_3 and M_P work in their linear region and M_1 works in saturation we can simply calculate the resistance of the switches and the readout current using the following formulae:

$$R_{on} = \partial v_{ds} / \partial i_{ds} \cong \frac{1}{k \cdot \left(\frac{w}{l}\right) \cdot \left(v_{gs} - v_t\right)} \tag{1}$$

$$i_d \cong \frac{k}{2} \cdot \frac{w}{l} \cdot (v_{gs} - v_t)^2 \tag{2}$$

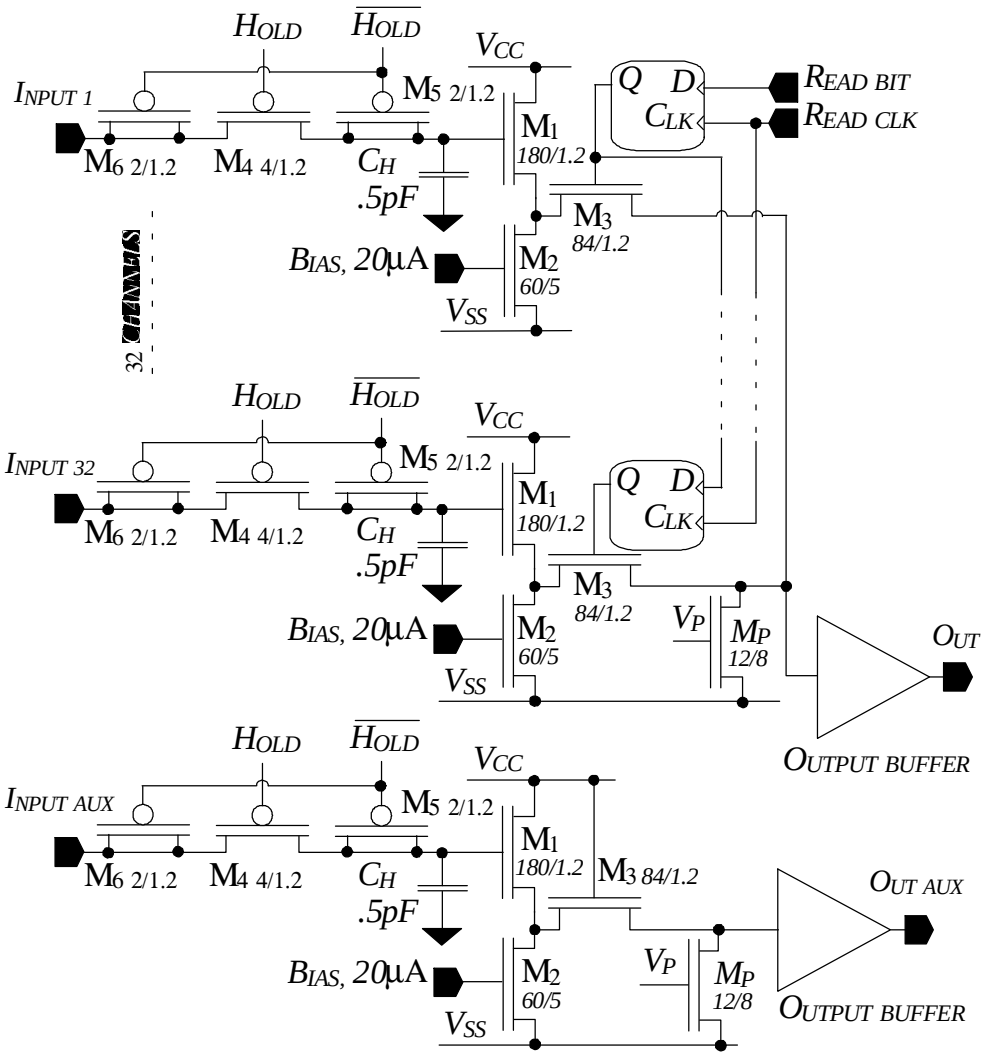

Fig. 1. Schematic diagram of the multiplexer.

Because the resistance of M_P is about 4.1kΩ and the switch resistance is about 100Ω the small nonlinearity which comes from the M_3 switch (its resistance is a function of Uout) can be neglected. The current flowing in the readout channel is in the range of 300 ÷ 600μA for the input voltage swing 0 ÷ 1V. It provides a slew rate not less than 75V/μs for line parasitic capacitance of 4 pF. To obtain the assumed speed of the MUX of 20 MHz for a maximum load capacitance 20 pF an additional output buffer is required.

The schematic diagram of the output buffer is shown in Fig. 2. The configuration used in the circuit is based on the well known push-pull circuit. The push-pull CMOS inverting amplifier built with M_1 and M_2 transistors is controlled by two error amplifiers. The error amplifiers biased with 300μA set the DC operating point and apply negative feedback to the gate of the common-source M_1 and M_2 transistors. For the transistor sizes given in Fig. 2 and

nominal power supply ±2 V, the current flowing through the transistors M_1 and M_2 is about 5 mA. This provides an A class buffer which gives high linearity and low output resistance.

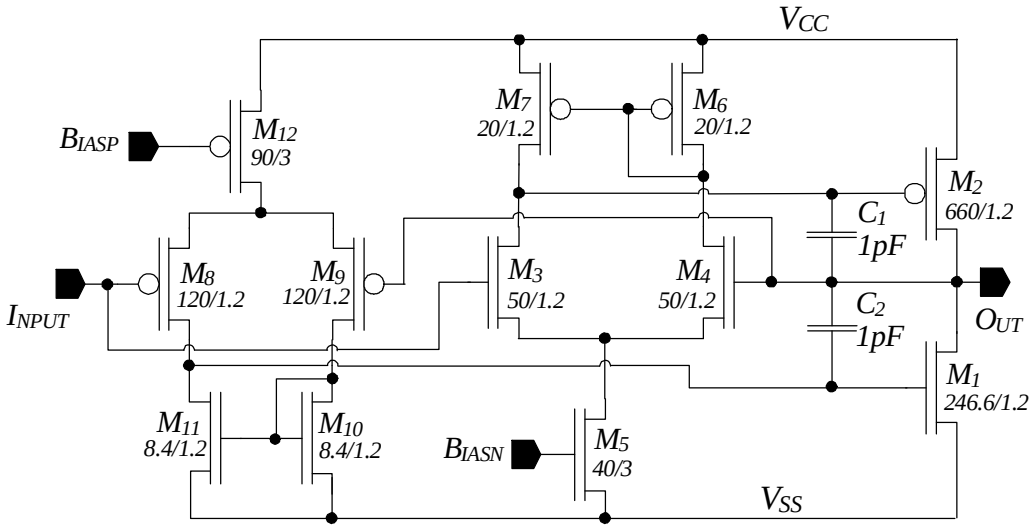

Fig. 2. Schematic diagram of the output buffer.

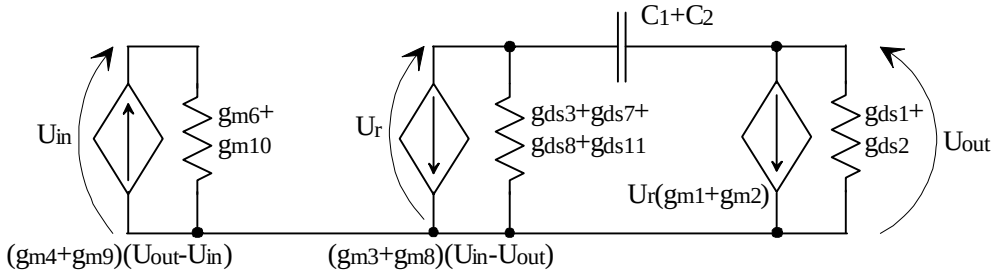

Fig. 3. Simplified equivalent model of Fig. 2.

The simplified equivalent model of the output buffer is shown in Fig. 3. Assuming that the transconductances gmi of the transistors used in the error amplifiers are the same and the transconductances gmo of the output devices are the same, we can find the expressions for the gain and the output resistance. Using nodal analysis we can write:

$$Uout = \frac{g_{mi}}{g_{dsi}} \cdot \frac{g_{mo}}{2 \cdot g_{dso}} (Uin - Uout) \tag{3}$$

Solving for Uout/Uinp yields the gain of the buffer:

$$A = \frac{A_1 \cdot A_2}{1 + A_1 \cdot A_2} \cong 1 \tag{4}$$

where $A_1 = g_{mi} / 2 \cdot g_{dsi}$ is the gain of the error amplifier and $A_2 = g_{mo} / g_{dso}$ is the gain of the output push-pull stage in open loop configuration. The small signal output resistance of the buffer can be calculated from equation (5):

$$i_{out} = 2 \cdot Ur \cdot g_{mo} + 2 \cdot Uout \cdot g_{dso} \tag{5}$$

Substituting equation (3) and (4) and solving equation (5) for Uout/Iout gives:

$$Rout = \frac{1}{2 \cdot g_{dso}} \cdot \frac{1}{2 + A_1 \cdot A_2} \tag{6}$$

The output resistance of the buffer is the output resistance of the push-pull stage divided by the open loop gain of the error amplifier and the output stage. For the given values the output resistance is about 1Ω.

The presented output buffer is a typical second-order circuit. The compensation of the buffer is done by adding the C1, C2 Miller capacitors. The 5 mA current flowing through M1, M2 provides not only the low output resistance but also the high bandwidth which is our basic goal. The unity-gain bandwidth can be shown to be approximately

$$GB \cong \frac{2 \cdot g_{mi}}{C_1 + C_2} \tag{7}$$

With regard to compensation, the goal was to achieve a phase margin equal to 60° for the nominal 10pF load capacitance. Assuming that the RHP zero is placed ten times higher than GB the second pole must be placed 2.2 times higher than GB. The following relationship applies:

$$\frac{2 \cdot g_{mo}}{C_1 + C_2} \rangle 10 \cdot \left(\frac{2 \cdot g_{mi}}{C_1 + C_2} \right) \tag{8a}$$

Therefore,

$$g_{mo} \rangle 10 \cdot g_{mi} \tag{8b}$$

and furthermore

$$\frac{2 \cdot g_{mo}}{Cload} \rangle 2.2 \cdot \frac{2 \cdot g_{mi}}{C_1 + C_2} \tag{9}$$

Combining equations (8b) and (9) gives the requirement for the Miller C1, C2 capacitors: $C_1 + C_2 \rangle 0.22 \cdot Cload$. In our case the transconductance gmi and gmo are 935μS and 12mS respectively. This allows a 60° phase margin for C1 = C2 = 1pF for 10pF load capacitance.

3. LAYOUT

The 32 channels of the multiplexer were placed in 42.4μm pitch. These channels are separated by the diffusion guardrings to cancel cross-talk between the neighbours. The presented design is a typical mixed analogue and digital circuit. A digital circuit is placed close to the analog circuit. To avoid cross-talk between the analogue and digital parts the power supply is separated. To decrease the coupling from the digital part through the substrate, the clock lines are placed symmetrically (clock and clock bar) over the POLY 1 layer connected externally to the ground.

4. RESULTS

The -3dB bandwidth of the buffer is equal to 115 MHz and the settling time for a 1V step at the input is 25ns as shown in Fig. 4 and Fig. 5 respectively. A voltage gain of 0.75 is measured. and the power dissipated by the multiplexer is about 23mW. The output response of the multiplexer is presented in Fig. 5. The upper trace shows the output waveform measured for a readout clock of 20 MHz. The settling time for 1V step at the input is about 30ns which shows that we have a good safety margin with respect to 20MHz operation. The channel offset spread together with cross-talk from neighbour channel is less than 5mV as shown in Fig. 6.

5. CONCLUSION

An analogue multiplexer for the serial readout of multichannel front end system for particle detector has been presented. The design has been optimised to set a settling time less than 30ns with the nominal power consumption. For the nominal capacitive loads 20MHz readout speed and 23mW power dissipation are obtained. The AMUX chip has already been used in the test of silicon particle sensors and in the future will be implemented in a more sophisticated read-out chip consisting of charge preamplifier, shaper and analogue memory cell.

6. REFERENCES

- Philip E. Allen, Douglas R. Holberg, “CMOS Analog Circuit Design” (Holt, Rinehart and Winston, Inc., 1987)

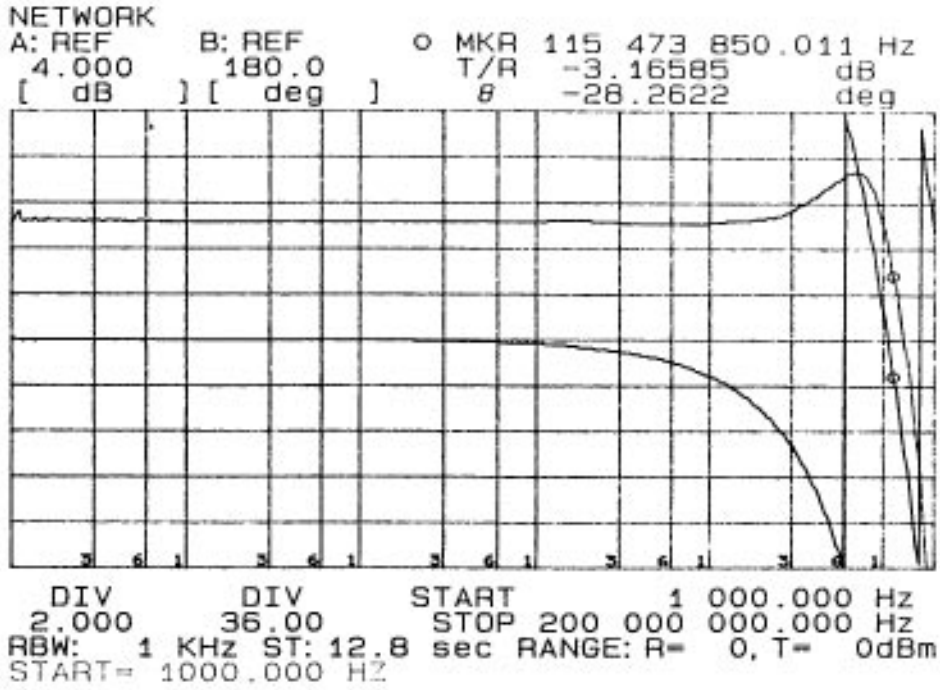

Fig. 4. Gain bandwidth of the output buffer.

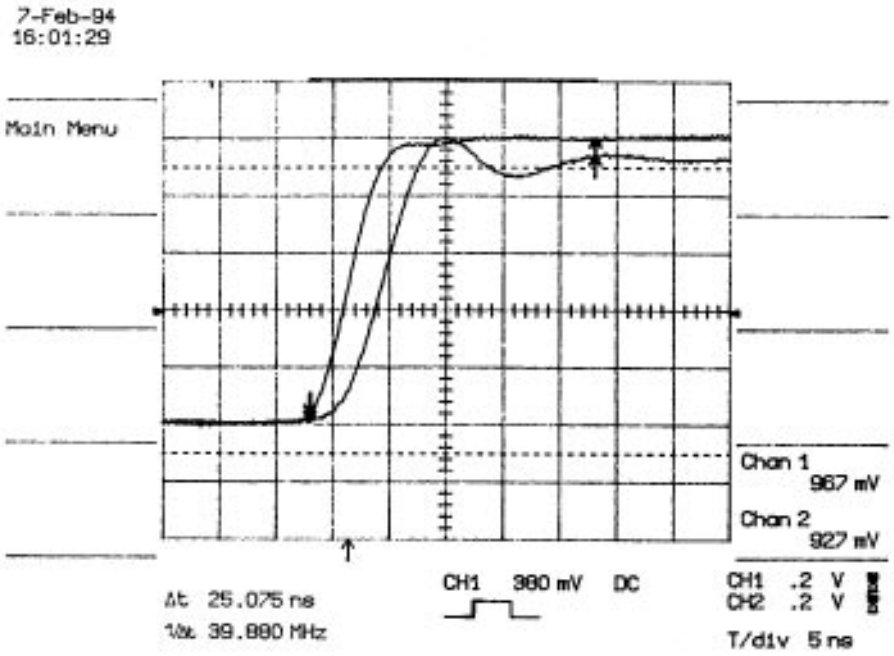

Fig. 4. Settling time for 1 V step on the input.

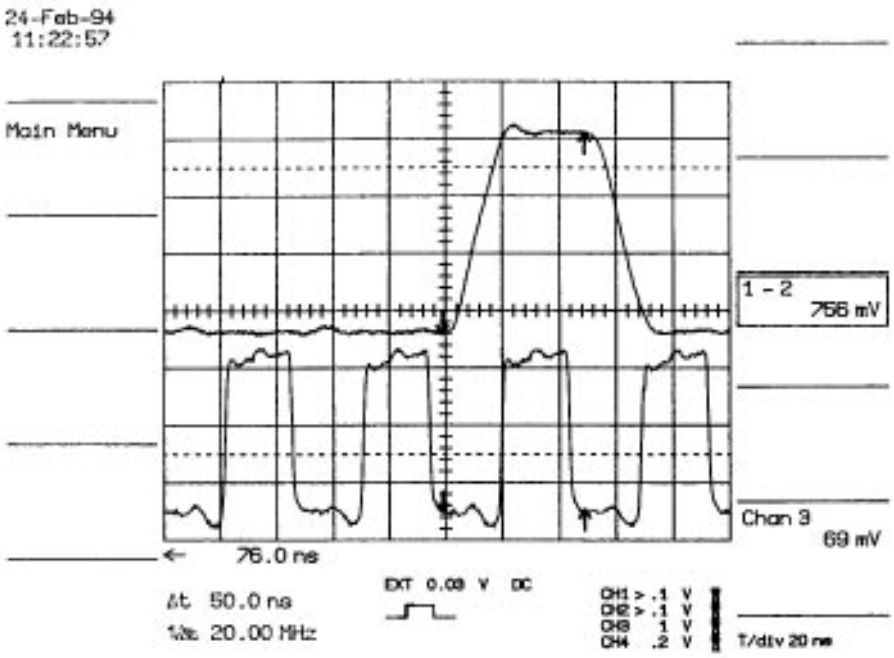

Fig. 5. Performance of the multiplexer with 1 V step at the input of one channel and 20 MHz read-out clock.

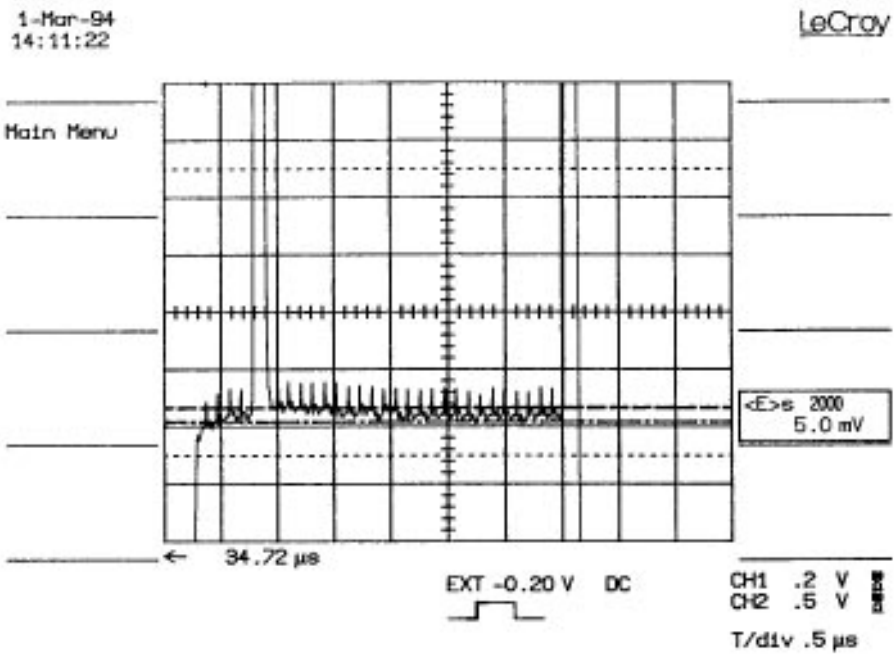

Fig. 6. Offset variation between AMUX channels - 1V input in channel nr 5.