CERN SCHOOL OF COMPUTING

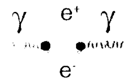
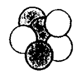
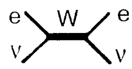
Sopron, Hungary 9 September 1994

Overview of Data Acquisition for LHC

S. Cittolin/CERN-ECP

- Introduction
- LHC experiments
- Data acquisition structures
- Frontend
- Level-1 trigger
- Fast controls
- Readout
- Event Builder
- High trigger levels
- Conclusion

Short History & New Frontiers

	$\lambda = \hbar / p$		$T \approx t^{-1/2}$	
	10^{-10} m	< KeV	>300.000 Y	**1900.... Quantum Mechanics Atomic Physics**
			≈ 300 sec	**1940-50 Quantum Electro Dynamics**
	10^{-15} m	≈ GeV		**1950-65 Nuclei, Hadrons Symmetries Field theories**
	10^{-16} m	> GeV	≈ 10^{6} sec	**1965-75 Quarks Gauge theories**
	10^{-18} m	100 GeV	≈ 10^{-10} sec	**SPS, $p\bar{p}$ 1970-83 ElectroWeak Unification, QCD**

Charge	6*3 Quarks	6 Leptons	Charge
2/3	u	ν_e	0
-1/3	d	e	-1
3 "Colours" each quark	c s	ν_μ μ	2 "Flavours" in each doublet
R G B	t b	ν_τ τ	

LEP 1990
3 families

Tevatron 1994
Top quark

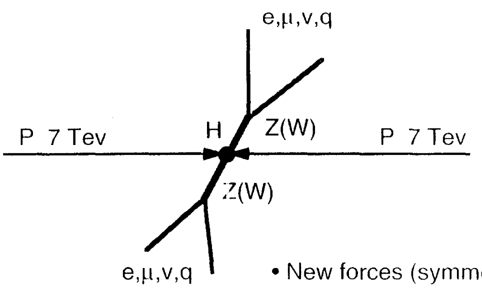
Higgs ? Supersymmetry ? — 10^{-19} m — ≈ TeV — ≈ 10^{-12} sec — **LHC Origin of masses The next step...**

GRAND Unified Theories ? — 10^{-31} m — ≈ 10^{13} TeV — ≈ 10^{-38} sec — **Underground Labs Proton Decay ?**

Quantum Gravity? Superstrings ? — 10^{-34} m — ≈ 10^{16} TeV — ≈ 10^{-42} sec — **?? The Origin of the Universe**

The next step

- **HIGGS**
  Electroweak symmetry breaking
  Origin of masses



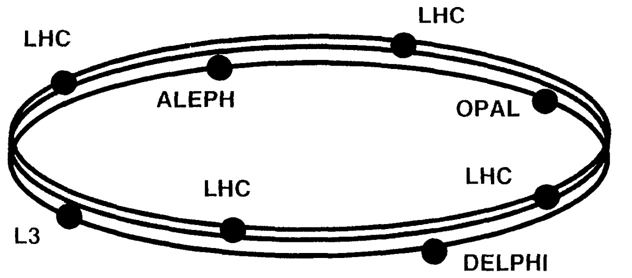
- New forces (symmetries)
- New particles
- Super symmetries
- Next step in compositness

....

> The next step needs to search for a wide range of massive objects. The hadron colliders can provide the exploratory physics with high constituent √s and with high luminosity, but at the expense of clean experimental conditions

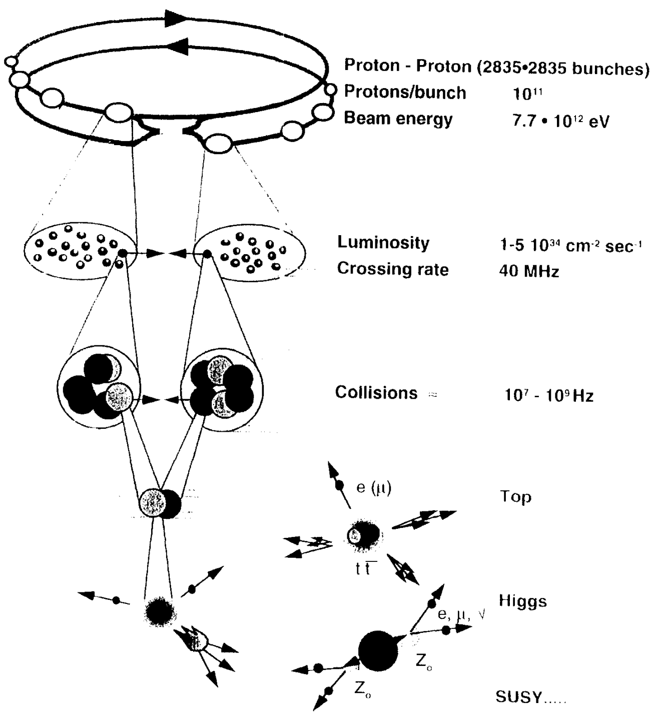
LHC project

Two superconducting magnet rings in the LEP tunnel.



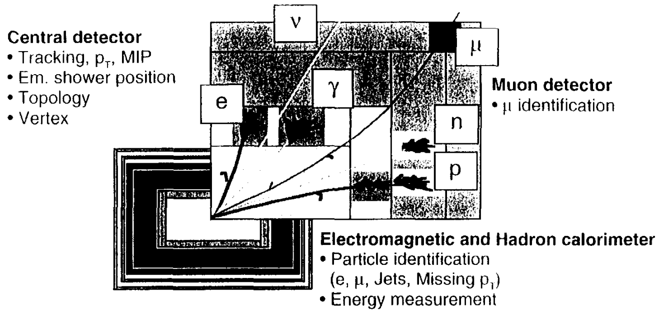
			√s		Luminosity
LEP	e^+	e^-	**200**	**GeV**	**$3 \cdot 10^{31}$ cm^{-2}s^{-1}**
LHC	p	p	**15.4**	**TeV**	**10^{34}**
	e	p	**1.7**	**TeV**	**10^{32}**
	P_b	P_b	**1312**	**TeV**	**10^{27}**

LHC collisions

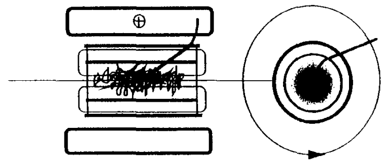


Selection rate 1/10000000000000

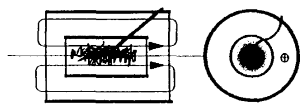
LHC detectors and experiments



ATLAS **A Toroidal LHC ApparatuS**

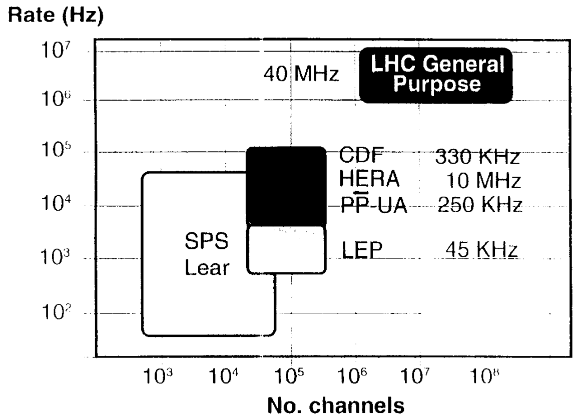


CMS **Compact Muon Solenoid**

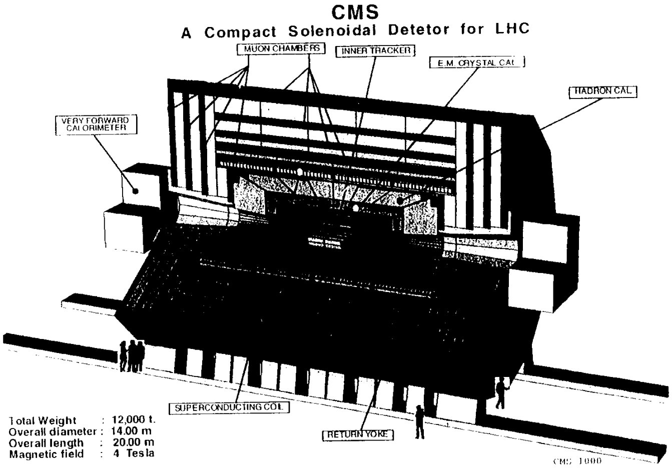


LHC parameters

	LEP	SppS	HERA	LHC
BX period	22 µs	3.8 µs	96 ns	**25 ns**
Interactions/BX	<< 1	~1	<< 1	**~ 20**
% Intn to select	100 %	0.1 %	100 %	**0.001%**
# calo towers	~ 10^4	~ 10^3	~ 10^4	**~ 10^5**
# tracking chan.	~10^4	~10^4	~10^4	**~10^7**

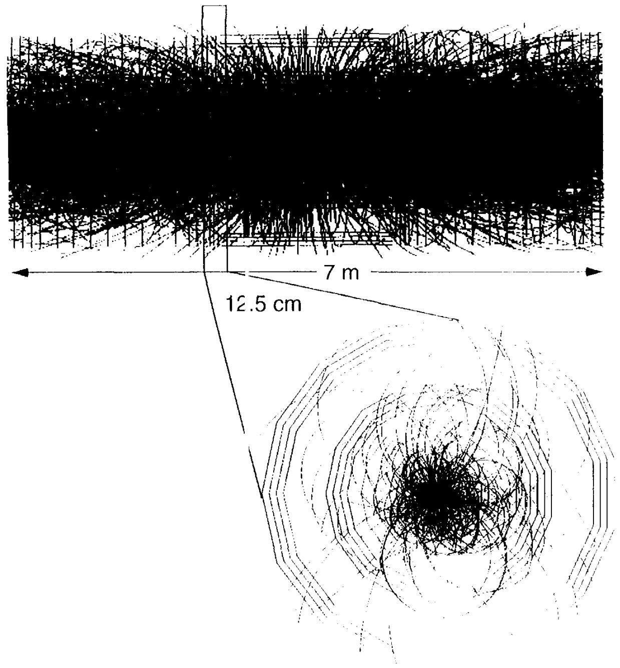


Compact Muon Solenoid. CMS

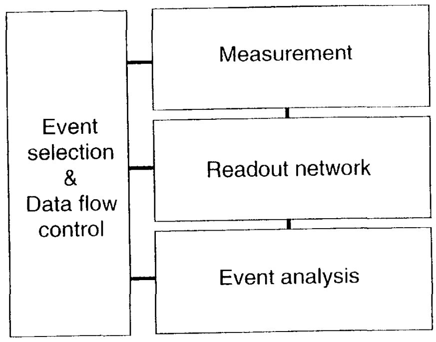


CMS central tracking

Central tracking at L = 1.8 10^{34} (50 ns integration, ≈ 2000 tracks)



Data acquisition structure



- Trigger levels
- Trigger steps in present colliders
- Multilevel data acquisition
- Second level trigger
- CMS data acquisition

Event rates at LHC

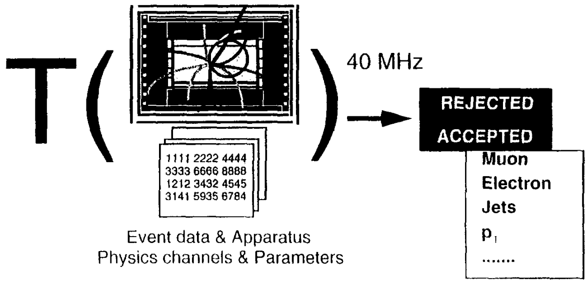
Rates from background of physics triggers.

Top		
l + jets	p_t^{μ} > 40 GeV	**200 Hz**
	p_t^{e} > 40 GeV	**$5 \cdot 10^4$ Hz**
e + μ	p_t^{μ} > 50 GeV	**100 Hz**
	p_t^{e} > 50 GeV	**400 Hz**
Higgs		
4 l	$p_t^{2\mu}$ > 20 GeV	**25 Hz**
	p_t^{2e} > 20 GeV	**10^3 Hz**
e ν j j	p_t^{e} > 100 GeV	**15 Hz**
SUSY		
p_t^{m}+jets	p_t^{3j} > 200 GeV	**500 Hz**
4 l +jets	$p_t^{2\mu}$ > 30 GeV	**10 Hz**
	p_t^{2e} > 30 GeV	**10^2 Hz**

LVL-1 rate 10^4 - 10^5 Hz

Event selection

The trigger is a function of :



Since the detector data are not all promptly available and the function is highly complex, T(...) is evaluated by successive approximations called :

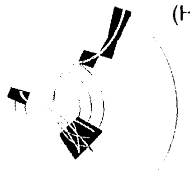
TRIGGER LEVELS
(possibly with zero dead time)

The final aim is to look for ≈ 1/10000000000000

Trigger levels

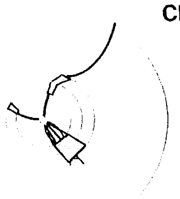
40 MHz

Particle identification
(High p_T electron, muon, jets, missing E_T)



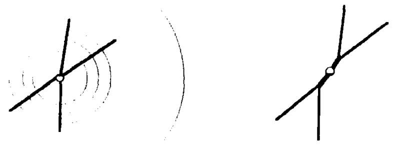
- Local pattern recognition and energy evaluation on prompt macro-granular information

Clean particle signature (Z, W, quarks..)



- Finer granularity precise measurement
- Kinematics. Effective mass cuts and event topology
- Track reconstruction and detector matching

Physics process identification

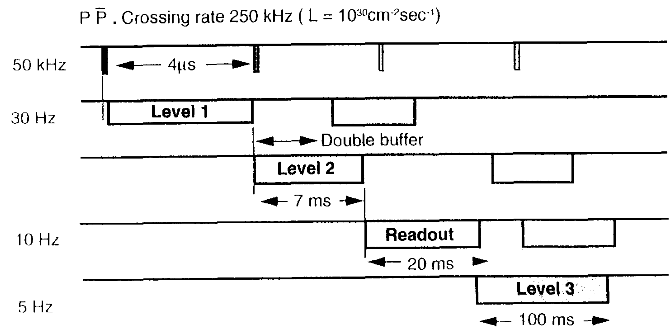


- Event reconstruction and analysis

10..100 Hz

SPS collider

UA1 Timing

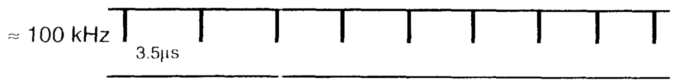


- Level 1 trigger inter bunch crossings
- Detector cell memory less than 4μs
- Almost no event overlapping. Clean events
- Most of electronics outside the detector

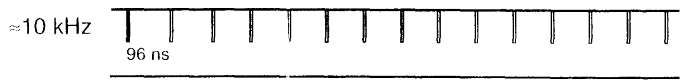
LEP,....

LEP. Crossing rate 30 kHz

Tevatron. Crossing rate 280 kHz

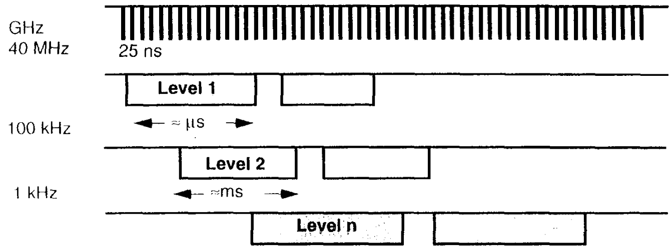


HERA. Crossing rate 10 MHz

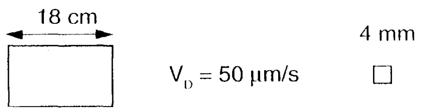


LHC

LHC. Crossing rate 40 MHz ($L = 10^{33} - 4 \cdot 10^{34} cm^{-2}s^{-1}$)



- Level 1 trigger time exceeds bunch interval
- Detector cell memory greater than 15 ns
- Event overlap & Signal pileup
- Very high number of channels



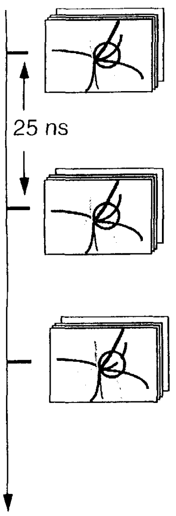
UA1 drift cell
T_{max}=3.8μs

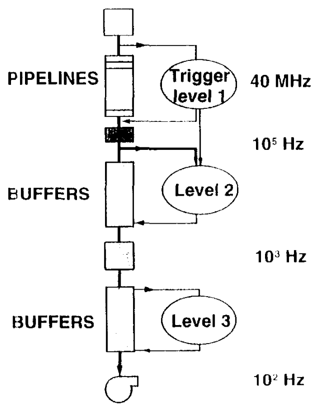
LHC drift cell
T_{max}= 40 ns

Multiple crossing resolution

LHC readout structures

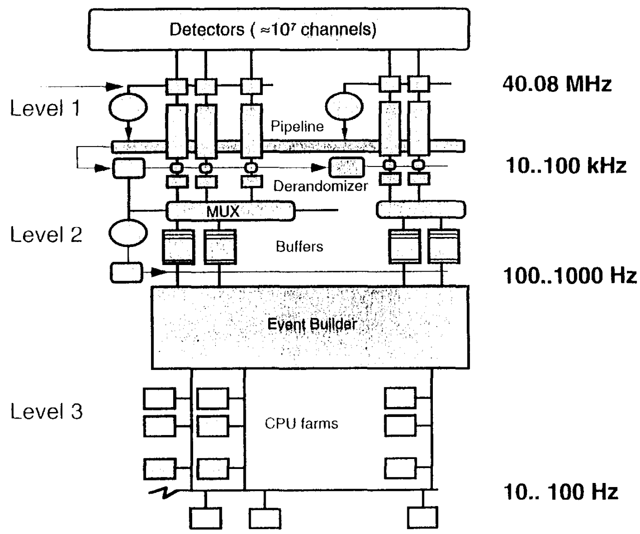
$\approx$ 20 Collisions / 25ns 10^7 channels
(10^9 event/sec) (10^{16} bit/sec)



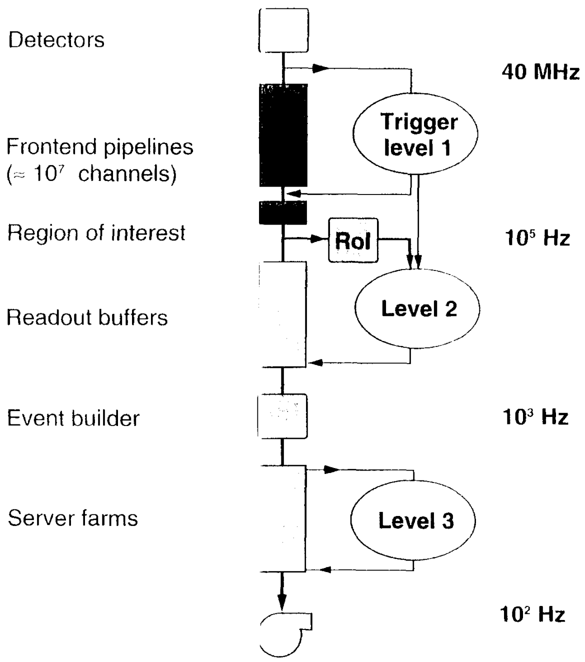


Multi-level readout and analysis system

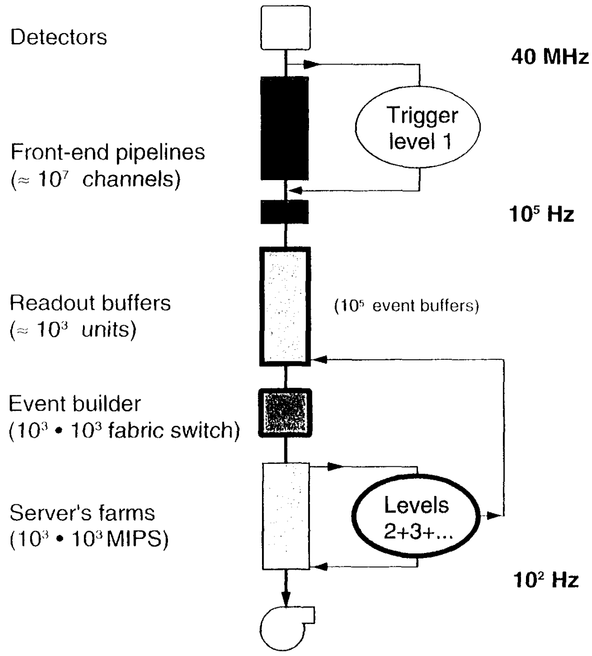
Standard DAQ layout



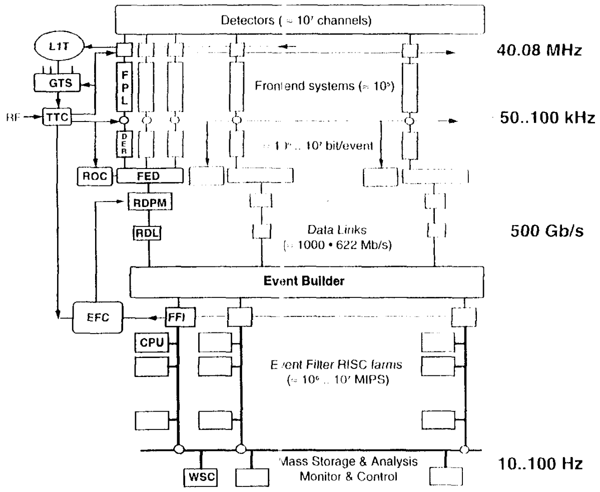
DAQ logical levels



CMS logical levels

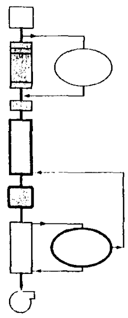


CMS data acquisition



L1T	Level-1 Trigger
GTS	Global Trigger System
TTC	Timing, Trigger and Control
FPL	FrontEnd Pipeline
DER	DeRandomizer
ROC	ReadOut Controller
FED	FrontEnd Driver
RDPM	Readout Dual Port Memory
RDL	Readout Data Link
FFI	Filter Farm Interface
EFC	Event Flow Control
WSC	Work Station Cluster

CMS two physical levels

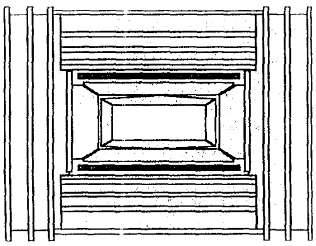


- Reduces the number of building blocks simpler design, easier maintenance and upgrades
- Simplifies the data flow
- Exploits the commercial components 'state of the art' memory, switch, CPU
- Upgrades and scales with the machine performances flexibility in logical redistribution of resources
- Makes full use of the computing power anyway needed for the off-line analysis

Technology ansatz

- The CPU processing power increases by a factor 10 every 5 years (at constant cost)
- The memory density increases by a factor 4 every two years (at constant cost)
- The 90's are the data communication decade

CMS data acquisition parameters



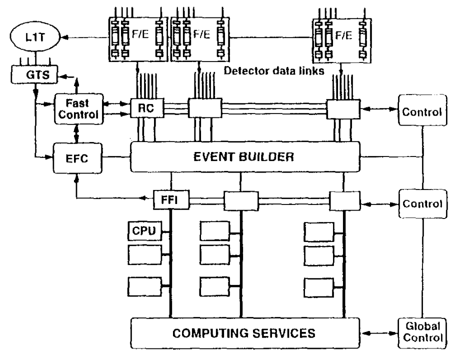
Number of channels and data volumes (at 10^{34} luminosity)

Detector	No. Channels	Occupancy%	Event size (kB)
Pixel	80000000	.005	100
InnerTracker	16000000	3	700
Preshower	512000	10	50
Calorimeters	250000	10	50
Muons	1000000	.1	10
Trigger			10

Average event size	1 MB
Level-1 trigger rate	100 kHz
No. of Readout units (200-5000 Byte/event)	1000
Event builder (1000•1000 switch) bandwidth	500 Gb/s (*)
Event filter computing power	$5 \cdot 10^6$ MIPS
Data production	Tbyte/day
No. readout crates	300
No. electronics boards	10000

(*) In order to achieve the data acquisition figure of 100 kHz event rate after the level 1 trigger, the tracking data must not be moved into the readout network until the associated event has passed the test of the high trigger levels based on the information from the other detectors. This operation (called virtual level-2) is *expected to reduce* the event rate (for the tracker data) by at least one order of magnitude

CMS data acquisition subsystems



- Detector frontend
- First level trigger
- Readout network
- Fast controls
- Event builder
- Event filter

Subsystems and functions:

RC **Readout Crate.**

Event Builder. Multiport switch network

EFC **Event Flow Control.** *Event scheduling and filter task control*

FFI **Filter Farm Interface.** Event data assembly into processor memory. The system includes the farm status communication with the EFC and the control. FFI functions may be part of the future farm computer architecture.

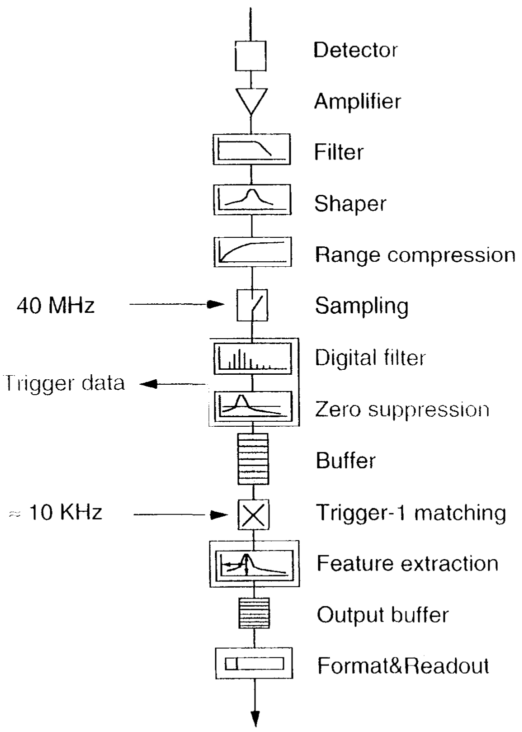
CPU Event filter processing unit. It may be a single workstation board or a unit in a multiprocessor server.

Fast Control. Trigger and EFC signals broadcasting to *readout crates. Status collection from readout modules and* feedback to the trigger processor.

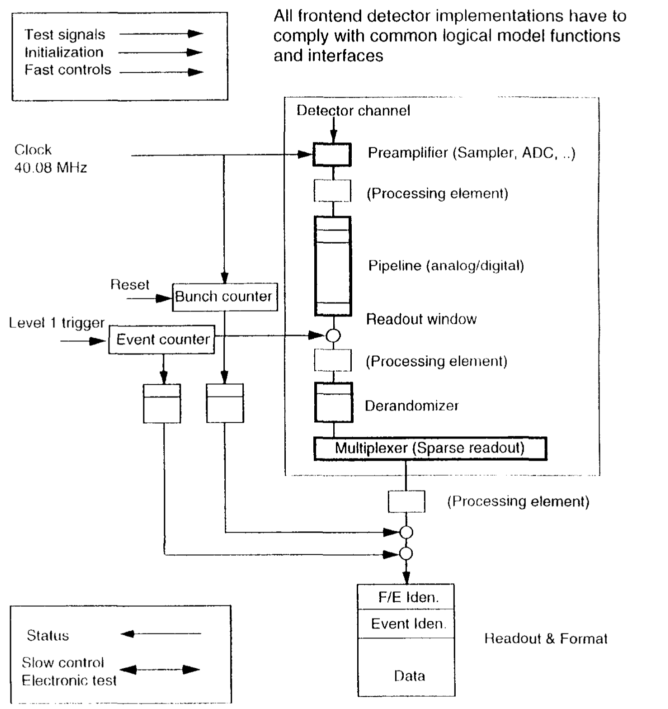
Control. System test,initialization, monitoring etc. Supervision of operations associated to the data flow main steps.

Services. *Control room analysis, display and monitoring* consoles, WAN connections, mass storage and data archives

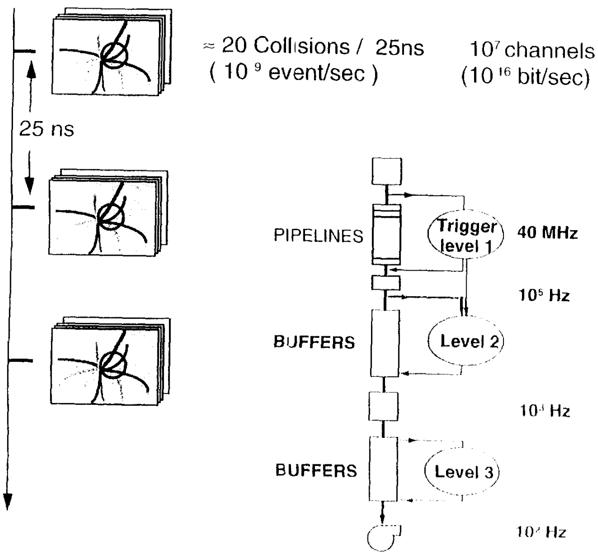
Frontend structure



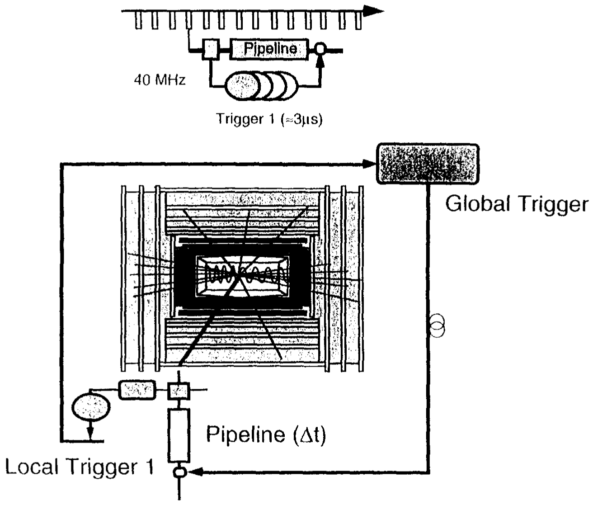
Frontend functional model



Pipeline

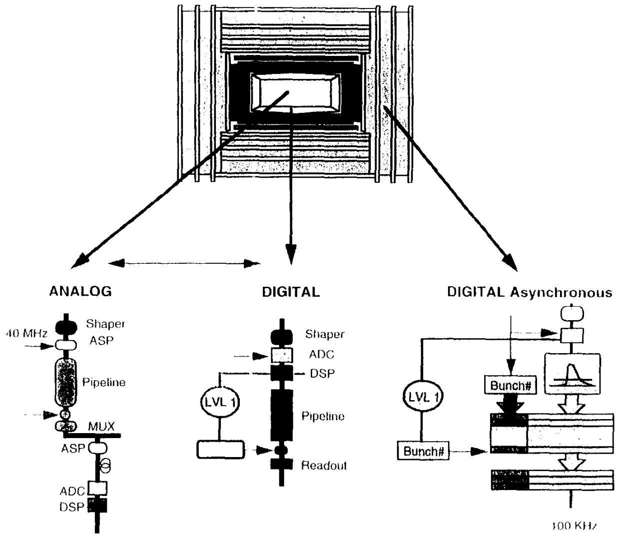


Pipeline delay



Δt = TOF	1 - 50	ns
+ Detector to FE	10 - 100	
+ Preprocessing	100	
+ to Local Trigger	10 - 100	
+ Local Trigger	500	
+ to Global Trigger	300	
+ Global Trigger	500	
+ Distribution	500	
	> 2000	ns

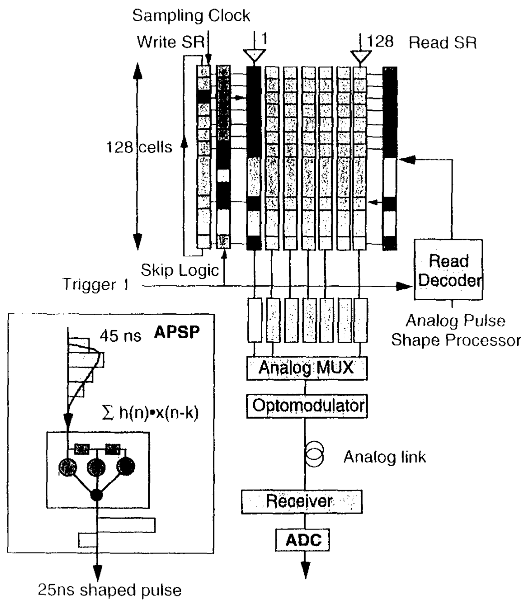
Frontend type



Low dynamic range and resolution(≤10-bits)
Good packaging and power consumption
High number of channel > 10^6

Large dynamic range (15bits)
Digital filtering
Radiation hard
High power consumption

Silicon strip detector. RD-20



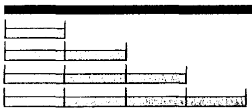
- Slow amplifier
- Analog memory
- Bunch crossing recovery
- Pileup removal

Analog to digital conversion

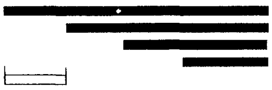
Digitizing means measuring something (charge, amplitude, time..) that is compare it with a reference unit.

Entity to be measured

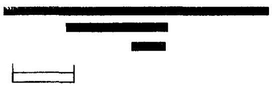
Ruler unit



Compare entity with a series of rulers in sequence (standard ADC, counting)
or in parallel (FADC, decoding)

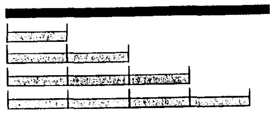


Compare entity with a ruler, subtract ruler from entity
(Sigma Delta ADC)



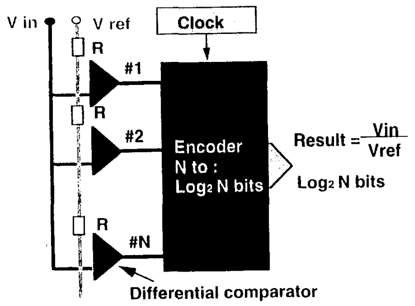
Compare entity with a ruler then subtract ruler from entity and halve the result
(HARP pipeline ADC)

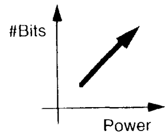
Flash ADC



Compare entity with a series of rulers in sequence (standard ADC, counting)
or in parallel (FADC, decoding)

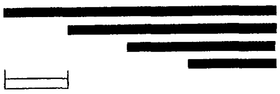
Flash ADC





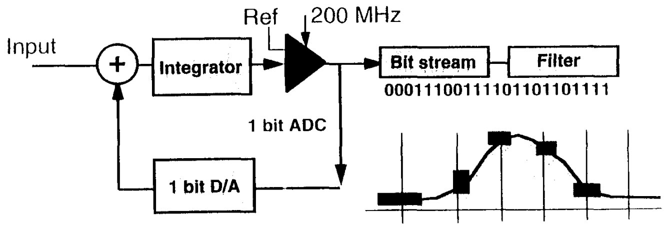
Dynamic range	critical for	Calorimeter (15-16 bits)
Resolution "		Calorimeter (9-10 bits)
Power consumption	"	Inner detectors
Speed	"	All (n• 67MHz n≥1)

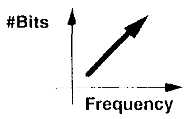
Sigma delta



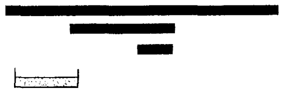
Compare entity with a ruler,
subtract ruler from entity
(Sigma Delta ADC)

Sigma Delta ADC



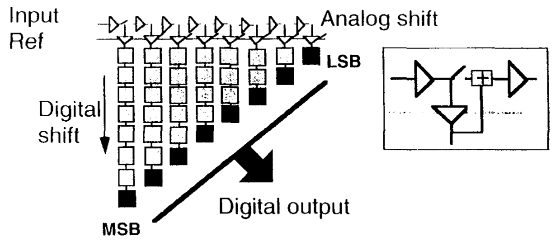


Pipeline conversion

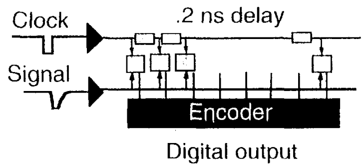


Compare entity with a ruler
then subtract ruler from entity
and halve the result
(HARP pipeline ADC)

ADC pipeline (CERN-LAA HARP) 12 Bits 1MHz

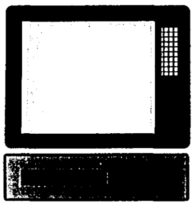


Time Memory Cell (KEK/Hiroshima/NTT)



Industry

In the last 20 years, the requirements of telecommunication and in particular to television have strongly contributed to the development of standard technology (CMOS, BiCMOS) and mass production by industry.
Together with other fields high energy physics experiments have exploited these developments extensively.



Flash ADC
Analog memory
Personal computers
Helical scan recording
Data compression
Image processing
Cheap MFlops
for image synthesis

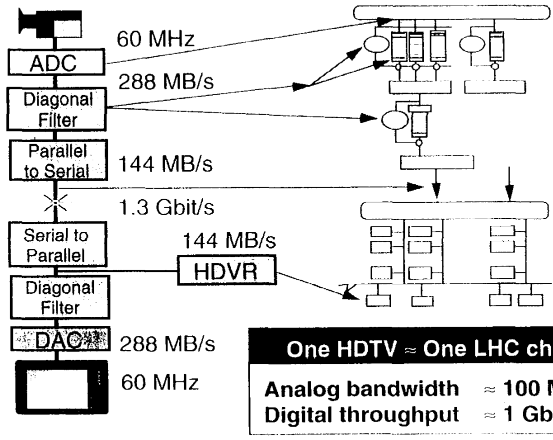
In recent years the world television industry has undertaken a new challenge :

High Definition TeleVision (HDTV).

This represents a tremendous effort of research and development in the field of standard technology.
In Europe it is organized under the project EUREKA 95.

HDTV chain

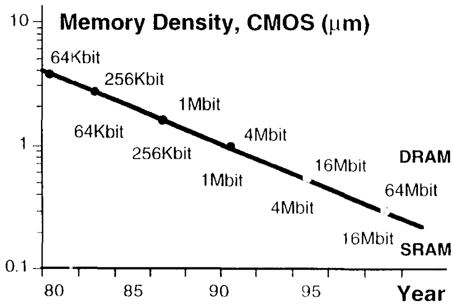
- **Digital**
  - ADC (144, 27 MHz, 10 bits)
- **Data compression**
- **Multi-standards**
- **High quality pictures**
  - Digital signal processor
  - Memory delays
  - Pipeline and data driven architectures
- **Transmission**
  - High speed (2 GB/s) optical links
- **Mass storage**
  - Parallel to serial converter
  - High speed (100 MB/s) recorders

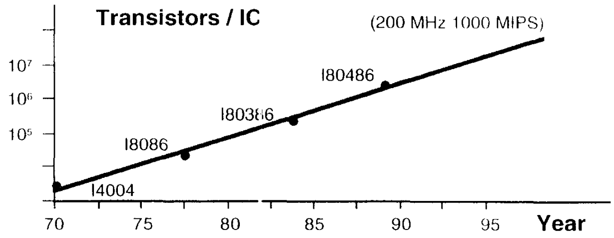


One HDTV ≈ One LHC channel

Analog bandwidth ≈ 100 MHz
Digital throughput ≈ 1 Gbit/sec

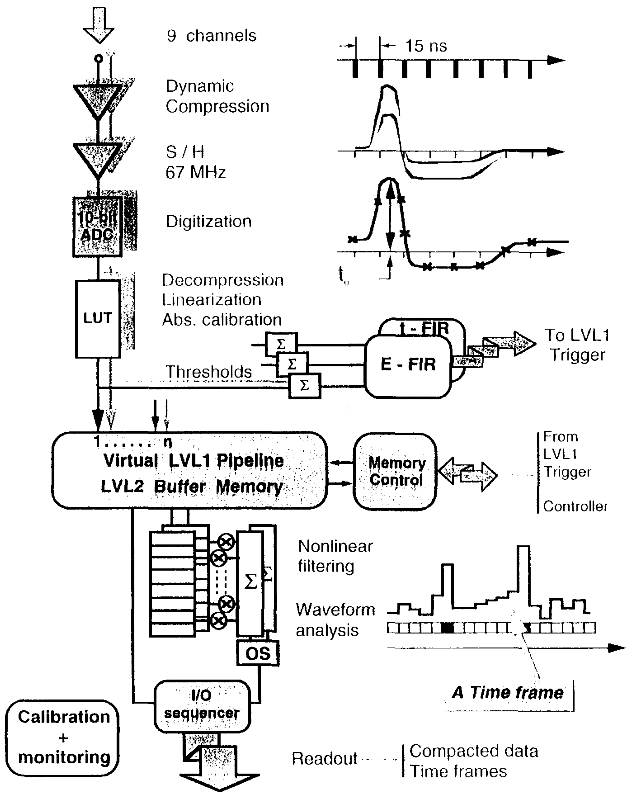
Trends





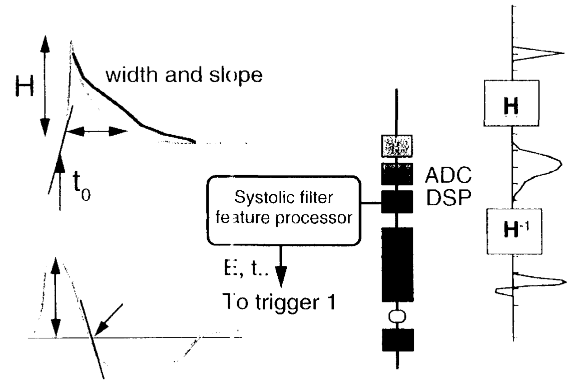
Collider/LEP	LHC
≈ 10^5 channels	≈ 10^7 channels
≈ 10^5 byte/ event	≈ 10^6 byte/ event
≈ 10^5 Hz rate	≈ 10^7 Hz rate

Frontend readout microsystem. FERMI



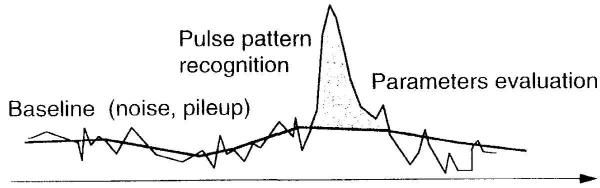
Digital signal processing

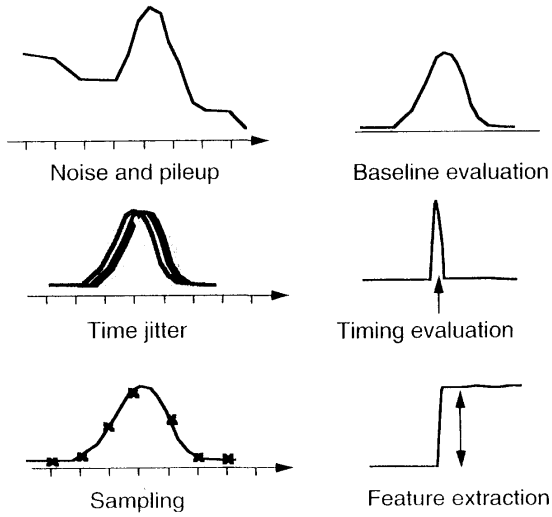
The signals generated by an LHC calorimeter cell will be diffused over more than one bunch crossing. A digital channel with programmable filter capability is needed to extract the physical information and to associate events within bunch crossings.
In addition the digital analysis can be the first step of the trigger process.



Apart from considerations of power consumption, electronics packaging and radiation hardness, it seems very attractive to go digital immediately after the preamplifiers, complementing the analog shaping with a **pipelined digital signal processor**.

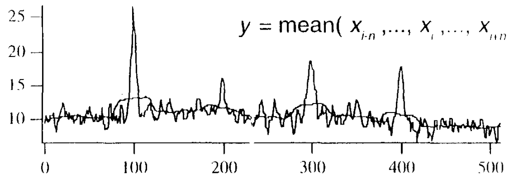
Digital signal processing



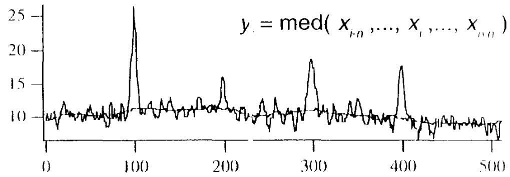


Baseline normalization

The purpose of the base line normalization is to remove the constant background and low-frequency components. The methods presented here are based on the subtraction of a signal mean value from the original signal. The analysis window length in base line normalization is substantially larger than the length of a typical filter.



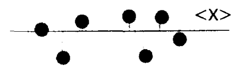
Arith netic mean



Standard median

Mean/Median. Baseline estimation

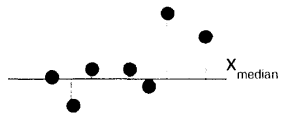
Mean
(gaussian error distribution)



$\langle x \rangle \rightarrow \text{Min}\ \{ \sum (x - \langle x \rangle)^2 \}$

$\langle x \rangle = (x_1 + x_2 + \ldots + x_n)/n$

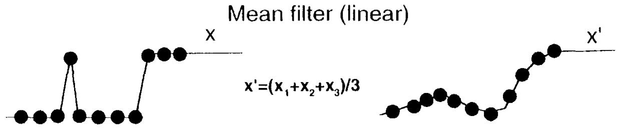
Median
(laplacian error distribution)



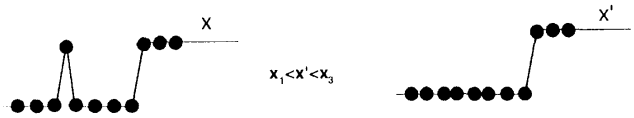
$x_{median} \rightarrow \text{Min}\ \{ \sum |x - x_m| \}$

$x_1 < x_i < x_{median} < \ldots + x_k$

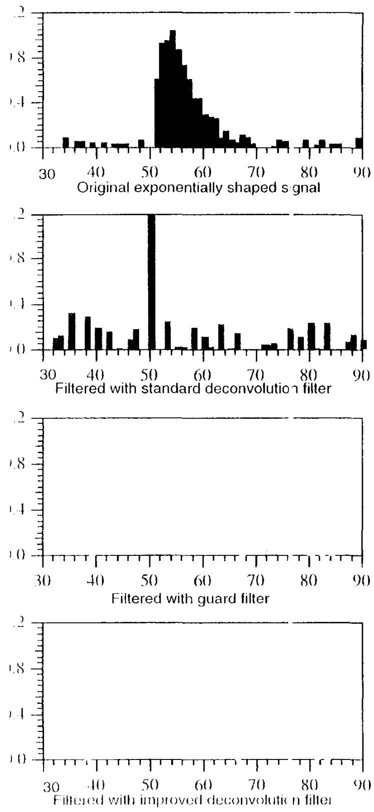
Mean filter (linear)



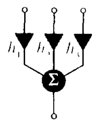
Median filter (non-linear)



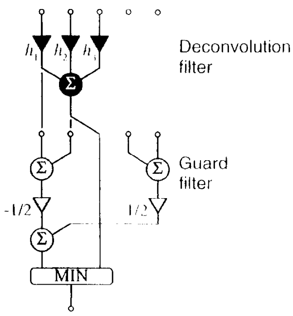
Non-linear deconvolution operator



- Delta pulse (height = 1) at i=50
- Signal with 5% additive white Gaussian noise
- Only positive signal displayed



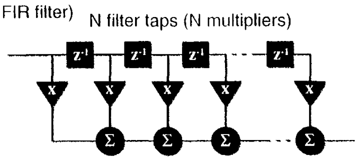
Standard deconvolution operator



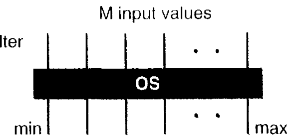
Improved linear-minimum hybrid deconvolution operator

Basic digital filters

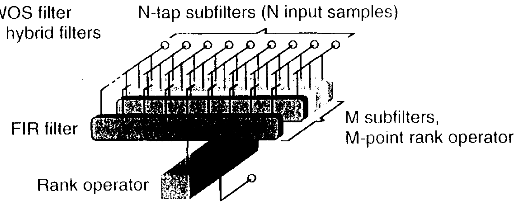
FIR (Finite Impulse Response) filter
- Time-domain design
- Frequency domain design
- Optimal filters (e.g. Wiener FIR filter)



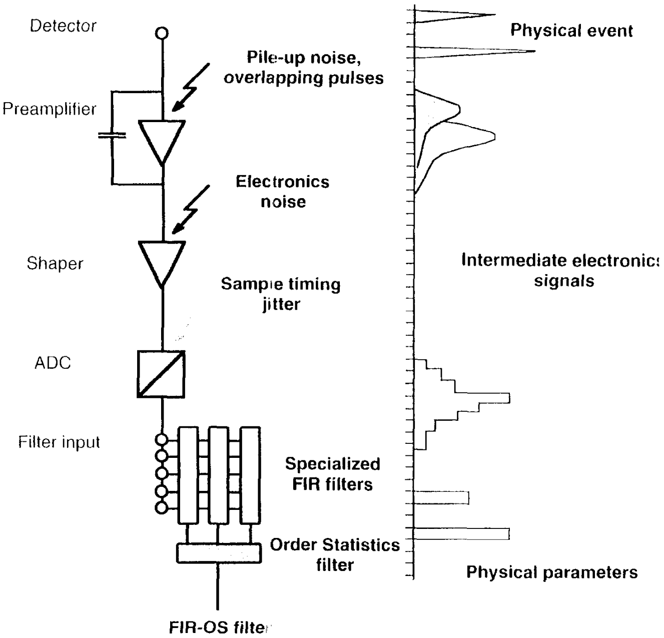
OS (Order Statistic) filter
- Time-domain design
- Rank order filter
- Weighted order statistic (WOS) filter



Hybrid filter
- FIR-OS filter
- FIR-WOS filter
- Other hybrid filters



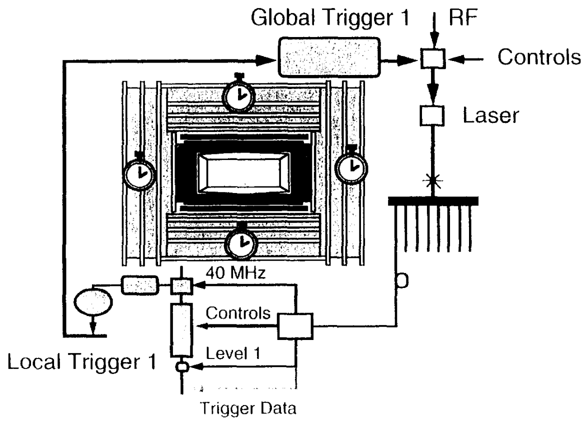
Hybrid filters for feature extraction



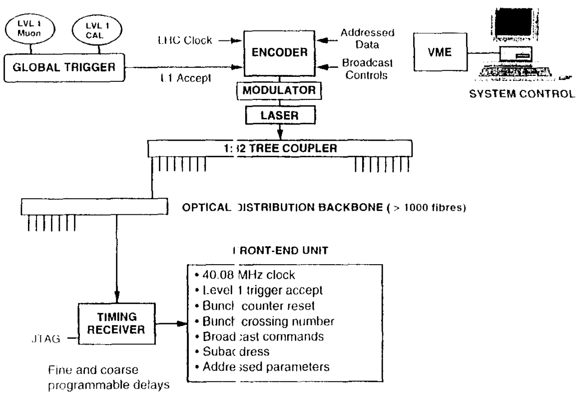
High precision measurements (16-bit range, 10-bit resolution)
Pipelined system running at 40 MHz

Timing, trigger and control distribution. TTC

Development of basic hardware and software components of a **multichannel optical-fibre timing distribution system** for LHC detector front-end electronics, and investigation of the feasibility of simultaneously exploiting the timing system for transmission of the level-1 trigger acceptance and addressable control information

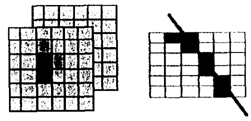


Timing, trigger and control distribution

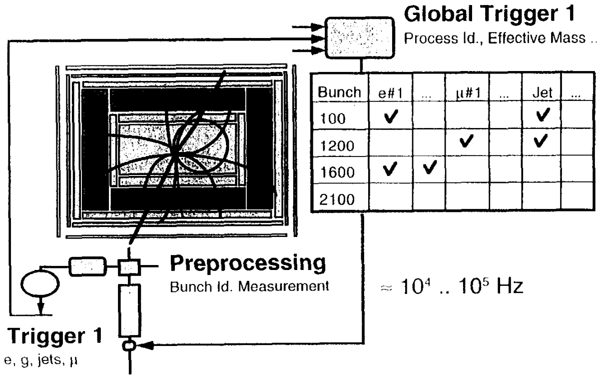


First level trigger

- **Signatures**
  - Electron/photon (isolation requirement)
  - Muons
  - Jets
  - Missing E_T
- **Background (e/γ)**
  - High-p_T jets



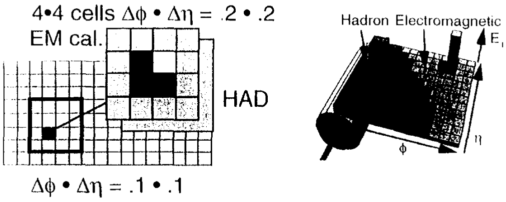
Cluster finding   Segment finding



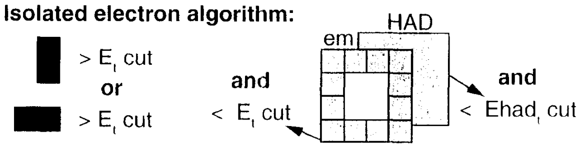
Bunch	e#1	...	μ#1	...	Jet	...
100	✓				✓	
1200			✓		✓	
1600	✓	✓				
2100						

Synchronous system 25ns pipelined
≈ μs latency (processing)
≈ μs latency (distribution)

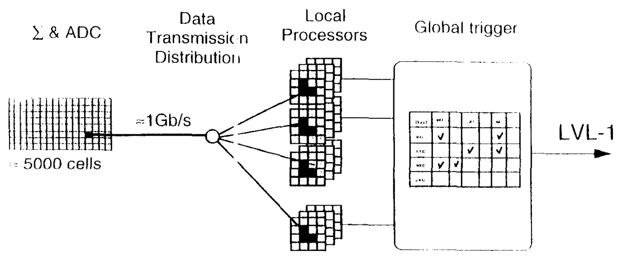
Calorimeter level-1



Isolated electron algorithm:

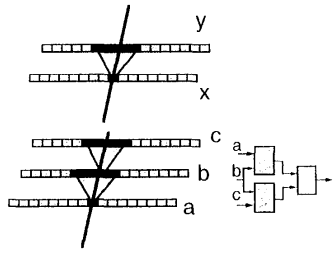


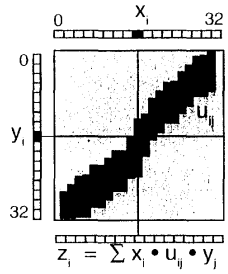
ASIC (RD-27). 16*8 input, .8μm CMOS Fujitsu 66.8 MHz
15ns pipeline. < 500 ns latency



Muon level-1 coincidence matrix

Segment identification in low occupancy detectors.

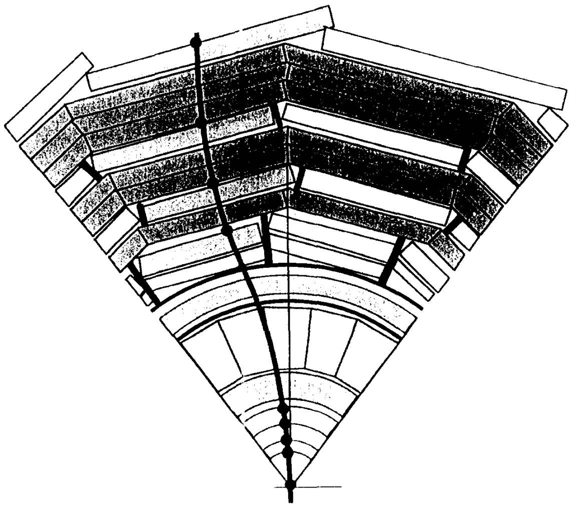




Muon first level trigger

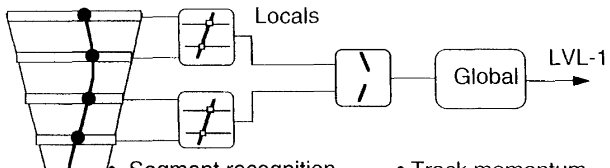
Trigger based on tracks in external muon detectors that point to interaction region

- Low-p_T muon tracks don't point to vertex
  - Multiple scattering
  - Magnetic deflection
- Two detector layers
  - Coincidence in "road"



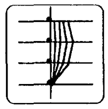
Detectors: RPC (pattern recognition), DT(track segment)

Muon level-1



- Segment recognition
  - Cone coincidence (RPC)
  - Mean timer (Tube)

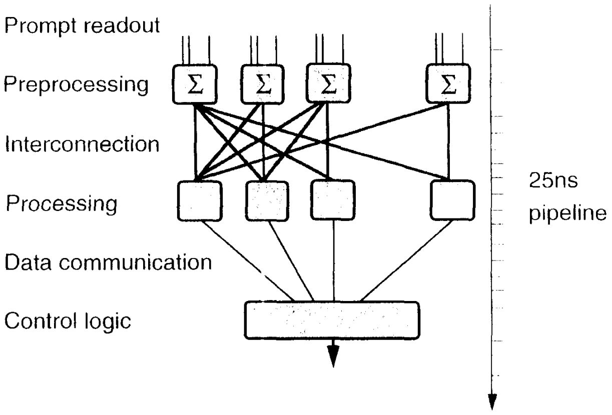
  or
- Logic mask



- Track momentum
  - Coincidence matrix
  - Logic mask

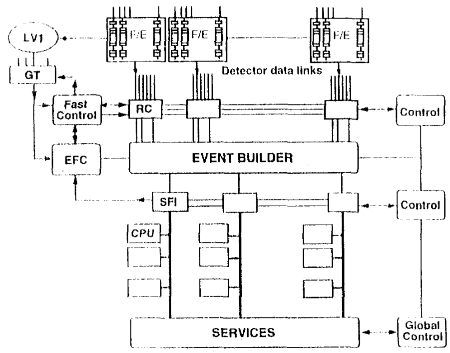
- Content addressable memories
- Matrix logic (ASIC, Gate array...)

Level-1 structure



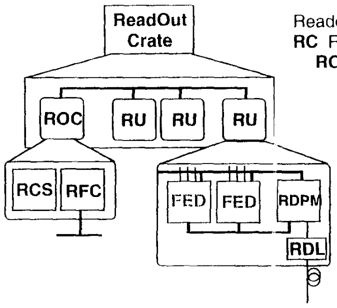
- Fast data link (≈1Gb/s)
- Pipelined processing elements (40,80,160 MHz)
- High speed interconnection network

Readout



- Readout crate
- Readout unit
- Dual port memory

Readout crate



Readout Crate subsystems:
RC Readout Crate
- **ROC** Readout Controller
  - **RCS** Readout Crate Supervisor
  - **RFC** Readout Flow Controller
  - **RU** Readout unit
    - **FED** FrontEnd Driver
    - **RDPM** Readout Dual Port Memory
    - **RDL** Readout Data Link

RCS Readout Crate Supervisor. RCS is a commercial VME processor. ROC performs the data acquisition control and monitoring and the local detector test and maintenance.

RFC Readout Flow Controller. RFC Unit generates and processes the signals used to monitor and control the data flow. The *unit provides also multi-crate* interconnection facilities (e.g. SCI) for local detector test and maintenance.

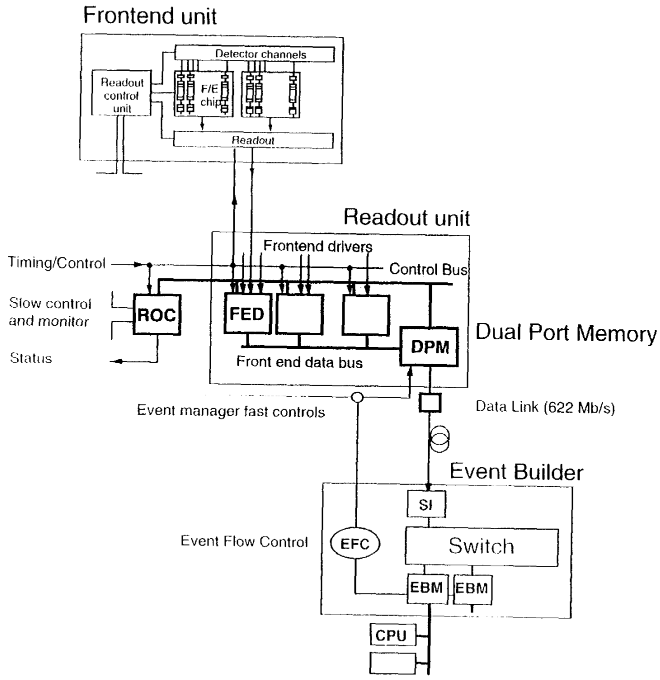
FED The FrontEnd Driver is a detector dependent module performing the data collection from the detector frontend electronics. The FED cost is included in the detector *electronics estimations*

RDPM The Readout Dual Port Memory is the data acquisition module used to buffer multi-event (up to 10') data and to communicate with the event builder switch. It may be implemented by a custom design, by an embedded processor system or by a standard desktop computer (the solution depends on the attainable performances such as 100 MB/s throughput and 100 MB memory)

RDL The digital data link (transmitter receiver and fiber) between the RDPM and the event builder

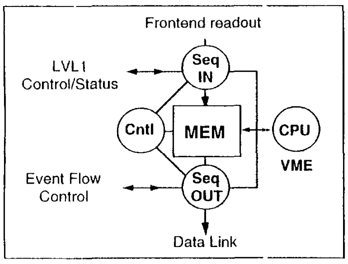
RU The Readout Unit is the logical and physical system performing the data acquisition functions. The composition (number of FED boards and the number of RUs in a crate) is determined by the *average data volume produced in each* partition and can vary with the detector type and the detector region. Moreover the total number of RUs (event builder ports) is related to the data link speed and the exploitable bandwidth (≈ 500 Gb/s) of the switch able to comply with the CMS requirements (100 kHz rate of 1MB events with high level trigger scheme based on partial event data building).

Readout unit



Dual port memory functions

- Autonomous Input/Output
- 100 MB/s throughput
- Large memory (up to 100MB)



SeqIN allocates buffers and reads data from F/E modules

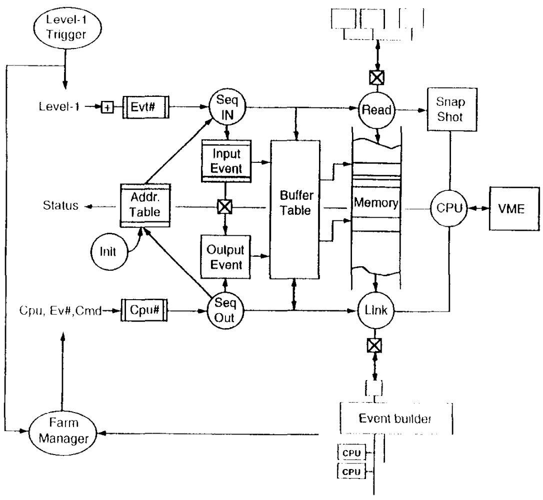
CPU monitors the status and handles faulty conditions. CPU(VME) may spy event data for monitoring

SeqOUT formats the data according to the data link standards and controls the transmission

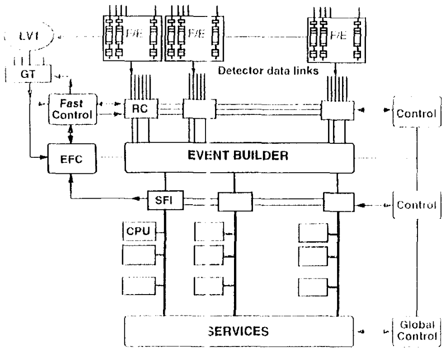
A DPM module operates as a dual access disk controller. At input, files (event buffers) have to be created, written and closed. At output, files (event buffers) have to be open, read and deleted.

Given the high throughput (≈ 100 MB/s) all I/O and control operations may have to be done by hardware units. A standard processor is used to recover from faulty situations and to manage errors and conflicts

DPM structure



Event builder

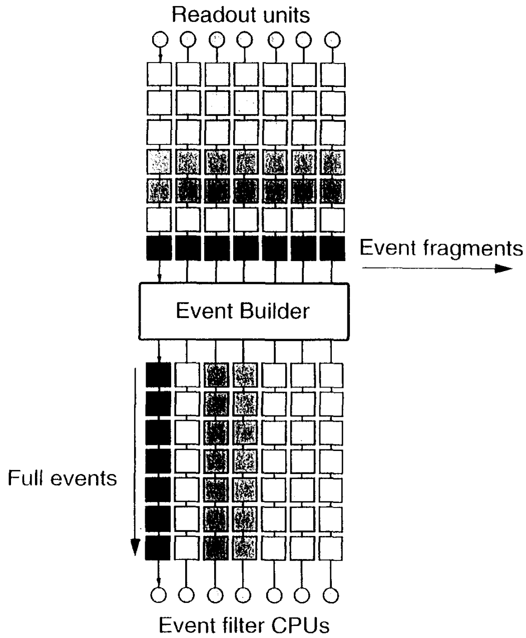


Readout Network & Event Builder

- ≈ 1000 • 266 Mb/s data links
- ≈ 100 • (10 to 1) multiplexers
- ≈ 100 • 100 2.4 Gb/s Switching network

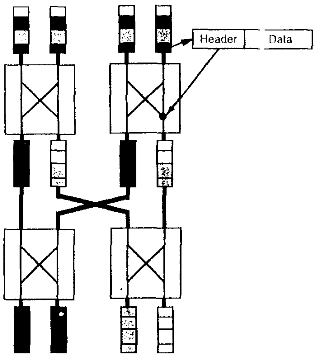
- ≈ **500 Gb/s aggregate bandwidth**

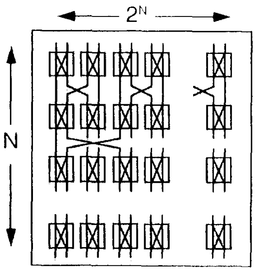
Event building



ATM

Asynchronous Transfer Mode network system.
ATM telecommunication standard
1992. 155 Mb/s ... 620 Mb/s ... 2.4 Gb/s 199X





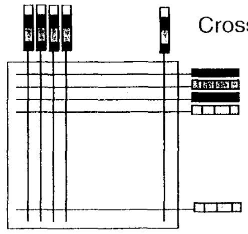
Standard ATM network

- Alcatel ATM. 155 Mb/s
- IBM prizma. 400 Mb/s
- AT&T Phoenix. 320 Mb/s

...... More on the market in the future

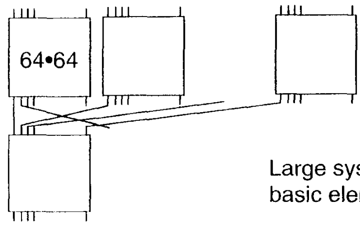
Fiber Channel

Fiber Channel is a standard for computer data communicatior



Crossbar switch based on Fiber Channel

ANCOR can provide 2048•2048 switches based on a 64•64 unit running at present at 266 Mb/s

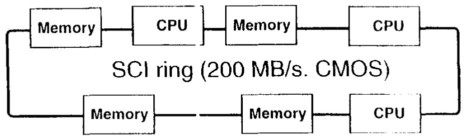


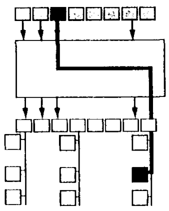
Large systems can be built from basic elements

Fiber Channel can be a very efficient way to event assembly when dealing with large data records. It can be a valuable candidate for event building in a scheme where many (≈100) event data blocks are transferred at the time

Scalable coherent interface. SCI

SCI is IEEE standard for processor intercommunication. It has to demonstrate its impact in the computer industry. Node interfaces are almost available and switches are under study





A SCI based event builder allows an event builder architecture where the processor accesses only the data needed at a given trigger level

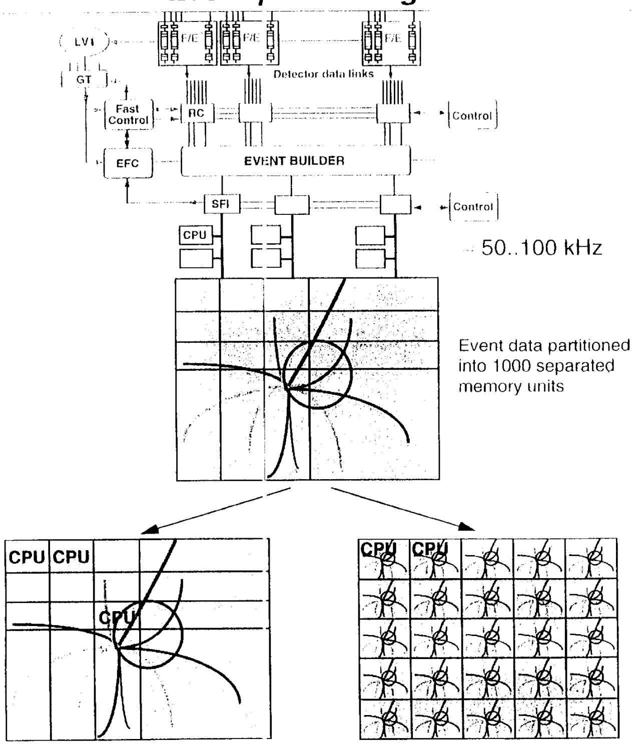
Event filter

The event filter consists of a set of high performance commercial processors organized into many farms convenient for on-line and off-line applications. The farm architecture is such that a single CPU processes one event.

- ≈ 100 farms of 50 processors
- ≈ 1000 MIPS/processor
- Trigger levels 2, 3 ..& Data analysis

1 event 1 sec	Event Filter	Analysis	Total Online&Offline
UA/LEP	4 MIPS	400 MIPS	**50 MIPS (30 Hz)**
LHC	400 MIPS	$4 \cdot 10^4$ MIPS	**$4 \cdot 10^6$ MIPS (10 KHz)** Latency ≈ ms to sec

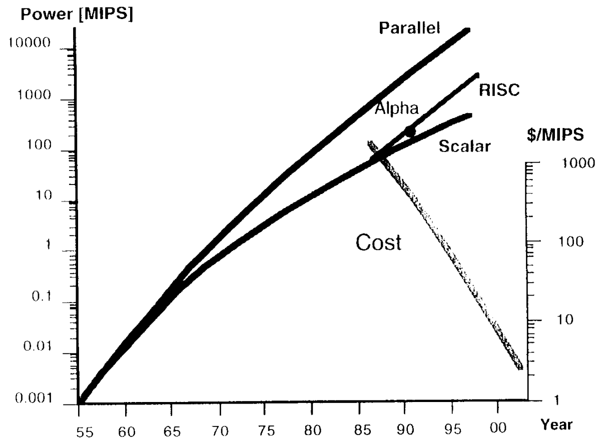
Event processing



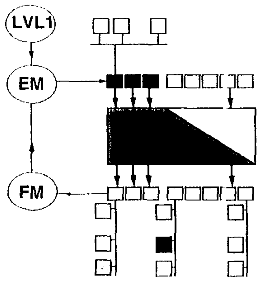
Massive parallel system

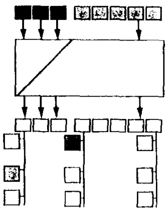
Farm of processors

CPU trends



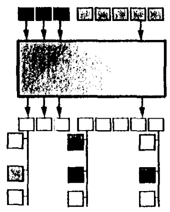
CMS virtual level-2





1) The level-2 selection uses the calorimeter, muon and preshower data. The sub-events are built using a fraction of the switch bandwidth (e.g. 30 %).

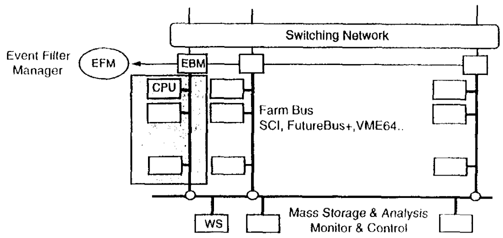
2) The rest of the event data is sent after the level-2 decision if the event is accepted



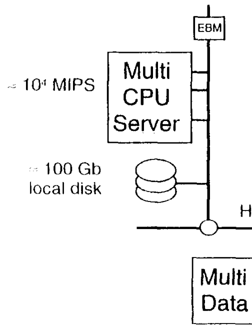
The two operations take place in parallel.
The sharing between the level-2 data sources and the rest is such to match the event builder bandwidth with the level-2 rejection rate.

- Up to 100 kHz with virtual level-2 mode
- Up to 50 kHz reading the full event data

Event filter today



Event filter unit



On/Off line computing unit :
Natural evolution of the laboratory computing model based on distributed computing servers with high bandwidth data interconnection and local data staging and archiving units

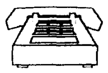
- RD-24 SCI interconnect link.
  - Hardware node (Dolphin design GaAs and CMOS).
  - Switches and bridges under study as well

Technologies

40 MHz, 10^7 channels

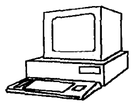
Frontend and trigger processors
- **In house VLSI design development**
- **Embedded systems. DSP industry**

500 Gb/s



Readout network
- **Telecommunication and computing industry**

≈ 10^6 MIPS



Event filter (levels 2&3....)
- **Computer industry. RISC processors and multiprocessor work stations**
- **Standard computer interconnect buses**

The CMS data acquisition system exploits standard industry components as far as possible, and a considerable part of the system is expected to be developed and installed by industry.

Switching network and farm power extensions can be made to track LHC machine improvements by adding the most performant and cost effective processors available at the time.