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Switching Trajectory Control for High Voltage Silicon Carbide Power Devices with Novel Active Gate Drivers

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a concentration in Electrical Engineering

by

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ABSTRACT

The penetration of silicon carbide (SiC) semiconductor devices is increasing in the power industry due to their lower parasitics, higher blocking voltage, and higher thermal conductivity over their silicon (Si) counterparts. Applications of high voltage SiC power devices, generally 10 kV or higher, can significantly reduce the amount of the cascaded levels of converters in the distributed system, simplify the system by reducing the number of the semiconductor devices, and increase the system reliability.

However, the gate drivers for high voltage SiC devices are not available on the market. Also, the characteristics of the third generation 10 kV SiC MOSFETs with XHV-6 package which are developed by CREE are approaching those of an ideal switch with high *dv/dt* and *di/dt*. The fast switching speed of SiC devices introduces challenges for the application since electromagnetic interference (EMI) noise and overshoot voltage can be serious. Also, the insulation should be carefully designed to prevent partial discharge.

To address the aforementioned issues, this work investigates the switching behaviors of SiC power MOSFETs with mathematic models and the formation of EMI noise in a power converter. Based on the theoretical analysis, a model-based switching trajectory optimizing three-level active gate driver (AGD) is proposed. The proposed AGD has five operation modes, i.e., faster/normal/slower for the turn-on process and slower/normal for the turn-off process. The availability of multiple operation modes offers an extra degree of freedom to improve the switching performance for a particular application and enables it to be more versatile. The proposed AGD can provide higher switching speed adjustment resolution than the other AGDs, and this feature will allow the proposed AGD to fine tune the switching speed of SiC power devices. In addition, a novel model-based trajectory optimization strategy is proposed to determine the

optimal gate driver output voltage by trading the EMI noise against the switching energy losses. For the 10 kV SiC power MOSFET, the detailed design considerations of the proposed AGD are demonstrated in this dissertation. The functionalities of the 3-L AGD are validated through the double pulse tests results with 1.2 kV and 10 kV SiC power MOSFETs.

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DEDICATION

This dissertation is dedicated to my parents, Lun Zhao and Xiaoxing Hu. My heartfelt gratitude goes to them for their everlasting love, strength and support through my entire life.

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LIST OF PUBLICATIONS

[1] S. Zhao *et al.*, "Adaptive multi-level active gate drivers for SiC power devices," *IEEE Trans. Power Electronics*.

[2] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao, and H. A. Mantooth, "An intelligent versatile model-based trajectory optimized active gate driver for silicon carbide devices," *IEEE J. Emerg. Sel. Topics Power Electron.*

Chapter 2 and Chapter 3 of this dissertation are reused from the contents of the aforementioned articles.

CHAPTER 1

INTRODUCTION AND THEORETICAL BACKGROUND

1.1 Background: The challenge and opportunity of SiC power devices

1.1.1 The demand of high frequency power converters

The power industry calls for the higher power density, efficiency, voltage rating, and operation temperature of semiconductor devices [1.1]. Generally, a high switching frequency is preferred because a high frequency converter requires smaller filter inductors and has higher control accuracy over the low frequency converter [1.2]. Figure 1-1 shows the size of a 20 kHz transformer and a 60 Hz transformer, both rated at 2.5 kVA.

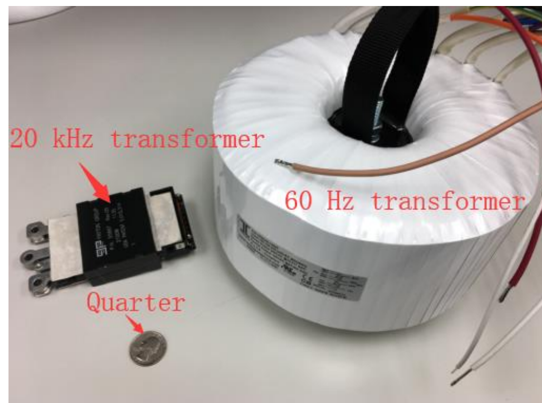

Figure 1-1 Comparison of a high frequency transformer and a low frequency transformer.

Limiting factor for increase switching frequencies is the high power loss of the conventional silicon semiconductor devices [1.3]. These power losses include the switching losses and the conduction losses. Generally, a higher switching frequency results in higher switching losses under hard switching conditions [1.4]. For a typical dc microgrid application, 400Vdc/2 kW, the silicon MOSFET can generally operates at frequencies lower than 50 kHz [1.5]. Since the switching losses are proportional to the switching frequency, at high frequencies, the switching losses will increase

to the degree that the heatsink cannot dissipate the heat. As a result, higher operation frequencies may present challenges for the thermal management of the system.

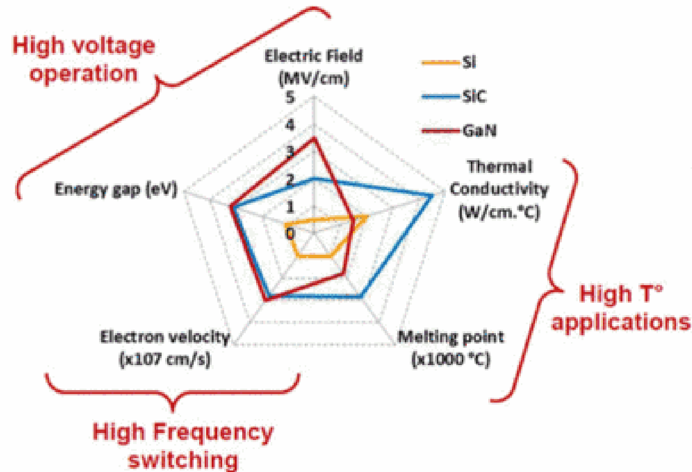

Figure 1-2 Summary of Si, SiC, and GaN relevant material properties [1.9].

Therefore, the application of wide bandgap (WBG) devices in the power industry will be the future trend since they can effectively increase the efficiency and reduce the thermal stress of the devices at higher frequencies [1.6].

1.1.2 Application of wide bandgap devices in the power converter

The most attractive characteristics of the WBG devices over the silicon (Si) devices are their low parasitics, i.e., low conducting resistance, low junction capacitance, and low parasitic inductance [1.7]. Due to the higher energy band, WBG devices can withstand higher avalanche breakdown voltage than their Si counterparts using the same die size [1.8]. There are various types of WBG materials such as gallium nitride (GaN), silicon carbide (SiC), and diamond. GaN and SiC are the two most commercialized WBG materials [1.8]. The comparison of SiC, GaN and silicon (Si) are as shown in Figure 1-2 [1.9].

GaN is more suitable for lower voltage applications because GaN has lower switching losses than the Si and SiC at a voltage levels lower than 600V [1.8]. Figure 1-3 shows the 600V/15A GaN power module with gate drivers developed by Texas Instruments. The compact design of the demo in Figure 1-3 can effectively reduce the parasitic inductance and capacitance on the PCB and boost the switching speed.

Figure 1-3 The Texas Instruments® GaN integrated half-bridge power module.

However, SiC dominates the medium-voltage level applications [1.9]. 10 kV SiC MOSFET and 15 kV SiC IGBT have been developed by CREE [1.10] [1.11]. The commercial products of Si counterparts with highest voltage rating on the market is the 6.5 kV IGBT. The development of the high voltage SiC semiconductor devices is significant since it can reduce the complexity of the converter system. Generally, for the medium voltage (3.3 kV-35 kV) application such as the distributed flexible AC transmission system (D-FACTS) and battery energy storage system (BESS), multilevel topologies are utilized to enable the use of lower voltage rated semiconductor devices for achieving higher output voltages [1.12]. However, using 1.2 kV power modules will require a significant amount of semiconductor devices which are connected in series to increase the output voltage. The overall system will be very bulky. Also, it will make the system very complicated due to relatively large number of control signals, and reduce the reliability of the

overall system [1.13]. Therefore, using the high voltage power devices will effectively reduce the potential risk of system faults, increase system reliability, and reduce the overall cost [1.14]. Table 1-1 shows the number of power devices needed for the 13.8 kV distributed energy storage system with different voltage ratings of SiC power MOSFET. From Table 1-1, the 10 kV SiC will reduce the levels of the cascaded H-bridge inverter for battery energy storage system application by half [1.15].

Table 1-1 Comparison of numbers of different voltage rating SiC devices on a 13.8 kV cascaded H-bridge inverter [1.15].

SiC Device	**DC Bus Voltage**	**# of cells per phase**	**AC 3Φ output**	**Number of Switching Devices**
1.2 kV	720 V	20	13.8 kV	360
1.7 kV	1.2 kV	10	13.8 kV	180
3.3 kV	2.6 kV	6	13.8 kV	108
6.5 kV	3.5 kV	4	13.8 kV	72
10 kV	7 kV	2	13.8 kV	36

As mentioned above, another benefit of the SiC power devices is the lower parasitic parameters over the Si counterparts. The 4-H SiC MOSFET has higher breakdown voltage, thus, the thickness of the die can be thinner than the regular Si die. This feature can dramatically reduce the parasitic capacitance and resistance, thus reducing the switching losses [1.16]. The comparison of Rohm SCT2280KEC SiC MOSFET and Microsemi Si APT13F120B MOSFET is shown in Table 1-2.

From Table 1-2, the SiC has lower conducting losses over Si counterparts. Also, the junction capacitance of SiC MOSFET is much lower than Si MOSFET. Therefore, the switching losses of SiC MOSFET is lower since the switching transient time is shorter. All of these superior characteristics enable SiC to dominate the market for power semiconductor for the voltage higher than 650 V in the future.

Table 1-2 Comparison of SiC MOSFET and Si MOSFET.

Parameter	SCT2280KEC	APT13F120B
Drain-source voltage	1.2 kV	1.2 kV
Continuous drain current	14 A	14 A
Maximum junction temperature	175 ℃	150 ℃
Gate-source charge	9 nC	24 nC
Gate-Drain charge	12 nC	70 nC
Reverse recovery charge	21 nC	1.12 μC
Current rise time	19 ns	15 ns
Current fall time	29 ns	24 ns
Continuous conduction drain-source resistance	280 mΩ	910 mΩ

1.2 Challenges of the SiC power devices applications

The application of SiC devices can reduce energy losses and increase the operation frequency, which increases overall power density. However, it also introduces challenges regarding electromagnetic interference (EMI) immunity. The EMI noise and the high cost hinder SiC devices from further commercialization [1.17]. The EMI noise will not only affect the power quality of the power load and power supply, but also increase the probability of failure [1.18]. Using novel gate drivers can effectively address the EMI issues.

Generally, a typical gate driver board consists of an isolated power supply, a digital isolator, and a gate driver buffer [1.4]. A typical gate driver board layout is as shown in Figure 1-4.

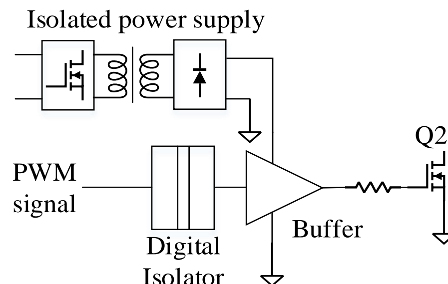

Figure 1-4 The basic layout of a gate driver.

As the key part that controls the power device switching speed, the gate driver is significant to the safe operation of the converter [1.4]. Specifically, the gate driver should provide enough EMI immunity capability to prevent the EMI noise from affecting the digital side of the power converters. Additionally, most gate drivers on the market provide over current protection which is vital to the converter. As demonstrated in the last section, application of high voltage SiC devices can increase the reliability and efficiency of the system, while it also brings about several major challenges: EMI immunity, isolation, and protection.

1.2.1 The EMI issues

High *dv/dt* is one of the major contributors of high EMI noise. Comparing with the Si power devices, the SiC has lower junction capacitance. Thus, the switching transient can be very fast. In other words, both the slew rate of drain-source voltage *dv/dt* and drain current *di/dt* of the SiC power devices are higher. The voltage of Wolfspeed C2M0045170 SiC MOSFET discreet module can increase from 0 V to 1.2 kV in 20 ns [1.19], which means *dv/dt* is 60 kV/µs. However, most gate drivers on the market can only isolate 50 kV/µs *dv/dt*.

Recently, a new packaging method, 3D packaging, can further boost the switching speed of the power devices [1.20]. In the case of 3D packaging, the SiC MOSFET can increase from 0 V to 800 V in 4 ns. The *dv/dt* is 200 kV/µs. High *dv/dt* can generate a high current flowing through the gate loop and results in a shoot-through failure [1.21]. Figure 1-5 shows a shoot through fault which occurred on a discreet SiC device implemented on a half bridge board.

Figure 1-5 The shoot through fault.

Figure 1-6 shows the Fast Fourier Transform (FFT) results of two signals with different slew rates. From Figure 1-6, higher slew rate signal has higher high-order harmonic components which is a major cause of the EMI noise. Therefore, reducing the *dv/dt* to a certain level will be helpful to reduce the EMI noise.

The first detrimental effect of EMI noise is the ringing on the waveform which may increase the ripple on the output waveform. The EMI propagation route is shown in Figure 1-7 [1.22].

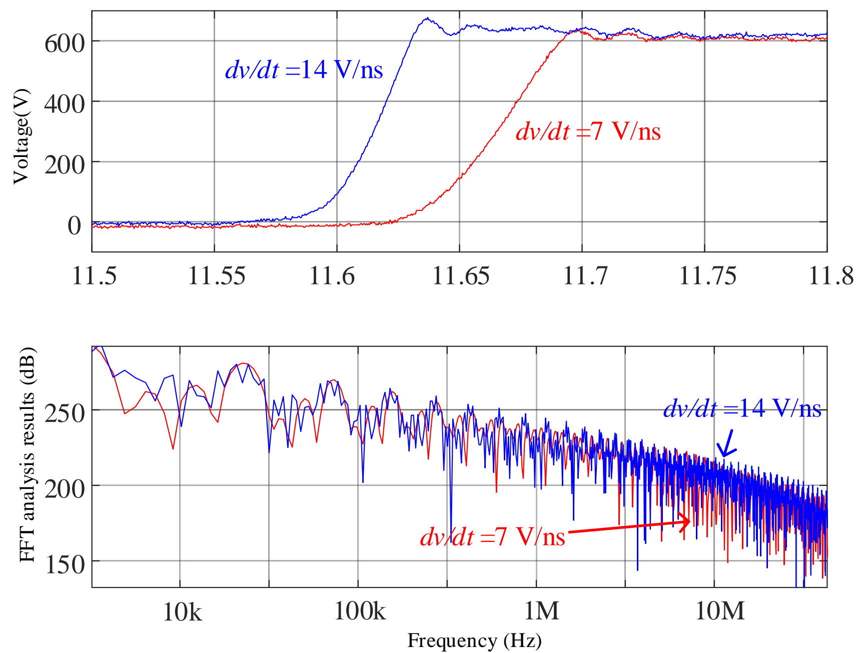

Figure 1-6 The FFT analysis results of two signals with different slew rates.

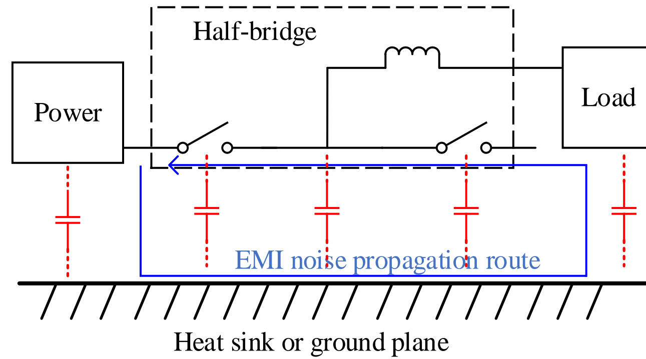

Figure 1-7 The EMI noise propagation route.

The high frequency noise can flow through the parasitic capacitors between the half-bridge and the ground plane to the load terminal and power supply terminal. Furthermore, when the digital side of the power converter is close to the ground plane, the common mode noise can influence the digital controller or gate signals and cause a failure [1.23].

Another problem caused by the high EMI noise which should be paid special attention is potential false triggering event. The drain-to-source voltage slew rate may interact with the parasitics in the circuit and cause a false triggering event. The equivalent circuit of a power MOSFET is shown in Figure 1-8 [1.24]. A power MOSFET typically incorporates some parasitic capacitors: gate-to-source capacitor C_{gs}, gate-to-drain capacitor C_{gd}, and drain-to-source capacitor C_{ds}. The parasitic inductors include drain inductor L_d, source inductor L_s, and gate inductor L_g [1.24].

As shown in Figure 1-8, when the power device turns off, C_{gd} will charge from conduction voltage to dc bus voltage and cause feedback gate current $C_{gd}dv/dt$. The variation of the charge on the Miller capacitor C_{gd} may cause a gate current to develop in the loop. With this gate current flowing through the gate resistor R_g, it may generate a voltage on V_{gs}. The maximum turn-off dv/dt

of a device can be calculated with Eq. (1-1). In Eq. (1-1), R_{g_int} is the intrinsic gate resistance of the power MOSFET.

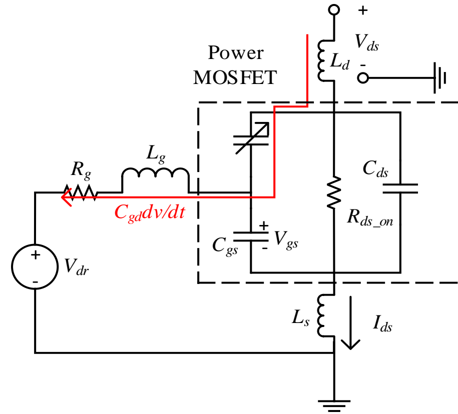

Figure 1-8 The equivalent circuit of a power MOSFET.

$$\frac{dv}{dt} \leq \frac{V_{th} - V_{dr_off}}{C_{gd} R_{g_int}} \tag{1-1}$$

If V_{gs} is higher than the gate-source threshold voltage of the power device, the power device will turn on falsely. High *dv/dt* may also cause high crosstalk noise. The crosstalk noise is the common mode noise which occurs on a gate driver for the half bridge module. The generation of the crosstalk noise can be found in Figure 1-9 [1.4].

From Figure 1-9, the potential of the upper switch changes will result in *dv/dt*. Even though the gate driver isolated power supply has isolation barrier, there is still parasitic capacitance between the primary side and secondary side of the barrier, i.e., C_{T1} and C_{T2}. C_{T1} and C_{T2} which provide potential current routes for the spread of the common mode noise. *dv/dt* can generate current flowing on C_{T1} and C_{T2} which will cause voltage on V_{gs} and a potential false triggering event.

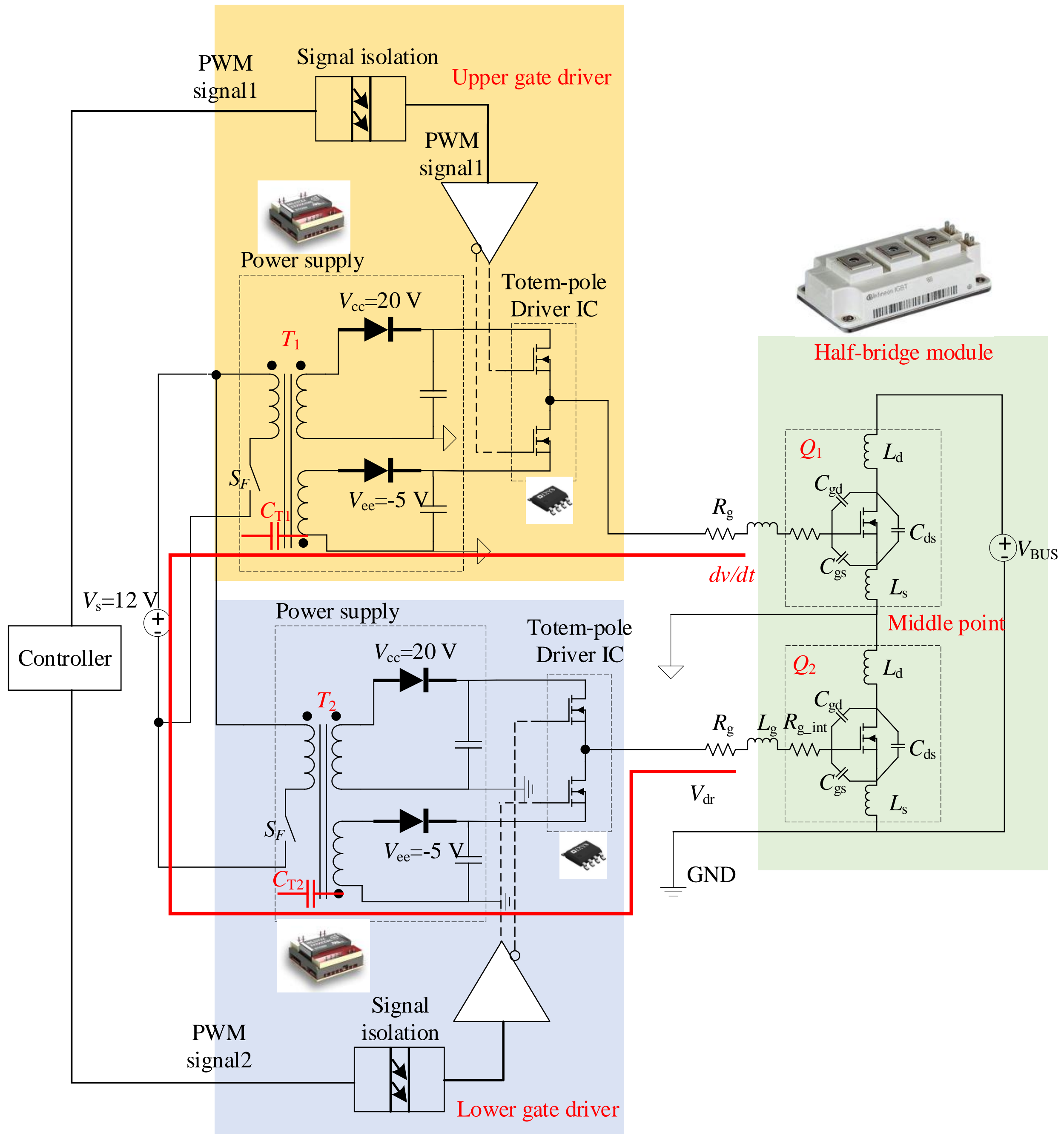

Figure 1-9 The crosstalk noise current route in a half-bridge module.

An example of the crosstalk noise in a full bridge is shown in Figure 1-10.

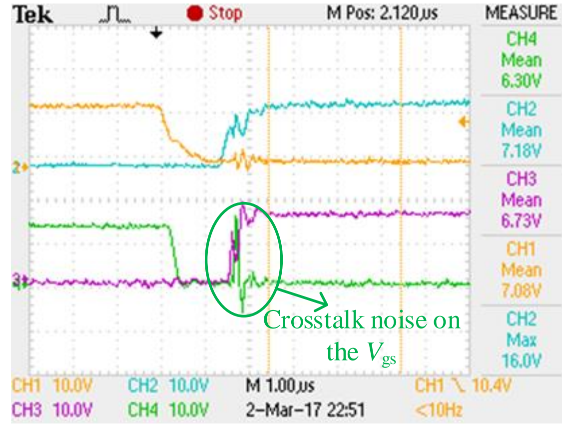

Figure 1-10 The crosstalk noise on the V_{gs}.

In Figure 1-10, CH3 and CH4 are the V_{gs} of the upper switch and the lower switch of a bridge, respectively. When the upper switch (CH3) is turning on, there is also a voltage spike on lower switch (CH4).

1.2.2 Voltage overshoot

Another problem of fast switching which must be addressed is the overshoot caused by high *di/dt*. Because of the parasitic inductance on the module, the high *di/dt* will result in overshoot voltage on the drain [1.4]. For the worst case, the overshoot voltage exceeds the maximum voltage rating of the MOSFET and result in the failure of the switches. To suppress the EMI noise brought by the high *dv/dt* and *di/dt*, there are several potential solutions. One method is to increase the gate resistance [1.25]. With higher gate resistance, the current for charging the C_{gs} will decrease. The I_{ds} is expressed in (1-2) [1.4].

$$I_{ds} = g_{fs}(V_{gs} - V_{th}) \tag{1-2}$$

g_{fs} is the transconductance. V_{th} is the threshold voltage. Therefore, the slower the V_{gs} increases, the lower the *dv/dt* will be. However, higher R_g will increase the power losses and the turn-off transient. The longer turn-off transient will dramatically increase the deadtime of the converter

required. A larger deadtime will cause more serious zero-crossing distortion and affect the output power quality of converter [1.26]. To suppress *dv/dt* and *di/dt*, some active gate driver methods are proposed. The active gating methods can be generally categorized into three kinds: variable gate resistance, multi-level voltage gate driver and current source gate driver [1.27].

1.2.3 Isolation

Isolation is an important design consideration for the high voltage SiC power MOSFET gate driver, especially for 10 kV level applications. The isolation for a gate driver board includes the power isolation and signal isolation. For the signal isolation, generally, there are four methods: magnetic isolation, capacitive isolation, optical coupling and monolithic coupling [1.28]. Magnetic isolation technique is widely used by Power Integrations, Infineon, and ON Semiconductor gate drivers [1.29]. It has high isolation strength and long lifetime. In addition, it provides the potential capability for bi-directional and multiple signals.

Table 1-3 The comparison of the different gate signal isolation technologies [1.29].

	Isolation	***dv/dt* immunity**	**Propagation delay**	**Integration level**	**Independent power supply needed?**	**Reliability**	**cost**
Optocoupler	Few kV	>50kV/μs	>400ns	Medium	Yes	Aging issue	$
Fiber optic	Several 10’s kV	>100kV/μs	Negligible	Medium	Yes	Good reliability	$$$$
Monolithic Level shifter	None	50kV/μs	-	Integrated on the IC	No	-	$
Pulse transformer	Several kV	>50kV/μs	<100ns	Bulky	No	Reliable	$
Capacitive coupling	Several kV	>100kV/μs	~20ns	Integrated on-chip or driver IC package	Yes	Very reliable	$$

The challenge is the coupling capacitance between the primary and secondary side. Also, the leakage magnetic flux is a source of radiative EMI noise. Other gate driver designers, such as

Broadcom and ABB, prefer optical coupling method [1.29]. The fiber optic is suitable for the high voltage and high power application, but it is much more expensive than the other methods [1.29]. Capacitive coupling is usually applied in the Texas Instruments gate driver products [1.29]. The advantages of the capacitive isolation are the fast dynamic speed and reliability. The comprehensive comparison of the different isolation methods is listed in Table 1-3 [1.29].

Comparing all the isolation methods, the fiber optic is the most suitable option for high voltage (≥3.3 kV) SiC power MOSFET. The major disadvantage of the fiber optic isolation is its high price. However, the price of the high voltage SiC power MOSFET is high as well. A CREE 10 kV SiC power MOSFET with XHV-9 package costs over $40,000. Therefore, reliability has higher priority than the cost.

The power supply should be galvanic isolated to prevent the high side voltage of a half-bridge module from affecting the low side. Generally, transformer isolation is used for the power supply. A flyback converter is the most commonly used topology for the gate driver [1.30]. However, to provide sufficient high voltage isolation the totem pole dc/dc converter can be used. In [1.31], an isolated power supply with fiber optics is adopted. It can provide 2 W power for the switching of the MOSFET. However, the price of the high power fiber optics is high, generally thousand dollars level. Moreover, the power supply of the fiber transceiver is very bulky and heavy. Therefore, the proposed method in [1.31] is not a cost-effective solution for a high voltage converter.

1.2.4 Short-circuit fault protection

Another challenge of the gate driver design for the SiC power device is the short-circuit protection. When a shoot-through fault happens in the half-bridge module, the current will increase to a very high level in a short time [1.32]. As analyzed previously, the SiC MOSFET devices have

small internal inductance L_s and small conduction drain-source resistance, so the channel current increases faster than their Si counterparts under short-circuit condition. As mentioned in the former sections, a SiC MOSFET has a smaller die than a Si counterpart. The thermal capacity of a SiC MOSFET is lower, and its short-circuit withstanding time (SCWT) is shorter [1.33]. Thus, the protection of SiC power device requires faster detection time and higher *di/dt* suppression capability.

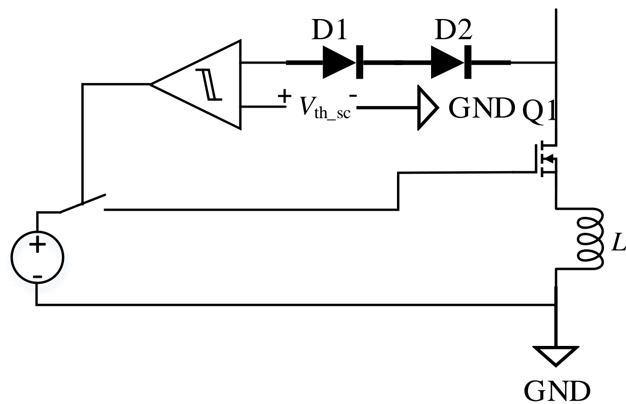

Figure 1-11 The conventional desaturation shoot-through protection.

The protection includes two steps: short-circuit detection and the switch turn-off [1.32]. There are several methods for the short-circuit detection. The most commonly used method is the desaturation (DESAT) sensing [1.32]. The drain-source voltage V_{ds} will be sensed and compared with a threshold voltage V_{th_sc}. For most gate drivers, such as TI ISO5851 and Broadcom, the V_{th_sc} is selected to be 9 V [1.34].

In Figure 1-11, the diodes are used to reduce the voltage on the comparator, such that V_{ds} is compared with a threshold voltage. When the V_{ds} is higher than 9 V, the drain current is very high. That mean the MOSFET works in saturated mode. To prevent short circuit, the gate driver will turn off to cut off the fault current. [1.35] introduces a method with the Rogowski coil. Compared with the conventional method, the Rogowski method provides galvanic isolation which makes it

suitable for the high voltage SiC power devices. It should be noted that Rogowski coil cannot measure the dc signals.

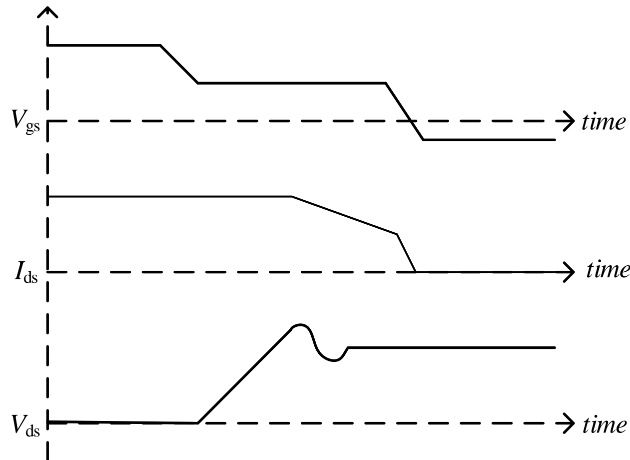

Figure 1-12 The conventional turn-off waveform for desaturation protection.

The fault current cut-off is significant since the fault current is generally very high. The hard switching will result in high *di/dt*. As analyzed previously, the high *di/dt* will generate a voltage on the parasitic inductor [1.36]. For the worst case, the overshoot voltage can damage the power device. The common solution utilized by commercialized gate drivers on the market is soft turn-off. The gate driver does not shut down the power device immediately. The driver voltage will decline to a level and hold for a while, then it will completely shut down the power devices [1.36]. The waveform is shown in Figure 1-12.

1.2.5 Gate current sinking

Gate current sinking capability is important to the gate driver. From Figure 1-8, when the power MOSFET turns off, the charge in the junction capacitor will be transferred back to the gate driver and result in the gate current. The gate current will be freewheeled in the isolated power supply which is a typically fly-back converter and finally disperse across the gate resistance [1.37]. Additionally, as mentioned in the previously, when the high side device of a half-bridge switches

off, current will be generated in the gate loop of the low side switch. This current should be dissipated to prevent a false-triggering event.

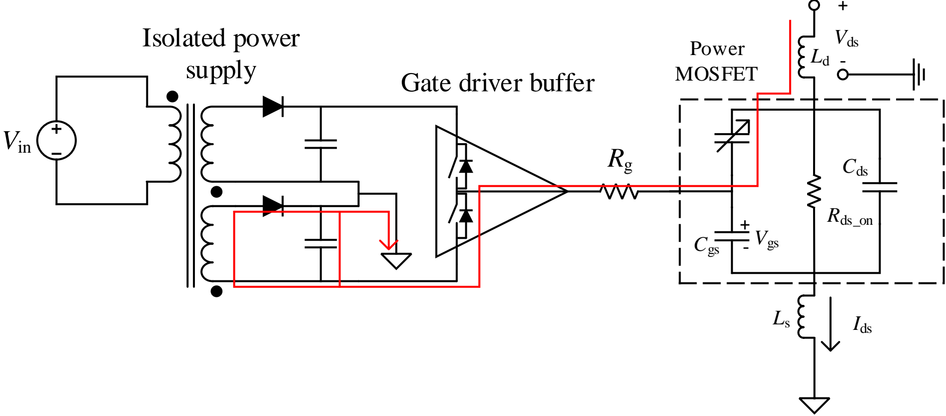

Figure 1-13 The route of sinking gate current.

From Figure 1-13, the sinking gate current will flow into the isolated transformer and the bypass capacitors. However, if the sinking gate current route is blocked due to the high gate loop impedance, it may cause the rise of gate-source voltage and the power device will fail to turn off. Therefore, gate current sinking is significant. A conventional gate current sinking technique is active Miller clamping, which is shown in Figure 1-14 [1.38].

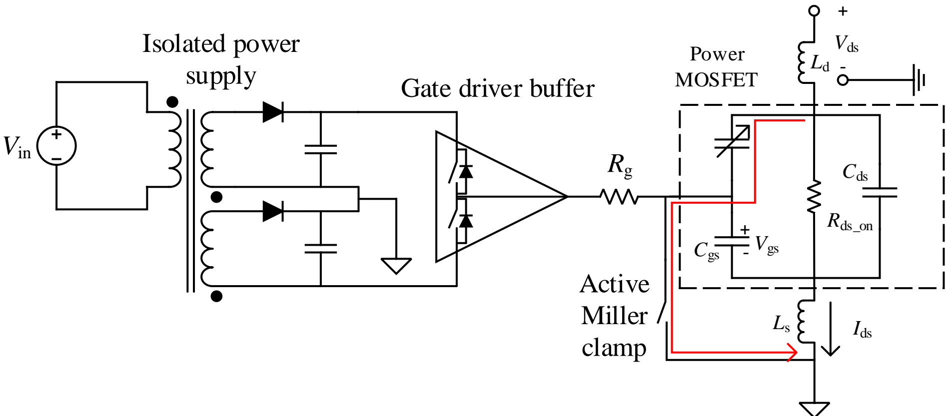

Figure 1-14 Active Miller clamping circuit.

Active Miller clamping circuit provides a shorter current route to sink the gate current and prevent the false triggering event. However, most active Miller clamping circuits require additional control signal which will increase the complexity of the system [1.39] [1.40]. For the 10 kV SiC MOSFET, due to the high junction capacitance and high *dv/dt*, the reversed gate current will be higher than 1.2 kV devices. Therefore, it should be carefully designed.

1.3 The state-of-the-art active gate driver technologies

1.3.1 The basic working principle of the slew rate control

The equivalent circuit of the gate driver during the switching process is shown in Figure 1-15 [1.41].

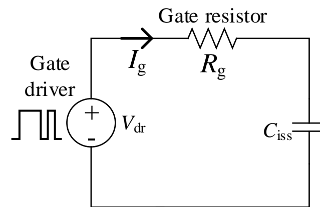

Figure 1-15 The equivalent circuit of the gate driver and power device system.

In Figure 1-15, C_{iss} is the intrinsic input junction capacitor of a power MOSFET. Through charging the gate junction of the power MOSFET, the channel can be formed and the power MOSFET is conductive. The fundamental working principle of all slew rate control methods is to adjust the charging/discharging speed of C_{iss}. From Figure 1-15, there are several factors affecting the junction capacitor charging/discharging speed: gate driver voltage, gate resistance, gate current, and C_{iss} [1.27]. Accordingly, the state-of-the-art AGD methods can be categorized into four categories: variable gate resistance method, variable input capacitance method, variable gate voltage method, and variable gate current method [1.27].

1.3.2 Variable gate resistance method

Variable gate resistance method [1.41]- [1.44] is the most commonly used methodology for the slew rate control. The working principle is depicted in Figure 1-16. Through utilizing different gate resistance for different stages in the switching process, *dv/dt* and *di/dt* can be adjusted. Through controlling the switches SW_{on2} - SW_{onn} and SW_{off2} - SW_{offn}, the amount of gate resistors connected in the gate loop can be changed and the total gate resistance can be adjusted. Generally, a high gate resistance is utilized during the Miller plateau period and a low gate resistance is utilized before and after the Miller plateau to shorten the transient delay duration. This method requires additional gate resistors and BJTs to provide more adjustable steps.

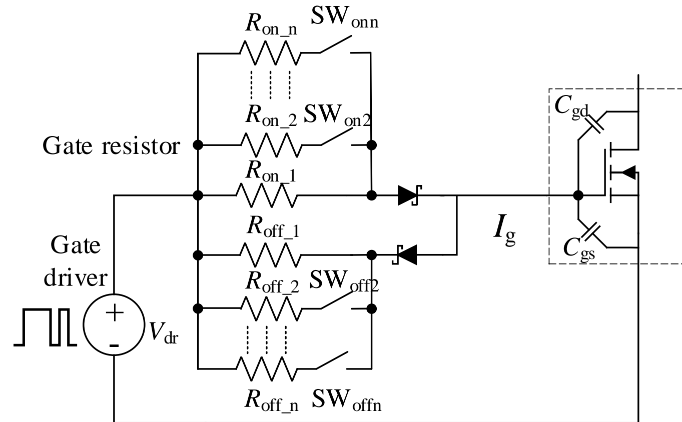

Figure 1-16 A typical circuitry of variable gate resistance method.

1.3.3 Variable input capacitance method

The variable input capacitance method adjusts the C_{iss} to control the switching slew rate, and its basic working principle is illustrated in Figure 1-17. In general, it can be implemented by adding an external capacitance in parallel with the Miller capacitor or gate-source capacitor C_{gs}, and as a result the charging speed can be adjusted. The performance of this method has been verified in [1.25], and [1.45]-[1.46].

Adding an external capacitor in parallel with C_{gs} is the most commonly used method. Another method uses an external capacitor connected in parallel with C_{gd} [1.25]. However, this method requires a high voltage capacitor to connect between gate and drain.

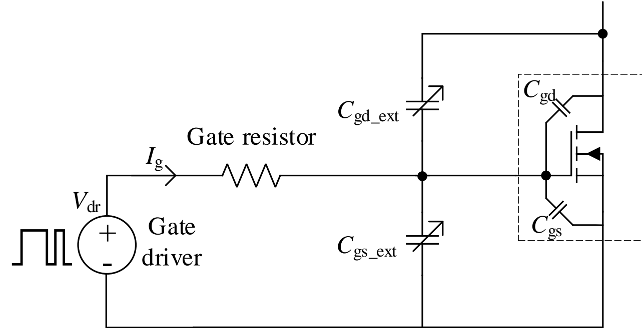

Figure 1-17 Different variable input capacitance methods.

1.3.4 Variable gate current method

Variable gate current method typically utilizes a current source gate driver. By adjusting the gate current, the switching speed can be controlled. Its feasibility for controlling the switching slew rate has been validated in [1.47] – [1.48], [1.61]. Additionally, [1.49] argues that the current source gate driver has a better gate loop oscillation damping capability. There are some commercialized current source gate drivers on the market already, such as the Infineon 1EDS20T12SV gate driver. The benefit of the current source gate driver is its constant *dv/dt* [1.49]. In other words, the current source gate driver can maintain the *dv/dt* of the power devices switching constant. This is because of the constant charging current on the input capacitor C_{iss}. Consequently, the increasing slew rate of V_{gs} is stable. However, the problem of the current source gate driver is the oscillation. The unmatched parameters will cause the oscillation in the gate current loop, thus result in fault turn-on [1.50]. In [1.49], the comparison of the current source gate driver and the voltage gate driver are given. An active current source gate driver is proposed in [1.51] to adjust

the switching speed of the power devices in a parallel/series-connected switch. The working principal is described in Figure 1-18.

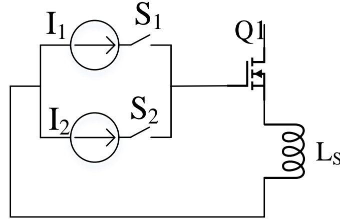

Figure 1-18 The working principal of an active current source gate driver.

In Figure 1-18, S1 and S2 will close at the switching transient delay duration, thus, there will be higher current charging on the C_{iss}. During the Miller plateau period, low current will charge the C_{iss}. [1.51] introduces a kind of AGD which uses a current mirror circuit to adjust the gate current. This proposed method will have lower *dv/dt* and *di/dt*, and thus reduces the risk of oscillation on the gate current route.

1.3.5 Variable gate voltage method

The variable gate voltage method can adjust the gate voltage during the switching transient to control the trajectory. It has gained attention since it is relatively easier to implement and closely related to conventional gate drive methods. The advantage of this method over the variable resistance method is the flexibility since the voltage level is easier to control. In addition, since the most prevalent shoot-through protection method is the desaturation protection which is also multi-level turn-off , this AGD method is easy to develop protection without adding any additional circuitry[1.36]. Different topologies for the variable gate voltage AGD methods are proposed in [1.52]-[1.54].

There are a couple of commercialized variable gate voltage method based AGD products on the market. Figure 1-19 shows the AgileSwitch Augmented Turn-off Gate Driver [1.55].

Figure 1-19 The AgileSwitch 62 mm series gate driver board.

Compared with the conventional gate driver, the AgileSwitch 62mm series gate driver board provides an internal voltage level for soft turn-off. However, this gate driver has a microcontroller for generating the output voltage level. To optimize the switching performance, the current feedback is sent to the microcontroller and the microcontroller will adjust the output voltage according to the operation condition.

1.3.6 Feedback intelligent active gate driver

A typical offline adjustment is as shown in Figure 1-20 (a). The offline adjustable method usually utilizes a constant intermediate level and duration for all operation conditions. This intermediate level is the intermediate voltage for variable gate voltage method or intermediate current for variable gate current method. Therefore, the offline methods are not adaptive.

Some offline AGDs are introduced in [1.41] and [1.46]. These approaches are cost effective and easy to implement [1.27]. However, they cannot optimize the performance of the power device, since the load current and bus voltage will influence the switching performance. In other words, even for the same power device, the performance indicators such as the *dv/dt*, *di/dt*, and the energy losses may be different under different operation conditions [1.56]. Thus, adaptive adjustment is necessary to optimize over operation conditions. [1.27], [1.44], [1.51], and [1.57] introduce several

types of adaptive AGD methods. Most of the adaptive AGDs utilize an inductor to measure the *di/dt* and an external capacitor connected across the gate-drain terminals to measure the *dv/dt*. [1.27] uses the analog PI controller to optimize the slew rate. A typical block diagram is as shown in Figure 1-20 (b).

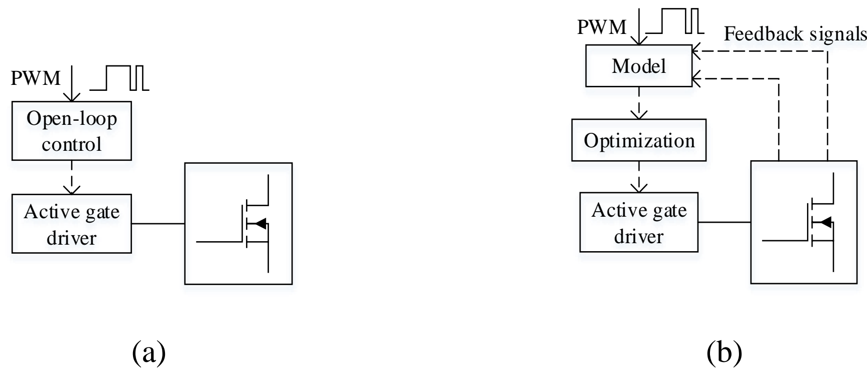

Figure 1-20 The comparison of online and offline active gating methods. (a) The offline method. (b) The online/adaptive method.

Figure 1-20 (b) describes the online/adaptive active gating method. The adaptive method requires feedback signals which could be drain-source voltage, drain current, or dc bus voltage. The microcontroller will input the feedback signals into the model and calculate the performance parameters. The optimization algorithm will generate the optimal intermediate voltage and control the active gate driver. Due to the presence of the predictive model and optimization, each switching cycle can be controlled. Compared with the offline active gating methods, the adaptive method will improve the EMI noise and energy losses of the power device.

1.3.7 Conclusions of the AGD studies

The aforementioned sections introduce four kinds of AGD methods. The summary of the comparisons is given in Figure 1-21.

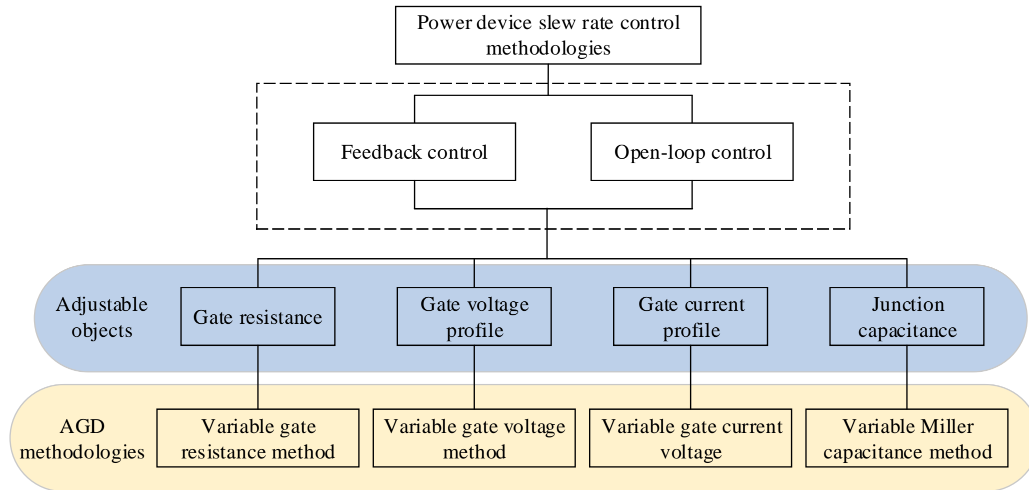

Figure 1-21 The classification of various AGD methodologies.

According to the control strategy, the state-of-the-art AGD methods can also be categorized into two major kinds: feedback control and open-loop control. The open-loop control can indeed reduce the EMI noise. However, due to the lack of feedback signals, it cannot adjust the output of the gate driver according to the operation conditions. Feedback control requires the feedback signals such as *dv/dt*, *di/dt*, bus voltage, and load current. It requires a high-speed processor to realize on-line calculation and optimization. The feedback control strategy can be realized with analog circuit or digital processor with model-predictive control.

1.4 Research of 10 kV SiC power devices

1.4.1 The applications of high voltage SiC power devices

As mentioned in Section 1.1.2, the application of 10 kV SiC power MOSFET can reduce the cascade level of the power converter, thus reduce the complexity of the whole system. This benefit enables them to be competitive in the future market for distribution system. Several companies are developing the high voltage SiC power devices, such as Wolfspeed and Rohm [1.62]-[1.63]. Wolfspeed 10 kV SiC MOSFETs with the third generation high voltage packaging technology have been sold on the market. There are limited amount of research groups having access to the

10 kV SiC MOSFET, i.e., North Carolina State University, Virginia Tech, University of Alabama, ETH Zurich, University of Tennessee at Knoxville, Ohio State University, Aalborg University, University of Texas at Austin, and KTH Royal Institute of Technology. Their work will be introduced as follows.

Several groups have reported the solid-state transformer using 10 kV SiC MOSFET [1.64] - [1.65]. The voltage total harmonic distortion of the solid-state transformer in [1.65] is much higher than the modular multi-level converter. The reason of this phenomenon is cascade connection can shave some harmonics of the output waveform. Therefore, the 10 kV SiC power MOSFET will be a potential prevalent solution for the ultra-high voltage applications such as 320 kVdc high voltage dc link. [1.66] has clarified the efficiency of high voltage dc transformer can reach 99% with the 10 kV SiC power MOSFET. [1.67]-[1.69] have performed characterization for the Wolfspeed 10 kV SiC MOSFET. However, all of the references above have reported the 10 kV SiC MOSFETs have higher switching slew rate than the 1.2 kV SiC devices. However, the high the high switching *dv/dt* and *di/dt* of 10 kV SiC MOSFET increases the difficulties to design the PCB since the electromagnetic interference (EMI) noise can be more serious. [1.70] have reported that the *dv/dt* may exceed 100 V/ns when using a 5 Ω gate resistor. The high possibility of false-triggering and crosstalk noise brings concern regarding the EMI immunity of the circuit design, especially the gate driver circuit.

1.4.2 The development of gate drivers for high voltage SiC devices

To address the aforementioned EMI noise issues, gate drivers with stronger EMI immunity capability and higher insulation level are necessary. CREE has developed a gate driver for 10 kV MOSFET with their own power supply modules [1.71]. Several groups from academia also reported the development of the conventional gate drivers for the 10 kV SiC MOSFETs in [1.72]

- [1.74], [1.77]. These candidate gate drivers are functional, but they cannot provide slew rate control capability. Since the isolated power supply is significant to the performance of a gate driver, [1.75] proposes a method using high power fiber transceivers as the power supply for gate drivers. The fiber optics are completely galvanic isolated which provides excellent EMI immunity performance. However, the volume of the laser generator are very bulky and pricey. Intelligent gate drivers are proposed in [1.70] for high voltage SiC power devices. The methodology is variable gate resistance AGD. However, this method only has two adjustment steps since only two different gate resistance values are utilized.

1.5 Problem definitions

As clarified in the aforementioned sections, the development of the gate driver is an important need for the commercialization of high voltage SiC power devices. This dissertation will focus on the optimization and design of the gate driver. Specifically, the gate driver aims at controlling the switching speed and balancing the EMI noise against energy losses of the SiC power device. As introduced in Section 1-3, there are different SOA AGD methodologies which can adjust the slew rate of the switching. For a 10 kV SiC power MOSFET, safety and protection are the foremost design consideration. Therefore, the variable gate voltage method is the most appropriate option since it can provide desaturation protection easily without an auxiliary circuit and it is simple to implement.

Other than the aforementioned advantages, variable gate voltage method is a good choice for parallel-connected power devices. The parallel-connected power devices are cost-effective solutions to increase the current rating with several low current rating devices. However, because the parasitics on the power devices are different, the drain current may not distribute evenly on the power device and this will affect the thermal stress significantly. The variable gate voltage method

can adjust the conduction resistance and the slew rate of the transient of the power losses. Thus, it can change both the dynamic and steady state current sharing on the parallel-connected power devices. Based on the analysis above, this is another advantage that leads this work to select the variable gate voltage method.

From the aforementioned information, the switching process should consider the tradeoff between the EMI noise and energy losses. In other words, reducing the energy losses will inevitably increase the EMI noise. Therefore, it is preferred to develop a theoretic model to evaluate the switching trajectory and energy losses.

1.5.1 Switching gate voltage profile selection

There are different variable gate voltage methods such as the S-shape turn-off profile [1.58], and two level (2-L) turn-off. S-shape turn-off profile can fine tune the turn-off process. However, due to the complexity of the S-shape voltage profile generator circuit, which is typically a high bandwidth digital-analog converter, it is not appropriate for this application. A 2-L turn-off AGD is reported in [1.59]. The 2-L AGD has long turn-off delay duration which will increase the deadtime significantly. Based on the analysis, a 3-L turn-off AGD is proposed to balance the EMI noise and the energy losses. The details of the proposed 3-L gate driving profile will be introduced in the next sections.

1.5.2 Hardware design consideration

There are several requirements for the 3-L turn-off AGD: high speed, high bandwidth, high voltage level adjustment resolution, digital control, and high gate current sinking capability [1.60]. Therefore, the circuit should be carefully designed. Typically, a high-speed digital-analog converter (DAC) can adjust the output voltage easily. However, DACs are generally unidirectional

and it does not provide current sinking capability. Thus, only using a DAC is not enough for the 3-L AGD design.

To satisfy these requirements, in this dissertation, a novel circuit for realizing a 3-L turn-off AGD is proposed. Also, the gate driver must have the capability to sink the feedback gate current quickly. Otherwise, it may result in false triggering event. Since most active Miller clamping circuits need additional control signals, a special gate current sinking circuit should be proposed to prevent false triggering.

1.5.3 Model of the SiC power MOSFET switching

As mentioned in the previously, a theoretic model is necessary for the online model-predictive active gate driver. There are several requirements for the theoretic model. The top-priority requirement is the accuracy. The model should be able to predict the slew rate, energy losses, and overshoot voltage accurately. There is no reference introducing the switching behavior of SiC power devices under multi-level turn-off. Therefore, it is significant to investigate the switching behavior and develop a trajectory model to describe the behavior.

Another consideration is the computation load. For the on-line calculation, the computation load of the model should not be too high. An overly-complex model is not possible to be calculated by a local controller in a short time. Therefore, the model development should carefully consider the tradeoff between computation load and the accuracy.

1.6 Outline

Chapter 2 describes the circuit of the proposed AGD circuit and the trajectory model. The working principle of the circuitry is depicted through analyzing the current flow of different substages. The proposed variable gate voltage profile and a trajectory model for the active gate

driver design is introduced. The behavior of SiC power MOSFET under multi-level switching will be analyzed with the proposed trajectory model. Based on the analysis results, the design criterion of the multi-level switching profile is given and the switching trajectory optimization algorithm is demonstrated.

Chapter 3 introduces the hardware realization of the proposed AGD on 1.2 kV SiC MOSFET. Double pulse tests (DPTs) are conducted to verify the functionality of the proposed AGD circuitry. Through analyzing the results of DPTs and compared with the analysis result of the trajectory model, the switching behavior of SiC MOSFET under multi-level turn-off is given. Also, it verifies the feasibility of the propose trajectory model.

Chapter 4 introduces the design of the proposed AGD for 10 kV SiC power MOSFET. Because the datasheet of the 10 kV SiC MOSFET is not available on the website, characterization for the device is conducted first. All the C-V and I-V characteristics are given in this chapter. The hardware realization of the AGD for 10 kV SiC MOSFET is introduced. The DPTs of 10 kV SiC MOSFET with proposed AGD are conducted. The experimental results are analyzed and compared with the trajectory model.

Chapter 5 focuses on the conclusions drawn from this dissertation and presents the outlook of the future work.

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CHAPTER 2

MULTI-LEVEL SWITCHING PROFILE, TRAJECTORY MODEL, AND ANALYSIS

2.1 Circuit and working principles of the active gate driver

2.1.1 Basic circuit schematics

Table 2-1 lists all the variables that are used in this dissertation. As introduced in Chapter 1, the AGD circuitry should be able to adjust the intermediate voltage level digitally. Also, it should provide enough current sinking capability. To meet these requirements, a circuit for the variable driver voltage AGD is proposed as shown in Figure 2-1 [2.21]. It should be noted that the proposed circuit has been introduced in [2.21].

As shown in Figure 2-1, the proposed AGD system comprises four major sections: a voltage selector, a local controller, an adjustable voltage regulator, and a current sinking circuit. The local controller receives the pulse width modulation (PWM) signal as well as the feedback signals of V_{BUS} and I_{O} from the upper level main control unit. The local controller is generally a very high-speed processor such as an FPGA or CPLD. The local controller can calculate the optimal intermediate voltage and corresponding duration of each substage based on the feedback signals. It should be noted that the feedback signals are V_{BUS} and I_{O}. Because these two signals are generally measured by the converter sensors for control, the AGD need no extra sensors. Compared with the gate driver proposed in [1.27], this proposed multi-level AGD does not need high bandwidth sensors for measuring V_{ds} and I_{ds}. With the optimization results, the local controller can control the adjustable voltage regulator and the voltage selector to generate the optimal V_{dr} profile. For a power MOSFET, the gate charge will return to the gate driver, i.e., the adjustable voltage regulator, during the turn-off process. Since the voltage regulator is an op-amp circuit may has limited current sinking capability. Failing to sink the gate current may cause a false trigger event. Therefore, a

current sinking circuit can effectively reduce the risk of false triggering event caused by the reversed flowing gate current.

Table 2-1 Definitions of the variables.

Part	Variable	Definition
Power MOSFET	C_{gs}	Gate to source capacitance
	C_{gd}	Gate to drain capacitance (Miller capacitance)
	C_{ds}	Drain to source capacitance
	C_{iss}	Input capacitance, usually equals to C_{gd}+C_{gs}
	g_{fs}	Transconductance
	k_{p}	Saturation current transconductance factor in A/V^2
	L_{s}	Equivalent parasitic inductances on the source side
	L_{d}	Equivalent parasitic inductances on the drain side
	R_{g_int}	Internal gate resistance
	V_{ds}	Drain to source voltage
	V_{th}	Threshold voltage
	I_{ds}	Drain to source current
	I_{sat}	Drain to source current under saturation condition
	R_{ds_on}	Drain-source on-state resistance
	V_{on}	Conduction drain-source voltage
	$V_{miller1}$	Miller plateau voltage
	ϕ_{0}	Gate junction potential parameter
Gate driver	R_{g}	Gate driver resistor
	R_{g_off}	Gate driver resistor for speeding up turn-off process
	V_{dr}	Output voltage
	V_{int}	Intermediate driver voltage
	V_{dr_on}	Normal turn-on voltage (+20V for most SiC power MOSFETs)
	V_{dr_off}	Normal turn-off voltage (-5V for most SiC power MOSFETs)
	V_{f_on}	Faster turn-on voltage (Higher than V_{dr_on})
	t_{int}	Duration of the V_{int}
	t_{delay}	Turn-on/off delay duration of the power device
	V_{BE_on}	Threshold base-to-emitter voltage of the BJT Q1
Diode	C_{d}	Parasitic junction capacitance
Load inductor	L	Inductance
	C_{L}	Winding parasitic capacitance
	I_{O}	Load current
Dc power supply	V_{BUS}	Dc bus voltage

The proposed AGD circuitry has five operation modes: normal turn-on, slower turn-on, faster turn-on, normal turn-off, and slower turn-off mode. The normal turn-on/off modes have two stages of driver voltage which make them same as the conventional gate driver. The faster turn-on and slower turn-on/off modes can adjust the switching speed actively. Through utilizing different modes for turn-on and turn-off, the proposed AGD can provide 3×2=6 switching modes. The working principle of the proposed AGD circuitry will be introduced in detail in the following sections.

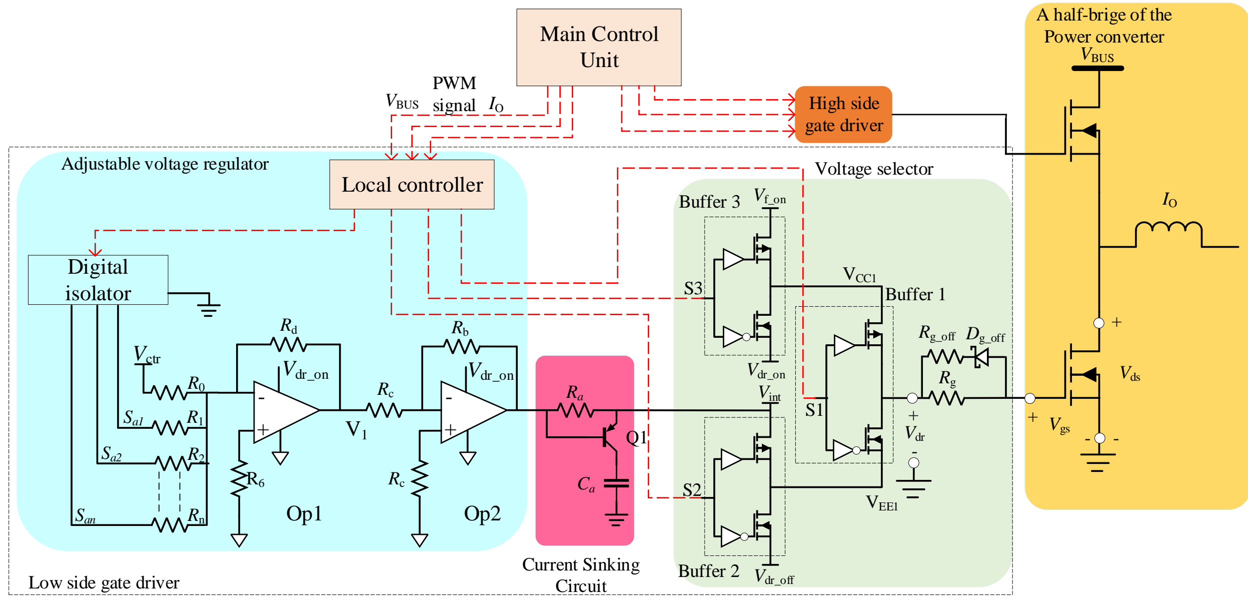

Figure 2-1 The circuit schematics of the proposed active driving system.

2.1.2 The working principle of the adjustable voltage regulator

V_{int} is generated by the adjustable voltage regulator. Through changing its level, the switching transient speed can be adjusted. It includes an analog adder circuit to adjust the voltage level and a voltage amplifier to boost the maximum output current and amplify the voltage level. Through changing the connection of input impedance, the local controller can control the analog adder circuit to adjust the output voltage level. If there are *n* resistors connecting between the input side of the Op1 and the output side of the digital isolator, the adjustable voltage regulator can provide

2^n voltage adjustment steps. For example, a 5-channel digital isolator with five different resistor values can provide 32 adjustment steps. The voltage amplifier's output voltage can be calculated with Eq. (2-1).

$$V_{\mathrm{int}} = V_{\mathrm{ctr}}\left(\frac{1}{R_0} + \frac{S_{a1}}{R_1} + \frac{S_{a2}}{R_2} \cdots \frac{S_{an}}{R_n}\right) R_{\mathrm{d}} \frac{R_{\mathrm{b}}}{R_{\mathrm{c}}} \tag{2-1}$$

In Eq. (2-1), R_0 is used to provide the fundamental bias voltage. In other words, R_0 will provide the lower limit of voltage adjustment. V_{ctr} is the voltage of the digital isolator power supply. S_{a1}-S_{an} are the control signals from the local controller. R_1-R_n are the resistors connected between the local controller and the input side of the digital adder circuit. Through adjusting the total resistance in the circuit, V_{int} can be changed. Their values are denoted by Eq. (2-2).

$$R_1 = 2^1 R_2 = 2^2 R_3 = 2^{n-1} R_n \tag{2-2}$$

As mentioned in Chapter 1, this increased amount of control regarding the voltage levels can allow for more design freedom. Compared with the other methodologies, such as the variable gate resistance method, the proposed AGD has much higher voltage adjustment resolution.

2.1.3 The working principle of the current sinking circuit

The gate current sinking auxiliary circuit is used to reduce the risk of false triggering event probability which is caused by the high reversed flowing gate current. Its working principle is depicted in Figure 2-2 [2.1].

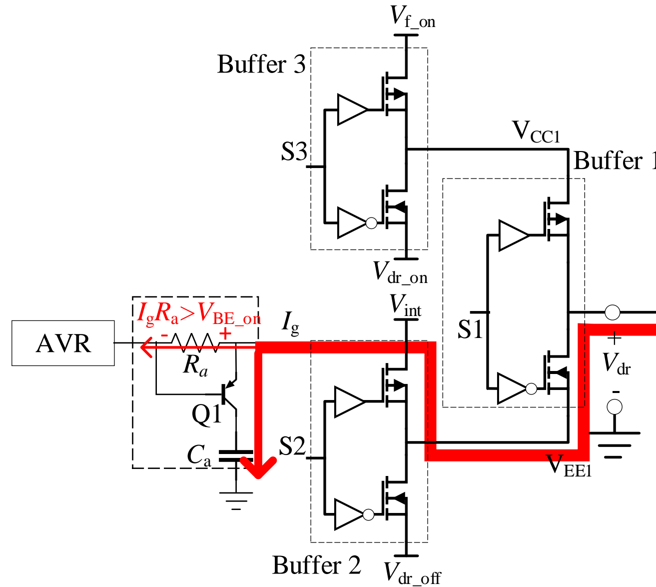

Figure 2-2 The working principle of the current sinking circuit.

During the turn-off switching transient, I_g flows reversely from C_{iss} to the adjustable voltage regulator to reduce V_{gs}. As mentioned above, to increase the gate current sinking capability of the adjustable voltage regulator, the current sinking circuit is adopted. The current sinking capability of the voltage regulator is limited since it is formed with op-amps. Some op-amps, such as the totem pole structure op-amps, have the same maximum sinking current with the maximum sourcing current. However, since the current sinking capability of the op-amps is still limited and the peak reversed gate current can reach over 9 Amperes in some conditions, it is still necessary to use the current sinking circuit at the output side of adjustable voltage regulator.

The current sinking circuit consists of a PNP BJT Q1, a capacitor C_a for isolating the negative biased gate voltage, and a resistor R_a. When I_g flows on R_a, it generates a voltage denoted by $I_g R_a$. When $I_g R_a$ is higher than the threshold base-to-emitter voltage of Q1, as shown in Eq. (2-3), Q1 turns on and I_g will flow into C_a but not the op-amp. In this way, the false-triggering event is prevented. C_a should be a low parasitic inductance capacitor which has enough capacitance to sink

all the gate charge of the MOSFET and still maintain the voltage. However, a large capacitor is generally bulky in size. Therefore, the design of C_a should trade the value over size.

$$I_g R_a \geq V_{BE_on} \tag{2-3}$$

In Eq. (2-3), V_{BE_on} is the base-to-emitter threshold voltage of Q1.

2.1.4 The working principle of the voltage selector

Because the switching transient is typically at the nanosecond level, the generic digital-to-analog circuit is not able to be used to generate the turn-off voltage profile. The voltage selector, which is formed with three cascade-connected gate driver buffers, i.e., Buffer1-3, is utilized to generate the proposed multi-level driver voltage profile. Buffer1's output pole is connected to the gate of the power MOSFET. The gate signal of Buffer1 is the same with the PWM signal. Buffer3 is used for turning on the power device. Its negative pole is connected to V_{dr_on} and the positive pole is connected to a higher voltage V_{f_on} which is used to speed up the turn-on process. The V_{dr_on} of most SiC power MOSFETs is +20 V. The positive input pole of Buffer1 is connected with the output of Buffer3.

Buffer 2 serves to slow down the switching transient. Its output side is connected with the negative pole of Buffer 1. The positive pole of Buffer2 is connected to V_{int} which is regulated by the adjustable voltage regulator. The negative pole of Buffer2 is connected to V_{dr_off} which is typically -5 V for most SiC power MOSFETs. Through controlling the signals of S1, S2, and S3, the voltage selector can output the driver voltage V_{dr} profile for switching which is calculated by the local controller optimization algorithm. How the voltage selector generates the five operation modes will be illustrated in the following sections.

2.1.5 Slower turn-on mode of the voltage selector

Slower turn-on mode adopts V_{int}, which is typically a value between $V_{miller1}$ and V_{dr_on}, to slow down the turn-on process. Because V_{int} is lower than V_{dr_on}, C_{iss} is charged with lower gate current, and thus the turn-on speed is reduced. The different stages of the slower turn-on mode are introduced in the forms of current routes figures as shown in Figure 2-3.

Stage I. It is the normal turn-off stage before the rising edge of the PWM signal. In this stage, S1-S3 are all at low level to ensure that V_{dr} equals to V_{dr_off}.

Stage II. This stage is the turn-on delay duration and it occurs after the local controller receives the rising edge of PWM signal. During this period, through pulling up S1, V_{dr} increases to V_{dr_on} and V_{gs} increases from V_{dr_off} to V_{th}. Because this stage does not generate high EMI noise, its duration can be shortened to reduce the total duration of the turn-on process.

Stage III. This stage occurs after the end of the turn-on delay stage. In this substage, V_{ds} is decreasing to V_{ds_on} and I_{ds} is increasing to I_O. S1 remains at the low level and S2 switches to high level. In this case, V_{dr} decreases from V_{dr_on} to V_{int} which is the optimal value to trade the EMI noise against the switching losses. Because V_{int} is lower than V_{dr_on} and higher than $V_{miller1}$, the turn-on process is slowed down. It should be noted that V_{int} must be higher than $V_{miller1}$. Otherwise, the AGD cannot completely turn on the power MOSFET.

Stage IV. This stage occurs after the power MOSFET turns on completely. V_{ds} decreases to V_{ds_on} and the current rises to load current I_O. V_{gs} will increase to V_{dr_on} to completely open the channel. Buffer1 is pulled up to high level and V_{dr} increases to V_{dr_on} to reduce R_{ds_on}.

The normal turn-on mode will only include Stage I and II.

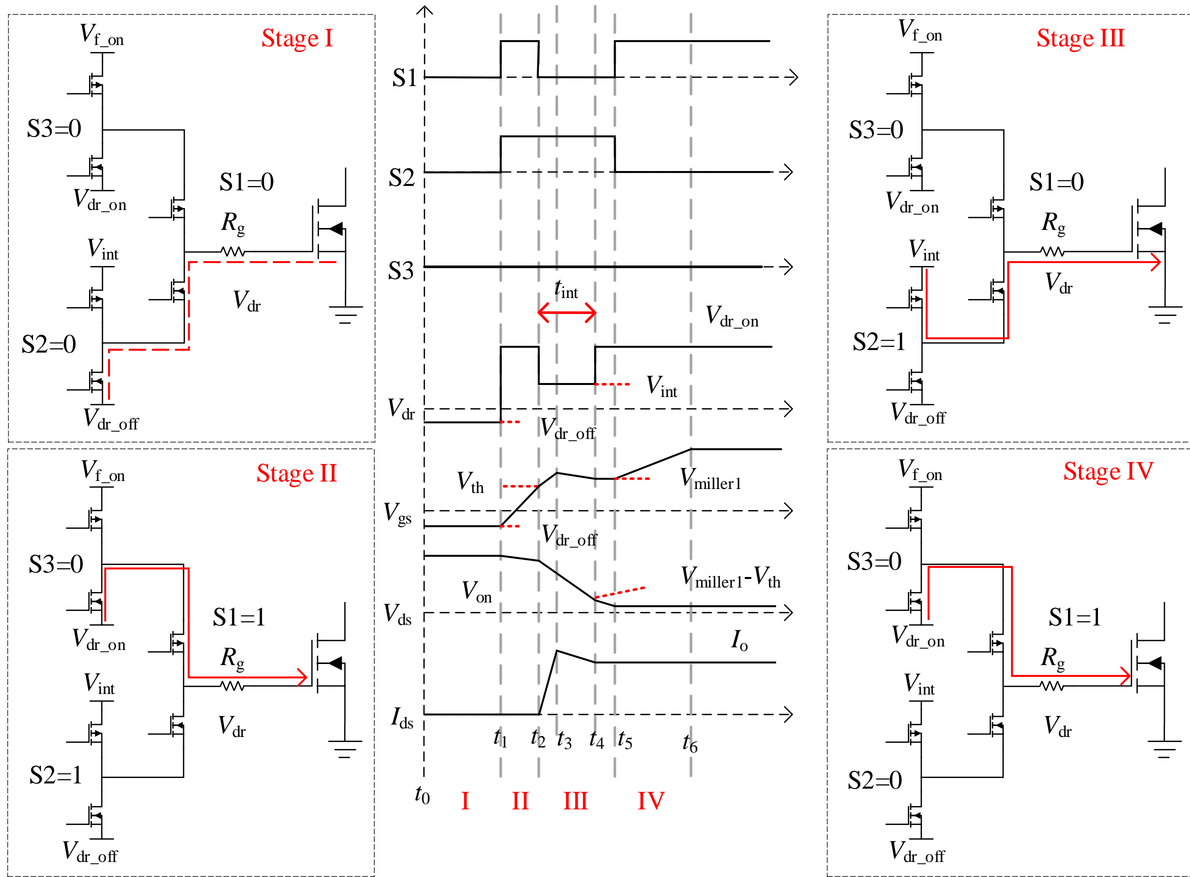

Figure 2-3 The current flow of the slower turn-on process.

2.1.6 *Faster turn-on mode of the voltage selector*

The turn-on process can be sped up through using the faster turn-on mode. In this mode, the energy losses can be reduced while it increases EMI noise inevitably. Therefore, it is appropriate for the scenario that the parasitics of the power converter PCB are low. Also, for the soft switching condition, the turn-on loss is on the body diode and it cannot be controlled by the gate driver. Therefore, faster turn-on mode is appropriate for soft switching as well.

As shown in Figure 2-4, the faster turn-on process can be demonstrated through analyzing current route of different stages. V_{f_on} is higher than V_{dr_on} and it is used to turn on the device with higher speed. For most SiC power MOSFETs, the range of V_{f_on} is between +25 V and V_{dr_on} [2.2].

Since V_{f_on} is higher than V_{dr_on}, it allows the junction to be charged in a higher speed than the conventional turn-on mode and thus speed up the turn-on process.

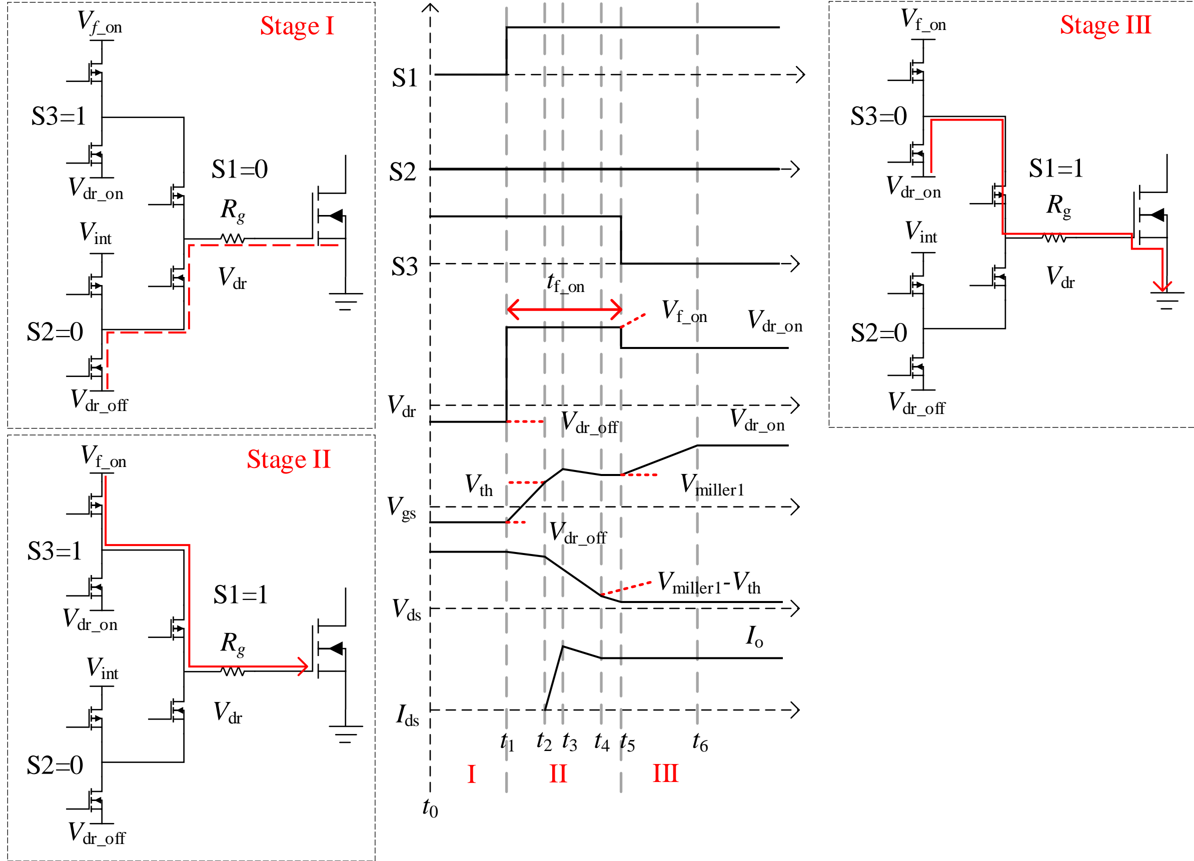

Figure 2-4 The current flow of the faster turn-on process.

Stage I. This stage occurs before the rising edge of PWM signal and the power MOSFET is switched off. Similar with the slower turn-on mode, S1 and S2 are set to low level and V_{dr} is V_{dr_off}. S3 remains at high level to prepare for turn on the device in higher speed.

Stage II. When the local controller detects the rising edge of PWM, the AGD starts to turn on the power MOSFET. S1 changes to high level and V_{dr} increases from V_{dr_off} to V_{f_on}. With the higher driver voltage V_{f_on}, the turn-on can be sped up compared with the normal turn-on mode. The duration of this stage covers the V_{ds} falling period and I_{ds} rising period.

Stage III. After V_{ds} reduces to V_{ds_on} and I_{ds} increases to I_O, S3 switches to low level and V_{dr_on} is selected to be V_{dr}. V_{dr_on} is recommended for the driving the MOSFET in continuous conduction. V_{f_on} cannot be used for continuous conduction because higher V_{dr} results in I_{sat} and thus makes the shoot-through current higher and more catastrophic under [2.2]-[2.3]. Moreover, V_{dr_on} is recommended by the manufacturer since it considers the balance of the lifetime and efficiency. V_{f_on} for normal conduction causes faster degradation of the power devices.

2.1.7 Slower turn-off mode of the voltage selector

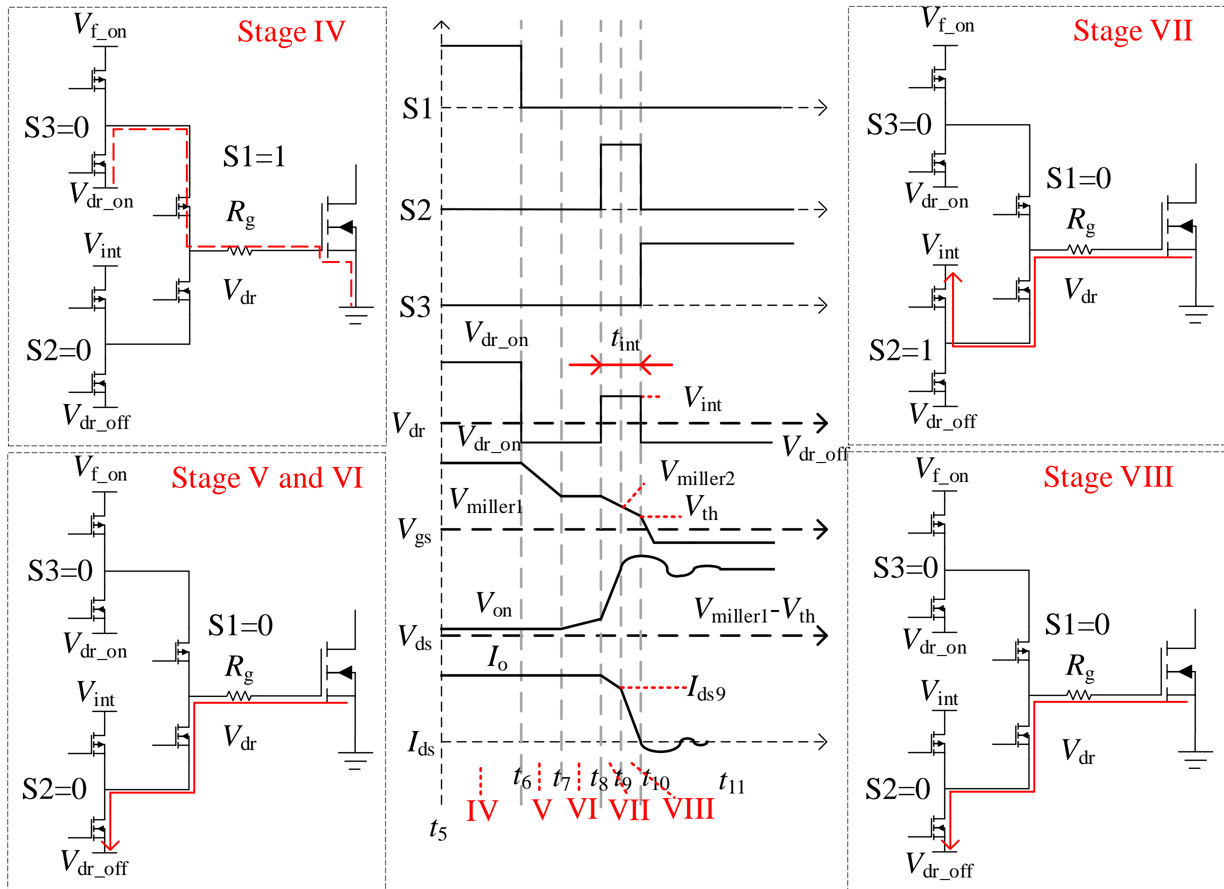

Figure 2-5 The current flow of the slower turn-off process.

When the EMI noise is too high, AGD can use slower turn-off to slow down the switching process and prevent the false-triggering event. In Figure 2-5, the working principle of the slower turn-of process is introduced in details through analyzing different stages of the current.

Stage IV. This stage occurs before the power MOSFET turns off. The power MOSFET is still conducting. S1 is at high level. S2 and S3 remain at low level and V_{dr} is V_{dr_on}.

Stage V. When the local controller receives falling edge of the PWM signal, the AGD starts to shut down the power MOSFET. This stage comes first and it only covers the turn-off delay period. For the reason that speeding up this process does not increase the EMI noise dramatically, this period is preferred to be shortened through changing V_{dr} to V_{dr_off}. Both the S1 and S2 are pulled down to low level.

Stage VI. After the turn-off delay ends, V_{ds} starts to increase and I_{ds} starts to decrease. This stage generates high EMI noise and overshoot voltage on V_{ds}. To suppress the EMI noise and V_{ds} overshoot, a higher V_{dr}, i.e. V_{int}, is utilized to slow down the turn-off process. In this stage, S2 changes to high level and V_{dr} switches to V_{int}. Through using different levels of V_{int}, the turn-off process can be slowed down to a desired level.

Stage VII. After the power MOSFET turns off, V_{dr} should decreases to V_{dr_off} for normally shut down the devices. Since V_{dr_off} is negative biased voltage, it can effectively prevent a false triggering event. In this stage, S1 remains at the low level and S2 is pulled down to V_{dr_off}.

It should be noted that if only stage IV and V are performed, the AGD will be in normal turn-off mode.

2.2 The switching trajectory model of SiC MOSFET

The working principle of the proposed AGD circuitry has been introduced in the Section 2.1. It will be helpful to understand the switching behavior of the SiC MOSFET under multi-level switching and quantify the switching performance. In this section, the switching trajectory model of SiC power MOSFET will be analyzed. The model will be utilized to design the turn-on/off gate driver voltage profile. All the switching periods will be introduced through depicting each stage of the switching transient process. It should be noted that the switching behavior of turn-on process is similar to the turn-off process. Therefore, only the switching behavior of SiC MOSFET under turn-off will be introduced. It is not necessary to repeat the same analysis on the turn-on process. The analysis results can be utilized for the optimization algorithm which will be introduced in the next section.

2.2.1 The concept of the on-line model-based feedback control

As introduced in Chapter 1, the feedback control is necessary. Some references use the analog proportional integral differential (PID) controller to realize the compensation for the slew rate control. The high speed of the analog controller enables it to be a good choice for the switching behavior control. However, the analog PID controller requires sophisticated design consideration. Also, its accuracy is determined by the bandwidth. The PID parameters cannot be changed actively when all the passive components are integrated on the PCB [2.4]. To address these issues, this dissertation adopts the on-line model-based feedback control. The model-based feedback control is different from the PID controller. It has the model inside the local controller to predict the behavior indices, such as the energy losses, *dv/dt*, *di/dt*, and the total turn-off duration of next switching cycle. Based on the prediction results, the local controller will select the optimal operation point for next switching cycle [2.5][2.6].

As introduced in the aforementioned sections, the trajectory model for on-line optimization should have enough accuracy for the prediction while the computation load should be reduced for the on-line computation. The trajectory model of SiC MOSFET for on-line optimization has not been reported in the previous references. In this section, the comprehensive literature investigation is conducted first.

[2.7] depicts the behavior of GaN transistors driven by an active gate driver. The turn-off process under different V_{int} levels is illustrated. However, the influence of V_{int} level on the slew rate is not quantitatively investigated in [2.7]. A mathematic model for evaluating the energy losses of the SiC power MOSFET is introduced in [2.8]. The proposed model considers the variation of C_{gd} with V_{ds}. The accuracy of this model is enough for switching behavior prediction. Nonetheless, since this model contains some high order equations, it is difficult to finish the calculation within a switching cycle which is generally microsecond level. Moreover, this model only considers the conventional turn-off. A mathematic model for predicting the power MOSFETs switching trajectory is described in [2.9]. It is over-complex since it considers all the possible parasitic inductors on the circuit. These details dramatically increase the order of the equation and make it difficult to solve. [2.10] theoretically compares three types of AGD for IGBTs. An analytical model for the IGBT turn-on process is also proposed and analyzed. However, the model of [2.10] is specifically for Si IGBT. It ignores the turn-off process which is also important for the SiC investigation.

As introduced in the last section, it is necessary to develop a trajectory model for SiC MOSFET to quantitatively analyze how V_{int} affecting the performance of the proposed AGD. With the trajectory model, the AGD can realize the model-based trajectory control strategy. The working principle is given in Figure 2-6.

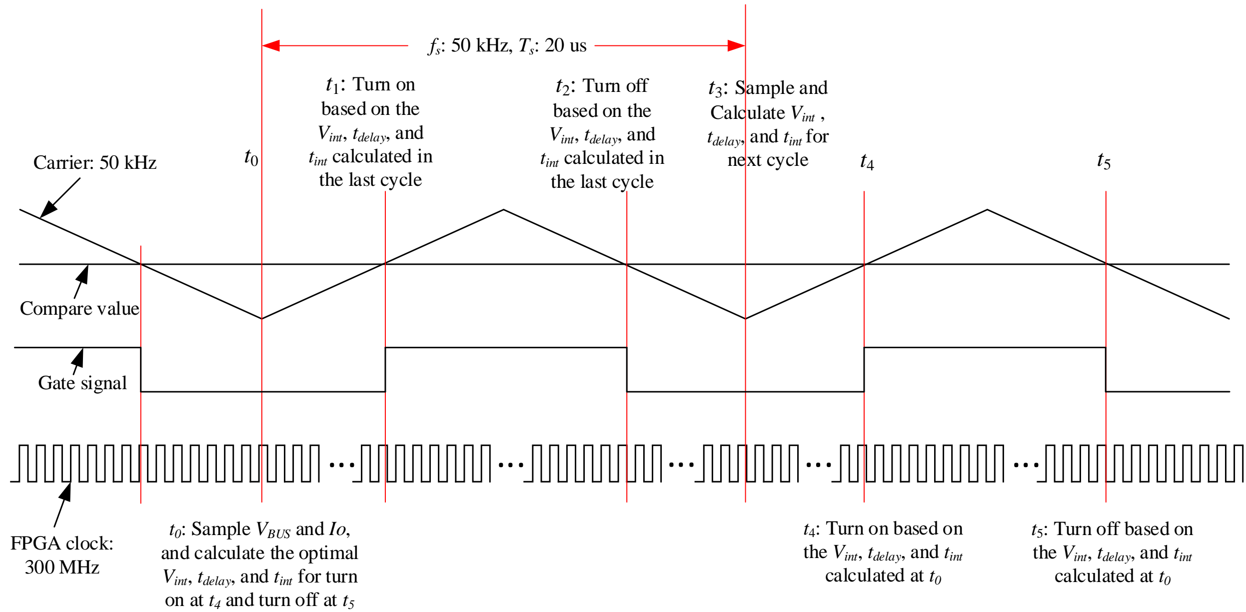

Figure 2-6 The processing flow of the controllers of active gate driver.

As shown in Figure 2-6, the local controller receives the feedback signals, such as V_{BUS} and I_{O}, in a cycle before the switching. For example, in Figure 2-6, t_0 is the start point of this switching cycle and t_3 is the start point of next switching cycle. At t_0, the local controller will calculate the switching features, such as *dv/dt*, *di/dt*, and energy losses, of next cycle (t_3-t_5). Since the load current does not change a lot in a switching period, the predicted results based on the feedback signal at time t_0 will be close to the actual values at t_3. Then the optimized V_{int} and corresponding duration of each substage of next switching cycle can be calculated with the prediction results. With the computation results, it will optimize the switching trajectory for the next cycle.

The following sections will introduce how to calculate the duration of each substage, *dv/dt*, *di/dt*, and energy losses with the trajectory model. It should be noted that the V_{int} for turn-on and turn-off are both generated by adjustable voltage regulator, but the values are different.

2.2.2 Turn-on process

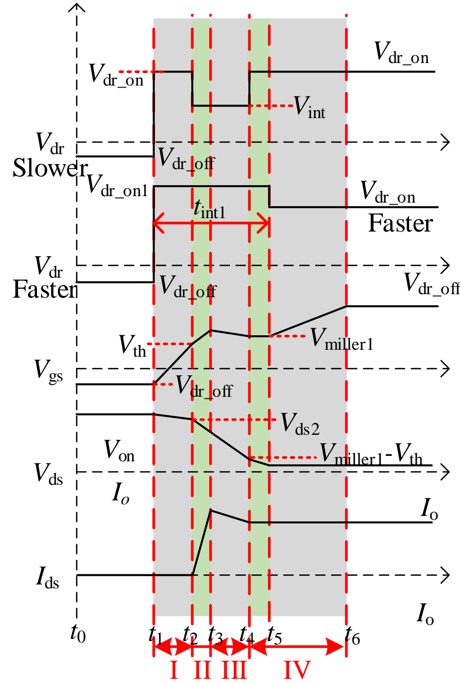

Figure 2-7 The waveform of turn-on process.

The driver voltage V_{dr} of faster turn-on mode and slower turn-on mode is different. However, since they are all turn-on process of power MOSFET, these two conditions can be analyzed with a same trajectory model. The waveform of turn-on process is shown in Figure 2-7. The first curve is V_{dr} of slower turn-on mode and the second curve is V_{dr} of faster turn-on mode.

2.2.2.1 ***Stage I (t_1 - t_2) - The turn-on delay***

In this stage, junction capacitances C_{gs} and C_{gd} begin to charge through R_g. Herein, R_g=R_{g_ext} + R_{g_int}. V_{gs} increases from V_{dr_off} to threshold voltage V_{th}. V_{ds} and I_{ds} do not change in this substage. t_{delay} can be calculated with Eq. (2-4)[2.11].

$$t_{delay} = t_2 - t_1 = R_g C_{iss} \ln\left(\frac{V_{dr} - V_{dr_off}}{V_{dr} - V_{th}}\right) \tag{2-4}$$

In Eq. (2-4), V_{dr} is selected as V_{dr_on} for the slower turn-on mode and V_{f_on} for the faster turn-on

mode. From Eq. (2-4), V_{dr} is preferred to be a high value since the EMI noise is low in this process. It should be noted that the C_{iss} in Eq. (2-4) is the value when V_{ds} is high.

2.2.2.2 ***Stage II ($t_2 - t_3$) – Current rising period***

In this stage, I_{ds} will increase from zero to load current I_O. It should be noted that the current overshoot also happens in this substage. However, the current peak is determined by the reverse recovery current of the anti-parallel diode of the complimentary switch. The drain current can be calculated with Eq. (2-5) [2.12].

$$I_{ds}(t) = g_{fs}\left[V_{gs}(t) - V_{th}\right] \tag{2-5}$$

The duration time of this period can be calculated with Eq. (2-6).

$$t_3 - t_2 = \frac{C_{iss}\left(V_{miller1} - V_{th}\right)}{I_{g2}} = \frac{I_O C_{iss}}{g_{fs} I_{g2}}, \tag{2-6}$$

where I_{g2} is the average gate current in this substage and $V_{miller1}$ is the first Miller plateau voltage which can be calculated with Eq. (2-7) [2.12].

$$V_{miller1} = V_{th} + I_O / g_{fs} \tag{2-7}$$

With the aforementioned equations, I_{g2} can be calculated with Eq. (2-8) [2.12].

$$I_{g2} = \frac{V_{dr} - 0.5V_{th} - 0.5V_{miller1} - L_s I_O / \left(t_3 - t_2\right)}{R_g} \tag{2-8}$$

Combining Eq. (2-6) and Eq. (2-8), the duration time of this substage can be calculated as shown in Eq. (2-9).

$$t_3 - t_2 = \frac{C_{iss} R_g I_O + L_s g_{fs} I_O}{g_{fs}\left(V_{dr} - 0.5V_{th} - 0.5V_{miller1}\right)} \tag{2-9}$$

V_{dr} is selected as V_{dr_on} for the slower turn-on mode and V_{f_on} for the faster turn-on mode. Accordingly, *di/dt* of this period can be calculated with Eq. (2-10).

$$di/dt = \frac{g_{\mathrm{fs}}\left(V_{\mathrm{dr}} - 0.5V_{\mathrm{th}} - 0.5V_{\mathrm{miller1}}\right)}{C_{\mathrm{iss}}R_{\mathrm{g}} + L_{\mathrm{s}}g_{\mathrm{fs}}} \tag{2-10}$$

Due to the voltage drop on the stray inductance L_s, V_{ds} decreases from V_{BUS} to V_{ds2} at t_2. V_{ds2} can be calculated with (2-11).

$$V_{\mathrm{ds2}} = V_{\mathrm{BUS}} - L_{\mathrm{s}}di/dt \tag{2-11}$$

The energy losses of this substage, E_{IR} of this substage, can be calculated with Eq.(2-12).

$$E_{\mathrm{IR}} = \frac{I_{\mathrm{O}}\left(t_3 - t_2\right)\left(V_{\mathrm{BUS}} + 2V_{\mathrm{ds2}}\right)}{6} \tag{2-12}$$

2.2.2.3 ***Stage III ($t_3 - t_4$) – Voltage falling period***

In this period, V_{ds} decreases from V_{BUS} to normal conduction voltage V_{on}. I_{ds} equals to I_O constantly in this period. This period is within the Miller plateau period. Due to the non-linear characteristic of C_{gd}, its influence on *dv/dt* should not be neglected. The value of C_{gd} is variant during this stage and it varies with V_{ds} [2.13]. It can be evaluated with $C_{\mathrm{gd}} = \frac{C_{\mathrm{gd0}}}{\sqrt{1 + V_{\mathrm{ds}}/\phi_0}}$, where ϕ_0 is the gate junction potential parameter and C_{gd0} is the value of C_{gd} when V_{ds} = 0 V [2.14]. *dv/dt* can be roughly calculated with Eq. (2-16).

$$\frac{dV_{\mathrm{ds}}}{dt} = -\frac{I_{\mathrm{g4}}}{C_{\mathrm{gd}}} = -\frac{V_{\mathrm{dr}} - V_{\mathrm{miller1}}}{2R_{\mathrm{g}}\frac{C_{\mathrm{gd0}}}{\sqrt{1 + V_{\mathrm{ds}}/\phi_0}}} \tag{2-13}$$

I_{g4} is the average gate current in this substage and it can be calculated with Eq. (2-14)

$$\int \frac{2R_{\mathrm{g}}C_{\mathrm{gd0}}}{\sqrt{1 + V_{\mathrm{ds}}/\phi_0}}dV_{\mathrm{ds}} = \int \left(V_{\mathrm{miller1}} - V_{\mathrm{dr}}\right)dt \tag{2-14}$$

Solving Eq. (2-14) with the initial conditions: $V_{ds}|_{t=0} = V_{ds2}$ and substituting $t_{VF} = t$ (V_{ds}=0) into Eq. (2-14), the duration of this stage t_{VF}, i.e., the fall time of V_{ds}, can be evaluated with Eq. (2-15).

$$t_{\mathrm{VF}} = \frac{4R_{\mathrm{g}}\phi_0 C_{\mathrm{gd0}} V_{\mathrm{BUS}} \left(\sqrt{V_{\mathrm{ds2}}/\phi_0 + 1} - 1\right)}{(V_{\mathrm{dr}} - V_{\mathrm{miller1}})} \tag{2-15}$$

With Eq. (2-15), average value of *dv/dt* can be easily obtained as shown in Eq. (2-16).

$$dv/dt = \frac{V_{\mathrm{BUS}}(V_{\mathrm{dr}} - V_{\mathrm{miller1}})}{4R_{\mathrm{g}}\phi_0 C_{\mathrm{gd0}} \left(\sqrt{V_{\mathrm{ds2}}/\phi_0 + 1} - 1\right)} \tag{2-16}$$

The energy losses in this substage can be calculated with Eq. (2-17).

$$E_{\mathrm{VF}} = \frac{V_{\mathrm{ds2}} I_{\mathrm{O}} t_{\mathrm{VF}}}{2} \tag{2-17}$$

2.2.2.4 ***Stage IV ($t_4 - t_6$) – Gate voltage rising time***

This substage begins after t_4 when V_{ds} has fallen to normal conduction voltage V_{on} and drain current is stable at I_O. V_{gs} continues increasing from $V_{miller1}$ to normal turn-on voltage V_{dr_on}. Therefore, the EMI noise of this period is low. Since duration of period (t_4-t_5) is generally short, only the duration of (t_5-t_6) is considered and it can be calculated with Eq. (2-18).

$$t_6 - t_5 = C_{\mathrm{iss}} R_{\mathrm{g}} \ln\left(\frac{V_{\mathrm{dr_on}} - V_{\mathrm{miller1}}}{0.1V_{\mathrm{dr_on}}}\right) \tag{2-18}$$

With the aforementioned equations, the trajectory of turn-on process can be derived.

2.2.3 Turn-off process

Similar to the turn-on process, turn-off process can be divided into turn-off delay, the first Miller plateau, voltage rise time, current fall time, and end switching time. However, there are two conditions of multi-level turn-off process which are determined by the levels of intermediate voltage. When $V_{int} > V_{th}$, the gate driver is not able to completely shut down the channel and I_{ds} is clamped at saturation current I_{sat}. The turn-off voltage waveform of the two situations are shown in Figure 2-8 and Figure 2-9. The turn-off process trajectory model has been published on [2.22].

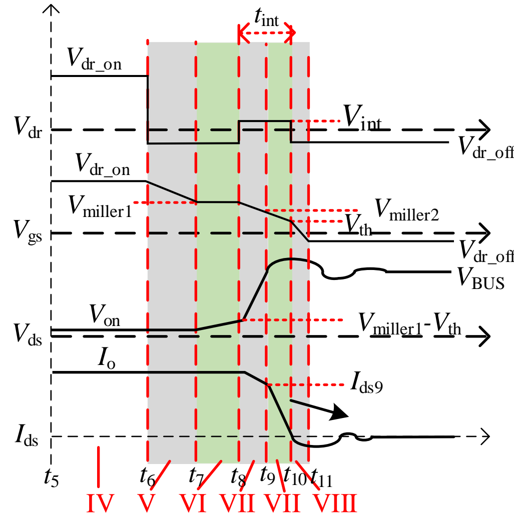

Figure 2-8 The basic waveform of the 3-L AGD under Situation I ($V_{int} \leq V_{th}$).

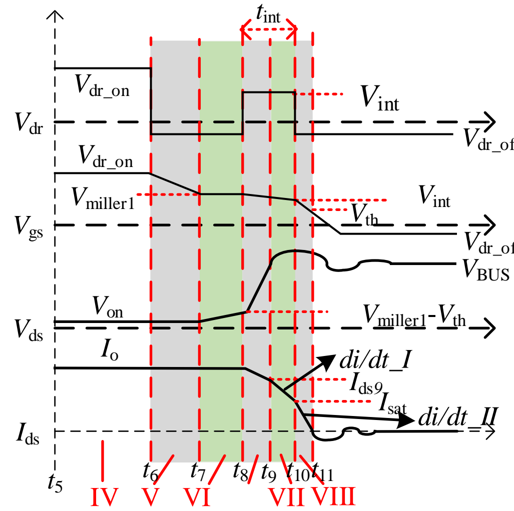

Figure 2-9 The basic waveform of the 3-L AGD under situation II ($V_{int} > V_{th}$).

The switching behavior of SiC MOSFET under the proposed 3-L turn-off V_{dr} profile will be analyzed with the trajectory model in the following sections.

2.2.3.1 ***Stage V ($t_6 - t_7$) - The turn-off delay***

During the time between t_6 and t_7, V_{dr} switches to V_{dr_off}. Junction capacitances C_{gs} and C_{gd} begin to discharge through R_g. The actual V_{gs} of the MOSFET decreases to $V_{miller1}$ which can be calculated with Eq. (2-7). The duration of the time delay is given by Eq. (2-19) [2.14][2.15]:

$$t_{\mathrm{delay}} = R_{\mathrm{g}}(C_{\mathrm{gs}} + C_{\mathrm{gd}})\ln(\frac{V_{\mathrm{dr_on}} - V_{\mathrm{dr_off}}}{V_{\mathrm{miller1}} - V_{\mathrm{dr_off}}}), \quad (2\text{-}19)$$

where C_{gs}+C_{gd} is denoted by C_{iss} on the datasheets of most MOSFETs. In Eq. (2-19), the MOSFET is still conducting. Therefore, the value of C_{iss} in this stage is the value when V_{ds} is low. Also, since V_{ds} and I_{ds} do not change, both the EMI noise and energy losses of this period are low. Only the total duration of this stage should be taken into consideration. From Eq. (2-19), t_{delay} is related with I_O and V_{dr}. This relationship between t_{delay} and I_O is plotted in Figure 2-10. It should be noted that Figure 2-10 uses the parameters of Wolfspeed C2M0045170 [2.16].

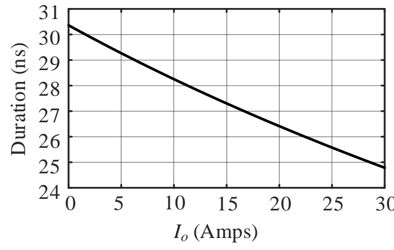

Figure 2-10 The duration of turn-off delay with the load current.

From Figure 2-10, a low V_{dr} and a high I_O can reduce the duration of the turn-off delay. Therefore, the gate driver output should be as low as possible to shorten this period. That is the reason why the 3-L turn-off utilizes V_{dr_off} for this substage. Also, as the MOSFET is still conducting, the power losses of this substage are the same as the on-state conduction power losses. The total energy losses of Substage V are given by Eq. (2-20).

$$E_{\mathrm{I}} = I_{\mathrm{O}}^{2} R_{\mathrm{ds_on}} t_{\mathrm{delay}} \quad (2\text{-}20)$$

From Eq. (2-20), it is obvious that with a longer turn-off delay, the energy losses will be higher. Another problem caused by long turn-off delay is the increased deadtime. The deadtime of the PWM signal should cover the entire switching process to prevent a shoot-through fault. However,

a long deadtime may result in high zero-crossing distortion and harmonics[2.17]. Therefore, in the 3-L turn-off design, the turn-off delay should be reduced.

2.2.3.2 ***Stage VI ($t_7 - t_8$) - The first Miller plateau***

During this stage, V_{gs} remains constantly at $V_{miller1}$ and V_{dr} remains at V_{dr_off}. V_{ds} starts to increase to $V_{miller1}$-V_{th} and I_{ds} remains constant at I_O. Since $V_{miller1}$-V_{th} is very low and the EMI issue is not high, the slew rate of this substage is low and it is preferable to shorten the duration of this stage with V_{dr_off}. The duration of Stage VI can be derived with Eq. (2-21).

$$t_{II} = \frac{R_g C_{gd}\left(V_{miller1} - V_{th} - V_{on}\right)}{V_{miller1} - V_{dr_off}}. \tag{2-21}$$

In this stage, C_{gd} should be the value when V_{ds} is almost zero. From Eq. (2-21), the duration of this stage is very short.

2.2.3.3 ***Stage VII ($t_8 - t_9$)- The voltage rise period***

During this stage, V_{dr} switchs from V_{dr_off} to V_{int} and the switching process can be slowed down. V_{ds} is increasing from V_{ds_on} to V_{BUS}, while I_{ds} drops to I_{ds9} because the channel is shutting down. The *dv/dt* of this stage can be evaluated with Eq. (2-22). In Eq. (2-22), I_{g9} is the average gate current in this stage, which can be deduced with: $I_{g9} = \frac{V_{miller1} - V_{int}}{2R_g}$. Similar to the voltage falling substage of the turn-on process, the non-linear C_{gd} should be considered.

$$\frac{dV_{ds}}{dt} = \frac{I_{g9}}{C_{gd}} = \frac{V_{miller1} - V_{int}}{2R_g \dfrac{C_{gd0}}{\sqrt{1 + V_{ds} / \phi_0}}} \tag{2-22}$$

Solving Eq. (2-22) with the initial conditions: $V_{ds}|_{t=0}$=0 (ignore V_{on}) and substituting t_{VR} =t (V_{ds}=V_{BUS}) into Eq (2-23), the duration of the rise time of V_{ds}, i.e. t_{VR}, can be derived from Eq. (2-23).

$$t_{VR} = \frac{4C_{gd0}R_g\phi_0(\sqrt{1+V_{BUS}/\phi_0}-1)}{V_{miller1}-V_{int}} \tag{2-23}$$

Also, *dv/dt* of this period can be calculated by Eq. (2-24).

$$\frac{dv}{dt} = \frac{V_{BUS}}{t_{VR}} = \frac{V_{BUS}\left(V_{miller1}-V_{int}\right)}{4C_{gd0}R_g\phi_0(\sqrt{1+V_{BUS}/\phi_0}-1)} \tag{2-24}$$

The energy losses of Stage III E_{VR} can be evaluated from Eqs. (2-25) and (2-26) where I_{ds9} is the I_{ds} at time t_9 [2.18].

$$E_{VR} = \int_{t=0}^{t_{VR}} V_{ds}I_{ds}dt = \frac{dv}{dt}\frac{\left(2I_{ds9}+I_O\right)t_{VR}^2}{6} \tag{2-25}$$

$$I_{ds9} = I_O - \left(C_d + C_L\right)\frac{dv}{dt} \tag{2-26}$$

Solving Eqs. (2-24) - (2-26), *dv/dt* and energy losses of the Substage VII can be plotted in Figure 2-11 and Figure 2-12.

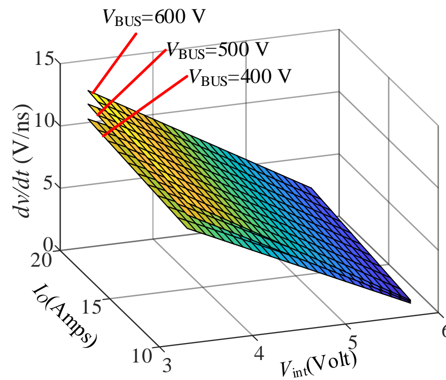

Figure 2-11 *dv/dt* vs. load current and V_{int}.

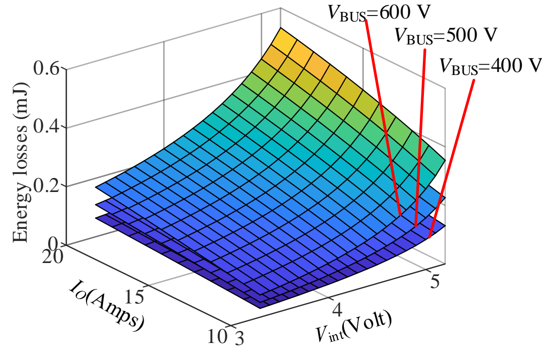

Figure 2-12 The energy losses of Stage III.

From Figure 2-11, *dv/dt* is determined by I_O and V_{int}. With lower I_O or higher V_{int}, the *dv/dt* is lower. The reason why this downward trend is very "linear" can be explained with Eq. (2-5). From Eq. (2-5), V_{miller} is proportional to I_O. With higher I_O, V_{dr} is closer to the $V_{miller1}$ and the turn-off process duration is longer, thus reducing *dv/dt*.

The energy losses of this substage are as shown in Figure 2-12. From Figure 2-12, high V_{int} and high I_O increase the turn-off energy losses during voltage rise stage.

2.2.3.4 ***Stage VIII ($t_9 - t_{10}$) and Substage VIII ($t_{10} - t_{11}$): The current fall period***

The turn-off process should be paid special attention since high V_{int} may clamp I_{ds} at I_{sat}, but not completely shut down the MOSFET. Therefore, the turn-off process under 3-L profile should be analyzed with consideration of two different situations: Situation I ($V_{int} \leq V_{th}$) and Situation II ($V_{int} > V_{th}$).

a) Situation I: $V_{int} \leq V_{th}$

At the end of this stage, V_{gs} drops down to V_{th}, V_{ds} remains at V_{BUS}, and I_{ds} drops from I_{ds9} to zero. V_{dr} decreases to zero finally to completely shut down the power device. After this stage, V_{dr} is decreased to V_{dr_off}. Due to the parasitic inductance and capacitance in the circuit, ringing occurrs after the turn-off process ends. V_{gs} continues falling from V_{int} to V_{dr_off}.

The duration of this stage t_{CF1}, can be derived with Eq. (2-27). In Eq. (2-27), I_{g5} is the average gate current of this stage and it is expressed with $I_{g5} = \frac{0.5(V_{th} + V_{int}) - V_{int} - L_s I_{ds4} / t_{CF1}}{R_g}$.

$$t_{CF1} = \frac{I_{ds4} C_{iss}}{g_{fs} I_{g5}} = \frac{R_g I_{ds4} C_{iss} + L_s g_{fs} I_{ds4}}{0.5 g_{fs} (V_{th} - V_{int})} \tag{2-27}$$

The energy losses of Stage IV are calculated in Eq. (2-28).

$$E_{CF} = \frac{t_{CF1} V_{BUS} I_{ds4}}{2} = \left[I_O - \left(C_d + C_L \right) \frac{dv}{dt} \right] \frac{\left(R_g I_{ds4} C_{iss} + L_s g_{fs} I_{ds4} \right) V_{BUS}}{g_{fs} (V_{th} - V_{int})} \tag{2-28}$$

E_{off}, the total turn-off energy losses, can be calculated as shown in Eq. (2-29).

$$E_{off} = E_{VR} + E_{CF} \tag{2-29}$$

It should be noted that in this stage, V_{ds} has been increased to V_{BUS}. Thus, C_{gd} should select the value when V_{ds} is high. Generally, this value can be found in the C-V curve on the datasheet. The duration of V_{int}, i.e., t_{int} in Figure 2-8Figure 2-9, can be evaluated with Eq. (12).

$$t_{int} = t_{VR} + t_{CF1} \tag{2-30}$$

The average *di/dt* can be calculated from Eq. (2-31) as

$$di / dt = \frac{I_{ds9}}{t_{CF1}} = \frac{g_{fs} \left(0.5 V_{th} + 0.5 V_{miller2} - V_{int} \right)}{R_g C_{iss} + L_s g_{fs}} \tag{2-31}$$

where $V_{miller2} = V_{th} + \left[I_{ds4} - (C_{gd} + C_{gs}) \frac{dv}{dt} \right] / g_{fs}$ and t_{CF1} is the duration of the first I_{ds} fall period.

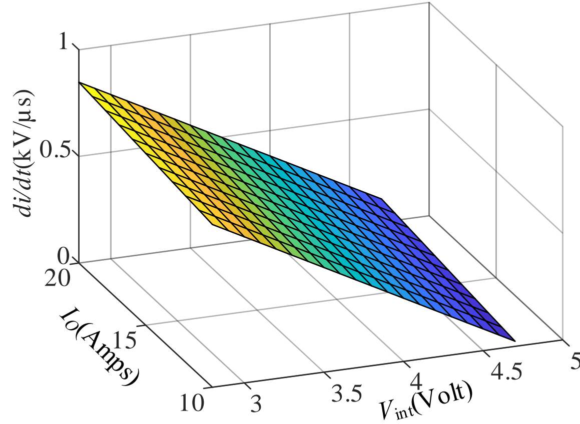

Figure 2-13 The *di/dt vs.* load current and V_{int}.

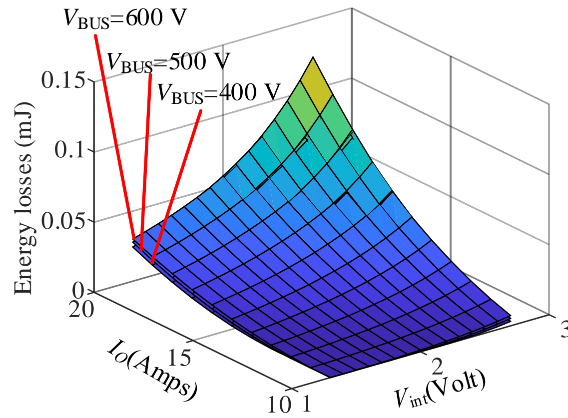

Figure 2-14 The energy losses E_{CF} *vs.* load current and V_{int}.

From Figure 2-13, the *di/dt* increases with I_O. *di/dt* and the energy losses also decreases with higher V_{int}. Also, with higher I_O, the energy losses increase.

b) Situation II: $V_{int} > V_{th}$

When V_{int} is higher than V_{th}, the MOSFET cannot shut down all the channel current during t_{int}. As a result, the MOSFET continues conducting at a certain current level. In other words, I_{ds} is dropped from I_{ds9} to the saturation current I_{sat}. In Stage V, when the V_{dr} drops down from V_{int} to V_{th}, I_{ds} will drop from I_{sat} to zero. In these two stages, C_{gd} should be the value when $V_{ds} = V_{BUS}$. The saturation current I_{sat} is given by Eq. (2-32) [2.19] [2.20].

$$I_{sat} = \frac{k_p}{2}(V_{int} - V_{th})^2 \quad (2\text{-}32)$$

where k_p is the saturation current transconductance factor in A/V^2. The relationship of I_{sat} with V_{int} and I_O can be plotted as shown in Figure 2-15.

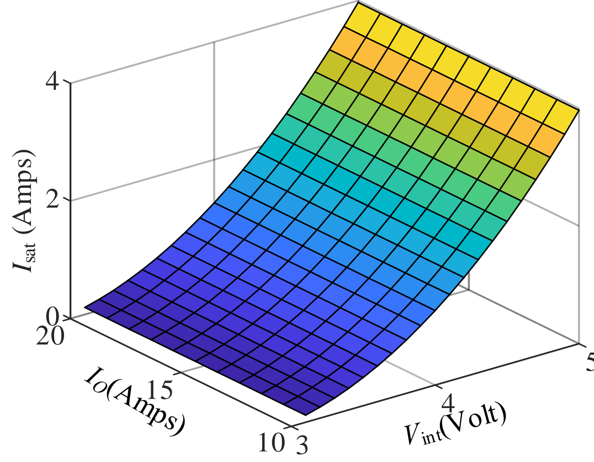

Figure 2-15 The saturation current I_{sat} *vs.* V_{int}.

From Figure 2-15, I_{sat} increases with V_{int}. For AGD design, when V_{dr} is too high, the channel current at the end of Substage IV will be high. I_{sat} should be accounted for when the I_{ds} is high, especially for over-current protection.

The duration of this stage t_{CF2} can be evaluated by Eq. (2-33). *di/dt_I*, which is denoted by the *di/dt* within the t_{int}, can be evaluated with Eq. (2-34).

$$t_{CF2} = \frac{R_g I_{ds4} C_{iss} + L_s g_{fs} I_{ds4}}{0.5 g_{fs}(V_{miller1} - V_{int})} \quad (2\text{-}33)$$

$$di/dt_I = \frac{I_O - (C_d + C_L)(V_{BUS} - V_{miller1} + V_d + V_{th})/t_{VR} - I_{sat}}{t_{CF2}} \quad (2\text{-}34)$$

di/dt_II, which occurs after the t_{int} in Stage V, is given by Eq.(2-35).

$$di/dt_II = \frac{I_{\text{sat}}}{t_{\text{V}}} = \frac{I_{\text{sat}}}{(C_{\text{gd}} + C_{\text{gs}})R_{\text{g}} \ln\left(\dfrac{V_{\text{int}} - V_{\text{dr_off}}}{V_{\text{th}} - V_{\text{dr_off}}}\right)} \tag{2-35}$$

With Eqs. (2-33) -(2-35), the relationship of *di/dt* with V_{int} and I_{O} under Situation II can be plotted as shown in Figure 2-16.

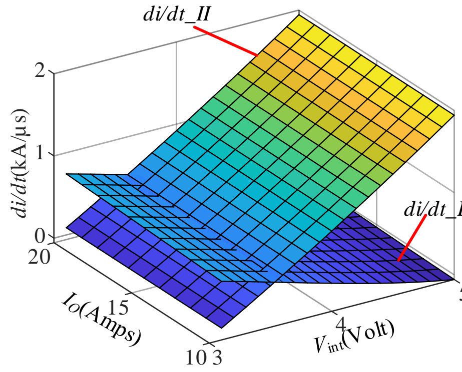

Figure 2-16 The *di/dt* under Situation II with different V_{int}.

From Figure 2-16, under Situation II, high V_{int} reduces *di/dt_I*. However, since it also increases I_{sat}, *di/dt_II* is increased as well.

The downside of the *di/dt* is the potential breakdown of the power device due to the parasitic inductance L_{s} and L_{d}. The maximum drain-source voltage $V_{\text{ds_max}}$, which can be evaluated from Eq. (2-36), occurs during the current fall time.

$$V_{\text{ds_max}} = \begin{cases} (L_{\text{d}} + L_{\text{s}})di/dt + V_{\text{BUS}}, & \text{When } V_{\text{int}} < V_{\text{th}} \\ (L_{\text{d}} + L_{\text{s}})\max(di/dt_I, di/dt_II) + V_{\text{BUS}}, & \text{When } V_{\text{int}} > V_{\text{th}} \end{cases} \tag{2-36}$$

In this case, the energy losses caused during the current fall, E_{CF}, can be calculated from Eqs. (2-37) - (2-39).

$$E_{\text{IV}} = \frac{t_{\text{CF2}} V_{\text{BUS}} (I_{\text{ds4}} + I_{\text{sat}})}{2} = \frac{t_{\text{CF2}} V_{\text{BUS}} \left[I_{\text{O}} - (C_{\text{d}} + C_{\text{L}})(V_{\text{BUS}} - V_{\text{miller1}} + V_{\text{d}} + V_{\text{th}}) / t_{\text{VR}} \right]}{2} + \frac{I_{\text{sat}} t_{\text{CF2}} V_{\text{BUS}}}{2} \quad (2\text{-}37)$$

$$E_{\text{V}} = \frac{t_{\text{V}} V_{\text{BUS}} I_{\text{sat}}}{2} = \frac{1}{2} V_{\text{BUS}} I_{\text{sat}} (C_{\text{gd}} + C_{\text{gs}}) R_{\text{g}} \ln \left(\frac{V_{\text{th}} - V_{\text{dr_off}}}{V_{\text{int}} - V_{\text{dr_off}}} \right) \quad (2\text{-}38)$$

$$E_{\text{CF}} = E_{\text{IV}} + E_{\text{V}} \quad (2\text{-}39)$$

The energy losses are plotted as shown in Figure 2-17.

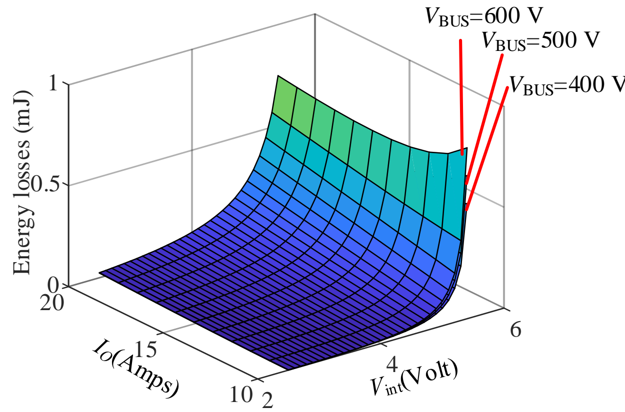

Figure 2-17 The turn-off losses E_{CF} under Situation II with different V_{int}.

2.3 Conclusions drawn from the theoretical analysis

2.3.1 The turn-on process

Table 2-2 Summary of the trajectory model equations for turn-on process with the AGD.

Values	**Faster mode** $V_{\text{dr}}=V_{\text{f_on}}$	**Slower mode** $V_{\text{dr}}=V_{\text{int}}$
Turn-off delay	(2-4)	(2-4)
dv/dt	(2-16)	(2-16)
di/dt	(2-10)	(2-10)
Total energy losses	(2-12)+(2-15)	(2-12)+(2-15)
t_{int}	(2-4)+(2-9)+(2-15)	(2-9)+(2-15)

As introduced in the aforementioned sections, the turn-on process can be divided into to two conditions: faster turn-on mode and slower turn-on mode. The equations for depicting the trajectory during turn-on process are concluded in Table 2-2. It should be noted that, for faster turn-on mode, V_{f_on} is used to replace the V_{int} in the equations.

The observation of the turn-on process is concluded as following:

1. V_{int} should be higher than $V_{miller1}$. Otherwise, it cannot turn-on the device completely. V_{f_on} should be higher than V_{dr_on}, but not be higher than the maximum gate-source voltage.

2. With lower V_{int}, the turn-on speed is further reduced and the energy losses are increased.

3. Turn-on losses are higher than the turn-off losses due to the non-linear C_{ds} and C_{gd}. Also, the most detrimental effect during the turn-on process is the overshoot I_{ds} which does not damage the device deadly. Therefore, it is not preferred to slow down the device to a very low level.

2.3.2 The turn-off process

There are two different situations for the turn-off process: Situation I $V_{int} \leq V_{th}$ and Situation II $V_{int} > V_{th}$. The equations for depicting the trajectory during turn-off process are concluded in Table 2-3.

Table 2-3 Summary of the trajectory model equations for 3-L turn-off.

Parameters	**Equations**	
	$V_{int} \leq V_{th}$	$V_{int} > V_{th}$
Turn-off delay	(2-19)	(2-19)
dv/dt	(2-24)	(2-24)
di/dt	(2-31)	(2-34) for *di/dt_I*
		(2-35) for *di/dt_II*
Total energy losses	(2-25)+(2-28)	(2-25)+(2-37)+(2-38)
t_{int}	(2-23)+(2-27)	(2-32)+(15)

1. V_{int} should be lower than V_{miller1} and higher than $V_{\text{dr_off}}$. A V_{int} which is higher than V_{miller1} will not increase V_{ds} to V_{BUS}.

2. With a higher V_{int}, the turn-off speed is further reduced and the turn-off losses are increased.

3. The voltage overshoot, which is caused by *di/dt* on the stray inductance, happens during the turn-off process. However, in Situation II, a very high V_{int} also increases the overshoot voltage since it increases *di/dt_II* dramatically. Therefore, it is not preferred to use a very high V_{int} level.

2.4 The model-based trajectory optimization algorithm

2.4.1 The cost function

As analyzed in the former sections, the optimization algorithm predicts the switching trajectory of the power device. The analysis results of the trajectory model clarify that high V_{int} can reduce the slew rate and reduce EMI noise, but it also causes high energy losses and decreases the efficiency of the system. Thus, the optimization algorithm should comprehensively consider the tradeoff of the energy losses against the EMI noise. A cost function is expressed in Eq. (2-40).

$$J = \alpha \frac{dv}{dt} / \left.\frac{dv}{dt}\right|_{\text{Normal}} + \beta \frac{di}{dt} / \left.\frac{di}{dt}\right|_{\text{Normal}} + \gamma E_{\text{loss}} / \left.E_{\text{loss}}\right|_{\text{Normal}}, \tag{2-40}$$

The cost function is introduced to help to select the optimal V_{int}. In Eq. (2-40), α, β, and γ are the weighting factors for *dv/dt*, *di/dt*, and energy losses respectively. The weighting factors selection follows the equation $\alpha+\beta+\gamma=1$. $dv/dt|_{\text{Normal}}$, $di/dt|_{\text{Normal}}$, and $E_{loss}|_{\text{Normal}}$ are the nominal values of *dv/dt*, *di/dt*, and energy losses under normal turn on/off mode respectively. The optimal results are the V_{int} value that results in the lowest J.

The weighting factors selection is based on the requirements of specific scenarios. For instance, when the PCB parasitics are high, the EMI noise suppression is the top priority factor. In this case, α and β should be large for the optimization algorithm. In contrast, when the PCB is well designed and the system efficiency is preferred to be high, γ can be selected higher than α and β. It should be noted that α and β are coupled and they represent the cost caused by EMI noise.

There are several constraints for the optimization algorithm. Since high *dv/dt* will damage the components on the PCB such as the digital isolator and isolated power supply, V_{int} selection should leverage *dv/dt* be within the limitation on the datasheet. During the turn-on process, high *dv/dt* leads to high overshoot current. Even though power devices can withstand short-term high current, it is necessary to reduce the overshoot current to a level lower than the maximum surge current of the power device.

$$I_{ds_max} = (C_d + C_L) dv/dt + I_O \tag{2-41}$$

During turn-off process, *di/dt* will cause overshoot voltage on V_{ds}. To avoid the partial discharging caused by the high voltage, the V_{ds} overshoot should be lower than V_{ds_max}. Thus, V_{int} selection for the turn-off should be subjected to Eq. (2-42).

$$V_{ds_max} = \begin{cases} (L_d + L_s) di/dt + V_{BUS}, \text{ When } V_{int} < V_{th} \\ (L_d + L_s) \max(di/dt_I, di/dt_II) + V_{BUS}, \text{ When } V_{int} > V_{th} \end{cases} \tag{2-42}$$

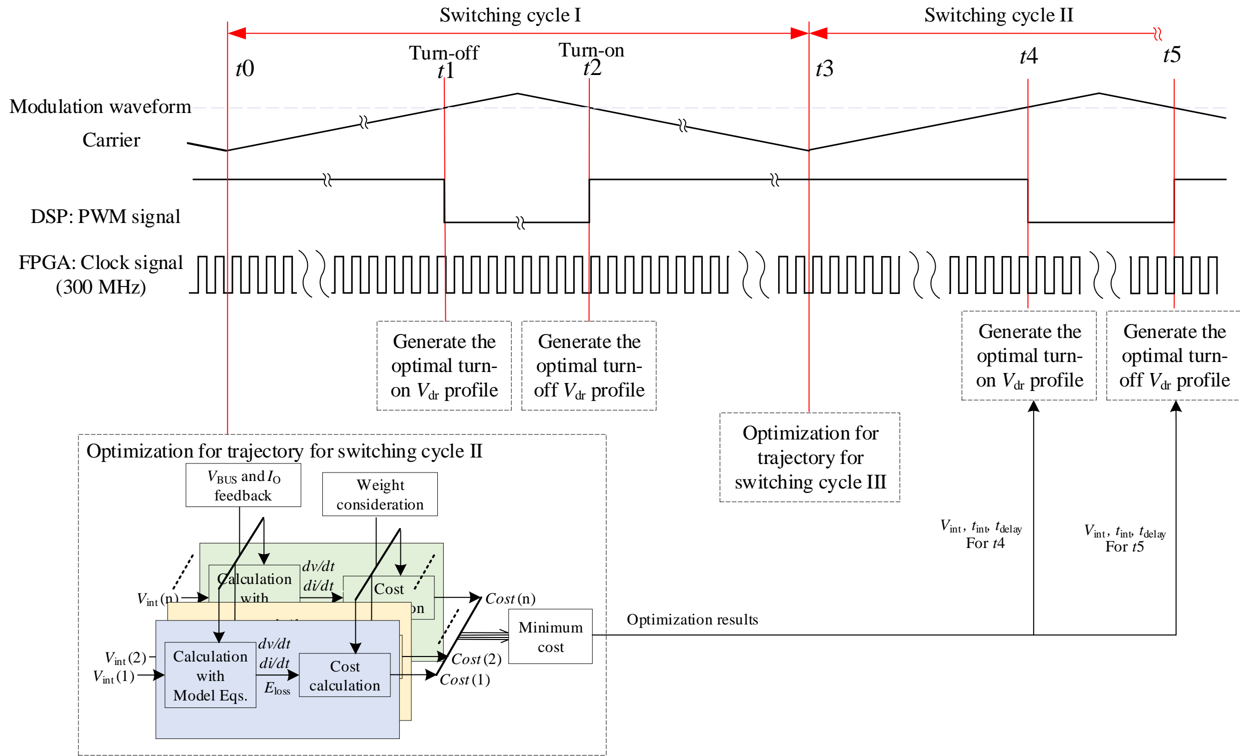

Figure 2-18 The flow chart of the proposed control scheme.

The energy losses also have an upper limitation due to the potential over-heated condition caused by energy losses. This upper limitation is determined by the thermal dissipation capability of the hardware. When the energy losses are higher than the upper limit, the power devices may be over heated.

The flow chart of the optimization is given in Figure 2-18. The on-line optimization algorithm is used to select the optimized V_{int} based on analyzing the V_{ds} and I_{ds} feedbacks. To guarantee there is enough time for the local controller to conduct the optimization calculation, the optimization is performed one switching cycle before the switching. For example, in Figure 2-18, the optimal V_{dr} profile of $t4$ and $t5$ (switching cycle II) have been determined at $t0$ which occurs at the beginning of switching cycle I. At $t0$, the local controller receives V_{BUS} and I_{O} feedback signals from the main control unit. Different V_{int} values will be input into the trajectory model and the total cost will be

calculated. The local controller will select the V_{int} with the lowest cost. Then the duration of each substage of switching for this optimal V_{int} will be calculated. With the duration of each substage and optimal V_{int} value, the corresponding V_{dr} profile for the next switching cycle is now determined.

2.4.2 A case study

To help understand the optimization algorithm, a case study is carried out comparing two different SiC MOSFETs: CREE C2M0040120 and Rohm SCH2080KE under the same experimental and simulation setup. The datasheet parameters of these two MOSFETs are given in Table 2-4. From Table 2-4, all the parameters of the two power MOSFETs are comparable apart from g_{fs}. In other words, with the same setup, only one parameter g_{fs} can significantly affect the switching process.

Table 2-4 The comparison of the parameters of two SiC Power MOSFETs

Parameter	**C2M0040120**	**SCH2080KE**
Maximum V_{ds}	1200 V	1200 V
Maximum I_{ds}	60 A	40 A
R_{ds_on}	40 mΩ	80 mΩ
g_{fs}	15.1 S	3.7 S
C_{gd0}	860 pF	1090 pF
C_{gd}(800V)	11 pF	20 pF
C_{gs}	1883 pF	1830 pF
C_{ds}	140 pF	155 pF
V_{th}	2.6 V	2.8 V

First, the cost function of the Rohm SCH2080KE is analyzed. Based on the parameters from Table 2-4, the cost value *vs.* V_{int} and load current I_O under different groups of α, β, and γ combination can be drawn in Figure 2-19. Figure 2-19 (a) shows the condition that α and β are high (α=0.6, β=0.15, γ=0.25). This condition is preferred when the switching transient needs to be slowed down. Figure 2-19 (b) reveals the curve for the scenario when the switching transient is

preferred to be sped up. The setup of the weight coefficients are given as: α=0.1, β=0.05, γ=0.85. Figure 2-19 (c) is the average weight consideration mode when the *dv/dt* and *di/dt* suppression with the efficiency of the system are equally important. The weight coefficients are selected equally: α=β=γ=1/3. It should be noted that since α and β represent the EMI noise. Thus, the balanced weight should be α+β=γ.

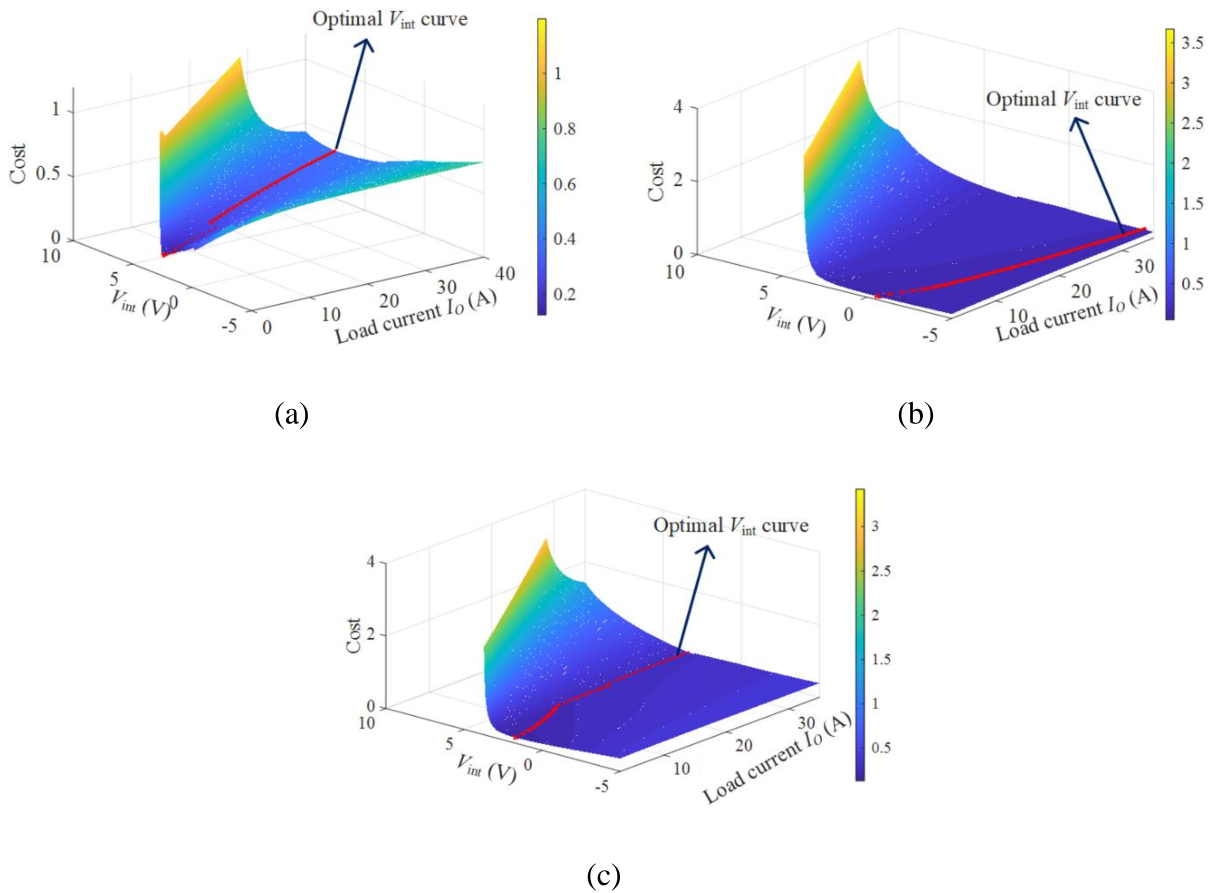

Figure 2-19 The cost under different weight conditions. (a) High EMI suppression weight (α=0.6, β=0.15, γ=0.25). (b) High efficiency weight (α=0.1, β=0.05, γ=0.85). (c) Average weight (α=1/3, β=1/3, γ=1/3).

To compare the switching waveform of these two MOSFETs, the dc bus voltage is set to be 500 V for both MOSFETs. First, the optimal V_{int} curve should be plotted. Based on the analysis with the proposed trajectory model, the optimal V_{int} of these two power MOSFETs is as shown in Figure 2-20 (a) and (b).

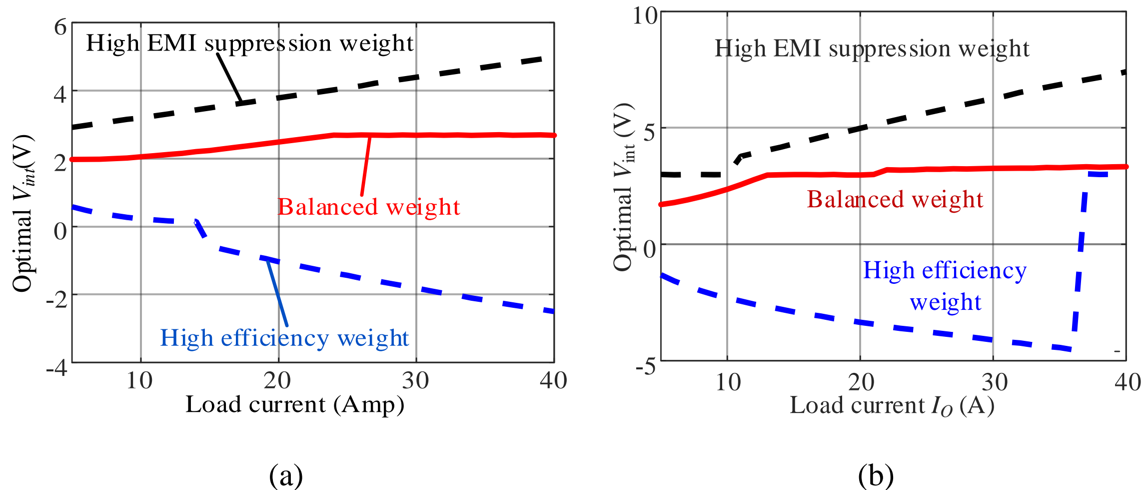

Figure 2-20 The optimized V_{int} selection for two different SiC power MOSFETs. (a) CREE C2M0040120. (b) Rohm SCH2080KE.

In Figure 2-20, the curve of Rohm SCH2080KE is "steeper" than the CREE C2M0040120. It occurs due to different g_{fs} values of these two MOSFETs. The g_{fs} of SCH2080KE is only 0.2 of C2M0040120. From Eq. (2-5), the V_{miller1} of SCH2080KE will be significantly influenced by I_{O}.

In the balanced condition of Figure 2-20, the optimal V_{int} locates at the level close to V_{th}. This phenomenon occurs since the *di/dt* is the lowest while the energy losses do not increase dramatically. Therefore, V_{int}=V_{th} is the best choice for most conditions. It should be noted that in Figure 2-20 (b), the high energy losses weight condition has a sharp rise at I_{O}=35 A. This phenomenon can be explained with Eqs. (2-7) and (2-12). When I_{O} increases to a very high level , energy losses increase dramatically. However, since V_{miller1} increases as well, the *dv/dt* increases dramatically. When the rising trend of *dv/dt* dominates the cost function results, the optimization algorithm prefers to increase V_{int} to reduce the EMI noise.

2.4.3 Simulation verification

To validate the theoretical analysis in the former sections, the LTspice simulation is performed for these two SiC MOSFETs. The SPICE models of the MOSFETs can be downloaded from the

websites of Wolfspeed and Rohm. The simulations are conducted under the same voltage and current setup: V_{BUS}=500 V and I_O=30 A. Three situations which are corresponding to Figure 2-21 are compared, i.e. high efficiency, average weight, and high EMI suppression condition.

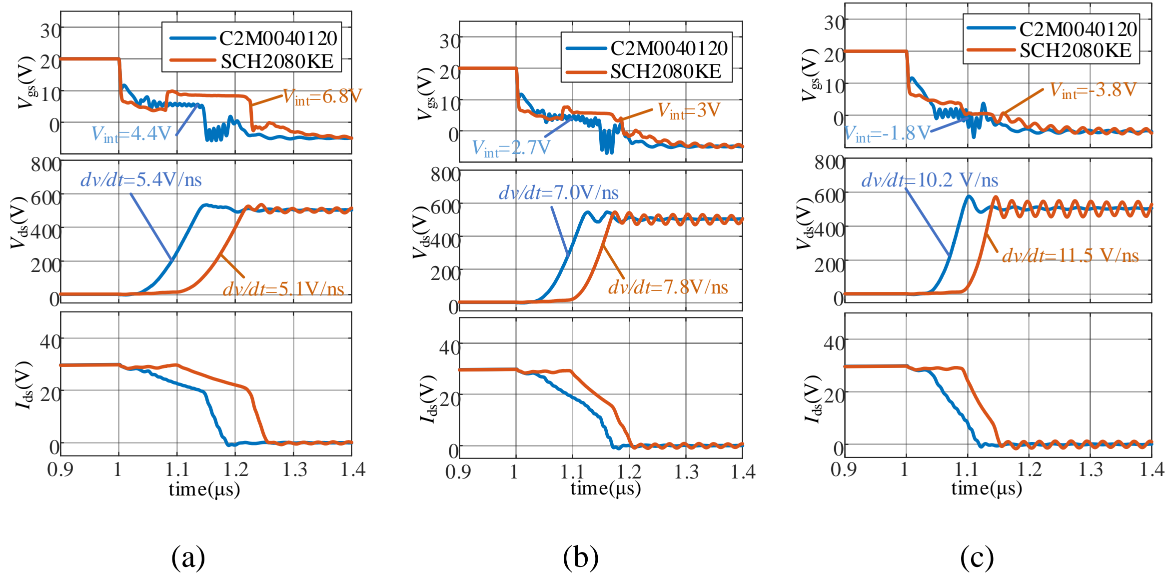

Figure 2-21 Simulation results of C2M0040120 and SCH2080KE comparison under different operation conditions. (a) High EMI suppression condition. (b) The average weight condition. (c) High efficiency condition.

From Figure 2-21 (a), *dv/dt* of SCH2080KE under V_{int} =6.8 V is similar to C2M0040120 under V_{int} =4.4 V. The reason of this result is due to higher g_{fs} of C2M0040120. To achieve the same EMI noise suppression performance, the V_{int} of SCH2080KE should be higher. Under the balanced condition, the V_{int} is selected around the V_{th}. *dv/dt* is reduced to a certain level while the energy losses do not increase dramatically. For the high efficiency mode, V_{int} of both MOSFETs is selected to be low (3.8 V for SCH2080KE and 1.8 V for C2M0040120).

2.5 Conclusions

In this chapter, the circuit schematics of the propose AGD is introduced. The current route of every substage is analyzed. The theoretical trajectory model for analyzing the switching process

of power MOSFETs are given. Based on the theoretical analysis, the switching behaviors of power MOSFETs under multi-level switching are analyzed. It indicates that high V_{int} can reduce the slew rate and thus reduce the EMI noise, but it also increases the energy losses. Also, some other variables such as the load current, dc bus voltage, and the gate resistance also affect the slew rate. Based on the theoretical analysis, the cost function is given to select the optimal V_{int}. The cost function considers the weight coefficients of slew rate, i.e., *dv/dt* and *di/dt*, and the weight coefficient of energy losses. For the case when the PCB layout is rationale, the weight coefficients of slew rate can be higher. However, for the case that the PCB layout is not perfectly designed, the weight coefficient of energy losses can be larger. Through adjusting the combination of weight coefficients, the optimal V_{int} curve can be adjusted. To help understand the design consideration, a case study is given in this paper. A Rohm MOSFET and a CREE MOSFET are compared and the optimal V_{int} curve for these two devices are plotted. The LTspice simulation is conducted to verify the proposed V_{int} selection. It should be noted the analysis is only for hard switching condition. For the soft switching condition, the analysis of the switching waveform should be different. In the following chapter, the theoretical analysis is introduced.

2.6 Reference

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CHAPTER 3

VERIFICATION OF THE PROPOSED ACTIVE GATE DRIVER ON 1.2 KV SIC POWER MOSFET

3.1 Hardware setup and design consideration

In this chapter, the double pulse tests (DPTs) experimental results of the proposed AGD with 1.2 kV SiC MOSFET are given in the first section. The second section will introduce the PCB design and the measurement consideration. Then the DPTs results are analyzed and compared with the theoretical analysis.

3.1.1 Hardware design

3.1.1.1 *Components selection*

The performance of the components will determine the performance of the gate driver board system. Therefore, the parts selection is significant to the board design.

A. FPGA controller

The functions of FPGA controller include optimization calculation of the driver voltage profile and controlling the gate driver circuit. It will optimize the switching transient trajectory based on the voltage and current feedback. Therefore, the requirement for the FPGA controller is computation speed which is determined by the clock frequency and amount of logic gates.

The clock frequency selection is relevant to the switching speed of the device. For a 1.2 kV SiC MOSFET, the switching transient process generally takes 20-50 ns. Therefore, the clock frequency of the FPGA should be at least 200 MHz which can provide 5 ns adjustable time resolution. The amount of logic gates determines how much computation load the controller can

calculate. In the experimental prototype, an Altera MAX10 [3.1] is selected due to its 400 MHz maximum clock frequency. The MAX10 series products provide different amount of I/O ports and logic gates versions. In this dissertation, Altera 10M08SCU169 which has over 8000 logic gates and 169 I/O pins is selected [3.1].

B. Voltage regulator op-amp

The parameters of the op-amps can determine the V_{int} generation. The selection of op-amp should comprehensively consider the tradeoff between the bandwidth and output power. The other features are not neglected such as the biased current and the noise. As mentioned in the previous sections, there are two op-amps in the active voltage regulator. Op1 works as an analog adder circuit which is not directly connected to the driver buffers. Therefore, it only requires enough bandwidth to realize the high-speed adjustment. Op2 is used to build a reverse voltage amplifier circuit. Since it generates V_{int} which is directly connected to the buffer and drive the MOSFET, its output power should be high to provide enough driving current. Also, because V_{int} changes cycle by cycle, the bandwidth of Op2 should be at least ten times higher than the switching frequency of the power MOSFET to provide on-line adjustment. For most 800 V – 1.7 kV voltage rated SiC power MOSFETs used in converter applications, the switching frequency is desired to be 10 kHz to 100 kHz. Therefore, Op2 should have at least 1 MHz bandwidth to provide online adjustment for V_{int}.

In this dissertation, Analog Devices AD817A [3.2], which has 50 MHz bandwidth and ±15 V power supply voltage, is selected for Op1. Texas Instruments LM675, which has 3 A output current capability, 60 V power supply range, and 5.5 MHz bandwidth, is selected for Op2 [3.3].

C. Digital isolator

There are two types of digital isolators in the proposed AGD, i.e., the one for the voltage regulator and the ones for driver buffers. All of these digital isolators should provide enough galvanic isolation between the digital side and analog side of the converter, especially the high side switch gate driver. Selection of the digital isolator should comprehensively consider these features: propagation delay, insulation voltage levels, and maximum *dv/dt*, and price. The maximum *dv/dt* is relevant with the application conditions. For instance, if the power converter is designed to have very high power efficiency, the switching transient is desired to be short and *dv/dt* to be high. Thus, a digital isolator with higher *dv/dt* immunity is required. For the ultra-high voltage isolation, fiber optics transceivers are preferred.

In this dissertation, Texas Instruments ISO7420 which has 50 V/ns common mode transient immunity (CMTI), 2 kV RMS voltage isolation, and 1 Mbps signaling rate, is chosen for the PWM isolation [3.4]. Texas Instruments ISO 7760 which has 100 V/ns CMTI capability, 6 channels, 5 kV RMS isolation, and 11 ns propagation delay is selected [3.5]. Thus, with an ISO 7760 connected between the FPGA controller and Op1, the active voltage regulator can provide 2^6=64 levels of V_{int} adjustment.

D. Driver buffers

Driver buffers are generally connected between the driver IC and the gate of MOSFET. Some driver ICs, such as TI ISO5851, have limited peak gate current. Due to the fast switching of SiC devices, the limitations of peak gate current do not drive the devices at high speed. Most driver ICs provide desaturation protection. Some gate driver ICs even provide the non-overlap protection or hardware deadtime to prevent shoot-through events. However, these functions can be realized

with FPGA controller and multi-level turn-off of AGD. Therefore, only gate driver buffers are necessary for this application.

The driver buffers which are typically totem-pole circuit are used to amplify the peak gate current. The most important parameters of the driver buffers include propagation delay time, peak drive current, and voltage range. The turn-on peak current can be roughly calculated with Eq. (3-1).

$$I_{g_pk} = \left(V_{dr_on} - V_{dr_off}\right) / R_g \tag{3-1}$$

In this dissertation, IXDN609 driver buffers are selected. The propagation delay of IXDN609 is 40 ns and the peak gate current is 9 A. These features enable it to be an attractive option for the WBG devices driving.

E. Gate resistors

Gate resistors are connected between the driver buffers and the gate of the power devices. It is used to limit the gate current that charges/discharges C_{iss} of the power devices and reduce the switching speed. Since gate resistors are series-connected in the gate loop, their parasitic inductance and power rating are important to the design.

There are different kinds of gate resistors: wire wound resistor, film resistor, and carbon resistor [3.6]. Wire wound resistors are generally used for high power applications. However, the long wires in the resistor will introduce long loop and high equivalent series inductance (ESL). Therefore, wire wound resistors are not a good option for the gate resistors [3.6]. A thick film resistor also introduces considerable ESL. Metal film resistor and thin film resistors have low ESL [3.6], so they are preferred for the gate driver. However, due to their intrinsic structure features, they are generally designed for the high power applications. When multiple gate resistors are

connected in parallel, which introduces better performances for the gate drive by reducing the associated ESL and the false-triggering probability. In this dissertation, parallel-connected thin-film resistors are used for the gate resistors.

3.1.1.2 ***PCB layout***

The CMTI capability of the gate driver board is highly relevant to the PCB layout design. The most significant design consideration is the gate loop parasitics. High gate loop parasitics increases the false-triggering probability. The parasitics on the PCB are determined by the length and width of the copper trace. The parasitic resistance of the trace can be calculated with Eq. (3-2) [3.7].

$$R = \frac{\rho \cdot Length}{w \cdot t_{\text{trace}}}, \tag{3-2}$$

where ρ is the resistivity, *Length* is the length, w is the width, and t_{trace} is the thickness of the trace. From Eq. (3-2), since the resistivity and thickness are determined on the PCB, the total parasitic resistance can be reduced through using shorter and wider trace.

The parasitic inductance of a trace on the PCB in μH can be calculated with Eq. (3-3) [3.8].

$$L = 2 \times 10^{-3} Length \left[\ln \frac{2Length}{w + t_{\text{trace}}} + 0.5 + 0.2235 \left(\frac{w + t_{\text{trace}}}{Length} \right) \right], \tag{3-3}$$

From Eq. (3-3), the self-inductance does not have a linear relationship regarding width and length. Also, the shape and angle of the trace will affect the total ESL. The driver buffers should be placed as closed as possible to the device to reduce the total loop length. It is recommended to use a grounding copper plane to replace the trace which can effectively reduce the loop of the feedback gate current.

There are several bypass capacitors placed close to the power supply pins of the driver buffers. They can reduce the power supply ripple and suppress the output voltage overshoot.

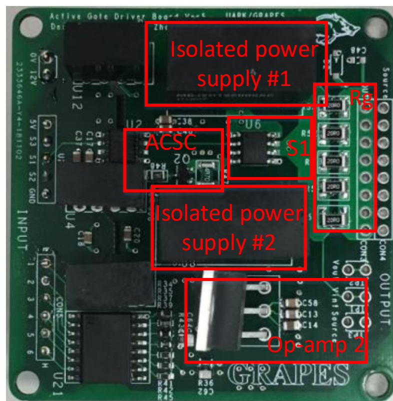
There are several suggestions for designing the PCB for the half-bridge board:

1. Several bypass capacitors should be placed as close as possible to the half-bridge. In this way, the parasitic inductance of the power loop can be reduced. Since the high-frequency noise has high impact on the waveform, it is desired to be filtered. The lowest value bypass capacitor should be closest to the half-bridge.

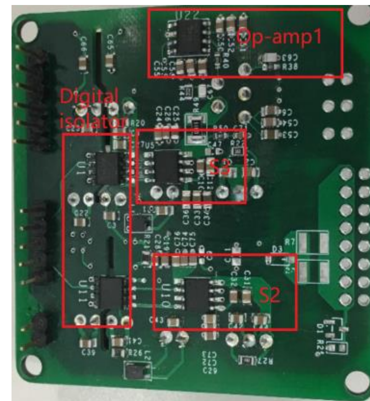
2. ANSYS Q3D is helpful to improve the design since it can extract the parasitics of the PCB layout. The Q3D guidance can be found in [3.11].

3. The gate loop inductance and common source inductance are significant to the performance of the PCB. Therefore, the gate loop should be as short as possible.

3.1.1.3 *Hardware prototype introduction*



(a)



(b)

Figure 3-1 The PCB of the proposed AGD board. (a) The top side. (b) The bottom side.

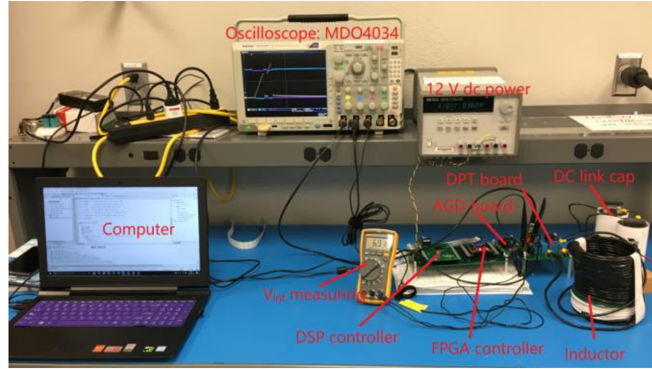


Figure 3-2 The DPT prototype setup.

Based on the aforementioned design consideration a PCB of the proposed AGD, as shown in Figure 3-1, is built for experimental verification. All the functional sections: current sinking circuit, voltage selector, and adjustable voltage regulator are integrated in the AGD board. The local controller is an Altera MAX10 10M08SCU169 FPGA chip. The local controller is on another PCB and connected to AGD through bus wires. The FPGA has 300 MHz bandwidth and over 8000 logic gates inside of the chip. The DPT experimental prototype is set up as shown in Figure 3-2. The device under test (DUT) is a Rohm SCH2080KE MOSFET.

The double pulse is generated by a TMS320F28335 DSP controller. The DSP controller and FPGA controller are placed on a same control motherboard and communicate via a parallel interface communication protocol (XIN). Another function of the DSP controller is sending the V_{BUS} and I_O feedback signals to the FPGA controller. The components of the experimental prototype and the AGD board are shown in Table 3-1.

The driver buffer is a IXDN609SI, which requires a 5 V minimum voltage for its power supply. Since the negative pole of Buffer2 is connected to V_{dr_on} which is 20 V, V_{f_on} should be at least 25 V. For most SiC power MOSFET, the maximum V_{gs} is 30 V. Therefore, taking a safety margin into consideration, V_{f_on} is selected as 25 V on the experimental prototype. Similar to Buffer2, the

negative pole of Buffer3 is connected to V_{dr_off} which is -5 V. Therefore, the adjustment range of V_{int} is from 0 V to 15 V.

Table 3-1 The experimental prototype configuration.

Parts		Part number/parameters
Multi-level active gate driver	Buffer1-3	IXYS IXDN609SI
	Op1	AD817A
	Op2	TI LM675
	Digital isolator	TI ISO7420
	Isolated power supply	Murata MGJ2D122005SC
	Digital isolator	TI ISO7420
	R_g	Four 20 Ω 1210 thin film
	Local controller	Altera 10M08SCU169 FPGA
Double pulse testbed and MOSFET	L	230 μH
	L_d	6 nH
	L_s	9 nH
	C_L	32 pF
Measurement	V_{ds} probe	Tektronix P5120
	V_{gs} probe	Tektronix P2220
	I_{ds} probe	T&M SDN-414
	Oscilloscope	Tektronix MDO4034B

As introduced in Chapter 2, V_{int} is generated by the adjustable voltage regulator and it should be higher than $V_{miller1}$. Since V_{int} is adjusted through changing the resistance connected in the analog adder circuit, the selection of the resistance should follow Eq. (2-1). Also, the V_{int} for slower turn-off is lower than the V_{int} for the slower turn-on. The V_{int} adjustment step length is related with R_1 of Figure 2-1. If the step is too small, the total adjustable range of V_{int} is shortened. Therefore, the design should consider the tradeoff between adjustment resolution and range. In the experimental prototype, a 6-channel digital isolator is utilized. Therefore, six resistors are connected and the adjustable voltage regulator can provide 64 adjustable steps which guarantee the adjustable resolution for V_{int}.

The bandwidth is another consideration for the adjustable voltage regulator design. The bandwidth of op-amps Op1 and Op2 should be at least ten times higher than the switching frequency of the MOSFETs. Otherwise, the adjustable voltage regulator will not be able to change V_{int} in prior to the switching time.

The reversed flowing gate current can be sunk by the current sinking circuit. The most significant components are the R_a resistance and V_{BE_on} of Q1. The selection of Q1 should follow Eq. (2-3). Since the value of R_a influences the threshold voltage of triggering, it cannot be too low. Meanwhile, it is connected in the gate loop, a large R_a increases high impedance into the gate loop and reduce the switching speed. Therefore, design of R_a should comprehensively consider the gate loop impedance and the current sinking capability. [2.1] demonstrates the detailed design consideration of the current sinking circuit.

3.1.2 Measurement for SiC

Due to the fast switching speed of SiC power devices, the measurement should be paid special attention. Inaccurate measurement may introduce serious EMI noise. For the DPT, V_{ds}, I_{ds}, and V_{gs} are the signals of interest. The measurement of V_{ds} requires high bandwidth high voltage rating probes. V_{gs} is generally 25 V level, so enough measurement bandwidth is the only requirement of V_{gs}.

3.1.2.1 ***Measurement bandwidth***

The oscilloscope bandwidth should be considered first. According to Nyquist theorem for digital acquisition, the selection of the oscilloscope sampling rate and measurement bandwidth should follow Eq. (3-4) and (3-5) [3.9].

$$Sampling\ \ rate \geq \frac{10}{\min\left(t_{\text{rise}}, t_{\text{fall}}\right)} \tag{3-4}$$

$$Bandwidth \geq \frac{0.35}{\min\left(t_{\text{rise}}, t_{\text{fall}}\right)} \tag{3-5}$$

In Eq. (3-4) and (3-5), t_{rise} and t_{fall} are the rise time and fall time of the signal respectively. The bandwidth of the voltage probe should be calculated with Eq. (3-6).

$$\min\left(t_{\text{rise}}, t_{\text{fall}}\right) \geq \frac{0.35}{\sqrt{f_{\text{BW,scope}}{}^{2} + f_{\text{BW,probe}}{}^{2}}}, \tag{3-6}$$

where $f_{\text{BW,scope}}$ and $f_{\text{BW,probe}}$ are the bandwidth in frequency of the oscilloscope and probe.

3.1.2.2 *Voltage probe connection*

(a)

(b)

Figure 3-3 Voltage probes connection. (a) Alligator connection. (b) Wire wound connection.

There are different voltage probes on the market: active probe and passive probe. The isolated voltage probe provides galvanic isolation, but the limited bandwidth and long connections make it not appropriate for the DPT. Generally, passive voltage probes have higher bandwidth. Most

passive voltage probes provide an alligator clip as the negative pole of the probe, which is as shown in Figure 3-3 (a).

Alligator clips can only be utilized to measure the low frequency signals due to its long wire. However, for the DPT, the ringing on the waveform, which are usually MHz level, are also signals of interest. Thus, it is preferred to use a wire wound connection which is shown in Figure 3-3 (b) to shorten the measurement loop [3.9]. The wire wound connection is soldered on the PCB. The probe tip is placed on the measurement point. Therefore, the parasitics in the measurement loop are reduced.

Wire wound connection is a cheap solution for the high bandwidth measurement. However, for some occasions, soldering is not allowed for the PCB. High voltage passive probes with BNC adaptors, as shown in Figure 3-4, can be used for the V_{ds} measurement in this situation. Tektronix has a commercialized BNC adaptor on the market, i.e., Tektronix 013029102, which can be connected with TPP0850 voltage probe. It should be paid attention since the maximum voltage of the BNC connector is generally limited (≤600 V). Therefore, it is not suitable for the measurement of DPT when V_{BUS} is higher than 600 V [3.9]. Using a voltage divider circuit with the BNC connector can be an option for V_{ds} measurement.

V_{gs} measurement does not require high voltage rating probe. However, it still requires high measurement bandwidth. For some cases, the size also matters. MCX connector and tips are recommended due to its compact size and ultra-high bandwidth. MCX connector is designed for the radiative frequency application (≥1 GHz). Tektronix has commercialized MCX connector tips on the market, i.e., 206-0663-xx. It can be connected to TPP1000 voltage probe.

Figure 3-4 The Tektronix 013029102 BNC connector adaptor [3.10].

3.1.2.3 *Current probe connection*

Similar to the voltage measurement, current measurement can be classified into two categories: isolated and non-isolated. Isolated measurement is based on Hall-Effect or Rogowski coil. The bandwidth is generally not as high as the non-isolated current probe. Pearson has a very high bandwidth (≥200 MHz) products such as Pearson 6596. A Rogowski coil can be used for very high current measurement. However, the bandwidth of most Rogowski coil products on the market is 30 MHz maximum.

Non-isolated current probes are generally very low ESL resistors such as shunt resistors. The bandwidth of shunt resistors can be as high as 1 GHz level. However, grounding point should be paid special attention when using shunt resistors.

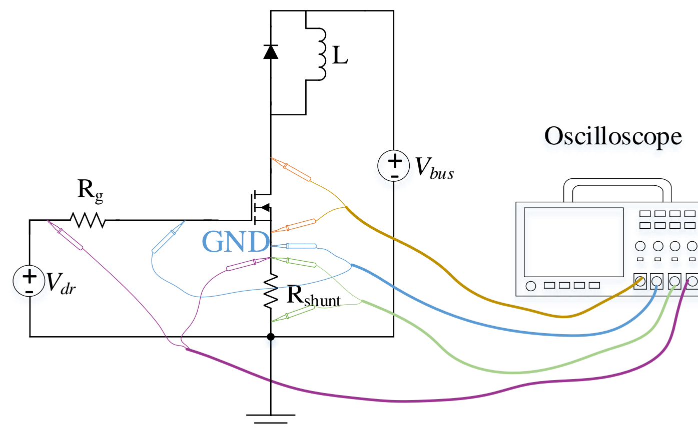


Figure 3-5 I_{ds} measurement with a shunt resistor.

From Figure 3-5, since the ground of the all channels of an oscilloscope is tied together, the negative poles of all the passive probes should be connected also.

3.2 Experimental results

3.2.1 Output waveform under light load

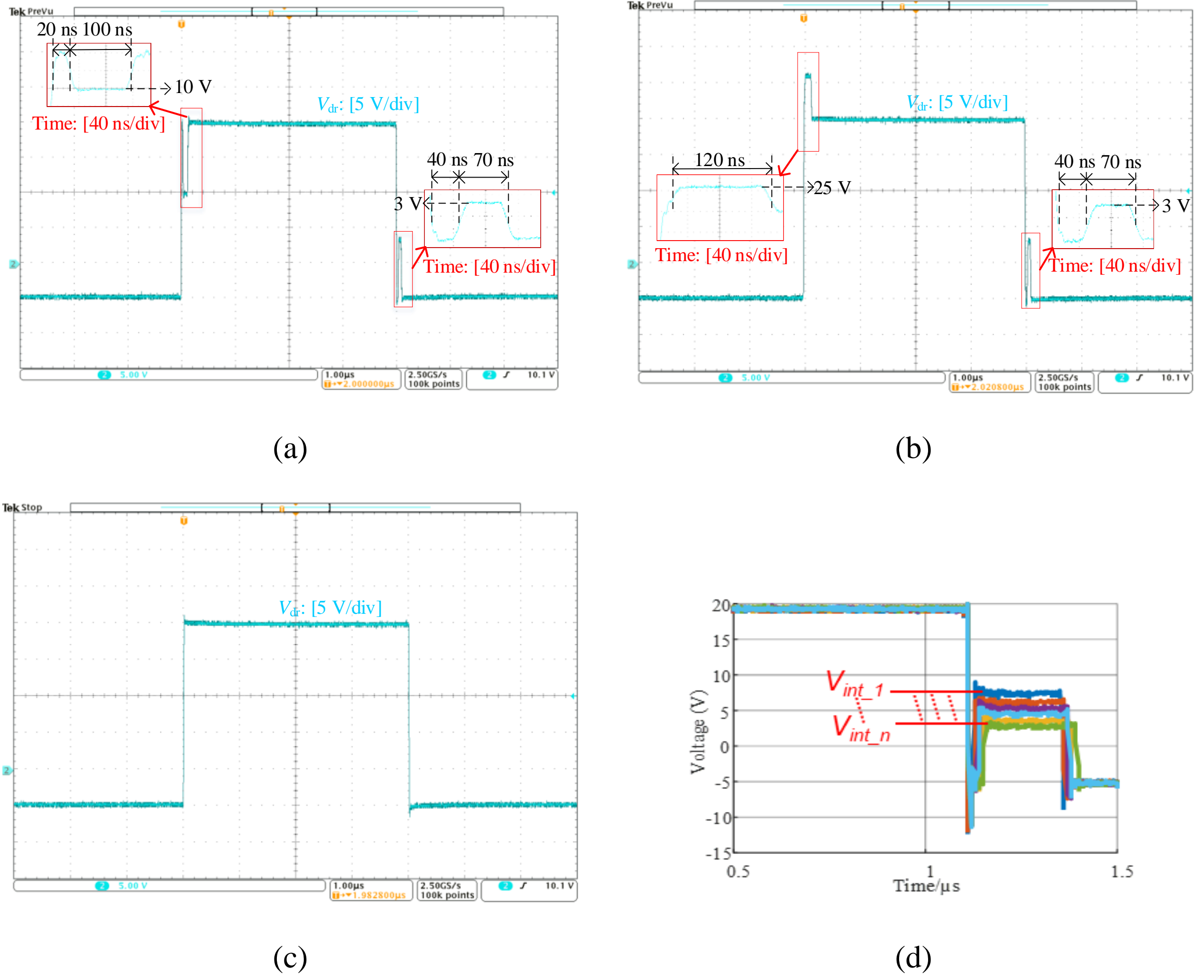


Figure 3-6. Several combining modes of gate driver output waveform. (a) Slower turn-on and slower turn-off. (b) Faster turn-on and slower turn-off. (c) Normal turn-on and normal turn-off. (d) Adjustable V_{int} on the slower turn-off waveform.

To verify that the proposed circuit can generate the proposed V_{dr} profile in the aforementioned sections, the driver is connected to light load. The experimental results of three combination of

driving modes are given in Figure 3-6. The light load is a 1 nF capacitor in parallel with a 20 kΩ ceramic resistor, which can simulate the gate junction of the SiC MOSFET.

Figure 3-6 (a) shows the waveform of slower turn-on mode with the slower turn-off. Figure 3-6 (b) shows the results of faster turn-on with the slower turn-off mode. Figure 3-6 (c) is the normal turn-on and turn-off mode output waveform. From Figure 3-6 (d), V_{int} levels and the duration of every substage of the driver voltage can be tuned by the FPGA controller. Due to 300 MHz clock frequency of the FPGA controller, the minimum time adjustable step is 3.3 ns. For most SiC power devices, the substages of the switching transient are longer than 10 ns. Therefore, the FPGA is fast enough. Figure 3-6 validates that the proposed AGD can generate the proposed multi-level V_{dr} profile.

3.2.2 DPT results of faster turn-on mode

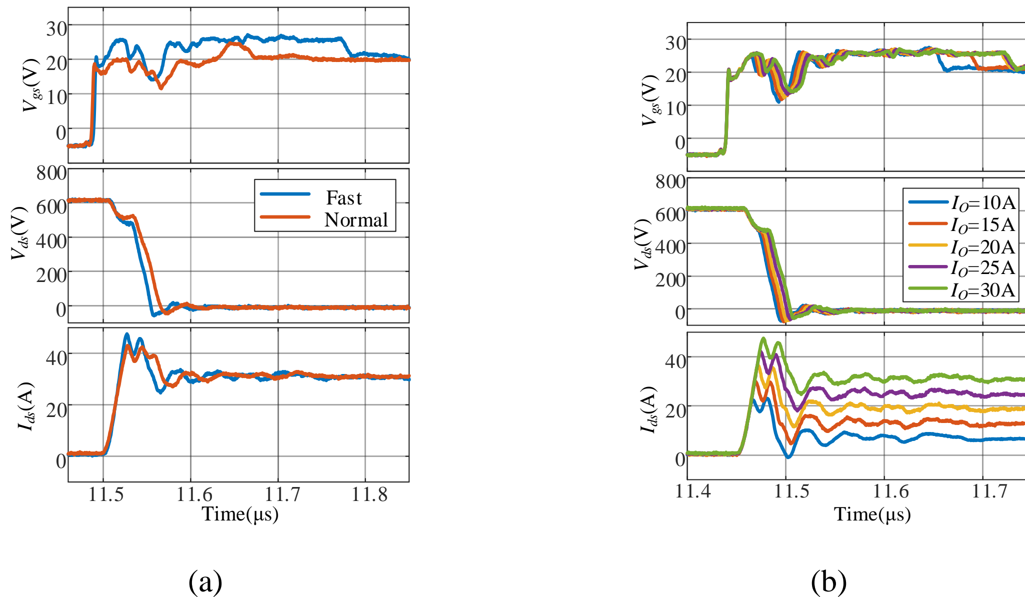


Figure 3-7 The experimental results of faster turn-on mode. (a) Comparison of faster turn-on model and normal turn-on mode. (b) Comparison of faster turn-on mode under different load current.

The DPT is conducted under V_{ds} = 600 V and I_{ds} = 30 A. DUT is SCH2080KE SiC MOSFET. Two groups of DPTs are conducted and compared: faster turn-on mode and conventional gate driver mode. t_{int} is set to be 340 ns while the turn-on process is only 80 ns. In fact, t_{int} should be 80 ns to only cover the turn-on process. However, during the turn-on transient, V_{dr} is affected by the gate current and V_{f_on} is not obvious. Therefore, t_{int} is set to be longer than the whole switching process to show a higher V_{dr} than V_{dr_on}.

Table 3-2 The comparison of faster turn-on mode and normal turn-on mode.

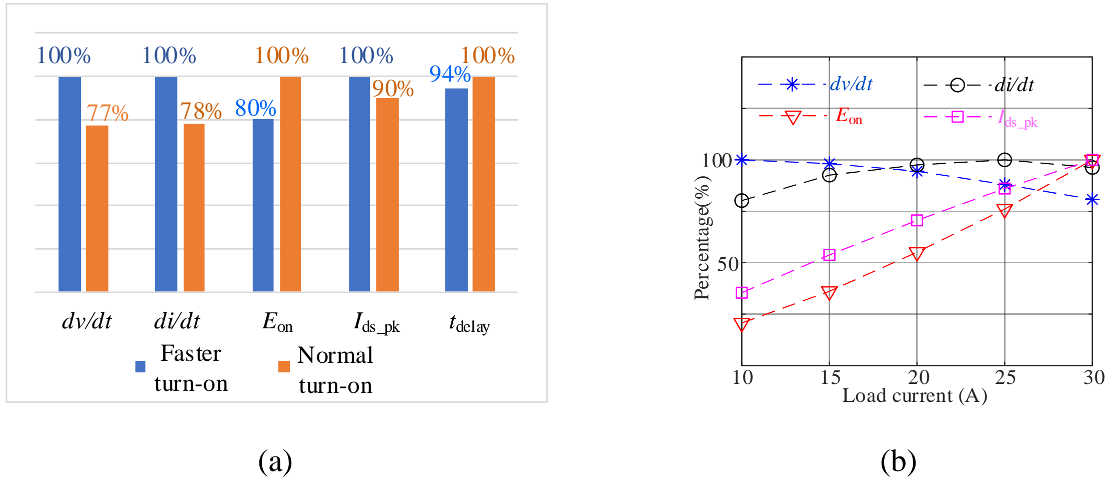
Parameters	Value		
	faster turn-on	Normal turn-on	Percentage
dv/dt	23.06 V/ns	17.75 V/ns	30%
di/dt	2.323 A/ns	1.813 A/ns	28%
E_{on}	619 μJ	770 μJ	-20%
I_{ds_pk}	47.6 A	43 A	11%
t_{f_on}	43 ns	57 ns	-25%

The experimental results of faster turn-on mode is shown in Figure 3-7. Figure 3-7 (a) shows the comparison of DPT results of faster and normal turn-on mode. I_O is 30 A and V_{BUS} is 600 V for these two scenarios. Figure 3-7 (b) shows the faster turn-on mode under different I_O. V_{BUS} = 600 V and V_{f_on} = 25 V for all the DPTs groups.

The data from Figure 3-7 (a) is listed in Table 3-2 and plotted in Figure 3-8 (a). To better compare the two conditions, all the indices shown in Figure 3-8 (a) are percentage that referred to the maximum value in the term.

From Figure 3-8 (a), in faster turn-on mode, the energy losses are reduced by 20% and t_{f_on} is shortened by 25%. However, *dv/dt* is increased by 23%, I_{ds_pk} is increased by 10%, and *di/dt* by 22%. The experimental results as shown in Figure 3-8 have verified that faster turn-on mode can

speed up the turn-on process. It indeed reduce energy losses, but it increases the EMI noise. The parameters in Figure 3-7 (b) are given in Table 3-3 and plotted in Figure 3-8 (b).



(a) (b)

Figure 3-8 Analysis of the DPT results. (a) The comparison of the faster turn-on and normal turn-on. (b) Faster turn-on mode under different load current conditions.

Table 3-3 The comparison of faster turn-on mode under V_{int} = 3 V and different load current.

Parameters	**Io**				
	10 A	**15 A**	**20 A**	**25 A**	**30 A**
dv/dt (V/ns)	27.1	26.7	25.9	24.5	22.93
di/dt (A/ns)	1.7	1.9	1.98	2.02	1.96
E_{on} (μJ)	234.7	313.9	411.7	519.3	642.3
I_{ds_pk} (A)	23	30	36.4	42.3	47.6

From Figure 3-8 (b), with higher I_O, E_{on} increases. However, the *dv/dt* reduces with I_O. The explanation can be referred to Section 2.3. With higher I_O, according to Eq. (2-7), $V_{miller1}$ increases and the gate current that charges C_{iss} changes. Therefore, slew rate changes.

3.2.3 DPT results of slower turn-on mode

The slower turn-on mode DPTs results are shown in Figure 3-9. Figure 3-9 (a) depicts the experimental results under V_{BUS} = 600 V, I_O = 30 A, and various values of V_{int}. Figure 3-9 (b) shows the experimental results under V_{BUS} = 600 V and V_{int} = 15 V, but different I_O.

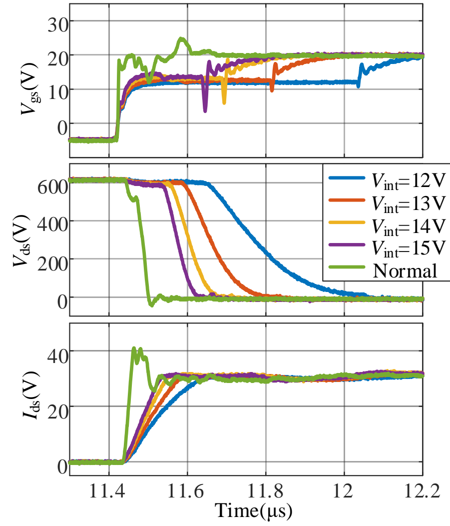


Figure 3-9 The experimental results of slower turn-on mode under different V_{int}.

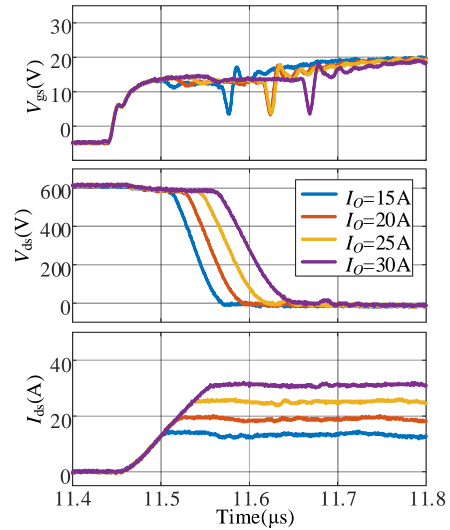


Figure 3-10 The experimental results of slower turn-on mode under different I_O.

The data extracted from Figure 3-9 (a) is listed in Table 3-4 and plotted in Figure 3-11 (a).

Table 3-4 Slower turn-on mode under different V_{int} levels.

Parameters	***V_{int}***				
	12 V	**13 V**	**14 V**	**15 V**	**Normal (20V)**
dv/dt (V/ns)	2.06	3.83	5.76	7.64	18.3
di/dt (A/ns)	0.16	0.22	0.28	0.34	1.17
E_{off} (μJ)	4712	2831	2114	1626	749
t_{int} (ns)	530.1	362	202.4	159.2	57.6

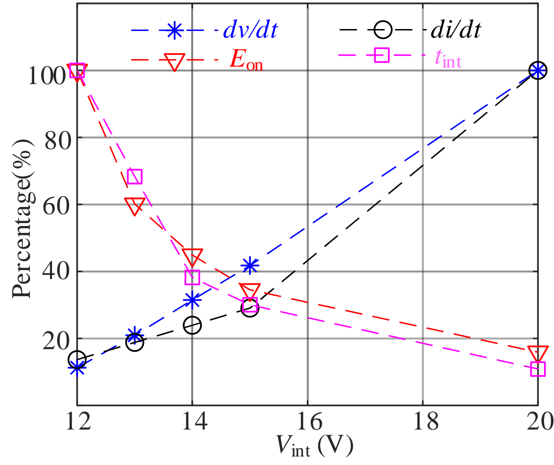


Figure 3-11 Analysis of the slower turn-on experimental results under different V_{int}.

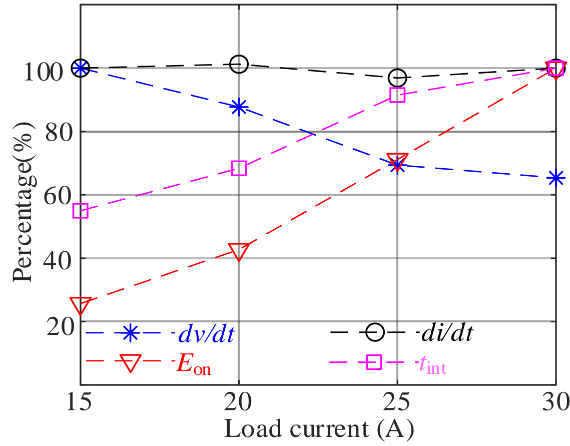


Figure 3-12 Analysis of the slower turn-on experimental results under different I_O.

Table 3-5 Slower turn-on mode under different load current I_O.

Parameters	I_O			
	15 A	**20 A**	**25 A**	**30 A**
dv/dt (V/ns)	10.91	9.57	7.57	7.13
di/dt (A/ns)	3.21	3.25	3.11	3.21
E_{on} (μJ)	442	735	1224	1720
t_{int} (ns)	90.4	112.4	150.4	164.4

From Figure 3-11, the proposed AGD can slow down the turn-on process with lower V_{int}. Accordingly, I_{ds} overshoot is decreased to zero. However, it inevitably increases t_{int} and E_{on}.

Therefore, the value of V_{int} should be carefully selected for the optimizing the switching process. The data of Figure 3-9 (b) is given in Table 3-5 and plotted in Figure 3-11 (b).

From Figure 3-12, with the same V_{int} level, *di/dt* is almost the same when I_O is different. However, the *dv/dt* reduces with higher I_O. This phenomenon is similar with faster turn-on mode. It can be explained with the same reason faster turn-on mode as well.

3.2.4 DPT results of slower turn-off mode

The slower turn-off mode DPTs results are shown in Figure 3-13. From the results, when the V_{int} increases, the peak V_{ds} and *dv/dt* decreases. Therefore, the proposed AGD can effectively slow down the turn-off switching speed and reduce the EMI noise without increasing t_{delay}. From Figure 3-13, higher V_{int} increases the energy losses in the turn-off process. Moreover, it also reduces *di/dt* and the peak value of V_{ds} is reduced.

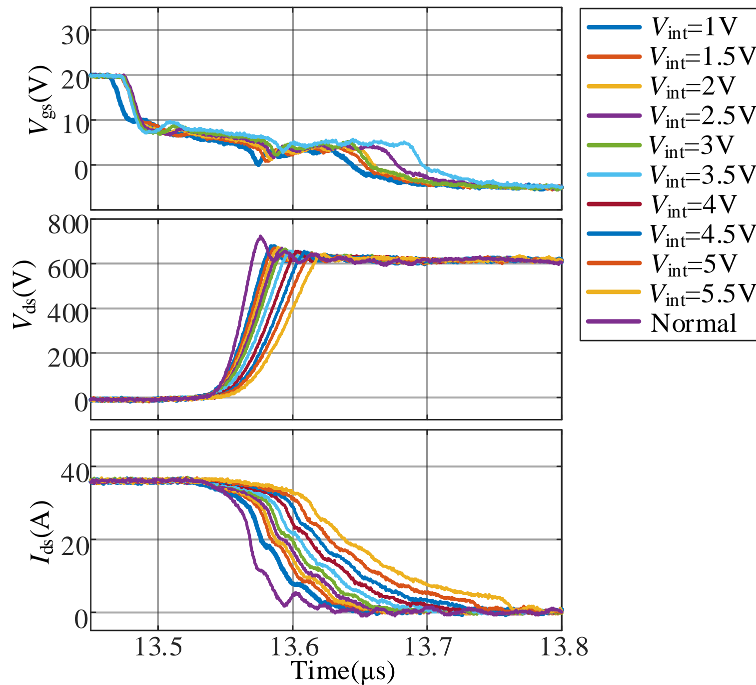


Figure 3-13 The experimental results of slower turn-off mode under different V_{int}.

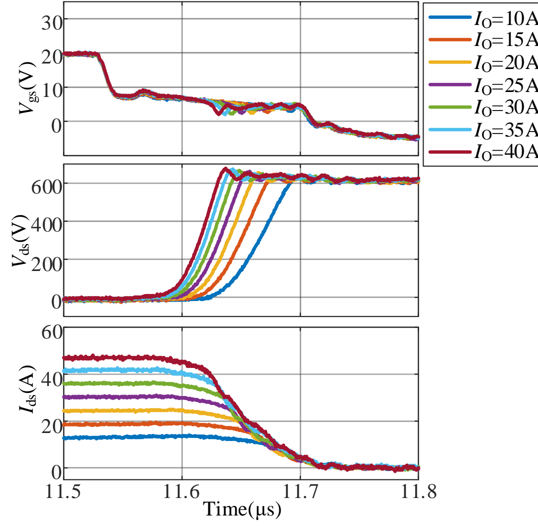


Figure 3-14 The experimental results of slower turn-off mode under different I_O.

The indices extracted from Figure 3-13 are listed in Table 3-6. Figure 3-14 shows the DPTs results of the AGD under different I_O in slower turn-off mode. The indices extracted from Figure 3-14 are listed in Table 3-7.

Table 3-6 Slower turn-off mode under different V_{int} levels.

V_{int} (V)	***Parameters***				
	***dv/dt* (V/ns)**	***di/dt* (A/ns)**	**E_{loss} (μJ)**	**V_{ds_pk} (V)**	**t_{int}(ns)**
Normal	22.32	0.86	289	724	38.4
1	15.9	0.62	530	678	60
1.5	15.43	0.51	596	670	69.6
2	15.12	0.48	641	674	74
2.5	14.52	0.47	690	666	77.2
3	13.85	0.46	716	656	82.4
3.5	12.76	0.43	819	656	88.4
4	12.21	0.41	895	656	93.6
4.5	11.68	0.34	1012	648	106.8
5	11.16	0.31	1127	648	117.2
5.5	10.24	0.27	1287	640	135.2

Table 3-7 Slower turn-off mode under different load current.

I_O (A)	**Parameters**				
	***dv/dt* (V/ns)**	***di/dt* (A/ns)**	**E_{loss} (μJ)**	**V_{ds_pk} (V)**	**t_{int}(ns)**
10	10	0.27	202	634	71.6
15	11.17	0.24	337	646	88
20	12.25	0.3	470	654	90
25	13.02	0.34	623	662	93
30	13.85	0.36	813	666	103
35	14.04	0.39	1023	674	110
40	14.37	0.40	1196	678	118

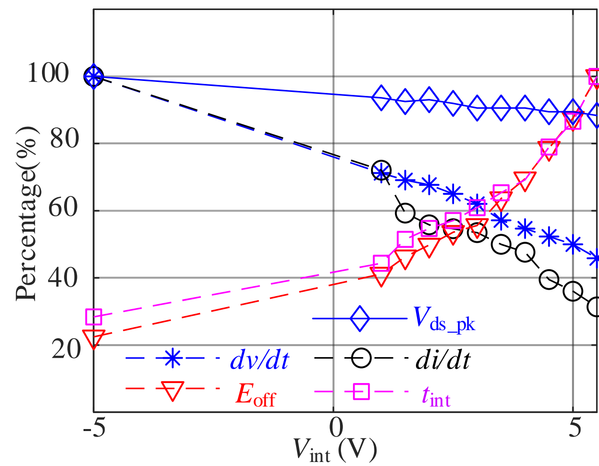


Figure 3-15 Analysis of the slower turn-off experimental results under different V_{int}.

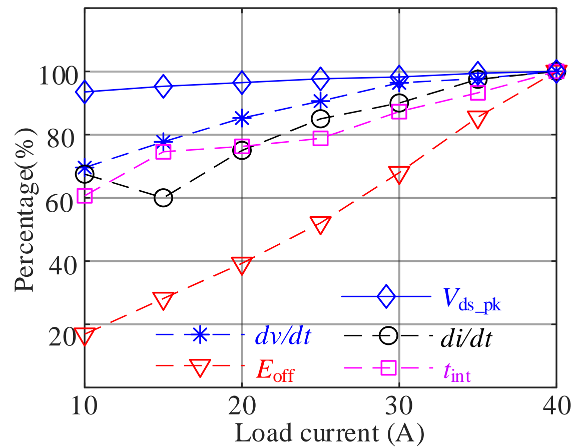


Figure 3-16 Analysis of the slower turn-off experimental results under different I_O.

Figure 3-15 clearly shows the trend observing from the data of Table 3-6 and Table 3-7. From Figure 3-15, higher V_{int} can increase the turn-off speed. Figure 3-16 is the analysis results of the

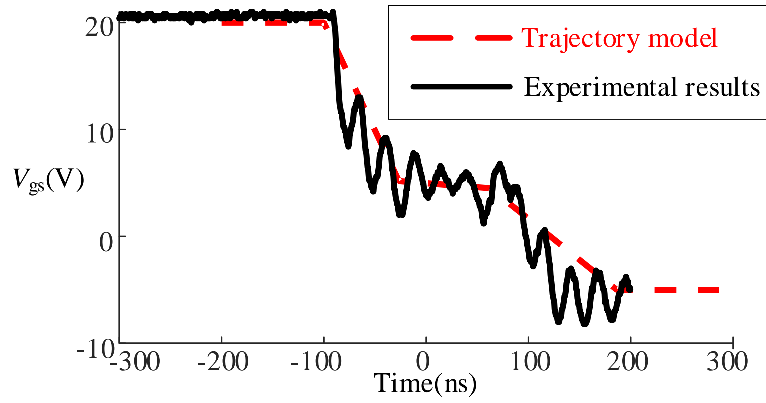
slower turn-off mode under different load current. From Figure 3-16, E_{off} increases with I_O. It has verified that with the same V_{dr}, the slew rate increases can be different under different I_O values. Therefore, the on-line feedback control is necessary.

3.3 Comparison of DPT results and the trajectory model under slower turn-off mode

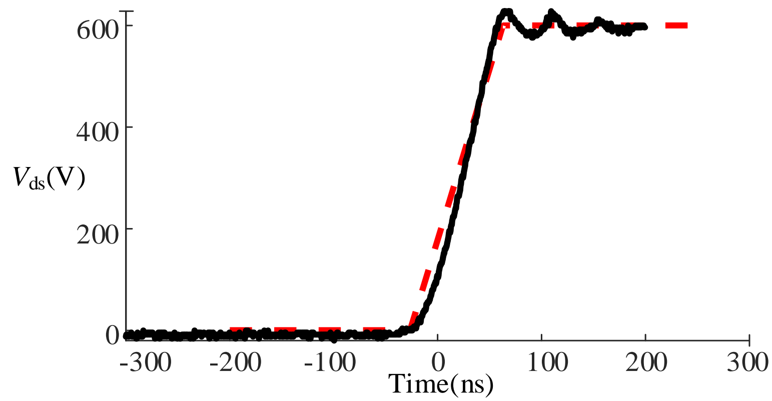
In this section, the DPT results and the results of trajectory model will be introduced. Because the analysis of turn-on process is similar with turn-off process, this dissertation will only discuss compare the turn-off process. The relationship between the various variables and the switching behavior has been explained in Chapter 2. This section will first validate that the trajectory model emulation results match the DPT results. Then the trend that how different variables change the switching behaviors will be compared. Based on the analysis of the DPT results and the trajectory model, several scenarios for the V_{int} selection will be introduced for better understanding of the design optimization consideration.

3.3.1 Comparison of trajectory model and experimental study

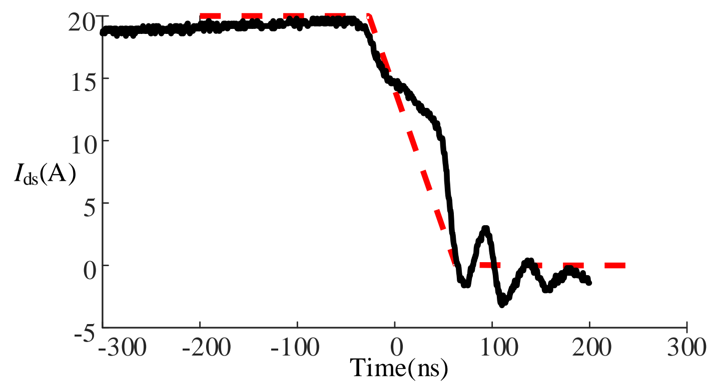
The experimental results and the trajectory model analysis results under the same conditions: V_{BUS} = 600 V, I_O = 20 A and V_{int} = 4.5 V are compared in Figure 3-17. From the comparison results, the trajectory model (the dashed curves) can perfectly track the waveform of the experimental results (the solid curves). There are slight differences between I_{ds} curves of the model and experimental results. This differences occur for the sake of non-linear V_{ds}. The trajectory model uses the average *di/dt* and *dv/dt* to simplify the calculation process. However, because the junction capacitance and gfs are not linear during the switching process, V_{ds} and I_{ds} are not straight lines.



(a)



(b)



(c)

Figure 3-17. The comparison of the trajectory model results and the experimental results. (a) gate-source voltage V_{gs}, (b) drain-source voltage V_{ds}. (c) drain-source current I_{ds}.

3.3.2 The dv/dt Consideration

As introduced in Chapter 1, *dv/dt* is the foremost consideration since it is the key factor to determine the EMI noise in the converter and feedback gate current [1.41]. The DPTs were conducted under bus voltages of V_{BUS} = 400 V, 500 V, and 600 V respectively. The *dv/dt* values of different load current and V_{int} are recorded and plotted as shown in Figure 3-18. When I_O increases, the *dv/dt* increases. This trend is in accordance with the trajectory model analysis results in Figure 2-11. It can be explained as follows: Since $V_{miller1}$ increases with I_O, as shown in Eq. (2-7). Therefore, it is farther away from V_{dr_off} and the current for discharging C_{gs} and C_{gd}. The turn-off transient is shortened and *dv/dt* will increase. However, with higher V_{int}, the *dv/dt* decreases. This is explained by the inspection of Eq. (2-7) and (2-24).

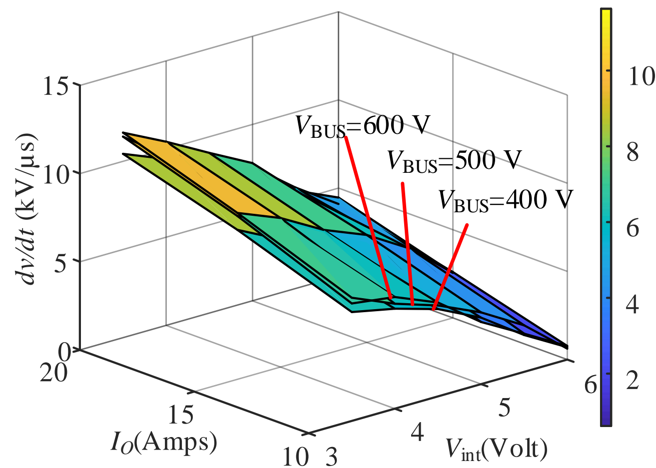


Figure 3-18 The experimental results of *dv/dt* of 3-L turn-off.

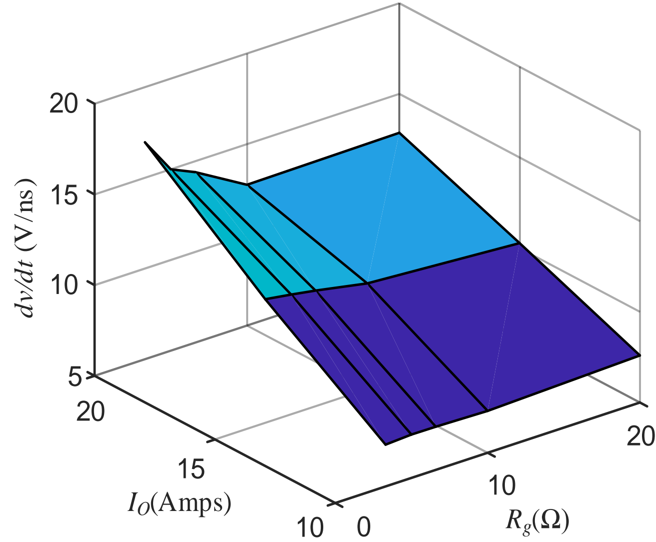


Figure 3-19 The experimental results of *dv/dt* of conventional turn-off under different R_g.

In Figure 3-18, the *dv/dt* values of V_{BUS} = 400 V, 500 V, and 600 V are very closed. It can be explained with Eq. (2-24). The discharging speed of C_{gd} determines the *dv/dt*. From $C_{gd} = \frac{C_{gd0}}{\sqrt{1+V_{ds}/\phi_0}}$, there is no significant change on C_{gd} changes when V_{BUS} ranges from 400 V to 600 V.

As mentioned in Chapter 1, the traditional method to adjust the slew rate is changing the gate resistance. Changing R_g has the same slew rate adjustment effect with the multi-level V_{dr} method. In this section, DPTs with conventional gate driver under different R_g is conducted and the experimental results are compared with AGD under different V_{int}. The purpose is to compare the slew rate control effect of these two methodologies. The *dv/dt* of the control groups plotted as shown in Figure 3-19. Figure 3-19 has validated using a high R_g can effectively reduce the *dv/dt* of turn-off process. Nonetheless, the slew rate controllability of conventional gate driver with various R_g is not as ideal as the proposed AGD methodologies. This is more serious when I_O is

low. In other words, it requires very high R_g to realize the same slew rate control effect with the multi-level V_{dr} method.

3.3.3 The di/dt consideration

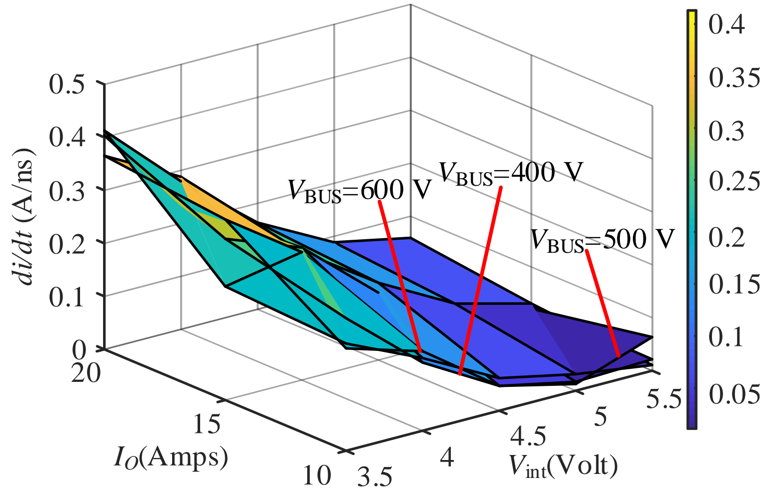


Figure 3-20 The *di/dt_I* under different V_{int}.

The slew rate of the I_{ds}, or *di/dt*, is the reason of overshoot on V_{ds}. For better understanding of the trend, in this dissertation, the DPTs with the proposed AGD under different V_{int}, I_O and *di/dt* are conducted and shown in Figure 3-20.

Similar to the theoretical analysis in Section 2.3.2.2, the *di/dt_I* decreases with higher V_{int}. I_O also impacts *di/dt_I* and *di/dt_II*. It should be noted that, in the range of 400 V to 600 V, V_{BUS} does not change *di/dt* significantly. Since the *di/dt_II* is highly affected by the ringings on the switching waveform, this dissertation will only discuss *di/dt_I*. Figure 3-20 only shows first *di/dt* period, i.e., *di/dt_I* since *di/dt_II* is difficult to capture.

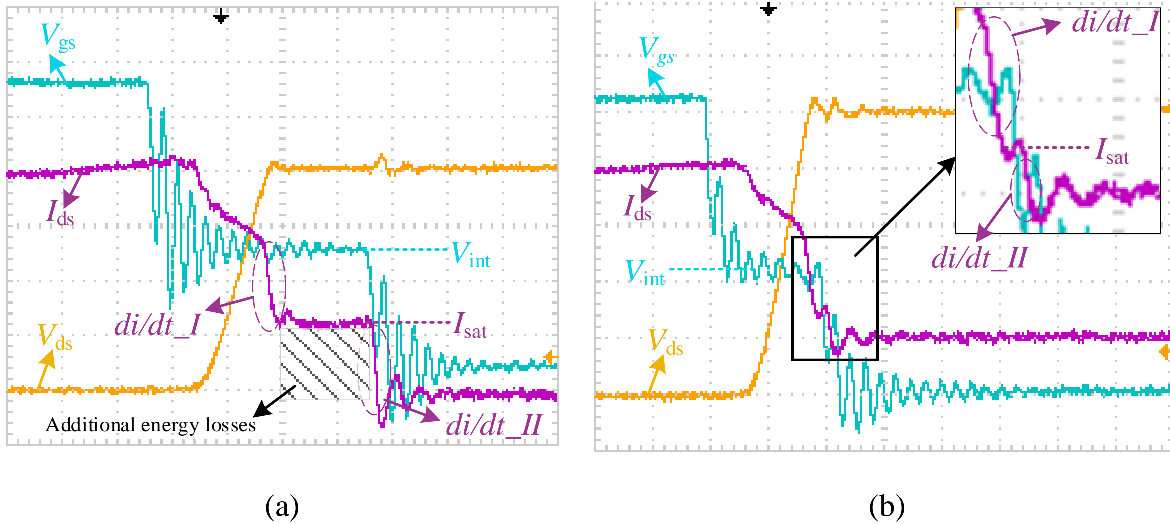


Figure 3-21 The waveforms of 3-L turn-off process when MOSFET is in Situation II. (a) A non-ideal turn-off profile: Time (100 ns/div), V_{ds} (100 V/div), V_{gs} (5 V/div), and I_{ds} (2.5 A/div). (b) An ideal turn-off profile: Time (100 ns/div), V_{ds} (100 V/div), V_{gs} (5 V/div), and I_{ds} (5 A/div).

From Figure 3-20, during V_{int}, the gate driver is able to fine tune *di/dt*. However, if V_{int} is higher than V_{th}, i.e., in Situation II, I_{ds} is clamped at the I_{sat}. I_{ds} can only drop from I_{sat} to zero after t_{int} when V_{dr} changes from V_{int} to V_{dr_off}. After Stage VIII, the power MOSFET is shut down completely and the slew rate of the second current fall period is denoted by *di/dt_II* in Figure 3-21(a). An good example of a non-optimal choice of V_{int} is shown in Figure 3-21(a). At the end of *di/dt_I*, I_{ds} is approaching I_{sat}. If V_{dr} keeps at $V_{int} > V_{th}$, I_{ds} will continue to be I_{sat}. This will generate extra switching losses. It should be noted that a low V_{ds} voltage overshoot is observed when *di/dt_II* occurs.

In Figure 3-21(a), the shadowed area is the period for the saturation current. It clearly depicts that a non-ideal V_{dr} profile may lead to extra energy losses. As explained in the former sections, this phenomenon occurs because the MOSFET stays in the saturation condition and the energy losses of this condition will be extremely high. It is essential to prevent the extra switching losses

caused by I_{sat}. V_{dr} should be changed to V_{dr_off} immediately after I_{ds} drops to I_{sat} as shown in Figure 3-21(b).

3.3.4 Turn-off duration

The turn-on/off delay duration affects the total switching transient duration. It is preferred to be shortened since there is no EMI noise in the turn-on/off delay substage. The most popular AGD technology available on the market is the AGD with two-stage turn-off [1.59]. This driver voltage profile is also widely used for soft-turn-off of desaturation protection that is integrated on the gate driver. Several examples are TI ISO5851 [1.34] and Avago ACPL-339J. Figure 3-22 shows the two-stage turn-off profile which uses V_{int} during all the turn-off process, while 3-L turn-off uses V_{dr_off} during this period[1.59]. It also has an intermediate voltage stage, same with V_{int} with the proposed AGD, to reduce the switching speed and suppress the EMI noise and overshoot V_{ds}. However, most desaturation protection gate driver does not adjust intermediate voltage actively. Additionally, the proposed AGD has shorter turn-off delay time than the two-stage turn-off.

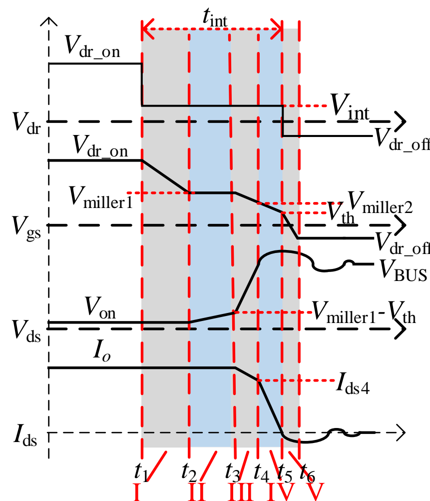


Figure 3-22 Switching waveform of a two-stage turn-off.

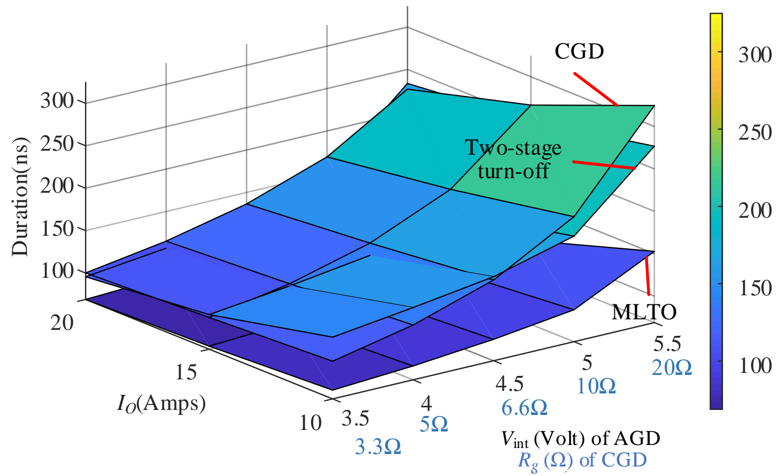


Figure 3-23 The comparison of turn-off duration of AGD and conventional gate driver.

From Figure 3-23, two-stage turn-off has longer turn-off delay duration than the proposed AGD. The phenomenon can be explained with Eq. (2-19). For the 3-L turn-off, V_{dr_off} is used for this substage while two-stage turn-off uses V_{int}. Therefore, for the reason that the turn-off delay of the proposed AGD is shorter, it can effectively shorten the total turn-off process duration. Figure 3-23 compares the total turn-off duration of the two-stage turn-off, the proposed AGD, and a conventional gate driver. From Figure 3-23, it is obvious that the proposed AGD has shorter turn-off process duration than the other two methods. This has been explained in the former section. In fact, the turn-off delay duration of the two-stage turn-off method is very close to the conventional gate driver.

3.3.5 Saturation current I_{sat}

The working boundary of the proposed AGD is relevant with I_{sat}. As illustrated in Figure 3-21, when V_{int} is higher than V_{th}, the AGD is not able to completely shut down the MOSFET and it leads to high extra energy losses. The DPTs results that depicts the relationship of I_{sat} *vs.* V_{BUS} and V_{int} can be plotted in Figure 3-24.

From Figure 3-24, I_{sat} is not influenced significantly by V_{BUS} at low level of V_{int}. However, at high levels of V_{int} , the influence of V_{BUS} on I_{sat} is obvious. This can be explained with Eq. (2-32). Figure 3-24 reveals the working zone of the propose AGD, i.e., the space above the surface of I_{sat} in Figure 3-24.

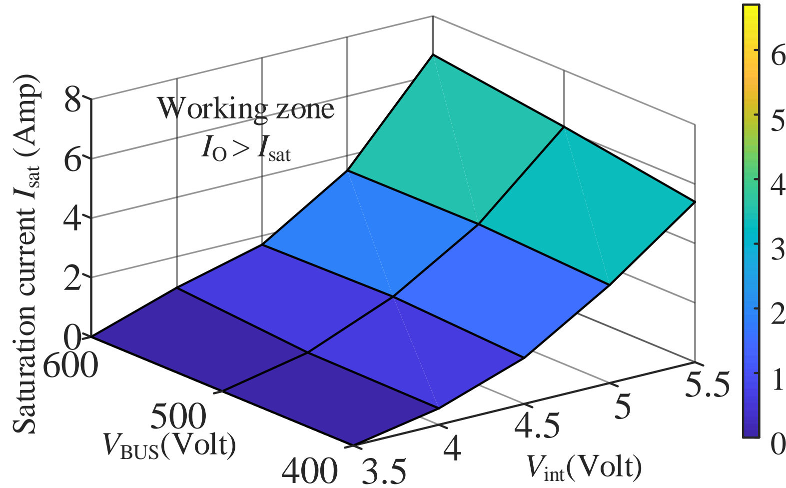


Figure 3-24 The saturation current of different V_{int}.

It can be explained as following: when I_O is lower than I_{sat}, the chosen level of V_{int} cannot turn off the MOSFET completely. In contrary, I_{ds} will continue increasing. In other words, *di/dt*, V_{ds} overshoot, and the energy losses are uncontrolled. Thus, the V_{dr} profile of the proposed AGD is not helpful for reducing the slew rate when $I_O < I_{sat}$. When I_O is too low and stay out of the working zone shown in Figure 3-24, V_{int} needs to be reduced to move the operation point to the left.

3.3.6 Energy losses E_{off}

The energy losses extracted from the DPT results under V_{BUS} = 400 V, 500 V, and 600 V are plotted in Figure 3-25.

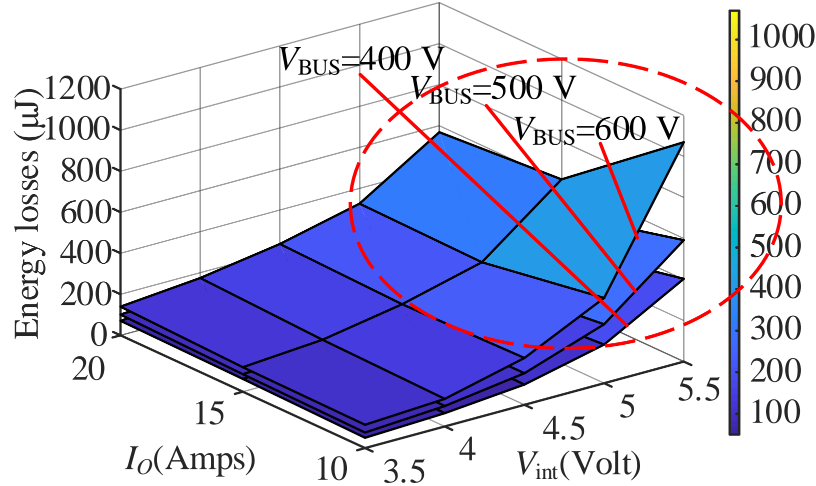


Figure 3-25 The comparison of energy losses during the turn-off transient.

From Figure 3-25, the turn-off losses increases when V_{int} increases. This is similar with the theoretical analysis results in the aforementioned sections in Eqs. (2-25) - (2-26) and Eqs. (2-37) - (2-39). The relationship between I_{O} and E_{off} is not linear. In other words, in some conditions, high I_O may not increase E_{off}. From Eqs. (2-37) - (2-39), when $V_{\text{int}} < 4.5$V, increasing I_{O} can lead to the increase of E_{off}. When $V_{\text{int}} > 4.5$ V, E_{off} is dramatically increased with low I_{O}. It is shown in the area in the red circle of Figure 3-25. This phenomenon can be explained with the following theory.

The total turn-off losses is a variable that is determined by V_{BUS}, I_{O}, and t_{int} comprehensively. As shown in Figure 3-25, when V_{BUS} and the other variables are constant, higher I_{O} causes higher *dv/dt*, so t_{VR} is shortened t_{VR}. The reasons are concluded as below.

When $V_{\text{int}} < 4.5$ V, increasing of I_{O} dominates the downward trend; the increase of I_{O} will lead to an increase of E_{off}.

When V_{int} is higher than 4.5 V, the E_{off} is already very high due to the long t_{off}. In this case, the decreasing of toff dominates the decreasing of E_{off}.

3.4 Conclusions of the experimental study

3.4.1 Conclusions of the experimental study

In this chapter, the hardware design consideration of SiC MOSFET is given. The experimental prototype is built to conduct the DPTs. The DPTs results are given and compared with the theoretical analysis results in Chapter 2. The theoretical analysis of the turn-on process can use the same methodology. The observations from the comparison results for turn-off process are summarized below.

1. V_{int} is the most significant factor that balance power efficiency and the EMI noise. A higher V_{int} can effectively reduce *dv/dt* and power efficiency. However, the relationship of *di/dt* and V_{int} should be divided into two specific situations. In Situation I, i.e., $V_{int} \leq V_{th}$, high V_{int} can effectively suppress *di/dt*. In Situation II, i.e., $V_{int} > V_{th}$, I_{ds} falling can be divided into two stages, i.e. *di/dt_I* and *di/dt_II*. In Situation II, high V_{int} decreases *di/dt_I*, but it also increases *di/dt_II*. Therefore, the calculation of *di/dt* should follow Eqs. (2-34) - (2-35).

2. I_O affects the Miller plateau voltage $V_{miller1}$ and $V_{miller2}$, so it also impacts the range of V_{int}. Eq. (2-5) reveals that high I_O leads to high $V_{miller1}$. Therefore, with the same level of V_{int}, higher I_O results in higher *dv/dt*. Meanwhile, with higher I_O, if the *dv/dt* is maintained constantly, a higher V_{int} needs to be performed. The relationship between I_O and energy losses should be analyzed comprehensively since it is determined by a lot of parameters. Its calculation can be referred to Eq. (2-28) and Eqs. (2-37) - (2-39).

Taking the fact that the V_{BUS} and I_O determine switching performance of the SiC power MOSFET into consideration, feedback control is necessary to realize the optimal control performance. When the V_{BUS} and I_O of the converter is different, V_{int} should be changed actively

to suppress the EMI noise to a certain level. These summary of the theoretical analysis of the turn-off process of the proposed AGD is given in Tables III and IV.

Table 3-8 Summary of the observations for the Situation I.

	t_{delay}	dv/dt	di/dt	E_{loss}	t_{int}
V_{int} ↑	-	↓↓	↓↓	↑↑	↑↑
I_O ↑	↓	↑	↑	~	~
V_{BUS} ↑	-	↑	↑	↑↑	↑↑

Table 3-9 Summary of the Observations for the Situation II.

	t_{delay}	dv/dt	di/dt_I	di/dt_II	E_{loss}	t_{int}
V_{int} ↑	-	↓↓	↓↓	↑↑	↑↑	↑↑
I_O ↑	↓	↑	↑	~	~	~
V_{BUS} ↑	-	↑	↑	↑	↑↑	↑↑

In Tables III and IV, "↑↑" means that it will increase dramatically, while "↑" means it will increase somewhat. "↓↓" and "↓" are opposites. "-" means there is no significant influence. "~" means that the relationship is not linear, so the trend is relevant to the other circuit parameters and it should be checked with the equation.

3.4.2 Experimental verification of the case study

In Chapter 2, the optimal V_{int} curve comparison is conducted with two different devices: CREE and Rohm. Chapter 3 has verified the V_{int} optimization algorithm with LTspice simulation. The selection will validate the two scenarios through DPTs with experimental prototype. The experimental results are shown in Figure 3-26.

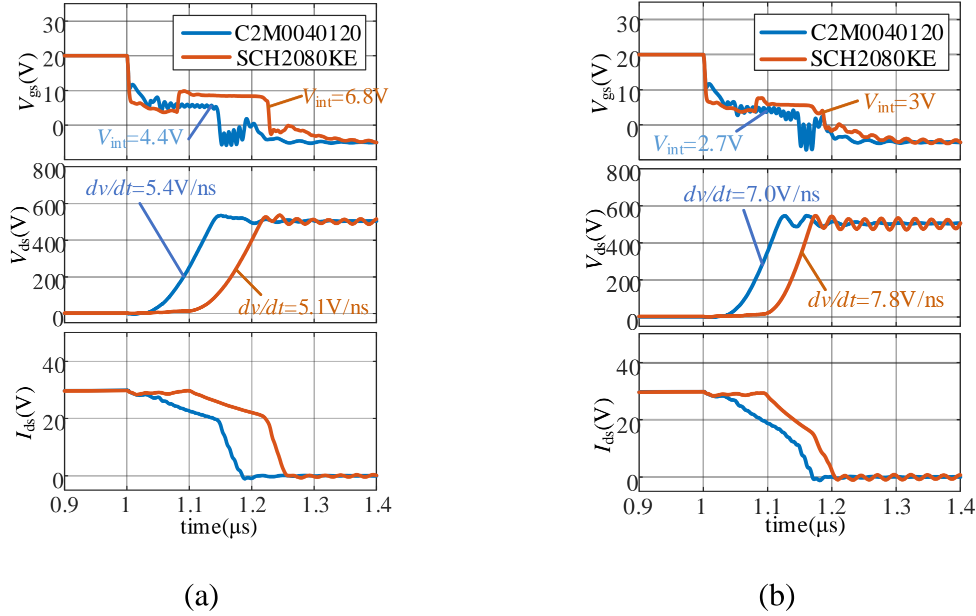


Figure 3-26 Experimental results of C2M0040120 and SCH2080KE under different scenarios. (a) High EMI suppression condition, (b) The average weight condition.

From Figure 3-26 (a), when I_O=20 A, to decrease the *dv/dt* to a same level (5.1 V/ns), the V_{int} of SCH2080KE should be selected as a higher value than C2M0040120. In Figure 3-26 (b), V_{int} of SCH2080KE should be 3V to reduce *dv/dt* to 7.8 V/ns while C2M0040120 only needs to be 2.7V. As analyzed in Chapter 3, this phenomenon is due to the different g_{fs} of these two MOSFETs. It also accordance with the theoretical analysis. Thus, when designing the optimization algorithm for these two SiC MOSFETs, the variation of optimal V_{int} curve of SCH2080KE with V_{int} should be larger than C2M0040120.

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CHAPTER 4

ACTIVE GATE DRIVER FOR 10 KV SIC MOSFET

4.1 Characterization of 10 kV SiC MOSFET

As introduced in Chapter 2, it is imperative to extract the parameters of the power device prior to designing the control algorithm and the gate driver voltage profile. However, the datasheet of the 10 kV SiC MOSFET is not available since 10 kV devices are not yet commercially available. It is desired to perform a static characterization for the 10 kV SiC MOSFET to extract the parameters, such as the junction capacitance, transconductance, and conduction resistance. The curve tracer used for this exercise is a Keysight B1505A. The DUT is the third generation of CREE 10 kV SiC half-bridge power MOSFET which uses XHV-9 package. The DUT is shown in Figure 4-1.

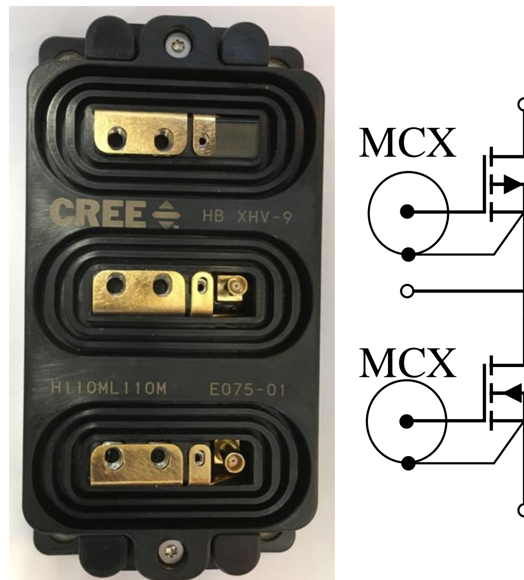


Figure 4-1 10 kV SiC power MOSFET with XHV-9 package.

The tested power module has two XPM3-10000-0350-ES dies, one each for the upper and lower switching positions. The parameters were extracted with the Keysight B1505A curve tracer

at 25°C and 150°C and the data were used to analyze the transient process of the power module. Keysight B1505A can provide static characterization under 3 kV and up to 10 A maximum.

4.1.1 Junction capacitance

Junction capacitance will affect the charging speed of the junction voltage and thus affect the switching speed [1.25] [4.1]. In prior to designing the AGD board, the characterization of the junction capacitance should be conducted. These capacitance include input capacitance C_{iss}, output capacitance C_{oss} and Miller capacitance C_{rss}.

4.1.1.1 *Input capacitance C_{iss}*

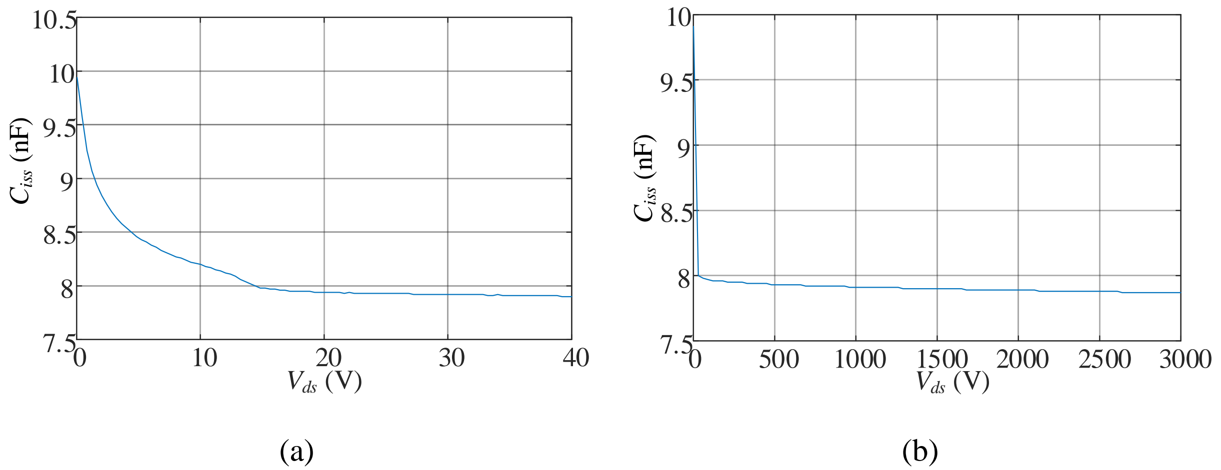


Figure 4-2 C_{iss} measurement results. (a) Maximum V_{ds} = 40 V. (b) Maximum V_{ds} = 3 kV.

C_{iss} is the sum of C_{gd} and C_{gs}. It affects the switching speed significantly as analyzed in the former chapters. C_{iss} is not a constant value which changes with V_{ds}. It can be approximated with $C_{\mathrm{gd}} = \dfrac{C_{\mathrm{gd0}}}{\sqrt{1+V_{\mathrm{ds}}/\phi_0}}$. Most datasheets of MOSFET provide the C_{iss} - V_{ds} curve. Since the B1505A can only sweep very limited amount of points, C_{iss} measurement should be conducted under different V_{ds} ranges, i.e., high maximum V_{ds} and low maximum V_{ds}. Sweeping frequency is 1 MHz.

The measurement results are shown in Figure 4-2. Figure 4-2 (a) and (b) are the results of 40 V maximum V_{ds} and 3 kV maximum V_{ds}. From Figure 4-2, C_{iss} is 9906 pF at V_{ds} = 0V and 7900 pF at V_{ds} = 3 kV respectively.

4.1.1.2 ***Reverse transfer capacitance C_{rss}***

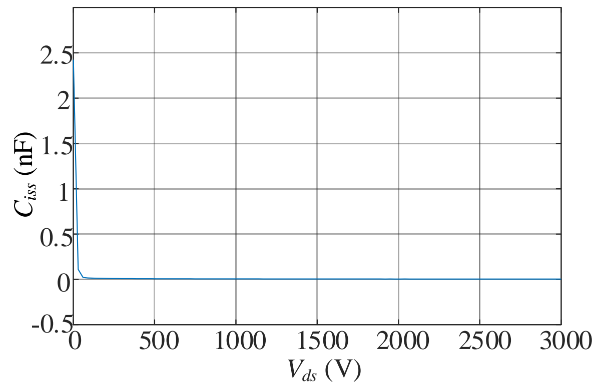


Figure 4-3 C_{oss} measurement results under maximum V_{ds} = 3 kV.

C_{rss}, which is the reverse transfer capacitance, equals to C_{gd}. C_{iss} measurement is conducted under 3 kV and 100 kHz. The measurement results are shown in Figure 4-3. C_{rss} is 2.417 nF under V_{ds} = 0 V and 4 pF under V_{ds} = 3 kV.

4.1.1.3 ***Output capacitance C_{oss}***

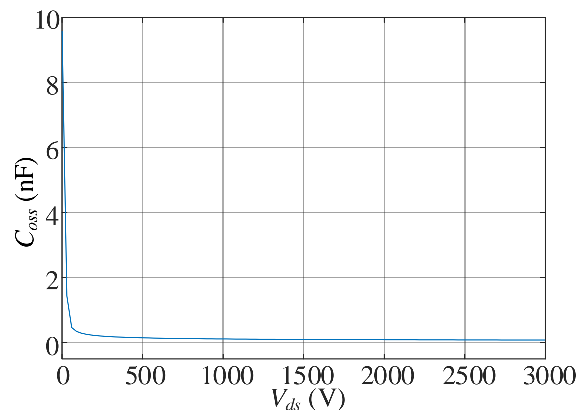


Figure 4-4 C_{oss} measurement results under maximum V_{ds} = 3 kV.

C_{oss} is the output capacitance which id denoted by C_{gd}+C_{ds}. C_{oss} measurement is conducted under 3 kV and 1 MHz. The measurement results are shown in Figure 4-13. C_{rss} is 9578 pF under V_{ds} = 0 V and 82 pF under V_{ds} = 3 kV.

4.1.2 Output characteristics

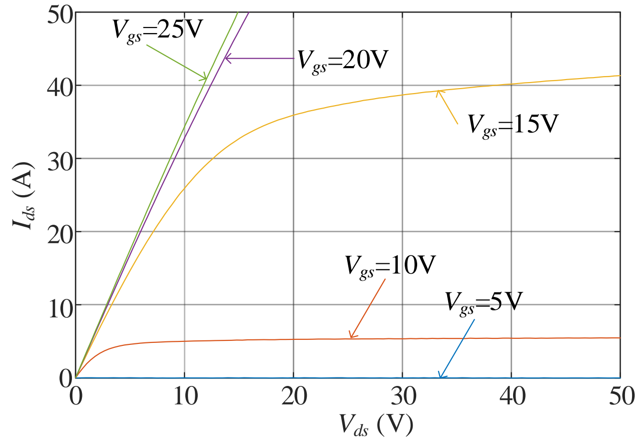


Figure 4-5 V_{ds} *vs.* I_{ds} for various V_{gs} at 25℃.

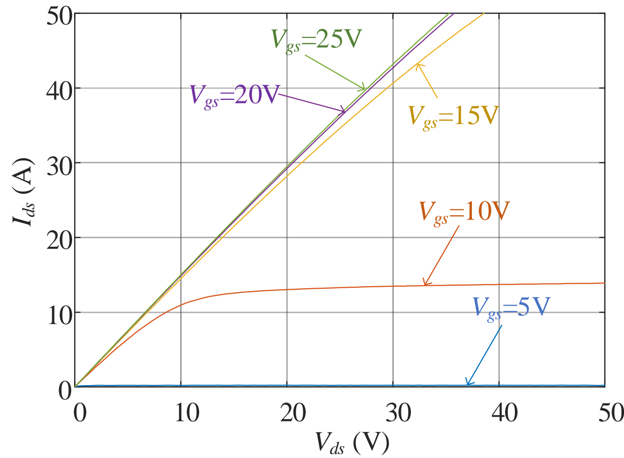


Figure 4-6 V_{ds} *vs.* I_{ds} for various V_{gs} at 150℃.

The output characteristics are the V_{ds} - I_{ds} curve under different V_{gs}. Because the maximum continuous I_{ds} is 19A, the maximum I_{ds} tested in the dissertation is 50 A and maximum tested V_{ds} is 50V. The characterization is conducted at 25℃ and 150℃. The I_{ds}-V_{ds} curves at 25℃ and 150℃ are given in Figure 4-5 and Figure 4-6 respectively.

Comparing Figure 4-5 and Figure 4-6, higher junction temperature increases the saturation current under same V_{gs}. The reason of this trend is that the lower gate-source threshold voltage V_{th} caused by the higher junction temperature. How V_{th} changes with the junction temperature Tj roughly follows Eq. (4-1) [4.2].

$$V_{th} = V_{th}|_{Tj=T_{room}} - \gamma_{th}(Tj - T_a) \tag{4-1}$$

In Eq. (4-1), T_a is the ambient temperature and γ_{th} is the coefficient of threshold voltage. From Eq. (2-32), when V_{th} is lower, the saturation current will increase. However, in the Ohmic region, higher junction temperature also results in higher R_{ds_on}.

Another curve of interest is the R_{ds_on} *vs.* I_{ds}. The characterization results at 25°C and 150°C junction temperature are shown in Figure 4-7 and Figure 4-8 respectively. From Figure 4-7 and Figure 4-8, R_{ds_on} for V_{ds} = 20 V at 25°C and 150°C are 300 mΩ and 663 mΩ respectively. Therefore, the SiC MOSFET tested shows a positive temperature coefficient feature which makes it suitable for the parallel-connection.

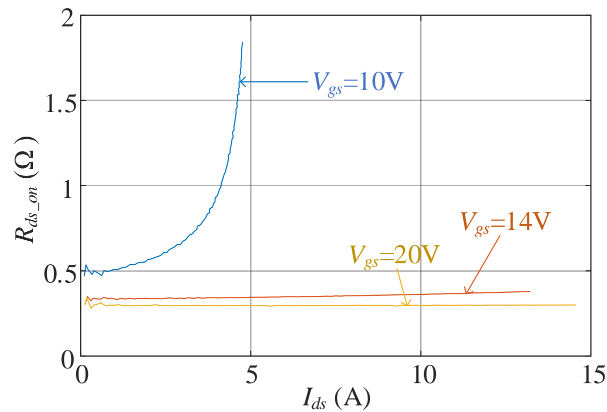


Figure 4-7 R_{ds_on} *vs.* I_{ds} curve at 25°C.

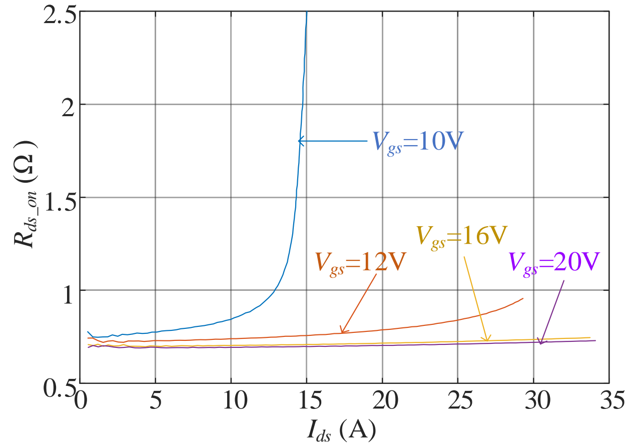


Figure 4-8 R_{ds_on} *vs.* I_{ds} curve at 150°C.

4.1.3 Transfer characteristic

Transconductance g_{fs} is defined with Eq. (4-2) [4.3].

$$g_{fs} = \frac{\Delta I_{ds}}{\Delta V_{gs}} \tag{4-2}$$

The V_{ds} should be set for the saturation region of power MOSFET. V_{ds} should be the case when I_{ds} is half of the maximum continuous drain-source current. The measurement results are shown in Figure 4-9.

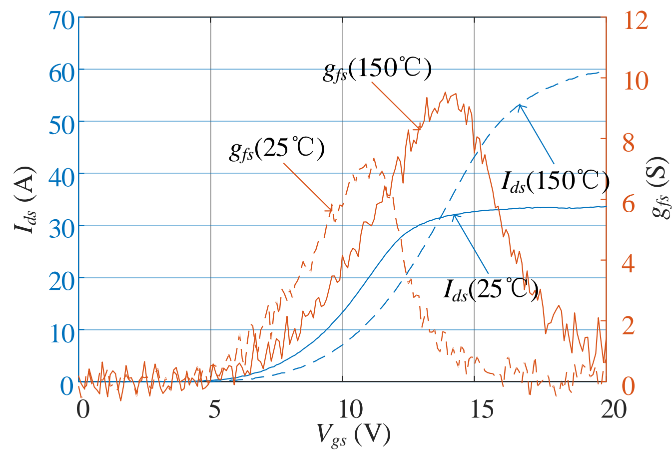


Figure 4-9 Transfer characteristic of the power MOSFET.

From Figure 4-9, the typical transconductance of XPM3-10000-0350-ES is 4 S at 25°C. With higher junction temperature, the transconductance also increases.

4.1.4 *Gate charge*

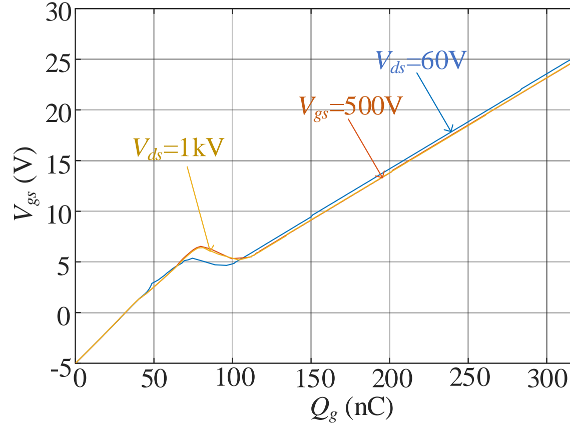


Figure 4-10 Gate charge characteristic under different V_{ds} at 25°C.

The gate charge characteristic under different V_{ds} at 25°C is given in Figure 4-10. From Figure 4-10, the gate charge increases with the

4.1.5 *Body diode characteristics*

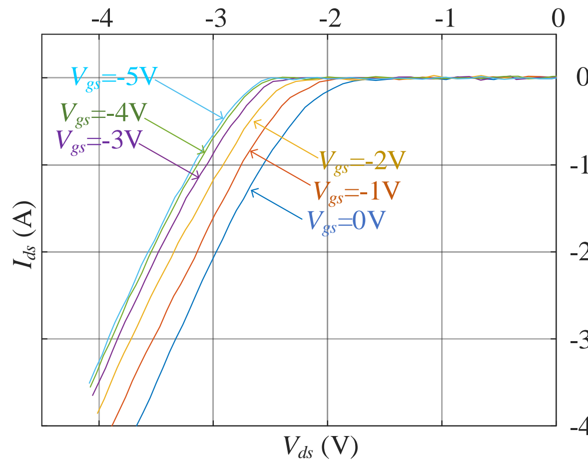


Figure 4-11 Body diode characteristic at 25°C.

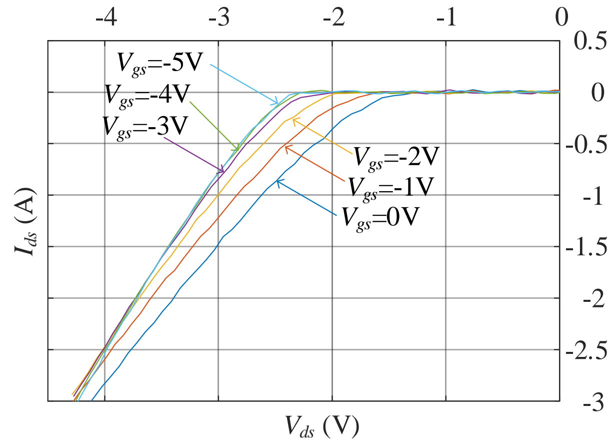


Figure 4-12 Body diode characteristic at 150℃.

The body diode characteristics are typically given in the third-quadrant I-V curve. V_{gs} is clamped at -5 V for this characterization. The characterization results at 25℃ and 150℃ are shown in Figure 4-11 and Figure 4-12 respectively.

Comparing Figure 4-11 and Figure 4-12, the body diode resistance increases when the junction temperature is higher.

4.1.6 The overall parameters

Table 4-1 The parameters of the tested 10 kV SiC MOSFET.

Symbol	**Parameter**	**Value**
V_{ds_max}	Maximum drain-source voltage	10 kV
I_{ds_max}	Maximum continuous drain-source current	19 A
V_{th}	Gate-source threshold voltage	4.3 V
R_{ds_on}	Drain-source on-state resistance	304 mΩ(V_{gs}=20 V)
g_{fs}	Transconductance	4.8 S
C_{iss}	Input capacitance	9906 pF (V_{ds}=0 V)
		7868 pF (V_{ds}=3 kV)
C_{oss}	Output capacitance	9577 pF (V_{ds}=0 V)
		8188 pF (V_{ds}=3 kV)
C_{rss}	Reverse transfer capacitance	2417 pF (V_{ds}=0 V)
		4 pF (V_{ds}=3 kV)
Q_g	Gate charge	69.5 nC

Based on the aforementioned characterization results, the parameters of the 10 kV SiC power MOSFET can be concluded in Table 4-1.

As shown in the aforementioned sections, all the parameters change with the external conditions such as V_{ds}, I_{ds}, and Tj. For the model predictive control, considering the variation will dramatically increase the computation load. Therefore, all the parameters listed in Table 4-1 are the typical values.

4.2 The gate driver board design

Chapter 3 has introduced the gate driver design consideration for the 1.2 kV SiC MOSFET. The basic circuit schematics of the gate driver for 10 kV SiC MOSFET is similar to 1.2 kV device. Due to the different voltage levels and EMI noise, the components of the AGD board are different. In this section, the component selection consideration is given.

4.2.1 Component selection

Due to the high voltage of 10 kV device, the component selection of 10 kV version is different from the 1.2 kV version. Apart from the *dv/dt* immunity, the isolation design should be paid greater attention.

4.2.1.1 ***Isolated power supply***

Among the several kinds of available commercialized isolated power supplies for 10 kV devices on the market, two products are the most popular: Power Integrations ISO5125i [4.4] and RECOM REC6 [4.5] [4.6]. For 10 kV isolation-level, ISO5125i provides 18 kV isolation [4.7], but it is not designed for on-board application due to the bulky size. Using such a power supply

can result in long gate loop and introduce high inductance. Therefore, a cascaded-connected power supply structure as shown in Figure 4-13 is proposed in this article.

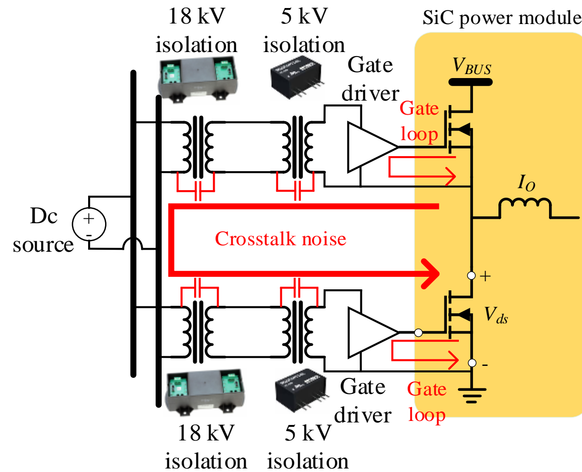


Figure 4-13 The cascaded connected power supply structure.

The 5 kV isolation power supply is generally compact and it can be located close to the power devices. Thus, the gate loop can be shortened and parasitics are reduced. Also, the cascaded connection can reduce the total parasitic capacitance in the crosstalk noise propagation route and reduce the EMI noise. It should be noted that, for some specific application when the dc link voltage is very high, 18 kV isolated power supply may not provide enough insulation capability. The power selection should follow IEC CEI 60664-1 standard [4.9].

4.2.1.2 ***Driver buffers and opamps***

The peak gate current can be calculate with Eq. (3-1). Since C_{iss} of the 10 kV SiC MOSFET is higher than 1.2 kV SiC MOSFET, an IXDN614 driver buffer is used. IXDN614 has 14 Amps peak gate current which lends it capability to drive the 10 kV SiC MOSFET. The other parameters of IXDN614 are same with IXDN609. The op-amps are the same with the AGD version for 1.2 kV MOSFET.

4.2.1.3 *Digital isolator*

A digital isolator is connected between the DSP controller and the gate of the MOSFET. It provides galvanic isolation for the gate signal. Considering that the dc bus voltage is 10 kV level, the digital isolator should have enough galvanic isolation capability. As introduced in Chapter 1, the fiber transceiver is the only choice for this application. Also, since it is completely galvanic isolated, it is immune to EMI noise.

The downside of the fiber transceiver is the high cost [4.8]. However, because 10 kV SiC MOSFET takes over $40,000, it is preferred to provide better protection for the device. The cost of the gate driver is not the major consideration. An Avago AFBR-2624Z fiber receiver is used for the gate driver. The propagation delay of AFBR-2624Z is 30 ns.

4.2.2 PCB design

Based on the components selection, the AGD is designed as shown in Figure 4-14.

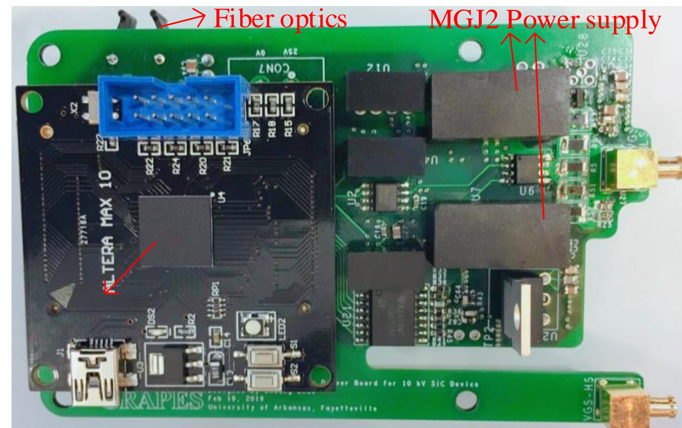


Figure 4-14 The AGD for 10 kV power MOSFET.

Since the fiber receiver has only one channel, the FPGA should be placed on the gate driver board. It also uses an Altera Max 10 FPGA controller. The gate resistance is 12 Ω.

It should be noted that XHV-9 package uses an MCX connector for the gate signal. The Kelvin source and the gate are on the MCX connector.

4.2.3 *Double pulse test setup*

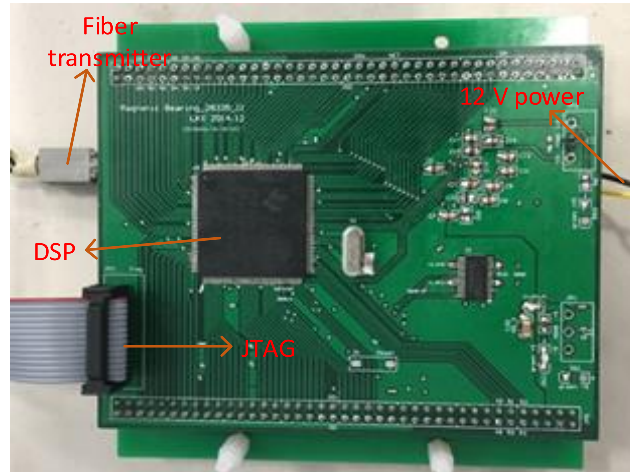


Figure 4-15 The DSP controller with a fiber transmitter.

Due to the dangers associated with performing DPTs for 10 kV devices, safety is the foremost consideration. The signal is generated with a DSP controller and communicated with a fiber transmitter which are shown in Figure 4-15.

The bus bar provides the connectors to the dc power supply and bypass capacitors for reducing the overshoot voltage. We have developed two versions for the bus bar: with a shunt resistor and without shunt resistor. The version with shunt resistor is shown in Figure 4-16. The lowest value multi-layer ceramic capacitor (MLCC) should be placed close to the module to filter the high frequency noise. Two 30 μF capacitors are connected as the dc-link capacitors. The selection of dc-link capacitor should ensure that the dc voltage will not decrease to very low level during the pulse.

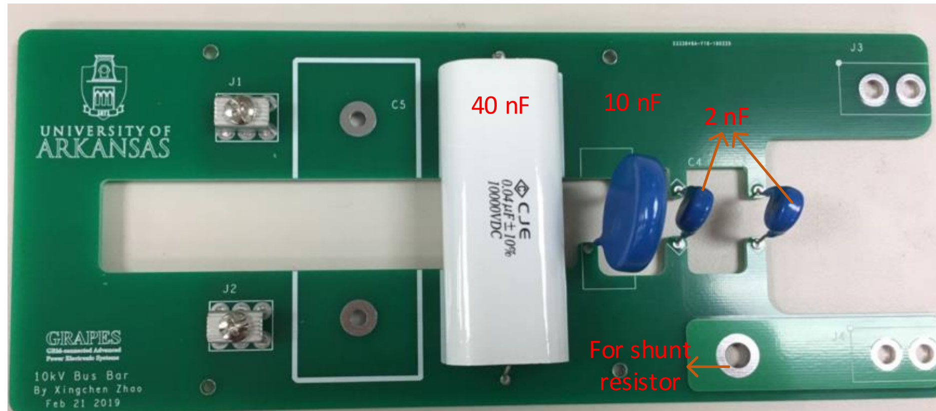
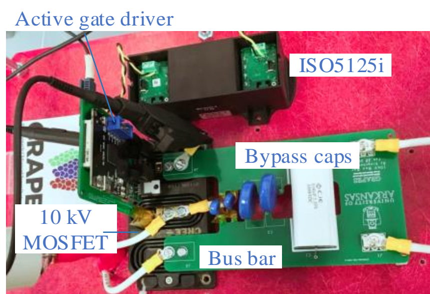
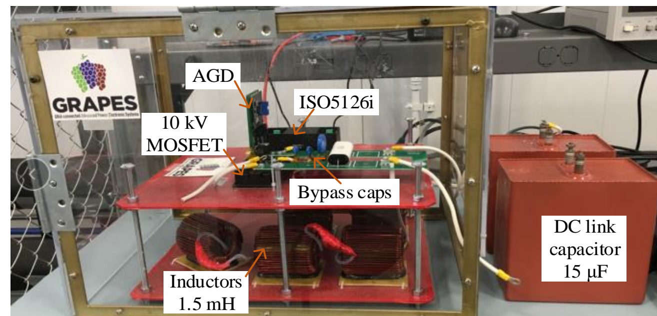


Figure 4-16 The DPT busbar for the 10 kV SiC MOSFET with shunt resistor.

With the aforementioned PCBs, a DPT prototype, as shown in Figure 4-17, is developed to measure the key parameters regarding the switching transients of the 10 kV SiC MOSFETs.



(a)



(b)

Figure 4-17 The double pulse test setup. (a) The test circuit. (b) The entire setup.

The load consists of five 1.2 mH inductors connected in series, so the total load inductance is 6 mH. The dc bus has two series connected 30 μF film capacitors, so the total dc-link capacitance is 15 uF. V_{ds} and V_{gs} are measured with Tektronix P6015A and TPP0500 probe. Tektronix P6105A can measure up to 40 kV voltage with a 75 MHz bandwidth. According to Eq. (3-6), the bandwidth is enough to measure V_{ds} of the 10 kV MOSFET. I_{ds} is measured with a PEM Rogowski coil which provides 30 MHz measurement bandwidth.

4.3 Experimental results for turn-off

The DPT is conducted with a 4 kV dc bus voltage and a load current of 20 A. The experimental results are given in Figure 4-18 - Figure 4-20. Figure 4-18 shows the experimental results with proposed 3-L AGD under different V_{int} levels. It should be noted that the lowest V_{int} selected for the DPT is 5 V. This does not mean the 5 V is the lowest V_{int} level the AGD can be. Changing the resistors of the adjustable voltage regulator can change the V_{int} adjustment range. Figure 4-19 compares the AGD mode under different load current conditions. In Figure 4-19, V_{int} is set to be 6.3 V for all the scenarios. Figure 4-20 compares the DPT results with conventional gate driver and active gate driver mode with V_{int} = 7.5 V.

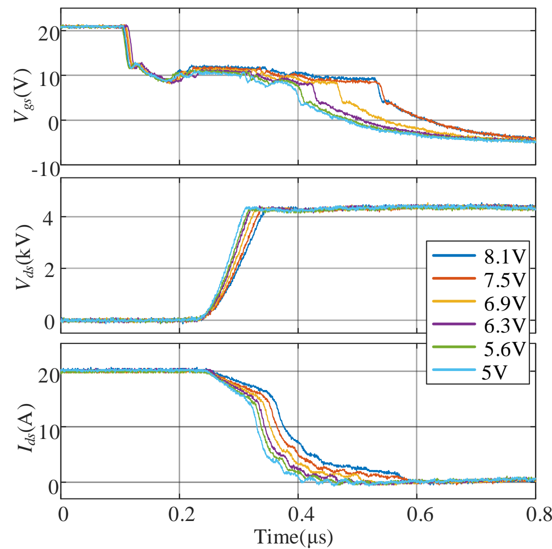


Figure 4-18 The experimental results of DPT under different V_{int}.

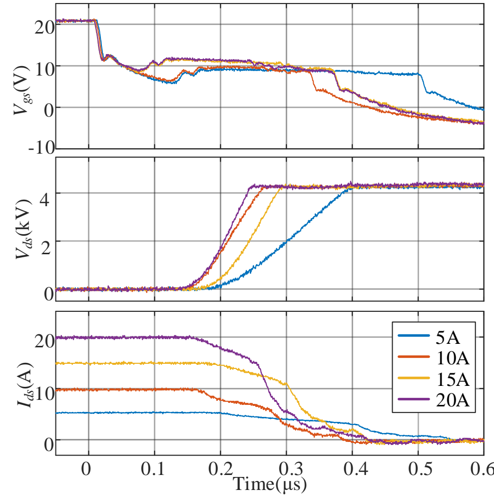


Figure 4-19 Active gating under different load current (V_{int} = 6.3V).

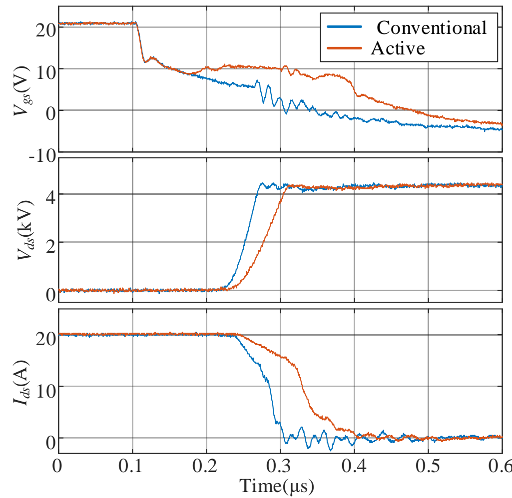


Figure 4-20 The comparison of conventional gate driver and proposed AGD (V_{int} =7.5 V).

From Figure 4-18, the switching slew rate of the SiC power MOSFET reduces with higher V_{int}. Also, with the proposed AGD, the turn-off delay does not change significantly under different V_{int}. Figure 4-19 reveals that *dv/dt* and *di/dt* increase dramatically with higher load current even with the same V_{int}. Therefore, to realize the optimal control function, online adjustment of V_{int} levels based on the load current and bus voltage feedback is necessary. Figure 4-20 shows that AGD can

effectively control the *dv/dt* and *di/dt* of the 10 kV SiC MOSFET. The data extracted from DPT results will be analyzed in the following sections.

4.3.1 The dv/dt consideration

Table 4-2 *dv/dt* under different V_{int}.

V_{int}	***dv/dt* (V/ns)**
Conventional (-5 V)	94.78
5 V	58.8
5.6 V	54.32
6.3 V	52.4
6.9 V	49.16
7.5 V	43.56
8.1 V	40.37

As analyzed in the first section, *dv/dt* should be considered first because it determines the EMI noise in the circuit [1.41]. The *dv/dt* values of Figure 4-18 are listed in Table 4-2. From Table 4-2, the *dv/dt* decreases when V_{int} increases. *dv/dt* values extracted from Figure 4-19 are listed in Table 4-3.

Table 4-3 *dv/dt* of AGD under different load current.

V_{int}	***dv/dt* (V/ns)**
5 A	21
10 A	34.2
15 A	37.4
20 A	42.9

From Table 4-3, when the load current I_O increases, *dv/dt* increases. This can be explained with Eq. (2-7). From Eq. (2-7), when I_{ds} is higher, V_{miller} is higher and V_{int} is closer to V_{miller}. Therefore, the gate current is reduced and C_{iss} charging speed is increased. *dv/dt* increases.

4.3.2 The energy losses comparison

The energy losses of the different double pulse test groups are listed in Table 4-4.

Table 4-4 The switching energy losses of AGD with different V_{int}.

V_{int}	**Energy losses**
Conventional(-5 V)	2302 μJ
5 V	4384 μJ
5.6 V	4629 μJ
6.3 V	4977 μJ
6.9 V	5555 μJ
7.5 V	6259 μJ
8.1 V	7410 μJ

From Table 4-4, V_{int} will dramatically increase the energy losses. Higher V_{int} slows down the switching transient and the energy losses can be calculated with the product of V_{ds} and I_{ds}. Therefore, Higher V_{int} will increase turn-off losses.

4.3.3 di/dt comparison

di/dt influences V_{ds} overshoot voltage. The *di/dt* of different groups are listed in Table 4-5. From Table 4-5, high V_{int} will significantly reduce the *di/dt*. Due to the fact that XHV-9 package has very low parasitic inductance, the overshoot voltage is not obvious in this case. It is hard to compare the overshoot voltage.

Table 4-5 *di/dt* of AGD with different V_{int}.

V_{int}	***di/dt*(A/ns)**
Conventional(-5 V)	0.34
5 V	0.158
5.6 V	0.145
6.3 V	0.138
6.9 V	0.122
7.5 V	0.109
8.1 V	0.097

4.4 Conclusions

In this chapter, the proposed AGD circuitry is applied to the 10 kV SiC MOSFET. The characterization for 10 kV SiC MOSFET is conducted first to extract all the parameters of the junctions under different junction temperature. The temperature sensitive parameters are also analyzed with the characterization results. Then the design consideration including the components and PCB layout design are introduced. The slew rate control effect has been verified with DPT under 4 kV V_{BUS}.

4.5 Reference

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CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusion

SiC power devices have the capability to approach ideal switches. Application of SiC power MOSFET can effectively reduce the switching losses of the power converter. The high switching slew rate may also introduce challenge over the EMI noise immunity. In some scenarios, the slew rate is preferred to be reduced even though it increases the switching losses. In some other scenarios, the switching is preferred to be sped up to reduce the switching losses. Therefore, the slew rate control of SiC power MOSFET based on the scenarios is necessary. In this dissertation, a versatile multi-level AGD circuit is proposed to improve the switching trajectory of a power device. Its various operation modes enable it to adjust the switching speed dynamically and be versatile for different scenarios. The faster turn-on mode utilizes higher driver voltage to speed up the turn-on process and reduce the switching losses. The slower turn-on mode adopts lower transient driver voltage to slow down the turn-on process and reduce the slew rate. The slower turn-off mode can reduce the turn-off transient to avoid the false-triggering probability caused by the gate current. Additionally, the proposed AGD circuit has a lot of adjustment steps which enables it to fine tune the switching speed.

A trajectory model for SiC MOSFET is proposed for the analysis of turn-on and turn-off process. Compared with the conventional trajectory model, it trades off the computation load and accuracy. The non-linearity of the Miller capacitance during the switching is considered and the two conditions of the multi-level driver voltage profile are investigated. The behavior of SiC power MOSFET under multi-level switching is analyzed with the proposed trajectory model the validated with experimental results. Based on the trajectory model, an online model-predictive optimization

control is proposed for this AGD topology. *dv/dt*, *di/dt*, and energy losses are evaluated and the optimal intermediate driver voltage is calculated to generate the optimal driver voltage profile. The hardware design considerations and the measurement are demonstrated comprehensively. The experimental prototype development for 1.2 kV SiC MOSFET and 10 kV MOSFET are introduced. DPT results have verified the functionality of the proposed AGD method.

5.2 Future work

The dissertation has investigated the AGD with model-based optimization algorithm. This method needs the datasheet parameters. In some situations, the parameters are not accessible. Moreover, changing the PCB layout may result in the variation of the parameters and these parameters can be difficult to measure. Therefore, in some conditions, it is necessary to use the real time feedback of the slew rate. In the future, the slew rate measurement circuit can be developed and the feedback can be sent to the local controller for realizing control.

Also, the proposed AGD circuitry is more complex than the conventional gate driver. It will increase the size of the gate driver board. To commercialize this proposed AGD technology, integrating the proposed circuitry into a application-specific integrated circuit is a good solution to reduce the size and expense.

Another application of the AGD is on parallel-connected power devices. Parallel-connection of power devices is an economical and popular solution for the high power converter. There are different combinations of parallel-connected devices: SiC MOSFET + Si IGBT, SiC MOSFET + SiC MOSFET, and Si MOSFET + Si IGBT. Due to the different parameters of the various power devices, the thermal stress on the devices is different. As introduced in Chapter 2, lot of parameters may affect the current dissipation on the parallel-connected devices such as the stray inductance,

junction capacitance, and the gate resistance. Even different packages of devices can change the current dissipation.

To completely release the performance of the parallel-connected power devices, the switching losses on the power devices should be adjusted through the gate driver. In the dissertation, the proposed AGD has been validated to be effective in slew rate control of power devices. Therefore, it is an appropriate option for the parallel-connected. In the future extension, the AGD will be utilized on the parallel-connected devices.

APPENDIX

This appendix shows the MATLAB code used for process the data of DPT. The data is extracted with Tektronix oscilloscope and saved in .csv files. This allows the user to input the data into MATLAB, calculate the *dv/dt*, *di/dt*, energy loss, with peak V_{ds}, and plot the figures of the waveform.

```
%% For the multi-level slowed turn-off mode for 10 kV
% Different Vint: 8.1 7.5 6.9 6.3 5.6 5
clear
clc
close all
sym SC

% Case 0: Vint=8.1V
SC0_1='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0002CH1.csv';
SC0_2='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0002CH2.csv';
SC0_3='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0002CH3.csv';

% Case 1: Vint=7.5V
SC1_1='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0003CH1.csv';
SC1_2='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0003CH2.csv';
SC1_3='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0003CH3.csv';

% Case 2: Vint=6.9V
SC2_1='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0005CH1.csv';
SC2_2='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0005CH2.csv';
SC2_3='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0005CH3.csv';

% Case 3: Vint=6.3V
SC3_1='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0007CH1.csv';
SC3_2='C:\Users\derek\Box\NCREPT-GRAPES_HV-
GateDriver\Test_Results\10_kV_April29_2019\tek0007CH2.csv';
```

```
SC3_3='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0007CH3.csv';

% Case 4: Vint=5.6V
SC4_1='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0008CH1.csv';
SC4_2='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0008CH2.csv';
SC4_3='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0008CH3.csv';

% Case 5: Vint=5V
SC5_1='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0009CH1.csv';
SC5_2='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0009CH2.csv';
SC5_3='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0009CH3.csv';

% Case 6: CGD
SC6_1='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0013CH1.csv';
SC6_2='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0013CH2.csv';
SC6_3='C:\Users\derek\Box\NCREPT-GRAPES_HV-GateDriver\Test_Results\10_kV_April29_2019\tek0013CH3.csv';

temp0_1 = csvread(SC0_1);
temp0_2 = csvread(SC0_2);
temp0_3 = csvread(SC0_3);

Time_0 = temp0_1(:,1)*1e6;   % Read the time
Vds_AGD_0 = temp0_1(:,2);   %  Read the Vgs
Vgs_AGD_0 = temp0_2(:,2);   %  Read the Vds
Ids_AGD_0 = temp0_3(:,2);   %  Read the Vgs

temp1_1 = csvread(SC1_1);
temp1_2 = csvread(SC1_2);
temp1_3 = csvread(SC1_3);

Time_1 = temp1_1(:,1)*1e6;   % Read the time
Vds_AGD_1 = temp1_1(:,2);   %  Read the Vgs
Vgs_AGD_1 = temp1_2(:,2);   %  Read the Vds
Ids_AGD_1 = temp1_3(:,2);   %  Read the Vgs

temp2_1 = csvread(SC2_1);
```

```
temp2_2 = csvread(SC2_2);
temp2_3 = csvread(SC2_3);

Time_2 = temp2_1(:,1)*1e6+0.002;   % Read the time
Vds_AGD_2 = temp2_1(:,2);   %  Read the Vgs
Vgs_AGD_2 = temp2_2(:,2);   %  Read the Vds
Ids_AGD_2 = temp2_3(:,2);   %  Read the Vgs

temp3_1 = csvread(SC3_1);
temp3_2 = csvread(SC3_2);
temp3_3 = csvread(SC3_3);

Time_3 = temp3_1(:,1)*1e6+0.008;   % Read the time
Vds_AGD_3 = temp3_1(:,2);   %  Read the Vgs
Vgs_AGD_3 = temp3_2(:,2);   %  Read the Vds
Ids_AGD_3 = temp3_3(:,2);   %  Read the Vgs

temp4_1 = csvread(SC4_1);
temp4_2 = csvread(SC4_2);
temp4_3 = csvread(SC4_3);

Time_4 = temp4_1(:,1)*1e6-0.005;   % Read the time
Vds_AGD_4 = temp4_1(:,2);   %  Read the Vgs
Vgs_AGD_4 = temp4_2(:,2);   %  Read the Vds
Ids_AGD_4 = temp4_3(:,2);   %  Read the Vgs

temp5_1 = csvread(SC5_1);
temp5_2 = csvread(SC5_2);
temp5_3 = csvread(SC5_3);

Time_5 = temp5_1(:,1)*1e6+0.001;   % Read the time
Vds_AGD_5 = temp5_1(:,2);   %  Read the Vgs
Vgs_AGD_5 = temp5_2(:,2);   %  Read the Vds
Ids_AGD_5 = temp5_3(:,2);   %  Read the Vgs

temp6_1 = csvread(SC6_1);
temp6_2 = csvread(SC6_2);
temp6_3 = csvread(SC6_3);

Time_6 = temp6_1(:,1)*1e6+0.010;   % Read the time
Vds_AGD_6 = temp6_1(:,2);   %  Read the Vgs
Vgs_AGD_6 = temp6_2(:,2);   %  Read the Vds
Ids_AGD_6 = temp6_3(:,2);   %  Read the Vgs

%------ Calculate the dv/dt, and Eloss , only for turn-off----------
iii=find( Time_0>72.4 & Time_0<73.1 & Vds_AGD_0<400 & Vds_AGD_0>200);
```

```
startpoint0=iii(1); %Vds rise start
iii=find( Time_0>72.4 & Time_0<73.1 & Vds_AGD_0<4000 & Vds_AGD_0>3700);
endpoint0=iii(1); %Vds rise end
iii=find( Time_0>72.4 & Time_0<73.1 & Ids_AGD_0<20 & Ids_AGD_0>18);
startpoint02=iii(end);  %Ids fall start
iii=find( Time_0>72.4 & Time_0<73.1 & Ids_AGD_0<3 & Ids_AGD_0>1);
endpoint02=iii(1);  %Ids fall end
dvdt0=(Vds_AGD_0(startpoint0)-Vds_AGD_0(endpoint0))/(Time_1(startpoint0)-
Time_1(endpoint0))
didt0=(Ids_AGD_0(startpoint02)-Ids_AGD_0(endpoint02))/(Time_1(startpoint02)-
Time_1(endpoint02))
Eon_0=0;
for i=startpoint0:endpoint02
   Eon_0=(Time_0(i+1)-Time_0(i))*Vds_AGD_0(i)*Ids_AGD_0(i)+Eon_0;
end
Tint0=(Time_0(endpoint02)-Time_0(startpoint0))*1e9
Vds_pk0=max(Vds_AGD_0)
Eon_0

iii=find( Time_1>72.4 & Time_1<73.1 & Vds_AGD_1<400 & Vds_AGD_1>200);
startpoint1=iii(1); %Vds rise start
iii=find( Time_1>72.4 & Time_1<73.1 & Vds_AGD_1<4000 & Vds_AGD_1>3700);
endpoint1=iii(1); %Vds rise end
iii=find( Time_1>72.4 & Time_1<73.1 & Ids_AGD_1<20 & Ids_AGD_1>18);
startpoint12=iii(end);  %Ids fall start
iii=find( Time_1>72.4 & Time_1<73.1 & Ids_AGD_1<3 & Ids_AGD_1>1);
endpoint12=iii(1);  %Ids fall end
dvdt1=(Vds_AGD_1(startpoint1)-Vds_AGD_1(endpoint1))/(Time_1(startpoint1)-
Time_1(endpoint1))
didt1=(Ids_AGD_1(startpoint12)-Ids_AGD_1(endpoint12))/(Time_1(startpoint12)-
Time_1(endpoint12))
Eon_1=0;
for i=startpoint1:endpoint12
   Eon_1=(Time_1(i+1)-Time_1(i))*Vds_AGD_1(i)*Ids_AGD_1(i)+Eon_1;
end
Tint1=(Time_1(endpoint12)-Time_1(startpoint1))*1e9
Vds_pk1=max(Vds_AGD_1)
Eon_1

iii=find( Time_2>72.4 & Time_2<73.1 & Vds_AGD_2<400 & Vds_AGD_2>200);
startpoint2=iii(1); %Vds rise start
iii=find( Time_2>72.4 & Time_2<73.1 & Vds_AGD_2<4000 & Vds_AGD_2>3700);
endpoint2=iii(1); %Vds rise end
iii=find( Time_2>72.4 & Time_2<73.1 & Ids_AGD_2<20 & Ids_AGD_2>18);
startpoint22=iii(end);  %Ids fall start
iii=find( Time_2>72.4 & Time_2<73.1 & Ids_AGD_2<3 & Ids_AGD_2>1);
```

```
endpoint22=iii(1);  %Ids fall end
dvdt2=(Vds_AGD_2(startpoint2)-Vds_AGD_2(endpoint2))/(Time_2(startpoint2)-
Time_2(endpoint2))
didt2=(Ids_AGD_2(startpoint22)-Ids_AGD_2(endpoint22))/(Time_2(startpoint22)-
Time_2(endpoint22))
Eon_2=0;
for i=startpoint2:endpoint22
   Eon_2=(Time_2(i+1)-Time_2(i))*Vds_AGD_2(i)*Ids_AGD_2(i)+Eon_2;
end
Tint2=(Time_2(endpoint22)-Time_2(startpoint2))*1e9
Vds_pk2=max(Vds_AGD_2)
Eon_2

iii=find( Time_3>72.4 & Time_3<73.1 & Vds_AGD_3<400 & Vds_AGD_3>200);
startpoint3=iii(1); %Vds rise start
iii=find( Time_3>72.4 & Time_3<73.1 & Vds_AGD_3<4000 & Vds_AGD_3>3700);
endpoint3=iii(1); %Vds rise end
iii=find( Time_3>72.4 & Time_3<73.1 & Ids_AGD_3<20 & Ids_AGD_3>18);
startpoint32=iii(end);  %Ids fall start
iii=find( Time_3>72.4 & Time_3<73.1 & Ids_AGD_3<3 & Ids_AGD_3>1);
endpoint32=iii(1);  %Ids fall end
dvdt3=(Vds_AGD_3(startpoint3)-Vds_AGD_3(endpoint3))/(Time_3(startpoint3)-
Time_3(endpoint3))
didt3=(Ids_AGD_3(startpoint32)-Ids_AGD_3(endpoint32))/(Time_3(startpoint32)-
Time_3(endpoint32))
Eon_3=0;
for i=startpoint3:endpoint32
   Eon_3=(Time_3(i+1)-Time_3(i))*Vds_AGD_3(i)*Ids_AGD_3(i)+Eon_3;
end
Tint3=(Time_3(endpoint32)-Time_3(startpoint3))*1e9
Vds_pk3=max(Vds_AGD_3)
Eon_3

iii=find( Time_4>72.4 & Time_4<73.1 & Vds_AGD_4<400 & Vds_AGD_4>200);
startpoint4=iii(1); %Vds rise start
iii=find( Time_4>72.4 & Time_4<73.1 & Vds_AGD_4<4000 & Vds_AGD_4>3700);
endpoint4=iii(1); %Vds rise end
iii=find( Time_4>72.4 & Time_4<73.1 & Ids_AGD_4<20 & Ids_AGD_4>18);
startpoint42=iii(end);  %Ids fall start
iii=find( Time_4>72.4 & Time_4<73.1 & Ids_AGD_4<3 & Ids_AGD_4>1);
endpoint42=iii(1);  %Ids fall end
dvdt4=(Vds_AGD_4(startpoint4)-Vds_AGD_4(endpoint4))/(Time_4(startpoint4)-
Time_4(endpoint4))
didt4=(Ids_AGD_4(startpoint42)-Ids_AGD_4(endpoint42))/(Time_4(startpoint42)-
Time_4(endpoint42))
Eon_4=0;
```

```
for i=startpoint4:endpoint42
   Eon_4=(Time_4(i+1)-Time_4(i))*Vds_AGD_4(i)*Ids_AGD_4(i)+Eon_4;
end
Tint4=(Time_4(endpoint42)-Time_4(startpoint4))*1e9
Vds_pk4=max(Vds_AGD_4)
Eon_4

iii=find( Time_5>72.4 & Time_5<73.1 & Vds_AGD_5<400 & Vds_AGD_5>200);
startpoint5=iii(1); %Vds rise start
iii=find( Time_5>72.4 & Time_5<73.1 & Vds_AGD_5<4000 & Vds_AGD_5>3700);
endpoint5=iii(1); %Vds rise end
iii=find( Time_5>72.4 & Time_5<73.1 & Ids_AGD_5<20 & Ids_AGD_5>18);
startpoint52=iii(end);  %Ids fall start
iii=find( Time_5>72.4 & Time_5<73.1 & Ids_AGD_5<3 & Ids_AGD_5>1);
endpoint52=iii(1);  %Ids fall end
dvdt5=(Vds_AGD_5(startpoint5)-Vds_AGD_5(endpoint5))/(Time_5(startpoint5)-
Time_5(endpoint5))
didt5=(Ids_AGD_5(startpoint52)-Ids_AGD_5(endpoint52))/(Time_5(startpoint52)-
Time_5(endpoint52))
Eon_5=0;
for i=startpoint5:endpoint52
   Eon_5=(Time_5(i+1)-Time_5(i))*Vds_AGD_5(i)*Ids_AGD_5(i)+Eon_5;
end
Tint5=(Time_5(endpoint52)-Time_5(startpoint5))*1e9
Vds_pk5=max(Vds_AGD_5)
Eon_5

figure(1)
subplot(3,1,1)
plot(Time_0,Vgs_AGD_0)
xlim([72.4 73.1]);
ylim([-10 25]);
hold on
plot(Time_1,Vgs_AGD_1)
plot(Time_2,Vgs_AGD_2)
plot(Time_3,Vgs_AGD_3)
plot(Time_4,Vgs_AGD_4)
plot(Time_5,Vgs_AGD_5)
plot(Time_6,Vgs_AGD_6)
grid
ylabel('Vgs(V)')
% legend('8.1V','7.5V','6.9V','6.3V','5.6V','5V')


subplot(3,1,2)
plot(Time_0,Vds_AGD_0)
```

```
xlim([72.4 73.1]);
ylim([-500 5500]);
hold on
plot(Time_1,Vds_AGD_1)
plot(Time_2,Vds_AGD_2)
plot(Time_3,Vds_AGD_3)
plot(Time_4,Vds_AGD_4)
plot(Time_5,Vds_AGD_5)
plot(Time_6,Vds_AGD_6)
grid
legend('8.1V','7.5V','6.9V','6.3V','5.6V','5V','-5V')
ylabel('Vds(V)')

subplot(3,1,3)
plot(Time_0,Ids_AGD_0)
xlim([72.4 73.1]);
ylim([-3 25]);
hold on
plot(Time_1,Ids_AGD_1)
plot(Time_2,Ids_AGD_2)
plot(Time_3,Ids_AGD_3)
plot(Time_4,Ids_AGD_4)
plot(Time_5,Ids_AGD_5)
plot(Time_6,Ids_AGD_6)
grid
ylabel('Ids(A)')
xlabel('Time(us)')
% legend('8.1V','7.5V','6.9V','6.3V','5.6V','5V')
```