Doctoral Thesis

ULTRA-LOW PHASE NOISE AND MULTIPLE FREQUENCY BAND FREQUENCY SYNTHESIZERS FOR 5G MOBILE SYSTEMS

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Approved by

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Abstract

This thesis mainly focuses on the design of the frequency synthesizers for 5G transceivers, which requires very low phase noise performance. Before introducing the design of the proposed low phase noise frequency synthesizer, fundamentals of the frequency synthesizer and the *LC* VCO are discussed in Chapter 2 and 3, respectively. From Chapter 4, the design of the previous works is detailed as follows.

In Chapter 4, the proposed multi-band LO generator is presented that concurrently can support existing cellular bands below 6 GHz and new millimeter-wave (mmW) bands for 5G. Using a low-noise reference-frequency doubler, a ΔΣ fractional-*N* phase-locked loop (PLL) generates GHz-range signals with low integrated phase noise (IPN). Then, injection-locked frequency multipliers increase these frequencies to mmW bands without degrading IPN. The LO-generator was fabricated in a 65-nm CMOS process. When the PLL is in the fractional-*N* mode, the measured IPN and RMS jitter integrated from 1 kHz to 100 MHz of the 29.23-GHz signal were −31.4 dBc and 206 fs, respectively. When the PLL is in the integer-*N* mode, the measured IPN and RMS jitter of the 28.8-GHz signal were −33.1 dBc and 172 fs, respectively. The silicon area was 0.95 mm^2, and the total power consumption was 36.4 mW.

In Chapter 5, the proposed ultra-low-IPN 28 − 31 GHz frequency synthesizer is presented. A GHz-range digital-sub-sampling PLL (SSPLL) at the first stage can achieve low in-band phase noise and a wide capture range. The optimally-spaced voltage comparators (OSVC) used in the SSPLL effectively minimizes the quantization noise. Since the following mmW injection-locked frequency multiplier (ILFM) has a very wide bandwidth, the proposed frequency synthesizer achieved ultra-low IPN and RMS jitter, i.e., –40 dBc and 76 fs, respectively, when it was fabricated in 65-nm CMOS process. The silicon area was 0.32 mm^2, and the total power consumption was 41.8 mW.

In Chapter 6, a wideband and low phase noise quadrature local oscillation (LO) signal generator for multi-standard cellular transceivers was proposed. Using the new LO-plan consisting of divide-by-6, divide-by-4, and divide-by-12 frequency dividers, the required frequency tuning range (FTR) of a VCO was reduced to 39%, which can be easily covered by a single *LC*-VCO. Due to the reduced FTR, the VCO can retain a high Q-factor and achieve low phase noise. The key building block of the new LO-plan is a quadrature divide-by-6 divider, capable of generating precise I/Q signals. To implement the quadrature divide-by-6 divider, we proposed a fully differential divide-by-3 divider with 50% duty cycle. Using the same idea, a fully differential divide-by-2 circuit was also proposed for divide-by-4 and divide-by-12 dividers. The proposed LO-generator was fabricated in a 40-nm CMOS process, and covered LO-frequencies of 0.56 – 2.92 GHz for multi-standard cellular transceivers. The LO-generator occupied a small silicon area of 0.15 mm^2 and achieved an excellent phase noise performance of –141.02 dBc/Hz at a 1-MHz offset from a 709-MHz LO-frequency.

In Chapter 7, a wideband *LC*-VCO with a g_m-switching technique was designed and fabricated in the 65-nm CMOS process. With a switchable secondary gate-biased active core as well as the primary one, the VCO operates in two different modes. In the low-frequency mode, where switches turn on the secondary core, the increased start-up gain facilitates low-frequency oscillation. In the high-frequency mode, where the switches isolate the secondary core from the primary core, the reduced capacitive loading allows for high-frequency oscillation. In addition, since the gate-bias of the secondary core transistors guarantees high transconductance of the secondary core, the switch size can be minimized, which further extends the upper boundary of the oscillation frequency. The VCO achieved a 41% frequency range, 3.36 – 5.1 GHz, and −123.1 dBc/Hz phase noise at the 1 MHz offset from the 4.21 GHz output frequency. The active silicon area was 0.24 mm^2, and power consumption was 8.7 mW at 5 GHz.

In Chapter 8, a clock generator is presented, which can provide multiple ultra-low jitter clocks with different frequencies. Using a time-interleaved multi-DCO calibrator, the frequencies of the multiple injection-locked DCOs were continuously tracked and corrected, independently, between 0.9 and 1.2 GHz with a 15 MHz step. Due to the calibrator, each clock was capable of maintaining an excellent jitter performance; the RMS-jitter was 309 fs at 930 MHz, and its variation was regulated to less than 9% over PVT.

Finally, Chapter 9 concludes this thesis with a summary of the proposed frequency synthesizer design for 5G mobile systems.

Contents

List of Figures

List of Tables

Technical Terms and Abbreviations

QAM	Quadrature amplitude modulation
2G	2nd mobile phone generation, e.g., GSM
3G	3rd mobile phone generation, e.g., UMTS
4G	4th mobile phone generation, e.g., LTE-A
5G	5th mobile phone generation
IPN	Integrated phase noise
EVM	Error vector magnitude
ADC	Analog to digital converter
RF	Radio frequency
LO	Local oscillation
LTE	Long-term evolution
NLOS	Non line of sight
Q-factor	Quality factor
PLL	Phase-locked loop
VCO	Voltage controlled oscillator
DCO	Digitally controlled oscillator
FOM	Figure-of-Merit
ILFM	Injection-locked frequency multiplier
RFD	Reference frequency doubler
SSPLL	Sub-sampling PLL
DSM	Delta-sigma modulator
XTAL	Crystal oscillator
PFD	Phase-frequency detector
CP	Charge pump
LF	Loop filter
BER	Bit error rate
AM	Amplitude modulation
PM	Phase modulation
FM	Frequency modulation
SSB	Single-sideband
SNR	Signal-to-noise ratio
NIC	Network interface card

DFF	D-flip flop
FTR	Frequency tuning range
NTF	Noise transfer function
BW	Bandwidth
MIM	Metal-insulator-metal
MOM	Metal-oxide-metal
CBM	Capacitance bottom metal
CTM	Capacitance top metal
CM	Common mode
DM	Differential mode
LTI	Linear-time invariant
LTV	Linear-time variant
ISF	Impulse sensitivity function
IoT	Internet of Things
mmW	Millimeter wave
FTL	Frequency-tracking loop
DLL	Delay-locked loop
PRBS	Pseudo-random binary sequence
TRX	Transceiver
PN	Phase noise
Q-noise	Quantization noise
PVT	Process-voltage-temperature
SH	Sample and hold
CA	Carrier aggregation
QVCO	Quadrature VCO
PPF	Poly-phase filter
ILRO	Injection-locked ring VCO
PSRR	Power-supply rejection ratio
TDC	Time-to-digital converter

1. Introduction

1.1 Motivation and Objective of Research

After the emergence of a wireless network, mobile communications have strongly influenced human life such as health, leisure, education, and industry, and it becomes indispensable to the lives of 7.5 billion people. As shown in Figure 1, for the past several decades, mobile communication systems have evolved gradually from 2G to 4G to satisfy the increasing demands from new multi-media contents, which requires high data rates. Recently, the demand for ultra-fast mobile communications has become unprecedentedly strong due to the emergence of new technologies that require high data throughput, such as virtual reality (VR), augmented reality (AR), massive Internet of Things (IoT), and 3D holograms. Therefore, global mobile data traffic is expected to exponentially grow up to 77 EB per month by 2022 (EB: exabyte = 10^{18} byte) according to *CISCO* [1].

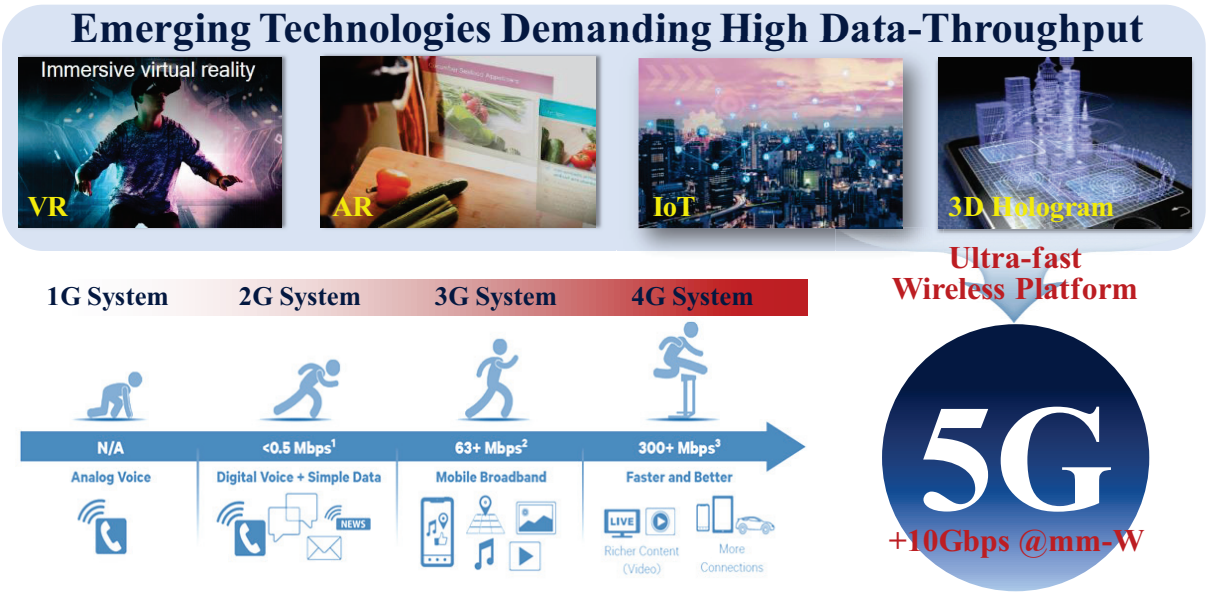


Figure 1. Evolution of communication systems and 5G for emerging IT technologies

As the next generation mobile system to satisfy this demand, 5G mobile communications attract a lot of attention as the next-generation wireless platform that provides more than 10Gbps data rate in mm-wave frequency bands. To achieve such high data rates, it is important to use high-order modulations, such as 64 or 256 QAM [2]−[5]. Thus, one of the most challenging tasks to design wireless transceivers for 5G systems is the generation of millimeter-wave (mmW)-band local oscillation (LO) signals that have an ultra-low integrated phase noise (IPN) even when the bandwidth is wide. For example, the high-order modulations require low the error-vector-magnitude (EVM); the 5G standard demands carrier signals having extremely low IPN, e.g. below −39 dBc at mmW bands. In addition, direct RF-data converts that use high-speed analog-to-digital converters (ADCs) to samples RF signals directly

are the emerging transceiver architecture. To satisfy the Nyquist criterion and minimize the effect of channel mixing, this new architecture also asks sampling clocks to have very high frequency and excellent noise performance [6]. The demands on the ultra-low IPN (or jitter) of high-frequency signals also increase in advanced wireline communications, such as SerDes systems, targeting ultra-high data rates more than 100 Gbps. Although applications are various from wireless to wireline as above, it is very same that to satisfy each of their requirements, the RMS jitter of mmW-band signals must be reduced to sub-100 fs.

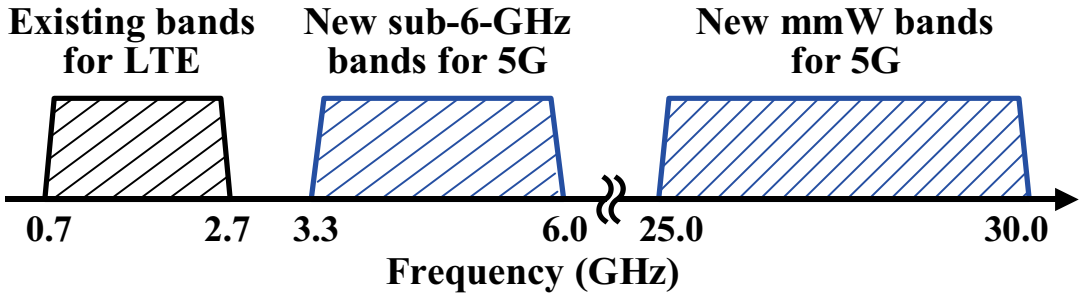


Figure 2. Frequency spectrum of existing bands and new bands for 5G system

Figure 2 shows the frequency spectrum for cellular systems, including existing bands for 4G long-term evolution (LTE) from around 700 MHz to 2.7 GHz [5], [7] and new frequency bands for 5G systems, including bands below 6 GHz and mmW bands. As shown in Figure 3, during the evolution of mobile communications, the key principle of the industry has been to ensure interoperability with past-generation standards and spectra. Based on this principle, mobile devices with backward compatibility easily can enter the markets of different countries, where the transition of networks to newer access technologies is still ongoing. This trend is expected to continue for 5G systems.

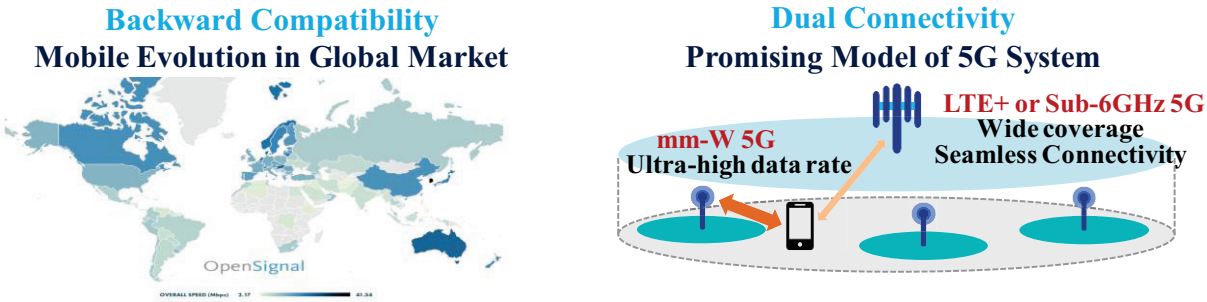


Figure 3. Key principles of 5G system; Backward compatibility and dual connectivity

In addition, to overcome the limited coverage of mmW signals and improve the robustness of communications even in non-line-of-sight (NLOS) environments, a realistic model of 5G systems is the dual-connectivity between LTE (or sub-6-GHz 5G) and mmW-band 5G, as shown in Figure 3. In this model, which is based on the concept of small cells [8], [9], LTE (or sub-6-GHz 5G) using spectrum

below 6 GHz will evolve in a way that it provides wide coverage and seamless connectivity, while mmW-band 5G enables ultra-high-bandwidth communications [9]. Therefore, considering the interoperability with existing standards and the dual connectivity of the practical 5G model, it is important for 5G transceivers to support multiple frequency bands in an efficient manner.

Recent, there have been many researches to develop phase-locked loops (PLLs) that directly synthesize signals in mmW bands [10]−[16]. However, those architectures have several intrinsic problems. First, they cannot achieve a very low IPN. The survey in [17] summarized the recently reported phase noises of PLLs using CMOS operating at different output frequencies. Also, the survey normalized the values of the phase noises to the same frequency. According to the survey, PLLs that directly generate mmW signals have much inferior phase noise performances than PLLs that generate GHz signals, such as 3 – 6 GHz. The main reason is the degraded quality factor (Q-factor) of *LC* tank in voltage-controlled oscillators (VCOs), which is a well-known phenomenon at high frequencies, such as in the mmW-band due to the skin effect and eddy current [18], [19]. The second problem of the direct mmW PLLs is their limited frequency-tuning range. Since the portion of the parasitic capacitance in the *LC* tank increases for the same resonance frequency, the VCOs that generate mmW signals cannot obtain a wide frequency-tuning range [20]. Third, when PLLs are required to generate LO signals for the lower frequency bands below 6 GHz, they must divide the output frequencies again, necessitating additional circuits and power.

For generating a low-noise mmW-bands LO signal, another possible solution is to generate an output frequency in the range of 3 − 6 GHz from a GHz-range PLL and then multiply the frequency to mmW bands by a frequency multiplier whose noise is extremely low. In the GHz frequency range, i.e., 3 − 6 GHz, a Q-factor of the tank of *LC* VCOs is much higher than that of mmW *LC* VCO and a portion of parasitic capacitance in the *LC* tank is much low. Thus, a GHz-range PLL can have better performances in terms of phase noise and frequency-tuning range. In addition, in this architecture, low-frequency bands can be generated naturally by the PLL without the use of additional circuits and power. Thus, if we want to achieve low phase noise along with a wide frequency-tuning range and low power consumption simultaneously, it is obvious that the cascading architecture using a GHz PLL and a frequency multiplier is a much better choice for generating LO signals for 5G transceivers.

In light of the above trends of the mobile communication systems, this thesis is dedicated to identifying a successful prototype for mmW-band low-phase-noise frequency synthesis. Using a cascade architecture of a GHz-range PLL and low phase-noise injection-locked frequency multipliers, characteristics of wideband low-noise frequency synthesis are analyzed, leading to the proposed design. A prototype is implemented to demonstrate the feasibility of the mmW-band low-phase-noise frequency synthesizers based on cascading architecture.

1.2 Thesis Organization

This thesis mainly focuses on an LO generator that can provide ultra-low IPN signals in multiple frequency bands, i.e., mmW bands and bands below 6 GHz. Based on cascading architecture explained above, the proposed LO generator uses a combination of a GHz-range PLL with high figure-of-merit (FOM) and low phase-noise injection-locked frequency multipliers (ILFMs) [21]. To further reduce the IPN, we also propose an ultra-low phase noise reference-frequency doubler (RFD). The proposed RFD increases the reference frequency, which suppresses the level of the in-band phase noise and the delta-sigma modulator (DSM) noise of the PLL. In addition, to further suppress the in-band phase noise of loop-building blocks, a digital sub-sampling PLL (SSPLL) is adopted for the GHz-range PLL. Consequently, the LO signal at 28 GHz from the proposed LO generator can achieve an ultra-low IPN that can satisfy the requirements of 5G systems.

Organization of this thesis is as follows. First, Chapter 2 and 3 focus on providing fundamentals. In Chapter 2, the basics of a PLL-based frequency synthesizer will be discussed along with the key metrics, explanation of each building blocks, and analysis on the phase noise and the stability. In Chapter 3, the basics of an *LC*-based VCO will be detailed; the basics of the *LC* resonator, design considerations, and the modeling of the phase noise based on the linear time-invariant and the linear time-variant analysis.

Through Chapter 4 and Chapter 5, the design of the proposed work for the 5G mobile system is presented. Chapter 4 introduces the design of the PLL-based frequency synthesizer with low phase noise targeting for 5G transceivers. Then, in Chapter 5, the low phase noise frequency synthesizer will employ the sub-sampling PLL rather than the CPPLL used in Chapter 4, to have a better phase noise performance.

Lastly, from Chapter 6 to Chapter 8, previous works will be presented as foundation research of the frequency synthesizer for 5G. In Chapter 6, the proposed design of the LO generator that can provide quadrature signals and low phase noise will be introduced. Chapter 7 only focuses on the wideband *LC* VCO design to break off intrinsic trade-off regard to the frequency-tuning range of the *LC* VCO. Chapter 8 discusses the design of the clock generator that can provide multiple output frequencies having independent output frequencies.

Finally, Chapter 9 concludes this thesis with the contributions of the proposed frequency synthesizer and previous research to the development of the 5G mobile systems.

2. Fundamentals of PLL-Based Frequency Synthesizers

2.1 Basic Characteristics

2.1.1 Basics Operation of PLL

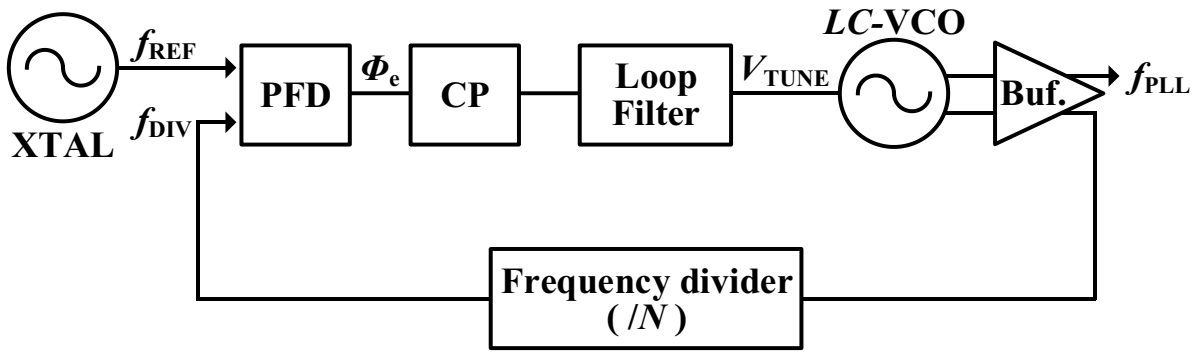


Figure 4. Block diagram of phase-locked loop

A phase-locked loop (PLL) is a control system that has been widely employed in many wireless and wired communications for providing a stable clock signal, which can be used to modulate or demodulate a signal, to synthesize a frequency at multiples of an input frequency, and to distribute clock pulses with a minimized clock skew in digital logic circuits, i.e., microprocessors. A basic structure of the PLL shown in Figure 4 is composed of a crystal oscillator (XTAL), *LC* VCO, a divide-by-*N* frequency divider, a phase-frequency detector (PFD), a charge pump (CP), and a loop filter (LF). f_{REF}, f_{DIV}, f_{PLL}, and Φ_e are the reference frequency, the output frequency of the frequency divider, the output frequency of the PLL, and the phase error (or phase difference) between f_{REF} and f_{DIV}, respectively. The XTAL provides f_{REF} to the PFD for detecting frequency drifts of the *LC* VCO. The PFD detects the phase or frequency difference between f_{REF} and f_{DIV}, and outputs Φ_e. According to Φ_e, the CP sources or sinks charges of the LF to adjust the value of V_{TUNE}. Thus, Φ_e can be reduced to zero by changing the output frequency of the *LC* VCO according to V_{TUNE}, as expressed as,

$$\omega_{PLL}=\omega_0+K_{VCO}\cdot V_{TUNE} \tag{1}$$

where ω_0, K_{VCO}, and V_{TUNE} are the initial frequency, the gain, the control voltage of the *LC* VCO, respectively. In this manner, the PLL can provide a stable output frequency even with process-voltage-temperature variations. When the PLL is locked, i.e., in steady state, the output frequency of the PLL can be expressed as,

$$f_{PLL}=N\cdot f_{REF} \tag{2}$$

where N is a dividing ratio of the frequency divider, which is an integer. As expressed in Equation (2), by changing the value of N, the output frequency of the PLL, f_{PLL}, can be changed with a resolution of f_{REF}, i.e., the PLL only can generate output frequencies at a multiple of f_{REF}. In this case, if the PLL is used for the RF transceivers, the channel spacing is restricted by f_{REF}. For reducing channel spacing to meet the channel spacing requirements of the wireless communications, (e.g. GSM channel spacing; 200 kHz) the PLL is forced to decrease the reference frequency by dividing f_{REF} before f_{REF} goes to the PFD. However, it eventually increases the dividing ratio of the frequency divider, N, and thus, the output phase noise of the PLL is degraded severely due to the reference phase noise amplification. In addition, due to the low f_{REF}, the bandwidth of the PLL is narrow [22], which means that slow settling time and little phase noise suppression of the *LC* VCO. To break this trade-off regarding the channel spacing, a fractional-*N* PLL was introduced by using delta-sigma modulator (DSM), as shown in Figure 5.

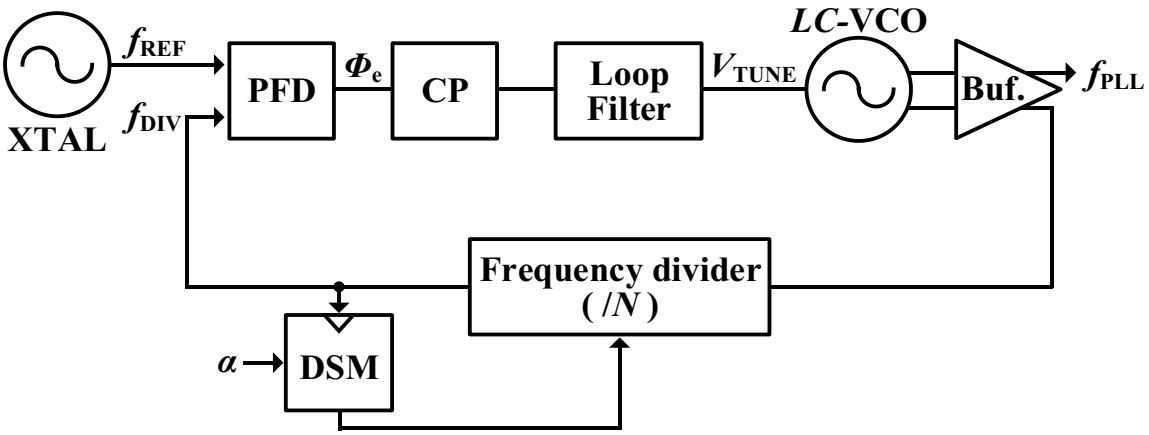


Figure 5. Block diagram of a fractional-*N* PLL

As shown in Figure 5, a DSM was additionally used to achieve a fine channel spacing without decrease f_{REF}. Therefore, in the fractional-*N* PLL, f_{REF} can be chosen to be much higher than the channel spacing. The output frequency of the fractional-*N* PLL can be represented as,

$$f_{PLL} = (N+\alpha) \cdot f_{REF} \tag{3}$$

where α is greater than or equal to zero and less than one.

2.1.2 Key Metrics of the PLL

Spectral purity is one of the most important performance characteristics of the frequency synthesizers. In modern RF communication systems, Error Vector Magnitude (EVM) is one of the key factors to represent the quality of the transmitted signal. Only when the EVM is low enough, the receiver can have an ability to recover the transmitted signal with a good Bit Error Rate (BER), since phase noise could degrade the sensitivity of the receiver due to a reciprocal mixing. In 4G wireless communication systems, the required EVM of the overall transmitter must be less than 3%, while the contribution of the PLL should be less than 2%. Therefore, to secure low phase noise performance of the frequency synthesizer is the most important task in modern RF communication systems. For the oscillators and PLLs in RF communication systems, noise performance is usually represented in terms of phase noise, meanwhile, noise is usually characterized in terms of jitter for the clock in microprocessors. In the following, the definition of phase noise and jitter is introduced and they are related to each other.

Spectral Purity: Phase noise

The well-known definition of phase noise is the frequency-domain representation of random fluctuations or variations in the phase of a signal. In the time domain, phase noise corresponds to jitter, deviations from the ideal periodicity of the signal. As shown in Figure 6(a), the output spectrum of an ideal oscillator can be represented as a single pair of Dirac delta functions at the oscillator's resonant frequency, since the ideal oscillator generates a pure sine wave, which can be quantified as,

$$V(t)=A\cdot\sin(2\pi f_0 t) \tag{4}$$

(a) (b)

Figure 6. (a) Spectrum of ideal oscillator (b) spectrum of a real oscillator

However, in practice, all real oscillators have noise components spreading the power of the signal to adjacent frequencies as shown in Figure 6(b), which can be expressed as

$$V(t)=A(t)\cdot\sin(2\pi f_0 t+\Phi(t)) \tag{5}$$

where A(t) and $\Phi(t)$ are amplitude and phase fluctuations, respectively. In case of the amplitude fluctuations, A(t), since the oscillator has a stable limit cycle, the amplitude fluctuations eventually decays away and the oscillator returns to the stable limit cycle. Thus, we can assume that A(t) can be represented as a constant A, rather than A(t). However, in case of the phase fluctuations, once the phase has shifted due to the fluctuations, the phase deviations only accumulate. Thus, Equation (5) can be represented as

$$V(t)=A\cdot\sin(2\pi f_0 t+\Phi(t)) \tag{6}$$

If we assume that $\Phi(t)$ is much smaller than 1 radian, the small-angle approximation can transform Equation (6) as

$$V(t)\approx A\cdot\sin(2\pi f_0 t)+A\cdot\Phi(t)\cdot\cos(2\pi f_0 t) \tag{7}$$

where the first and second term represents the ideal signal and the phase noise, respectively.

Oscillator's noise also can be represented as a phasor rotating around the rotating carrier phasor, as shown in Figure 7 [23].

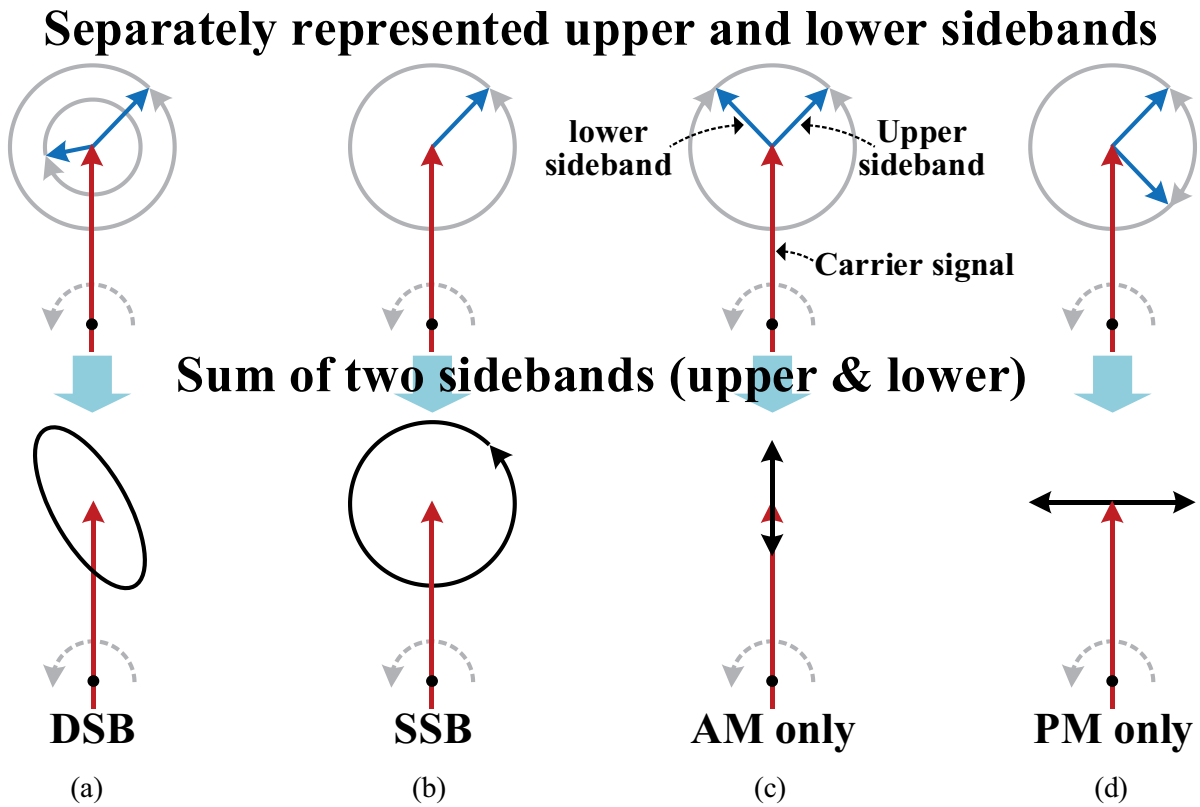


Figure 7. Phasor representation of a carrier signal with two sidebands in four difference cases

Figure 7 shows how the relationship between the amplitude and phase at two sidebands causes amplitude modulation (AM) and phase modulation (PM) in a carrier signal. The phasors in red and blue represent the carrier signal and the sidebands, respectively. In this figure, a frequency that the two sidebands rotate is the offset frequency, $\Delta\omega$. The upper sideband rotates in the same direction of the carrier signal with a frequency of $\Delta\omega$, meanwhile, the lower sideband rotates in the opposite direction of the carrier signal. In Figure 7(a), when the two sidebands are completely uncorrelated, the summed trace of the sidebands makes an ellipse whose size, shape, and orientation moves randomly. If we only focus on the upper sideband, i.e., single-sideband (SSB), the phasor diagram would be represented as Figure 7(b). However, if the noise is cyclostationary, two sidebands have a correlation, which means that the summed trace will remain unchanged. When there is only AM or PM noise source, the phasor diagram can be drawn as in Figure 7(c) and (d), respectively.

The SSB phase noise is defined as the ratio of power in a 1 Hz measurement bandwidth to the total power of the carrier signal at a frequency offset $\Delta\omega$ (or Δf) as shown in Figure 8 and the unit of phase noise is dBc/Hz. As shown, the real oscillator has phase noise "skirt" centered at the carrier frequency.

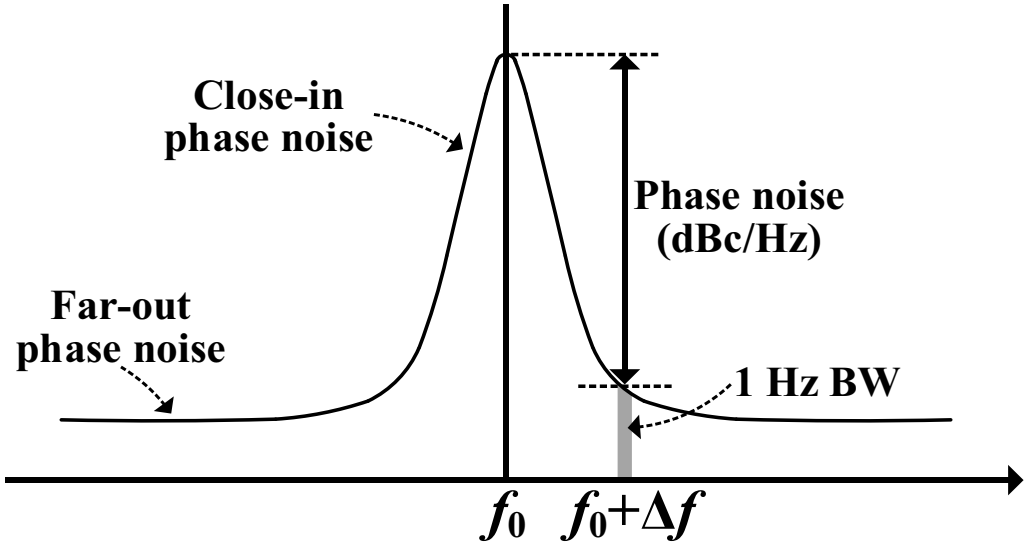


Figure 8. Difinition of phase noise in frequency domain

Phase noise also can be represented as,

$$L(\Delta f)=10\log_{10}\left(\frac{\text{Noise power in 1 Hz at } f_0+\Delta f}{\text{Carrier power}}\right) \tag{8}$$

where $L(\Delta f)$ represents SSB phase noise at the frequency offset of Δf. The details of phase noise in a real oscillator will be detailed in Chapter 3.

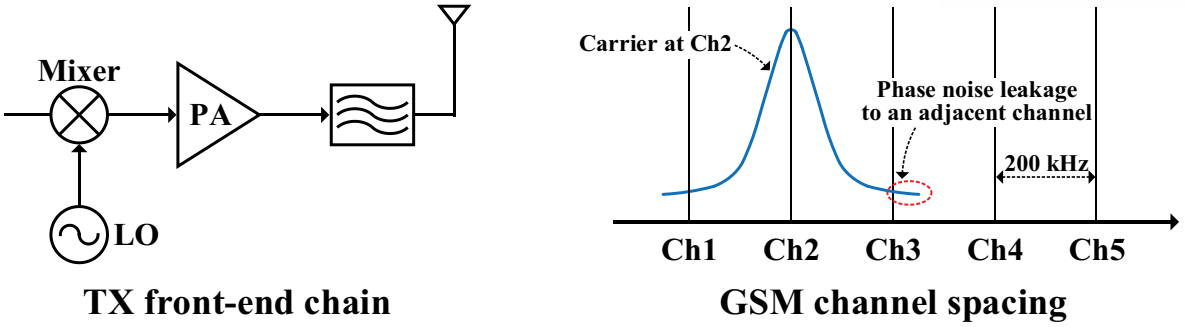


Figure 9. Phase noise in the transmitter chain

Figure 9 shows the front-end chain of the transmitter with a channel spacing of the GSM standard. As shown, the phase noise of the local oscillator (LO) will leak power into the adjacent channel; in this example, the power of the Ch2 leaks to Ch3. Generally, the power of the transmitted signal is large, i.e. about 30 dBm. Thus, when the channel spacing is narrow (e.g. GSM' channel spacing: 200 kHz), stringent phase noise is required on the LO in the transmitter not to hinder the adjacent channels.

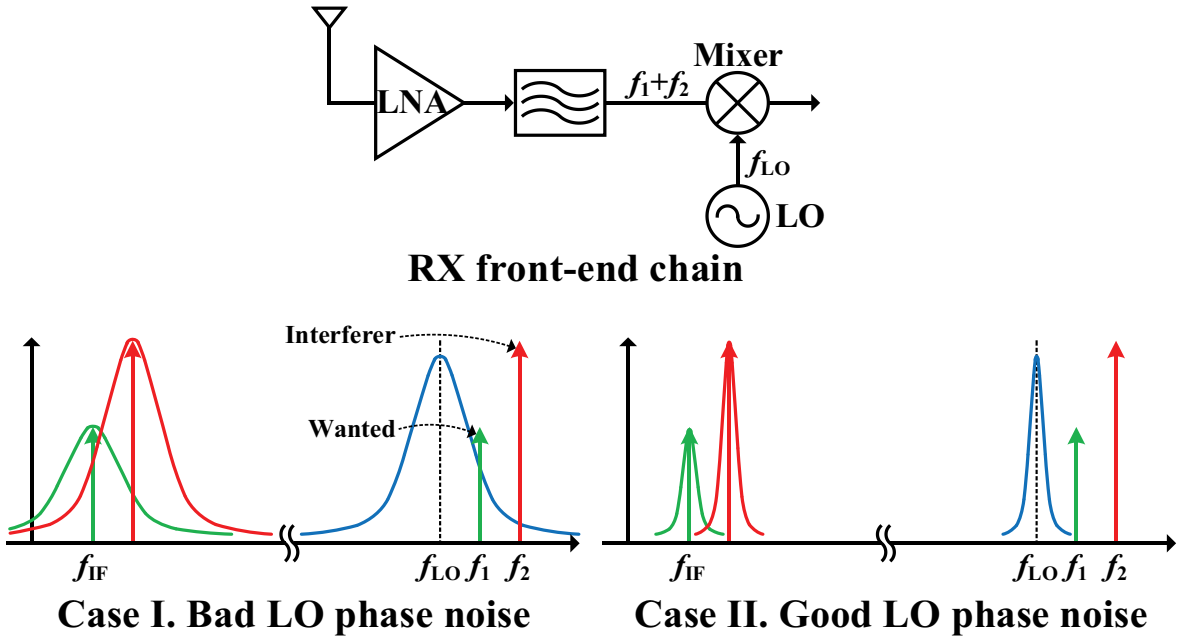


Figure 10. Phase noise in the receiver; reciprocal mixing

Figure 10 shows the concept of a reciprocal mixing in the receiver chain. As shown in Case I, when the phase noise of LO is noisy, the down-converted interferer degrades the signal-to-noise ratio (SNR) of the down-converted-wanted signal since the wanted signal is severely suffered from noise due to the tails of the down-converted interferer. However, as shown in Case II, when the phase noise of LO is good enough, the down-converted-wanted signal is not saturated by the tail of the down-converted interferer. Thus, the LO generators in the receivers, it is also important to achieve low phase noise.

Spectral Purity: Jitter

As explained above, for some application, jitter is more preferred metric measuring noise than the phase noise. Jitter is defined as the short-term variation of a signal with respect to its ideal position in time. Jitter is carefully considered in digital applications. For example, computers, data servers, network interface cards (NICs), embedded systems, etc. The types of jitter can be classified as shown in Figure 11.

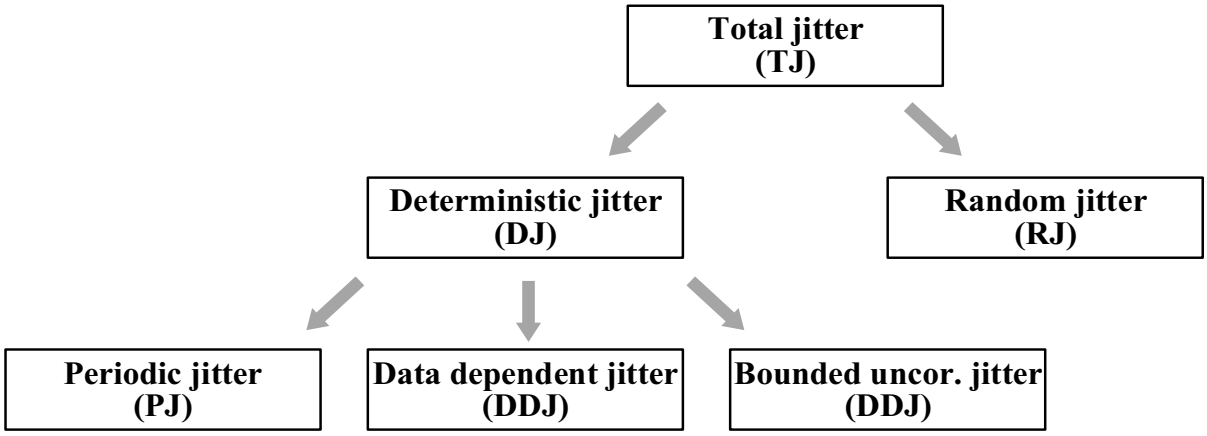


Figure 11. Jitter subcomponents of total jitter

As shown in Figure 11, total jitter can be categorized to deterministic jitter and random jitter. In the following table, characteristics and well-known causes of each jitter are simply summarized.

Table 1. Summary of jitter characteristics and causes

		Characteristics	Root causes
Random jitter		Gaussian Not bounded	Thermal noise
Deterministic	**Periodic jitter**	Non-gaussian Bounded	Electromagnetic interference (EMI)
	Data dependent jitter		Rise & fall time difference, ISI
	Bounded uncorrelated jitter		Crosstalk

Jitter can be measured with different methods according to the applications. Generally, there are four metrics for jitter measurement; period jitter (*PerJ*), cycle-to-cycle jitter (J_{CC}), phase jitter (σ_J), and time-interval error (*TIE*).

Period Jitter (*PerJ*)

Period jitter is defined as a variation of a signal period from the ideal period, which is typically replaced with the average period of the signal. Figure 12 shows how an oscilloscope measures period jitter.

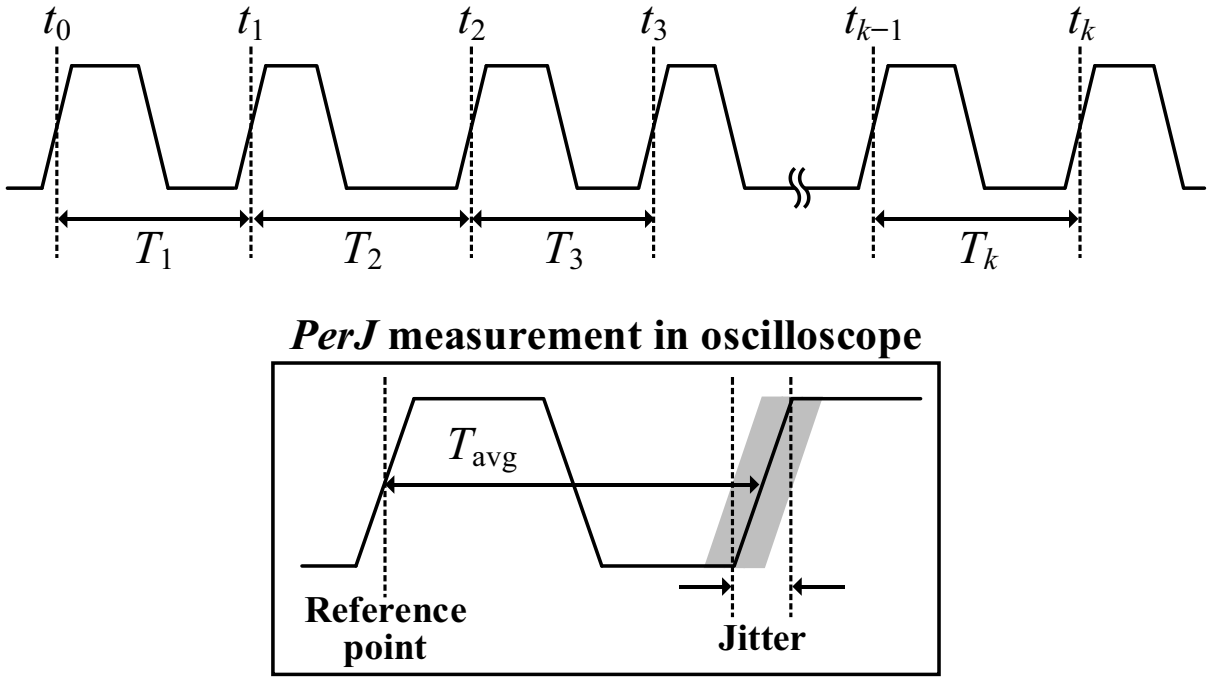


Figure 12. Measurement of period jitter

Based on the definition of period jitter and Figure 12, period jitter and that of RMS value can be represented as

$$PerJ(k) = T_k - T_{avg} \tag{9}$$

and

$$PerJ_{RMS} = STDEV(T_k), \tag{10}$$

respectively. Period jitter is extensively used in estimating timing margin in digital systems, i.e., setup time and hold time, by calculating the peak-to-peak value of period jitter.

Cycle-to-Cycle Jitter (J_{CC})

Cycle-to-cycle jitter is the difference of two adjacent clock period and it is dominated by the high-frequency noise components. It means that cycle-to-cycle jitter is not sensitive to low-frequency noise or slow frequency modulation of the oscillator frequency. Figure 13 and the following Equation (11) show how cycle-to-cycle jitter is calculated.

$$J_{CC}(k) = T_k - T_{k-1} = t_k - 2t_{k-1} + t_{k-2} \quad (11)$$

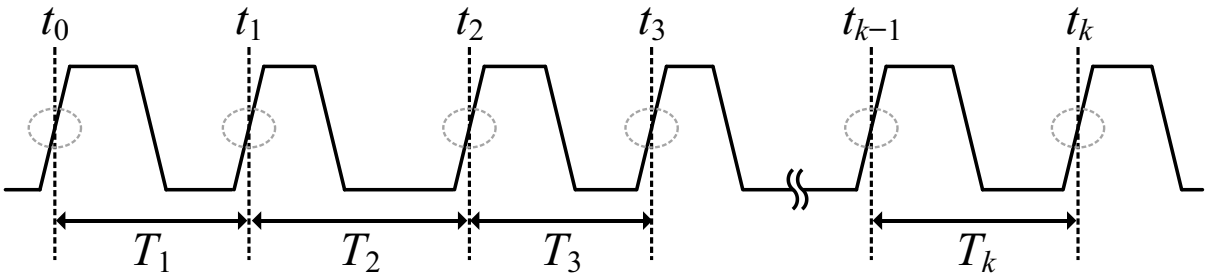


Figure 13. How to measure cycle-to-cycle jitter

Phase Jitter (σ_J)

Phase jitter is the integrated phase noise of a carrier over a specified offset frequency range as shown in Figure 14. In the time domain, phase jitter also represents edge variation relative to an ideal noise-free clock. It is an important metric in serial interface applications, such as PCIe, SATA/SAS, etc.

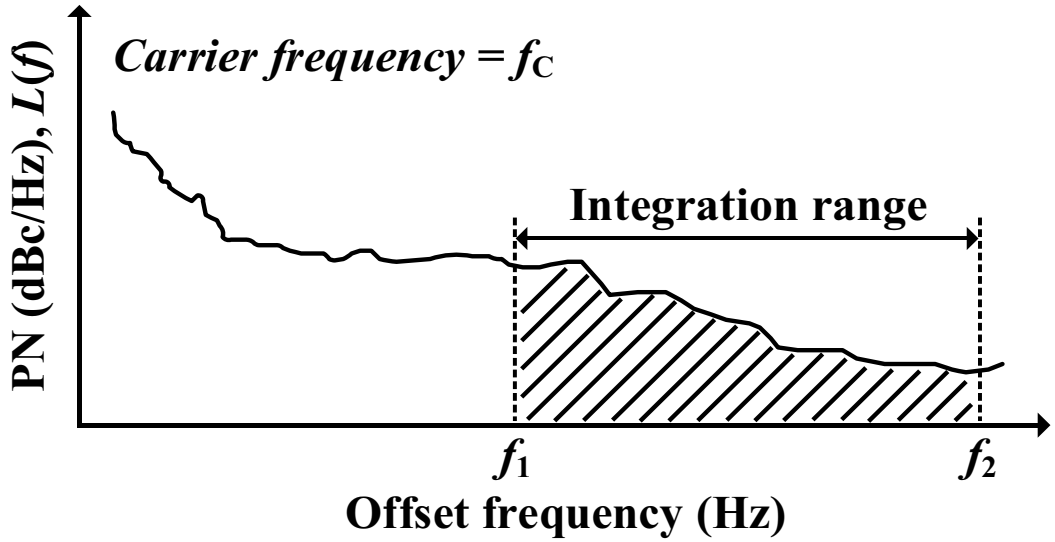


Figure 14. Phase jitter calculation based on the phase noise of a carrier

In mathematical presentation, based on Figure 14, RMS phase jitter can be calculated as

$$\sigma_{J,\mathrm{RMS}} = \frac{1}{\sqrt{2}\pi f_C} \cdot \sqrt{\int_{f_1}^{f_2} 10^{\frac{L(f)}{10}} \cdot df} \tag{12}$$

where $L(f)$ and f_C are SSB phase noise and carrier frequency, respectively.

Time Interval Error (*TIE*)

Time interval error of an edge is the time deviation of that edge from its ideal position measured from a reference point. Thus, sometimes it is called as accumulated jitter. Figure 15 clearly shows how to measure time interval error. The measured the time interval error can be represented as

$$TimeJ(k) = TIE_k = t_k - k \cdot T_C \tag{13}$$

In most cases, time interval error carries the same information of phase noise, and thus, by taking Fast Fourier Transform (FFT) to time interval error, we can approximate phase noise.

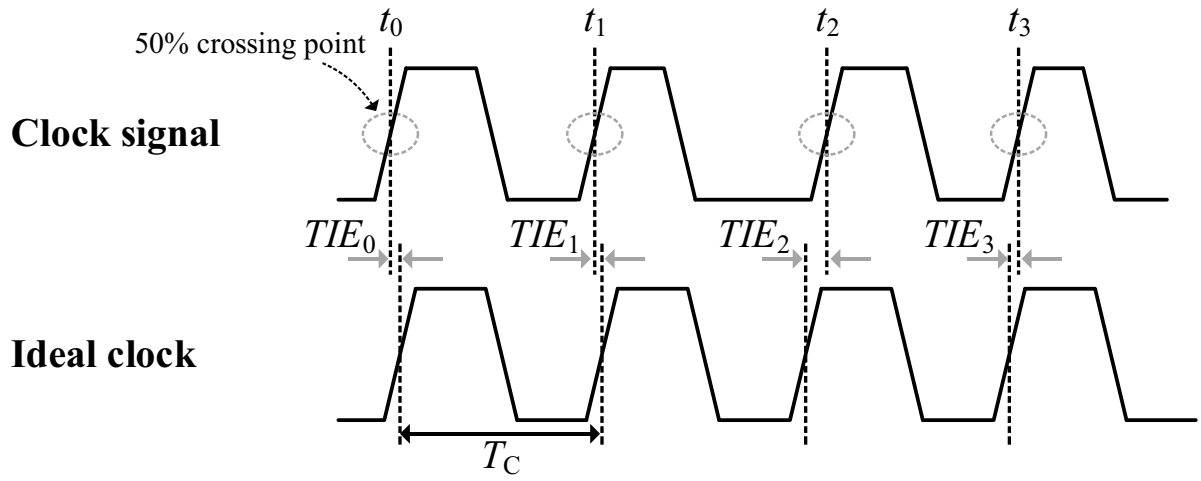


Figure 15. How to measure time interval error

In summary, both phase noise and jitter can be interchangeably used to estimate spectral purity performance, although the domain is different between phase noise (frequency domain) and jitter (time domain). Theoretically, if we have perfect measuring equipment, measured phase noise to an infinite offset frequency would show the same value as jitter. In reality, there will always be a discrepancy between phase noise and jitter. Table 2 shows the summarized characteristics of phase noise and jitter.

Table 2. Characteristics of phase noise and jitter

Phase noise	Jitter
❖ Measured by a spectrum analyzer or a phase noise analyzer ❖ Cycle-to-cycle or peak-to-peak jitter cannot be directly measured ❖ Easy to recognize random jitter and deterministic jitter (spur) ❖ RMS phase jitter can be measured by integrating specified integration range	❖ Measured by an oscilloscope ❖ Cycle-to-cycle or peak-to-peak jitter can be directly measured ❖ Generally, time domain equipment has a higher noise floor than frequency domain equipment

Spurious Tones in PLL

Basically, there are various causes for the spur generation in the PLL; the modulation signal at the control voltage of the VCO, fractional spurs when the PLL is in fractional mode, spurs from supply or ground, etc. In this section, only the spur from the modulation of VCO control voltage is detailed. When there is a modulation source at the VCO input, spur appears at the output spectrum of the VCO, as shown in Figure 16.

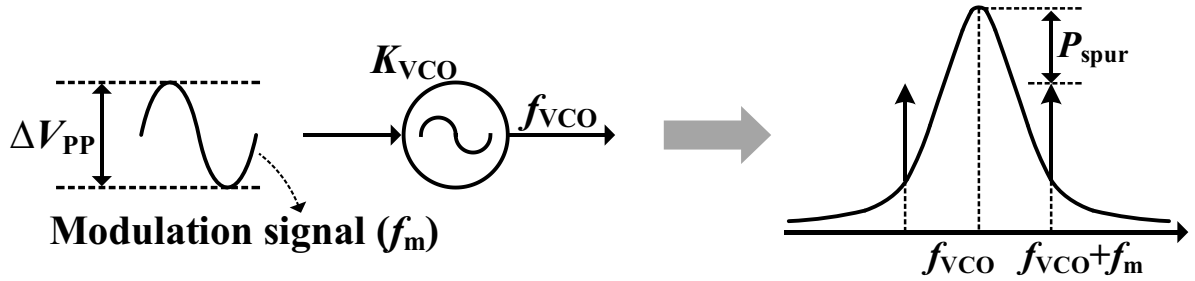


Figure 16. Spur at the frequency offset of f_m due to the modulation signal

To estimate the level of the spur due to the modulation signal, first, we need a frequency modulation (FM) theory [24]. Any FM signal can be expressed by using a Bessel function series with modulation index m, as shown below [25].

$$\begin{aligned} V(t) &= V\cdot\sin(\omega_{VCO}t + m\cdot\sin(\omega_m t)) \\ &= V\cdot[J_0(m)\cdot\sin(\omega_{VCO}t) \\ &+ J_1(m)\cdot\{\sin(\omega_{VCO}+\omega_m)t + \sin(\omega_{VCO}-\omega_m)t\} \\ &+ J_2(m)\cdot\{\sin(\omega_{VCO}+2\omega_m)t + \sin(\omega_{VCO}-2\omega_m)t\} + \ldots] \end{aligned} \quad (14)$$

For narrowband FM, i.e., m is much smaller than one, Bassel function $J(m)$ will be

$$J_0(m) = 1,\ J_1(m) = m/2, \text{ and } J_k(m) \approx 0 \text{ for } k \geq 2 \quad (15)$$

Therefore, by combining Equation (14) and (15), the FM signal can be simplified as

$$V(t) = V\cdot[\sin(\omega_{VCO}t) + m/2\cdot\{\sin(\omega_{VCO}+\omega_m)t + \sin(\omega_{VCO}-\omega_m)t\}] \quad (16)$$

From Equation (16), the level of the spur of the FM signal can be given in unit of dBc by

$$P_{spur} = 10\log_{10}\left(\frac{\text{SSB power of modulation signal}}{\text{Carrier power}}\right) = 10\log_{10}\left(\frac{J_1(m)}{J_0(m)}\right)^2 = 10\log_{10}\left(\frac{m}{2}\right)^2 \quad (17)$$

Note that in above derivation, our interest is the level of the spur in frequency synthesizers, which means that the carrier power and frequency are well defined, and the level of the spur is sufficiently lower than the carrier power. Thus, we are able to assume the modulation index is far less than 1, which simplifies the Bessel function. The good thing of the result in Equation (17) is that only with the modulation index, m, we can easily calculate the level of the spur, meanwhile, m inherently contains the information of the peak phase deviation. It means that we can easily relate the deterministic jitter due to the modulation signal with the level of the spur, i.e., the actual level of the spur can be calculated. When a square wave signal has deterministic jitter as a sine wave and random jitter, Figure 17 shows how the signal looks in the time domain and the frequency domain, respectively. As shown in Figure 17, random jitter in the time domain makes "skirt" around the carrier frequency, whereas deterministic spur in the time domain is converted to a pair of the spur in the frequency domain. For example, assume that we have a clock that contains 1% peak-to-peak deterministic jitter. Then, what would be the equivalent spur level in the frequency domain? Based on the Equation (17), the level of spur can be simply calculated. Since the amount of the deterministic jitter that reflected in one period of the clock is $0.01 \cdot 2\pi/2$, we can say that $0.01 \cdot 2\pi/2$ is a modulation factor. Thus, the calculated level of spur will be $20\log(0.01 \cdot 2\pi/2/2) = 20\log(0.005\pi) \approx -36$ dBc. Note that in wireline applications usually, the required level of the spur is not tight compared with the wireless applications, since if the level of the spur is below −40 dBc, the spur's contribution to the jitter is less than 1% [25].

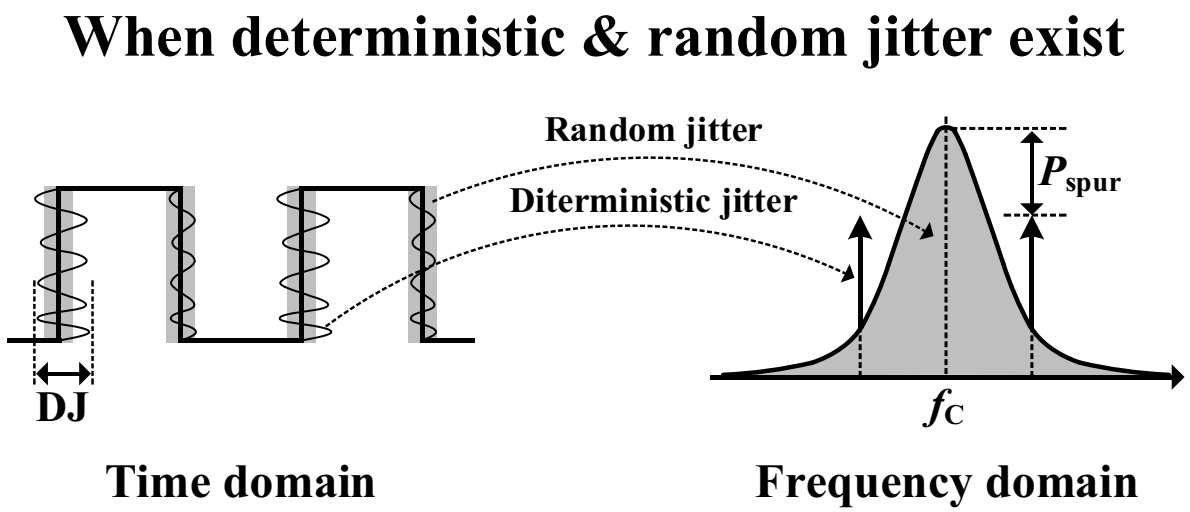


Figure 17. Time and frequency domain when there are deterministic and random jitter

In addition, the Equation (17) also can be applied to calculate the level of spur of the VCO when it has a modulation signal at the input of the VCO. Let's assume that we have a VCO operating at 1 GHz with a K_{VCO} of 100 MHz/V and a modulation sine wave signal operating at 100 MHz with 1 mV peak amplitude (peak-to-peak amplitude is 2 mV). To find out the modulation factor, we need to know the modulating frequency, f_m, and the max frequency deviation, Δf_D. Since we already know f_m as 100 MHz,

the remaining one is to figure out Δf_D due to the modulation signal. Δf_D can be easily calculated by $K_{VCO} \cdot 1$ mV, which is 100 kHz. Then the modulation factor will be 100 kHz/100 MHz, which is 0.001. Finally, the level of spur will be $20\log(0.001/2) = 20\log(0.0005) \approx -66$ dBc. Note that the level of spur has nothing to do with the carrier frequency, whereas K_{VCO} and f_m are the important factors.

Now, let's move on our attention to what would be the level of spur if frequency division happens? Here, one assumption is that the divider doesn't contribute jitter (or nosie). First, after the frequency division, the offset frequency, f_m, doesn't change. The frequency division is a kind of sub-sampling operation, thus, the absolute value of f_m, deterministic jitter, and random jitter will remain, as clearly shown in Figure 18. (total jitter is simplified as Δt in Figure 18) However, the clock period is increased by N times, which decreases the modulation factor after division by N times. Since the modulation factor is reduced by N times, the level of spur and phase noise will be also reduced by $20\log(N)$. In the same manner, when the frequency of the signal is multiplied by N times, the level of spur and phase noise will be also increased by $20\log(N)$.

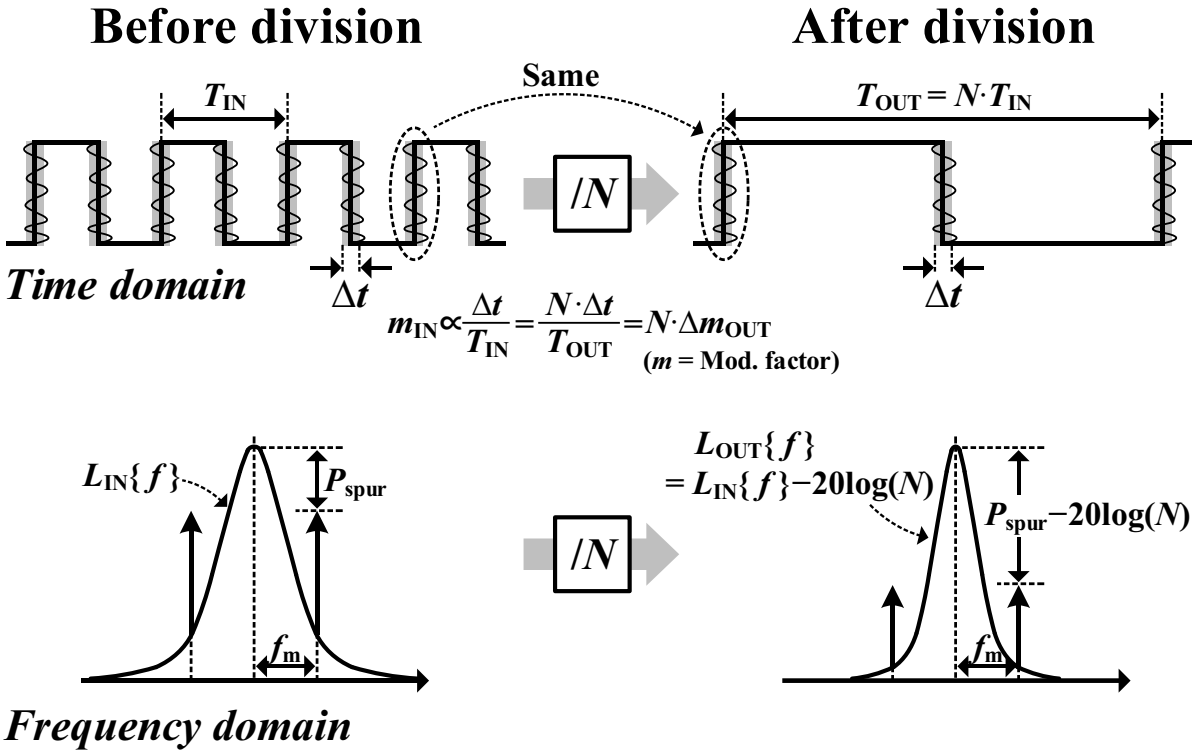


Figure 18. Effect of frequency division on spur and phase noise

In the design of PLL, another key design metric is the reference spur along with phase noise (or jitter). The reference spur means the spur located at the offset frequency of the reference frequency. Three major causes of the reference spur are: 1. mismatch of the PFD and the CP, which generates a static phase offset in the PLL, 2. Non-ideality from the PFD and the CP (e.g. up and down current

mismatches), 3. leakage current in the low pass filter (LPF). If there is static phase offset, the PLL tries to compensate the offset by generating a DC offset voltage at the LPF, which is the control voltage of the VCO in PLL. However, the accumulated DC offset voltage deviates the frequency of the VCO from the target frequency of the PLL, and thus, the PLL generates opposite static phase error to cancel the aforementioned static phase error, generated by the PFD and the CP. Since this behavior occurs in one reference clock period, it will make voltage ripple in the control voltage of the VCO at the reference frequency. In the same principle, the leakage current of LPF also creates a voltage ripple, which occurs the reference spur. In summary, when there is static phase offset, the reference spur occurs and limits the PLL to be used in some applications requiring tight spur performance.

Regions of Operation

When the PLL is designed, the capture (acquisition or pull-in range) and locking range (hold-in range) should be investigated. Let's assume that we have a PLL with a multiplication factor of N and a VCO whose frequency can be changed by the PLL. As shown in Figure 19, if the PLL is initially in steady state, i.e., in the locked condition, the frequency of the PLL, f_{VCO}, will track the input frequency multiplied by N, i.e., $N \cdot f_{REF}$, only when f_{REF} varies within from f_{Min}/N to f_{Max}/N. However, if f_{REF} is not in the range from f_{Min}/N to f_{Max}/N, the PLL will lose the lock status, i.e., the PLL cannot track $N \cdot f_{REF}$ anymore and the output frequency of the PLL will be f_0, which is the free-running frequency of the VCO. It means that the locking range of the PLL is from f_{Min}/N to f_{Max}/N [26]. To establish the locking status again, f_{REF} should be adjusted close enough to f_0. When f_{REF} starts to close to f_0 from the upper side, if the PLL is suddenly locked at the frequency of $(f_0+f_C)/N$, we call it as the maximum frequency of the capture range and vise versa. Thus, the capture range would be from $(f_0+f_C)/N$ to $(f_0-f_C)/N$, i.e., $2f_C/N$. Note that since the locking range of the PLL is wider than the capture range of the PLL, we can find there is a hysteresis in Figure 19 denoted as arrows in red.

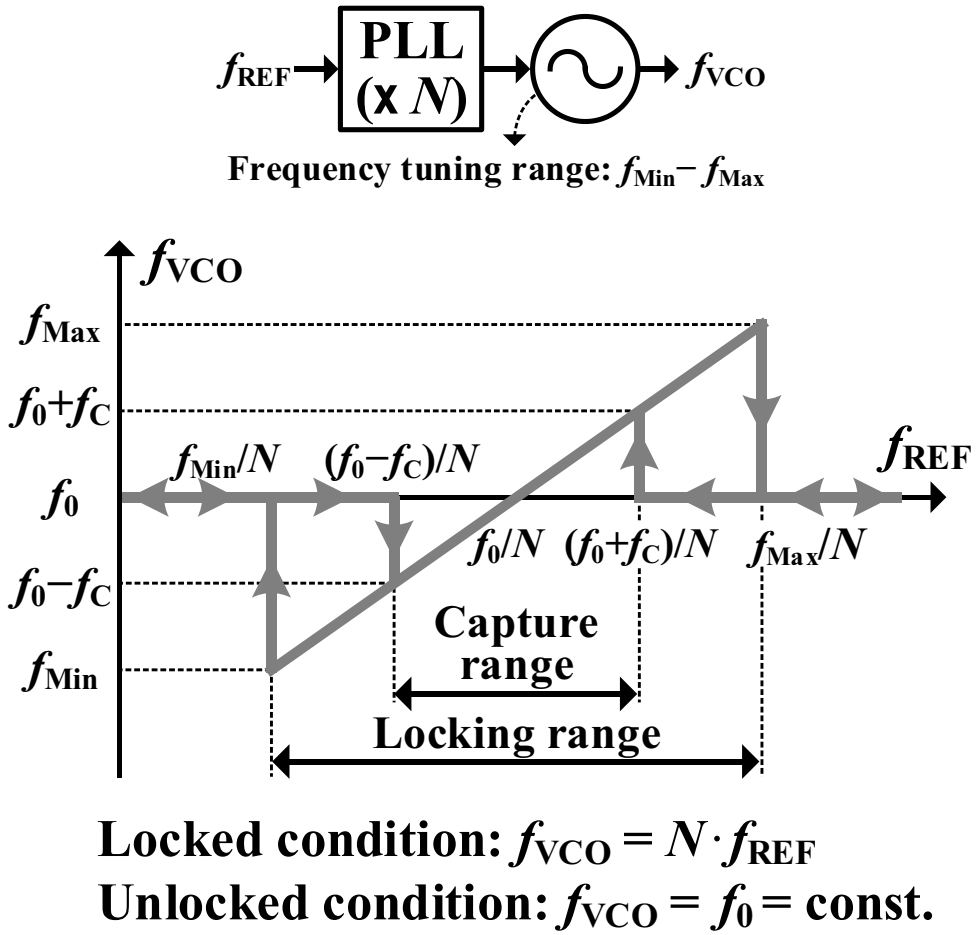


Figure 19. Locking range and capture range of the PLL

2.2 PLL Main Building Blocks

2.2.1 Phase-Frequency Detector and Charge Pump

In the PLL system, the main objective is to correct the frequency drifts in the VCO, which means a block that can detect the frequency drifts of the VCO is required. In charge pump (CP) PLLs, a phase-frequency detector (PFD) roles as the detection block. As shown in Figure 20, the PFD consists of two D-flip flops (DFFs) and a NAND gate. The CP consists of two switches and two current sources. The operation of the PFD is comparing the phase of the reference clock, f_{REF}, and that of the feedback clock, i.e., the divided VCO output, f_{DIV}, and then, providing a correction signal to the CP, i.e., S_{UP} and S_{DN}. The CP converts the correction signals to a corresponding amount in the current. As shown, when S_{UP} is in the high level, SW_{UP} is turned on and the sourcing current, I_{UP}, flows from the supply to the LPF. When S_{DN} is in the high level, SW_{DN} is turned on and the sinking current, I_{DN}, flows from the LPF to the ground. In this way, the current amount flows to the LPF is adjusted.

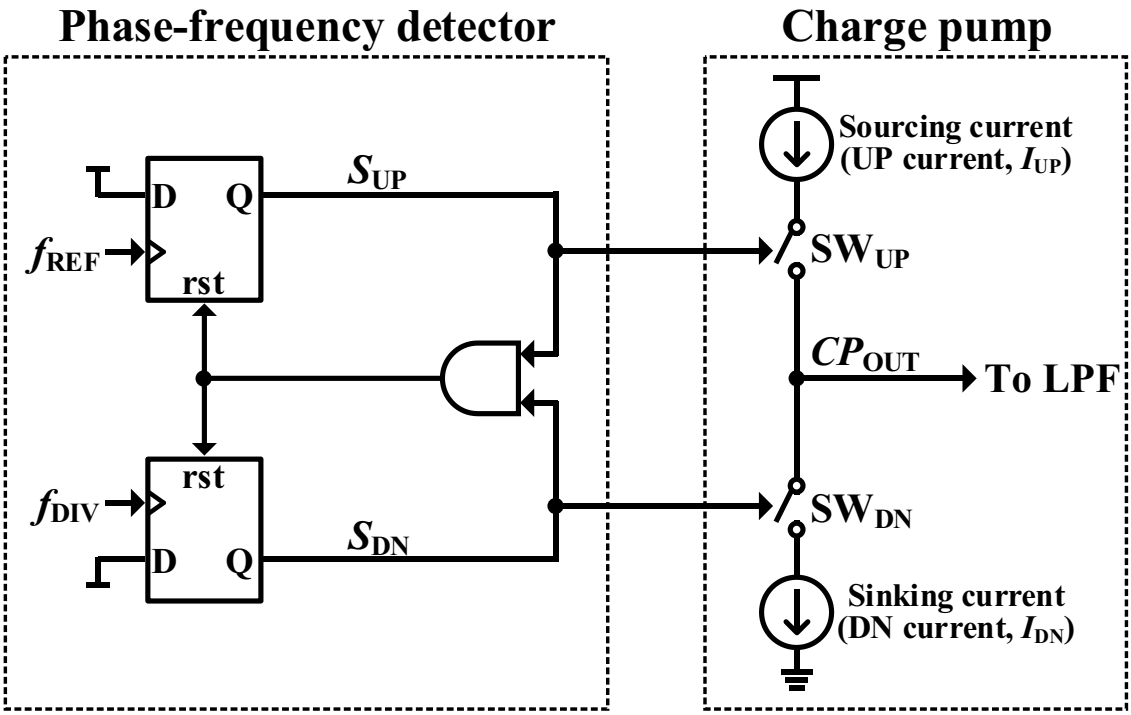


Figure 20. Simplified block diagram of the PFD and the CP

According to the status of the two inputs of the PFD, i.e., f_{REF} and f_{DIV}, the PFD can have three status, as shown in Figure 21. When the PFD is in the high impedance state if the rising edge of f_{REF} goes into the PFD first, i.e., f_{REF} leads f_{DIV}, the signal of S_{UP} turns to the high level and the sourcing current is enabled. In this manner, if the rising edge of f_{DIV} goes into the PFD first, i.e., f_{DIV} leads f_{REF}, the signal of S_{DN} turns to the high level and the sinking current is enabled. When the PFD detects both levels of S_{UP} and S_{DN} are high, both sourcing and sinking currents are disabled by turning off S_{UP} and S_{DN}.

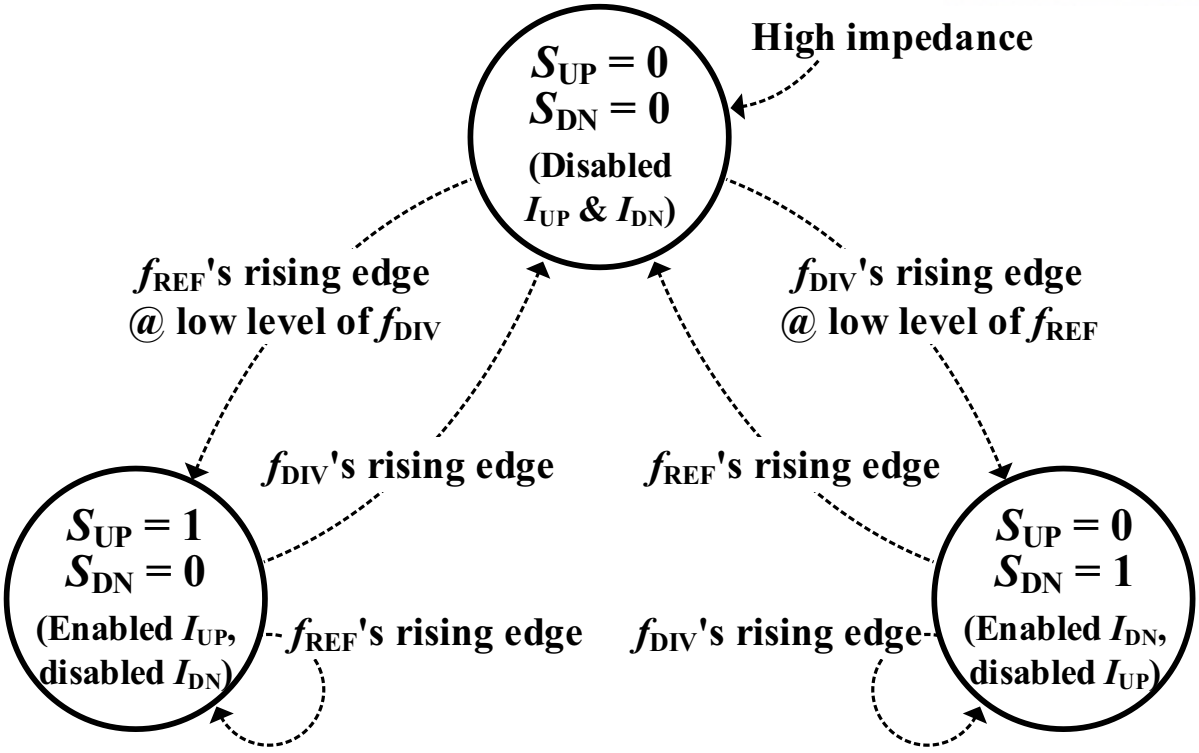


Figure 21. Operation of the PFD; three status

According to the operation of the PFD described above, the averaged output current of the CP can be drawn over the phase error between f_{REF} and f_{DIV}, $\Delta\phi$, as shown in Figure 22, which corresponds to the transfer function response of the PFD and the CP. As shown, the gain of the PFD and the CP, $K_{PFD\text{-}CP}$, can be easily calculated from the slope as follows.

$$\overline{K_{PFD\text{-}CP}} = \frac{I_{CP} - (-I_{CP})}{2\pi - (-2\pi)} = \frac{I_{CP}}{2\pi} \tag{18}$$

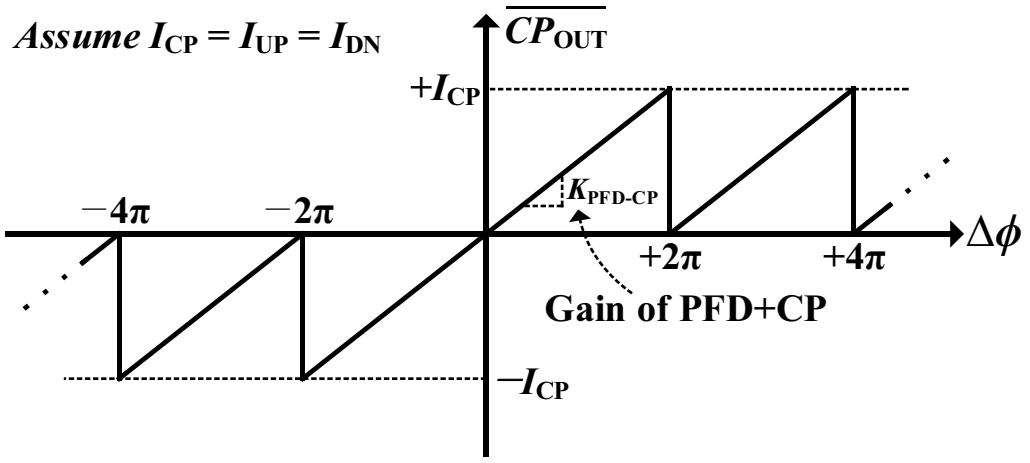


Figure 22. Transfer function of the PFD and CP

Practical Issue of the PFD Design: Dead Zone

When the PFD is implemented in real circuits as shown in Figure 23, there is a practical issue which is called as dead-zone. When the PLL reduces the phase error close to zero, due to finite turn-on time of the switches, SW_{UP} and SW_{DN}, the switches can not swiftly response the small phase errors, which means the switches are not fully turned on. Then, the average output current of the CP is almost zero when the phase error is near zero. As a result, the decreased gain of the PFD and the CP incurs the weak suppression of the VCO phase noise. Moreover, the non-linear transfer function of the PFD and the CP, as shown in Figure 23, would degrade the performance of the PLL in term of overall phase noise and fractional spurs.

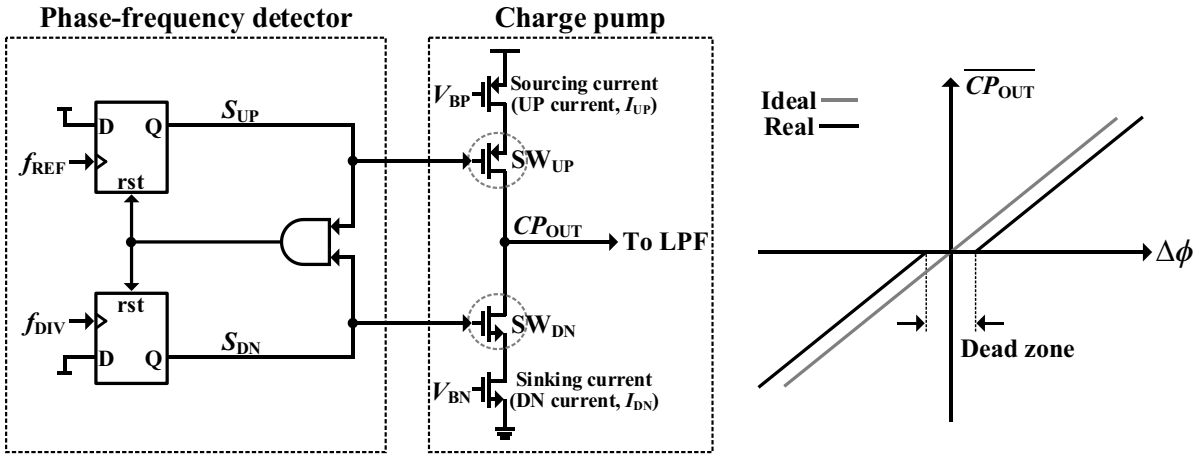


Figure 23. Real implementation of the PFD and the CP

To solve the problems occurred by dead zone, mainly, there are two solutions; First, at the output of the NAND gate, introduce a delay intentionally, which is greater than the finite turn-on time of the switches. In this way, when the phase error is close to zero, the average output current can properly respond to the small phase error. However, it could increase the phase noise of the CP. Second, attach a bleed current at the output of the CP. Due to the bleed current, the real transfer function in Figure 23 will shift to left or right along with x-axis. Therefore, we can avoid the dead zone when the phase error is small.

Practical Issue of the PFD Design: Cycle Slipping

When phase error is smaller than 2π, the PLL tracks the input frequency variation without no special issue. However, if the phase error is larger than 2π, the phenomenon called a cycle slipping happens [27]. Literally, the cycle slipping means the PFD misses the edges of the reference clock or the divided VCO signal. Figure 24 shows how the cycle slipping happens in the time domain. When f_{REF} is much faster than the divided VCO signal, f_{DIV}, the 5th edge of f_{REF} at t_4 is slipped since the 4th edge of f_{DIV} is not in between the 4th and 5th edge of f_{REF}. Thus, a sudden decrease of the duty cycle of the CP_{OUT}, results in the sudden voltage drop across the loop filter (specifically, across the resistor), which causes slow locking time of the PLL. Note that if the bandwidth of the PLL is wide enough, the PLL can correct the frequency of the VCO before the cycle slipping happens. Figure 25 shows the transient response of the cycle slipping in PLL.

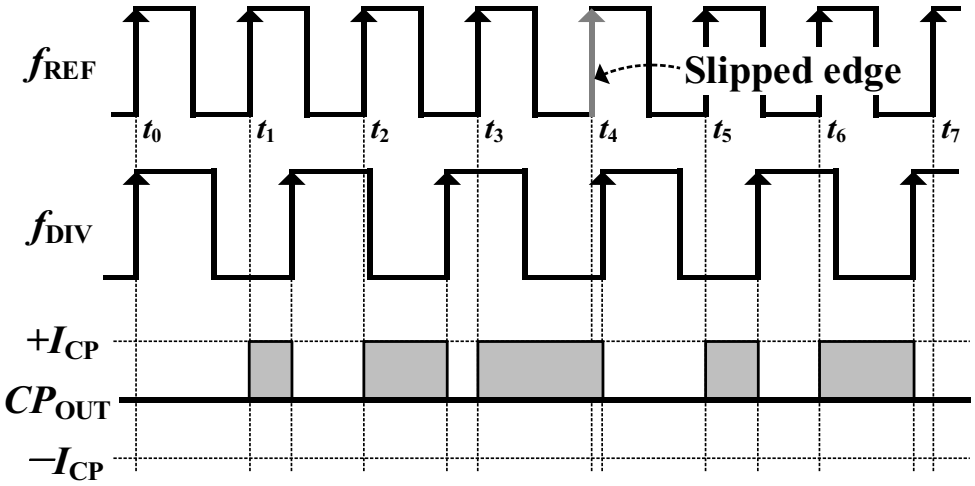


Figure 24. Timing diagram when the reference clock leads the feedback clock

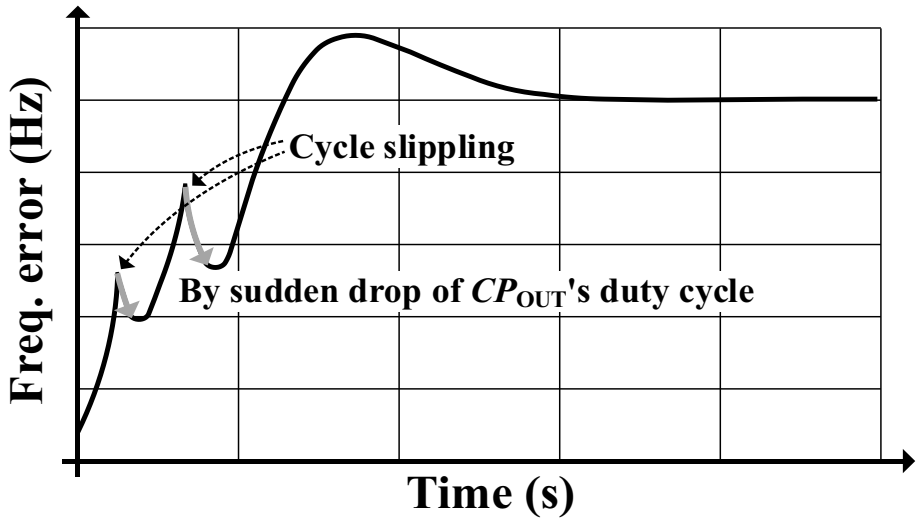


Figure 25. Transient response of the cycle slipping

2.2.2 Loop Filters

The loop filter is a kind of the low pass filter, which is connected to the output of the CP for translating the output current of the CP to the voltage for input of the VCO. However, the role of the loop filter is not just limited to the conversion of current to the voltage. Design of the loop filter determines many aspects of the PLL such as phase noise, spur, settling time (or bandwidth), and the stability. Even though an active type loop filter can be employed, in the design of CP PLLs, the passive type loop filter is mostly used, since the active type could degrade phase noise and increase the cost and the power consumption. Figure 26 shows the design of a typical passive loop filter, which consists of capacitors and a resistor. The role of R_2 is to introduce a zero together with C_2 to the transfer function of the loop filter for securing stability. Without the zero, the CP PLL cannot be stabilized since the PLL has two origin poles; one is from the loop filter and the other is from the VCO. Details about the stability will be introduced in Chapter 3. Also, C_1 is inserted between the output of the CP and the ground to prevent sudden voltage drop or jump across R_2 when the current from the CP sinks or sources the loop filter. Thus, C_1 contributes to the reduction of the voltage ripple at the control voltage, which could appear as the reference spur at the output of the PLL or degrade phase noise performance. For further reduction in phase noise and the ripple, R_3 (or R_4) and C_3 (or C_4) can be inserted in the loop filter for introducing additional poles to the loop filter before the VCO is connected. This is because one additional pole contributes an additional 20dB/dec slope to the transfer function of the loop filter. However, the location of the 3rd and 4th pole should be carefully designed not to degrade the stability (or phase margin). The order of the loop filter is determined by the number of the poles of the loop filter.

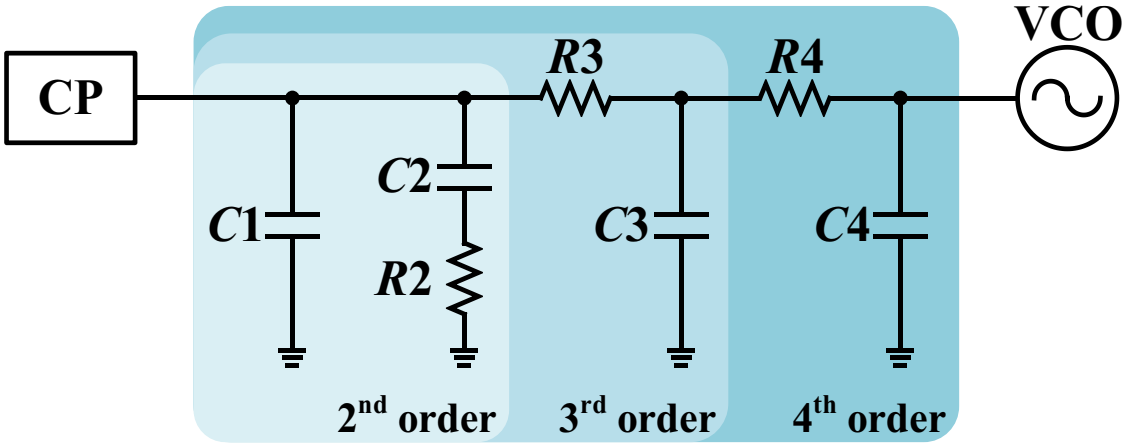


Figure 26. Typical design of the loop filter with passive components

To find out the transfer function of the loop filter containing the information of the location of zeros and poles is important to predict phase noise and spur, and to secure the stability of the PLL. Simply, the transfer function of the loop filter is an impedance since the input is current and the output is voltage. The transfer function of the loop filter, $Z_{LF}(s)$ can be generalized as follows.

$$Z_{\mathrm{LF}}(s) = \frac{1 + s \cdot B_0}{s \cdot (A_3 \cdot s^3 + A_2 \cdot s^2 + A_1 \cdot s^1 + A_0 \cdot s^0)} \tag{19}$$

All coefficients are calculated and the results shown in the below according to the order of the loop filter [27].

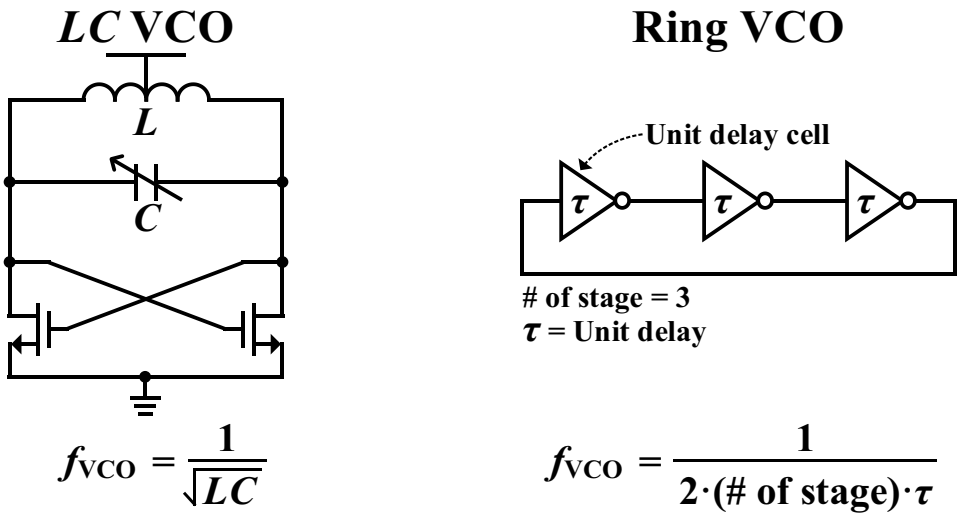
Table 3. The coefficients of the loop filter according to the order

Order	Coefficient	Calculated value
2	B_0	$R2 \cdot C2$
	A_0	$C1+C2$
	A_1	$R2 \cdot C1 \cdot C2$
	A_2	0
	A_3	0
3	B_0	$R2 \cdot C2$
	A_0	$C1+C2+C3$
	A_1	$R2 \cdot C2 \cdot (C1+C3)+R3 \cdot C3 \cdot (C1+C2)$
	A_2	$R2 \cdot R3 \cdot C1 \cdot C2 \cdot C3$
	A_3	0
4	B_0	$R2 \cdot C2$
	A_0	$C1+C2+C3+C4$
	A_1	$R2 \cdot C2 \cdot (C1+C3+C4)+R3 \cdot (C1+C2) \cdot (C3+C4)+ R4 \cdot C4 \cdot (C1+C2+C3)$
	A_2	$C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3+C4)+ R4 \cdot C4 \cdot (R3 \cdot C2 \cdot C3+R3 \cdot C1 \cdot C3+R2 \cdot C1 \cdot C2+R2 \cdot C2 \cdot C3)$
	A_3	$R2 \cdot R3 \cdot R4 \cdot C1 \cdot C2 \cdot C3 \cdot C4$

Note that the coefficient for the zero is independent to the order of the loop filter.

2.2.3 Voltage-Controlled Oscillators (VCOs)

The purpose of the VCO is to generate a frequency, which is controlled by the control voltage provided by the loop filter. In wireline and wireless communication systems, two types of the VCO are widely used; a ring VCO and an *LC* VCO. The simplified structure of the *LC* VCO and the ring VCO are shown in Figure 27(a) and (b), respectively. Basically, the *LC* VCO generates a frequency based on the resonance of the *LC* tank, thus, the output frequency of *LC* VCO is mainly defined by the value of the inductor and the capacitor. In the case of ring VCO, the output frequency is defined by the unit delay of the unit delay, τ, cells and the number of stages. Since one of the factors that determine the output frequency of the ring VCO is the unit delay, the ring VCO is more sensitive to the voltage and temperature (VT) variations. Table 4 shows the characteristics of the two VCOs.



(a) (b)

Figure 27. Simplified structure of: (a) *LC* VCO and (b) ring VCO with the defined frequency

Table 4. Characteristics of the ring and *LC* VCO

	Ring VCO	***LC* VCO**
Phase noise	Moderate or bad	Good
Freq. tuning range	Wide	Moderate or narrow
Multiple phases	Depends on the number of stage	Differential
Size (or area)	Small	Large
Scalability	Good	Not easy
Sensitivity to VT	Vulnerable	Robust

As shown in the above table, even though the ring VCO has many advantages over *LC* VCO such as wide frequency tuning range, multiple phases, scalability, and small chip size, the usage of ring VCO

in modern wireless communication systems is limited due to the moderate or bad phase noise performance. Thus, in this thesis, only the *LC* VCO will be further detailed in Chapter 3, since the *LC* VCOs are extensively used for high-performance frequency synthesizers.

Since the understanding of the characteristics of the VCO is important for the proper design of the PLL, in the following, each characteristic will be explained.

Gain of the VCO

The gain of the VCO is usually denoted as K_{VCO} and the unit is Hz/V. Figure 28 shows graphically the gain of the VCO with an assumption that the gain is constant. However, in the practical design of the VCO, K_{VCO} cannot be a constant value since f_{VCO} will be controlled by the V_{TUNE} connected to a varactor, which is a non-linear device. Thus, the variations of K_{VCO} could degrade the overall performance of PLL in terms of phase noise, stability, and settling time because the open loop gain of the PLL changes.

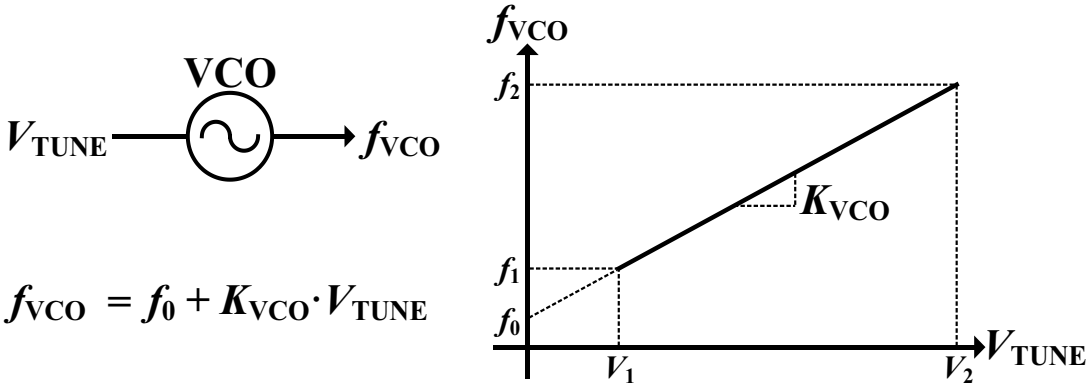


Figure 28. Graphical representation of the gain of the VCO

Frequency Tuning Range (FTR)

Literally, the frequency tuning range (FTR) means the range that the VCO can cover. As mentioned above, an *LC* VCO has narrower FTR than a ring VCO. For example, even though the ring VCO can easily cover octave frequency range, but the *LC* VCO is not. When we denote the minimum and the maximum frequency of the VCO as $f_{VCO,min}$ and $f_{VCO,max}$, the widely used definition of the FTR is

$$\text{FTR}(\%) = \frac{\text{VCO's frequency range}}{\text{VCO's center frequency}} \cdot 100\ (\%) = \frac{\left(f_{VCO,min} - f_{VCO,max}\right)}{\left(f_{VCO,min} + f_{VCO,max}\right)} \cdot 2 \cdot 100\ (\%) \qquad (20)$$

Overtly, having wide FTR is always desired in the design of the VCO. However, wide FTR has a trade-off, which is generally phase noise. This is because if there is a target frequency, for the wide FTR, the inductance should be small for the large variation in the capacitance, which implies that the Q-factor of the LC tank decreases. Therefore, the target FTR should be carefully designed not to sacrifice the phase noise.

Frequency Pushing

If the VCO is ideal, the output frequency of the VCO, f_{VCO}, only depends on the input voltage, i.e., V_{TUNE}. Unfortunately, in practice, f_{VCO} is also sensitive to the supply voltage of the VCO. Thus, as the supply voltage changes, f_{VCO} also changes. This phenomenon is called as the frequency pushing. Frequency pushing is expressed as Hz/V and it could be a positive or negative value. If the supply voltage is noisy, the VCO would have more frequency drift, which leads to the degraded phase noise. In addition, if the supply voltage has a glitch, the PLL could lose the locked status and starts again the settling process. To minimize the frequency pushing, first, the supply voltage should be well regulated. Second, an *LC* tank must be designed to have a high Q-factor to be robust to the environmental variations.

Frequency Pulling

When f_{VCO} varies due to the attached load at the output of the VCO, this phenomenon is called as the frequency pulling. Therefore, the frequency pulling can be minimized by isolating the VCO from the load. One of the popular methods is to insert a buffer or an amplifier since those have large reverse isolation.

2.2.4 Frequency Dividers

Integer-*N* PLL with a Prescaler

Frequency synthesizers can be implemented as an integer-*N* or a fractional-*N* PLL according to requirements of the PLL. Commonly, both types employ a prescaler in the feedback path. Prescaler means that an input frequency to the divider is scaled before it applied to the counter. The type of the prescaler can be changed according to the number of modulus such as a single, a dual, and a quadruple modulus prescalers. Among them, the widely used prescaler is the dual-modulus prescaler.

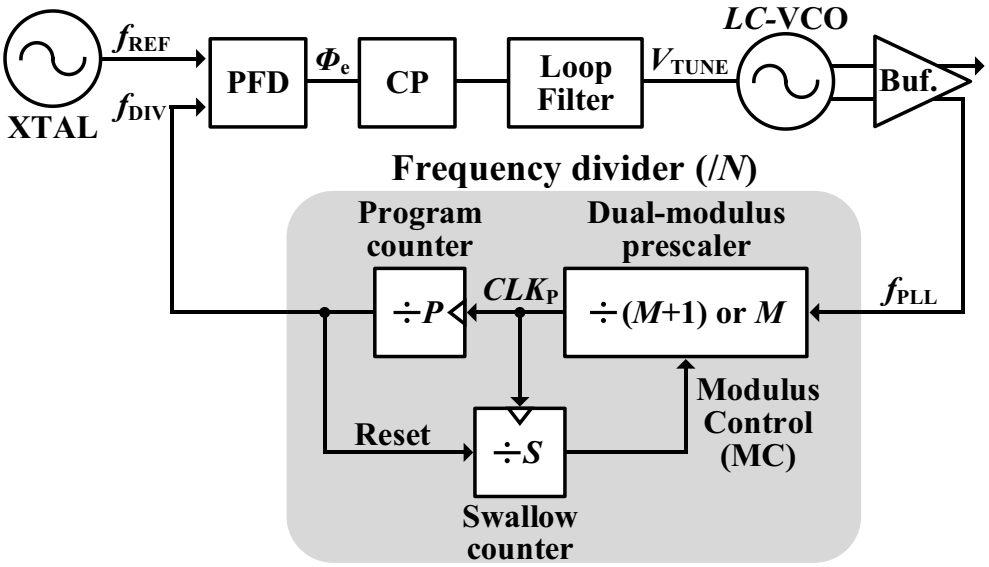


Figure 29. Integer-*N* PLL with the dual-modulus scaler for the frequency divider

Figure 29 shows when the dual-modulus prescaler is employed in the frequency divider for the integer-*N* PLL. The operation of the frequency divider is shown in the timing diagram in Figure 30 when *M* is two (dividede-by-2/3 prescaler), *P* is six, and *S* is four.

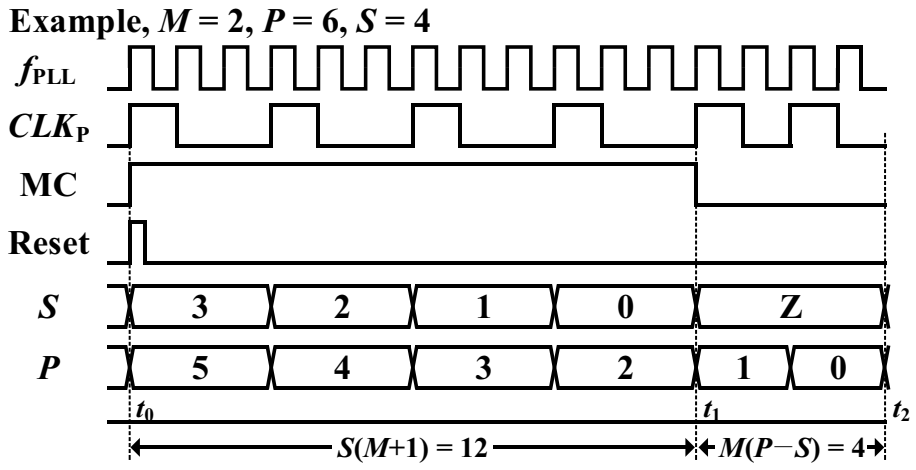


Figure 30. Timing diagram of the frequency divider

The operation of the divider is as follow. First, the division number of the prescaler is set as three by the prescaler (M=3), and the program and the swallow counter start to count edges of CLK_P until the swallow counter fully filled up. When the swallow counter is finished, i.e., at t_1, the MC signal is changed from high to low to set the value of M to two from three. The counted edges of f_{PLL} up to this point, i.e., during from t_0 to t_1, is $S\cdot(M+1)$, which is 12. After that, only the program counter still counts the edges of f_{PLL} until the program counter fully filled up. When the program counter is also finished, the reset signal is activated to reset the whole counters. The counted edges of f_{PLL} during from t_1 to t_2 is $M\cdot(P-S)$, thus the total counted number is $S\cdot(M+1) + M\cdot(P-S)$, i.e., $M\cdot P+S$ which is 16.

When the frequency divider is designed based on the prescaler and counters, one thing to note is that S must not be greater than P. If the condition is not satisfied, the reset signal will be activated before the program counter finishes its own operation. Thus, the frequency divider cannot provide the proper value of division number, N, and it will behave such a single modulus divider.

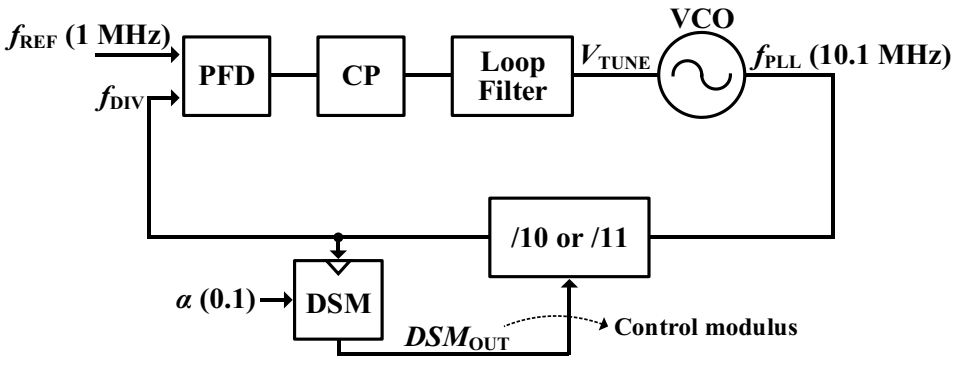
In addition, the frequency divider with a dual-modulus prescaler has a minimum division number if we want continuous division ratio, which is limited by the value of M. Since M is a quotient, maximum value of P is $M-1$. In this case, we can define the minimum continuous division number as $M\cdot(M-1)$. Even though we can have smaller division ratio than $M\cdot(M-1)$, it cannot guarantee continuity of the division ratio. According to the above explanation, the below summarizes minimum continuous division ratio according to the value of M [27].

Table 5. Summary of the continuous minimum division number for dual-modulus prescaler

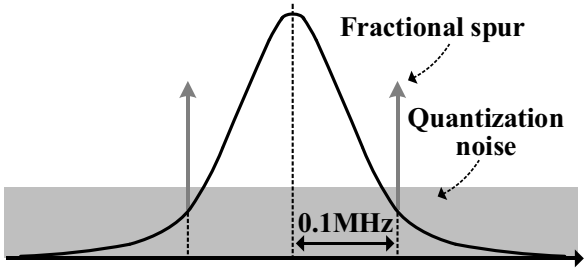
Prescaler division value (M)	**Minimum division number for continuity**
2 (2/3 prescaler)	2
4 (4/5 prescaler)	12
8 (8/9 prescaler)	56
16 (16/17 prescaler)	240
32 (32/33 prescaler)	992
64 (64/65 prescaler)	4032
$2^x\cdot(2^x/(2^x+1))$ prescaler) (x is integer)	$2^x\cdot(2^x-1)$

Fractional-*N* PLL with a Delta-Sigma Modulator (DSM)

As explained in Chapter 2.1.1, if the division number, *N*, is restricted to an integer value, it means that the channel spacing is also restricted to the reference frequency of the PLL. This implies that the reference frequency of the PLL should be reduced, which occurs many trade-offs such as phase noise and settling time. To isolate the dependency of the channel spacing to the reference frequency, the fraction-*N* PLL is now considered, which has a fractional division number rather than an integer. In general CP PLLs, the way to achieve the fractional division ratio is to toggle integer division numbers at every reference period by using the DSM. Figure 31(a) shows a simple fractional-*N* PLL to explain how to achieve the fractional division number. In this example, the reference and the output frequency are 1 MHz and 10.1 MHz, respectively, thus the PLL requires the division number of 10.1. The basic principle is to make the average of the toggled integer to be 10.1, i.e., of the ten cycles of the reference clock, the f_{PLL} is divided by 11 once, and divided by 10 for the remaining nine cycles. In this manner, the average division number can be 10.1 (11/10 + (10·9)/10 = 10.1) However, if the pattern of the toggled integer division number is the same and repetitive, i.e., (10, 10, 10, 10, 10, 10, 10, 10, 10, 11), (10, ···, 11), the pattern would generate fractional spurs at the offset frequency of 0.1 MHz and its harmonics, as shown in Figure 31(b). In addition, even though the average value of the division number is accurate, the instantaneous phase error at the input of the PFD due to the toggling generates quantization error (or noise) at the sideband. In the following, minimization of the fractional spurs and the quantization noise (Q-noise) is detailed.



(a)



(b)

Figure 31. (a) Basic principle for the fractional division ratio. (b) side effects of fractional-*N* PLL

In the fractional-*N* PLL, not to degrade the phase noise and the fractional spurs, the DSM must satisfy two requirements; 1. The sequence of the modulus control denoted as DSM_{OUT} in Figure 31(a), should be randomized. 2. Quantization noise should be also minimized not to degrade phase noise. Both conditions can be met by the proper design of the DSM.

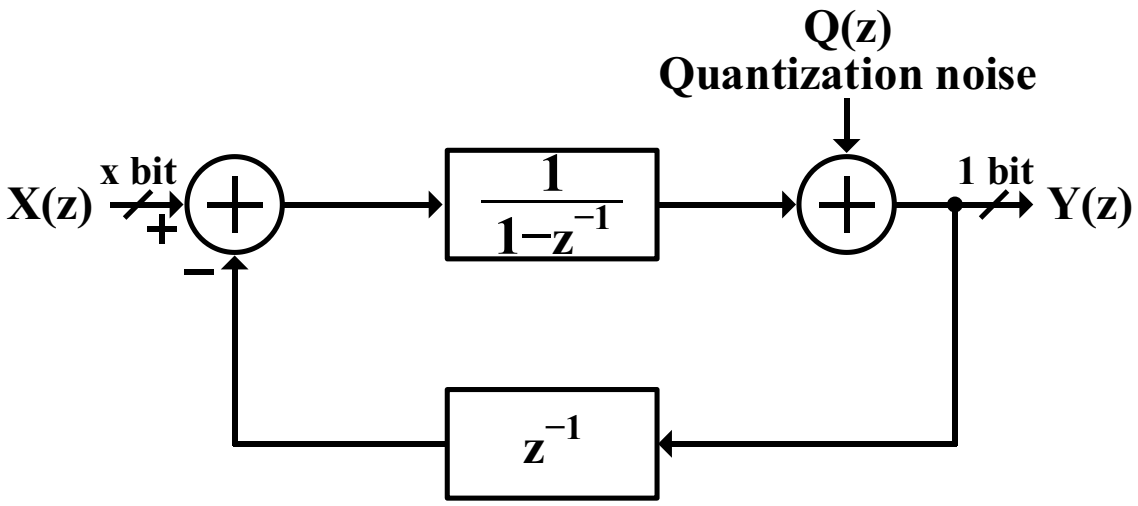


Figure 32. z-domain representation of the first order DSM

Figure 32 shows the z-domain representation of the first order DSM. X(z) and Y(z) represents input and output of the DSM and both are digital signal. The number of bits of X(z) is determined by the resolution of the DSM and Y(z) is a one-bit signal since the above DSM is first order. If X(z) is x bit, the resolution will be $1/2^x$. Since in the PLL the DSM operates at the divided VCO frequency, f_{DIV}, z^{-1} corresponds to a delay of T_{DIV}, the period of the f_{DIV}. It means that in steady state, the DSM will operate at the reference frequency. The transfer function of the first order DSM is expressed as

$$Y(z) = X(z) + Q(z)\cdot(1 - z^{-1}) \tag{21}$$

As shown in Equation (21), the first term is the input and the second term is the high-pass-shaped quantization noise. The term, $(1-z^{-1})$, qualitatively means a high pass filter since the current value is subtracted by the previous one. In a quantitative way, the shape of $(1-z^{-1})$ can be expressed as [28],

$$\frac{Y}{Q}(z) = 1 - z^{-1} \tag{22}$$

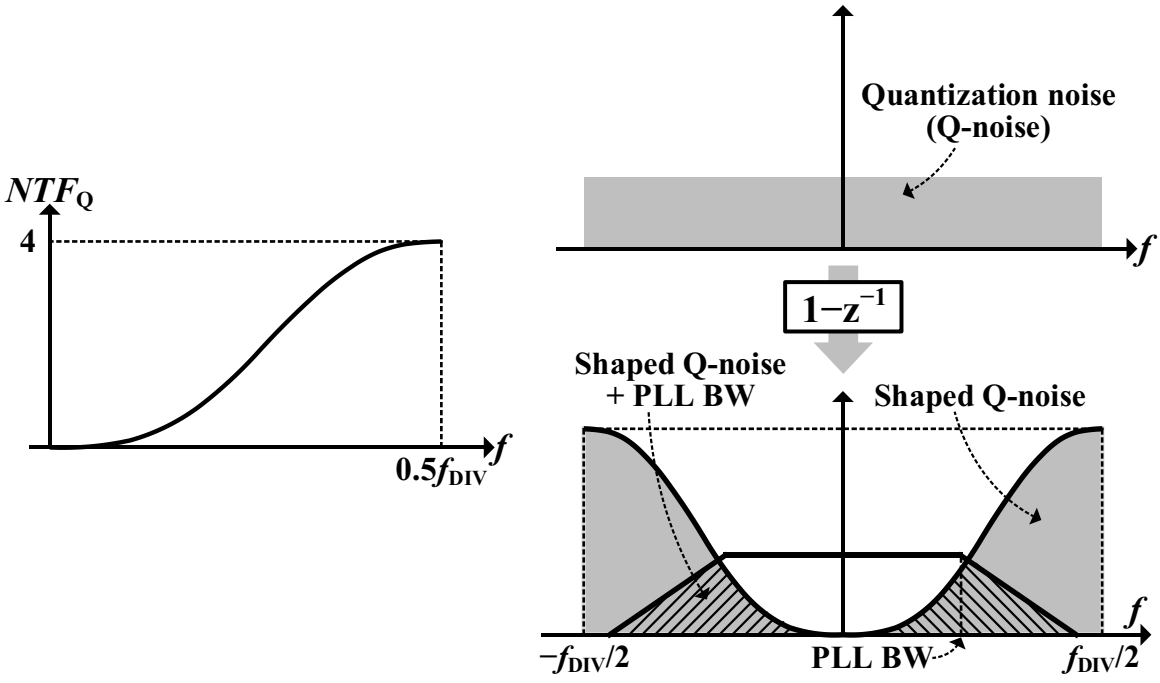
$$= e^{-j\pi f T_{DIV}}\left(e^{j\pi f T_{DIV}} - e^{-j\pi f T_{DIV}}\right) \tag{23}$$

$$= 2je^{-j\pi f T_{DIV}}\sin(\pi f T_{DIV}) \tag{24}$$

By taking the square both sides of Equation (24), the noise transfer function (NTF) of the quantization noise, NTF_Q, can be found as follows [28].

$$NTF_Q(f) = |2\sin(\pi f T_{DIV})|^2 \tag{25}$$

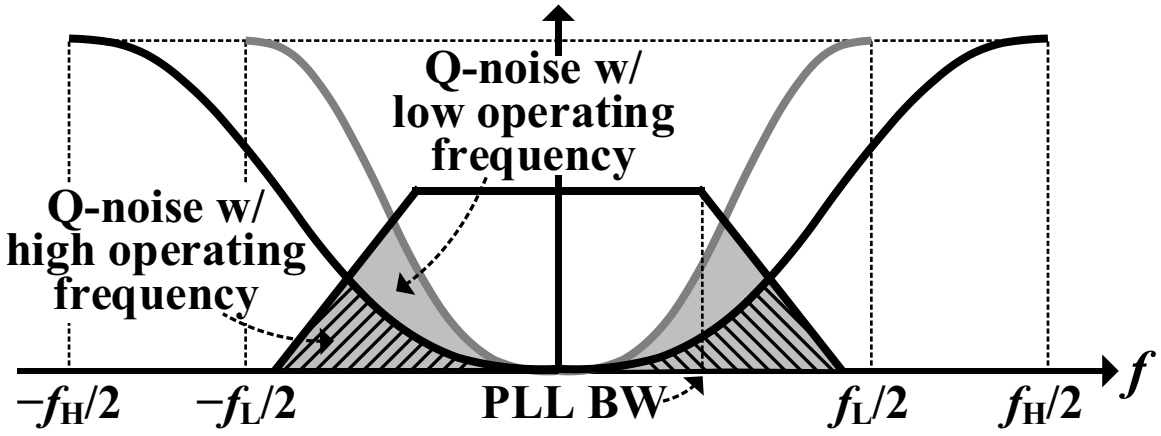
$$= 2|1 - \cos(\pi f T_{DIV})| \tag{26}$$



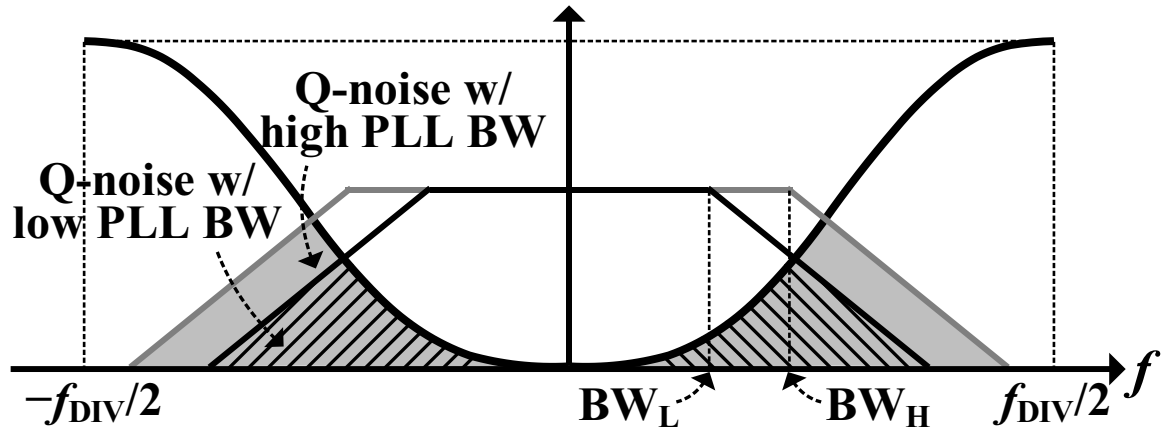
(a) (b)

Figure 33. (a) NTF of the first order DSM (b) noise shaping of Q-noise within the PLL

According to the Equation (26), the NTF of the first order DSM is drawn in Figure 33(a). As clearly shown, the NTF of the quantization noise is a high pass filter since the NTF contains one pole, which is an integrator. The NTF is maximum when the offset frequency is the half of the input frequency of the DSM, i.e., the divided VCO output frequency in the PLL. When Q-noise is considered within the PLL, as shown in Figure 33(b), first, the Q-noise is shaped by the first order high pass filter. Then, since the shaped Q-noise is again suppressed by the PLL bandwidth, the effective Q-noise at the output of the PLL will be the shaded area in red.



(a)



(b)

Figure 34. Two approaches to suppress DSM noise; (a) increase the operation frequency of the DSM (b) decrease the bandwidth of the PLL

When the same DSM is used, the most straightforward way to minimize the Q-noise within the bandwidth of the PLL is as follows. First, as shown in Figure 34(a), increase the operating frequency of the DSM from f_L to f_H to send noise energy to much higher frequencies. Second, as shown in Figure 34(b), decrease the bandwidth of the PLL from BW_H to BW_L to further filter out the Q-noise of the DSM by the bandwidth of the PLL.

The practical implementation of the first order DSM is shown in Figure 35. It consists of an adder and a DFF. The accumulated output will be the quantization error with a minus sign and the carry signal will be used for the modulus control signal, i.e., the average value of the Y(z) will be the same of X(z).

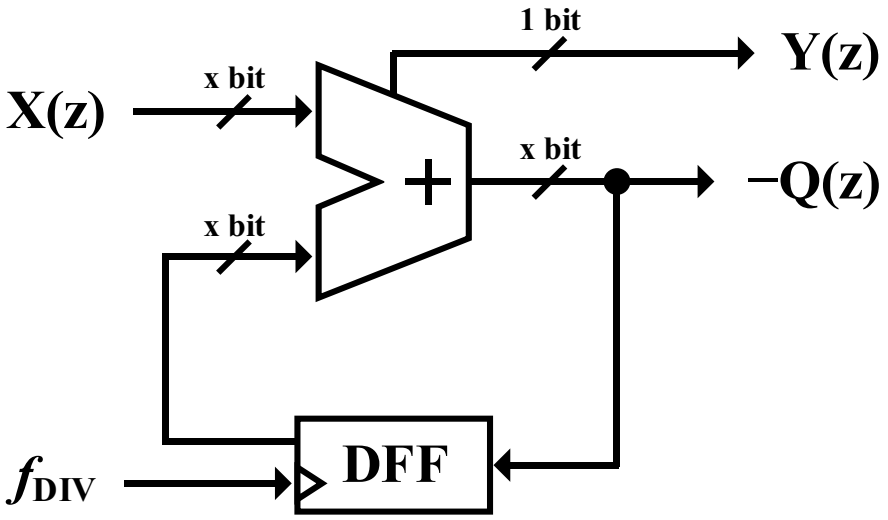


Figure 35. Real implementation of the first order DSM

For a more deep understanding of the operation of the DSM in Figure 35, the input and the output values of the DSM are summarized below Table 6 when X(z) is set as 0.25.

Table 6. Summarized input and output values when X(z) is 0.25

Time	X(z)	Accumulated value	Q(z)	Y(z)
0	0.25	0.25	−0.25	0
T_{DIV}	0.25	0.50	−0.50	0
$2T_{DIV}$	0.25	0.75	−0.75	0
$3T_{DIV}$	0.25	1	0	1
$4T_{DIV}$	0.25	0.25	−0.25	0
$5T_{DIV}$	0.25	0.50	−0.50	0
$6T_{DIV}$	0.25	0.75	−0.75	0
$7T_{DIV}$	0.25	1	0	1

As shown in the above table, the average number of Y(z) is 0.25, which we want to achieve using the DSM. However, the first order DSM is shown in Figure 35 still has two problems.

First, the sequence of Y(z) in Table 6 shows a certain pattern, i.e., (0, 0, 0, 1), (0, 0, 0, 1), …, which will be appeared as a fractional spur at multiple of a quarter of the input frequency of the DSM. Thus,

a technique called “dithering” can be used to randomize the pattern. One of the popular ways to introduce dithering is to randomize the least significant bit (LSB) of the DSM input. If the LSB is randomly toggled between 0 and 1 with the average of zero, the output pattern or periodicity of the DSM is broken, and thus, the level of the fractional spur can be suppressed. For the generation of a random sequence of the LSB, Pseudorandom binary sequence (PRBS) is widely used [28]. However, the PRBS still has periodicity, the fractional spur cannot be completely removed.

Second, the first order DSM may not be sufficient to suppress the Q-noise. To further shape the Q-noise, higher order DSMs could be considered. For the n^{th} order DSMs, the NTF will be

$$NTF_Q(f) = |2\sin(\pi f T_{DIV})|^{2n} \tag{27}$$

$$= 2^n|1-\cos(\pi f T_{DIV})|^n \tag{28}$$

Figure 36 clearly shows the noise shaping of the second-order DSM. Compared with the first order DSM, the second order DSM can send more energy of the Q-noise to the high frequencies. Thus, we can get better noise shaping by increasing the order of the DSM. However, the order of DSM cannot be raised unconditionally, since the DSM has a feedback loop and the order of DSM corresponds to the number of poles. Therefore, high order DSMs should be carefully designed not to degrade the stability of the DSM itself [29].

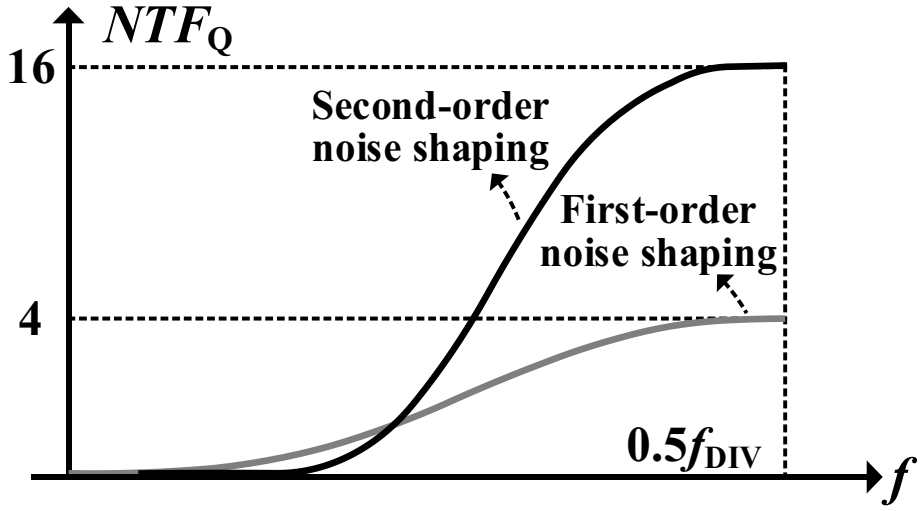


Figure 36. Noise shaping comparison between the first-order and the second-order DSM

In addition, according to the order of the DSM, the number of DSM output also increases. Generally, for the n^{th} order DSM, the range of the output signal will be from -2^{n-1} to $(2^{n-1}-1)$. For example, for the second order DSM, the output signal will be toggled between −2, −1, 0, and 1.

2.3 PLL Analysis

To properly design the PLL with given requirements, such as phase noise, settling time (or bandwidth), spur, and etc, it is important to understand the behavior of each block within the PLL and to understand the behavior of the entire PLL. In this subChapter, for enhancing the understanding of the PLL system, noise transfer functions of each building block of the PLL will be introduced. After that, based on the NTFs derived, the phase noise of the PLL will be investigated. Then, we move to the stability analysis of the PLL.

2.3.1 PLL Modeling with Transfer Functions

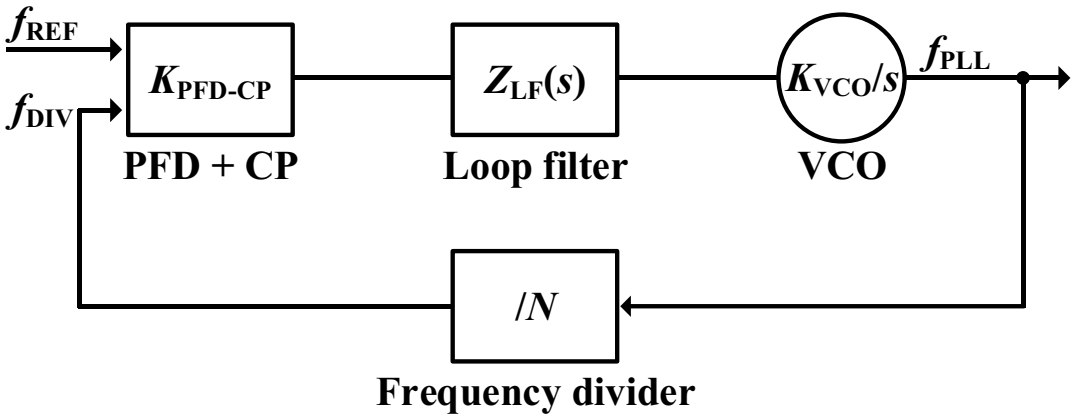


Figure 37. Basic structure of the PLL with transfer functions of each block

Figure 37 shows the PLL structure with each building blocks, whose gain or transfer function is denoted inside. In the above figure, K_{PFD-CP}, $Z_{LF}(s)$, K_{VCO}/s, and N are gain of the PFD and the CP, transfer function of the loop filter, gain of the VCO, and division number, respectively. Even though the PFD and CP work in the discrete time domain, the PLL can be linearly modeled in s-domain since the linear approximation has no discrepancy if the bandwidth of the PLL is assumed considerably lower than the reference frequency of the PLL, i.e., 10 times smaller than f_{REF} [22]. The feedforward and feedback gain of the PLL are denoted as $G(s)$ and F, respectively, and they are expressed as

$$G(s) = K_{PFD-CP} \cdot Z_{LF}(s) \cdot \frac{K_{VCO}}{s} \tag{29}$$

$$F = \frac{1}{N} \tag{30}$$

Based on the Equation (29) and (30), the open-loop gain and the closed-loop transfer function are derived as follows, which are denoted as $OL(s)$ and $CL(s)$, respectively.

$$OL(s) = G(s) \cdot F \tag{31}$$

$$= K_{\text{PFD-CP}} \cdot Z_{\text{LF}}(s) \cdot \frac{K_{\text{VCO}}}{s} \cdot \frac{1}{N} \tag{32}$$

$$CL(s) = \frac{G(s)}{1+G(s) \cdot F} \tag{33}$$

$$= N \cdot \frac{OL(s)}{1+OL(s)} \tag{34}$$

Since the closed-loop transfer function is defined in the phase domain between the input and the output of the PLL, it represents changes in the output of the PLL when the input of the PLL changes. In other words, $CL(s)$ represents the transfer function of the reference clock of the PLL. For the other building blocks of the PLL, transfer functions can be derived as summarized in below Table 7.

Table 7. Transfer function of the building blocks in the PLL

Building block	(Noise) transfer function
Input reference clock	$N \cdot \frac{OL(s)}{1+OL(s)}$
Frequency divider	$N \cdot \frac{OL(s)}{1+OL(s)}$
PFD and CP	$\frac{1}{K_{\text{PFD-CP}}} \cdot N \cdot \frac{OL(s)}{1+OL(s)}$
VCO	$\frac{1}{1+OL(s)}$
Loop filter	$\frac{K_{\text{VCO}}}{s} \cdot \frac{1}{1+OL(s)}$

In Table 7, note that the input reference clock, the frequency divider, and the PFD with the CP have the same factor in each transfer function, which is

$$\frac{OL(s)}{1+OL(s)} \tag{35}$$

In the above equation, the magnitude of $OL(s)$ monotonous decreases as the s increases, i.e., an increase of offset frequencies. Thus, when the offset frequency is low, i.e., within the bandwidth of the PLL, the $OL(s)$ is very large and vise versa. Therefore, the Equation (35) can be approximated into two regions; inside of the PLL bandwidth and outside of the PLL bandwidth, as shown below.

$$\frac{OL(s)}{1+OL(s)} \approx \begin{cases} 1 & \text{for } f \ll \text{PLL BW} \\ OL(s) & \text{for } f \gg \text{PLL BW} \end{cases} \tag{36}$$

In addition, the VCO and the loop filter have a same factor in each transfer function, which is

$$\frac{1}{1+OL(s)} \tag{37}$$

In the same manner, Equation (37) can be also approximated as follows.

$$\frac{1}{1+OL(s)} \approx \begin{cases} \dfrac{1}{OL(s)} & \text{for } f \ll \text{PLL BW} \\ 1 & \text{for } f \gg \text{PLL BW} \end{cases} \tag{38}$$

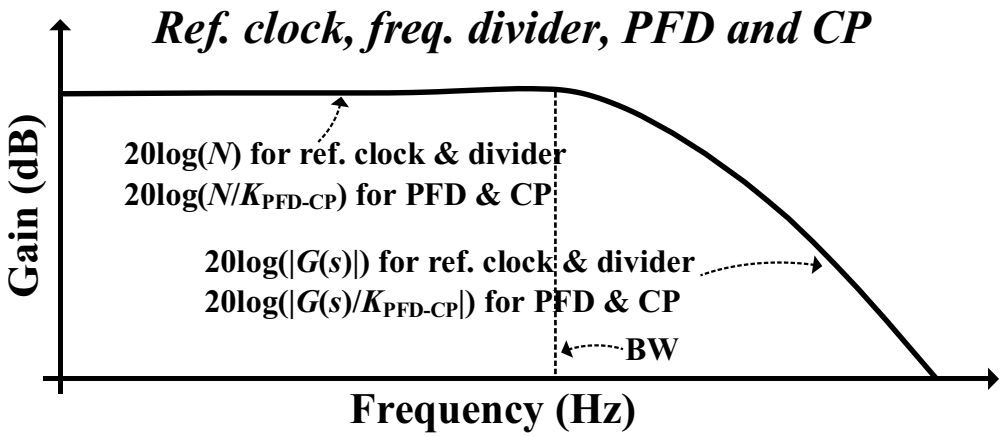
Based on the Equation (36) and (38), the transfer function of each building block can be grouped into two frequency ranges and summarized in Table 8 by considering other terms or coefficients.

Table 8. Summarized transfer functions into two ranges

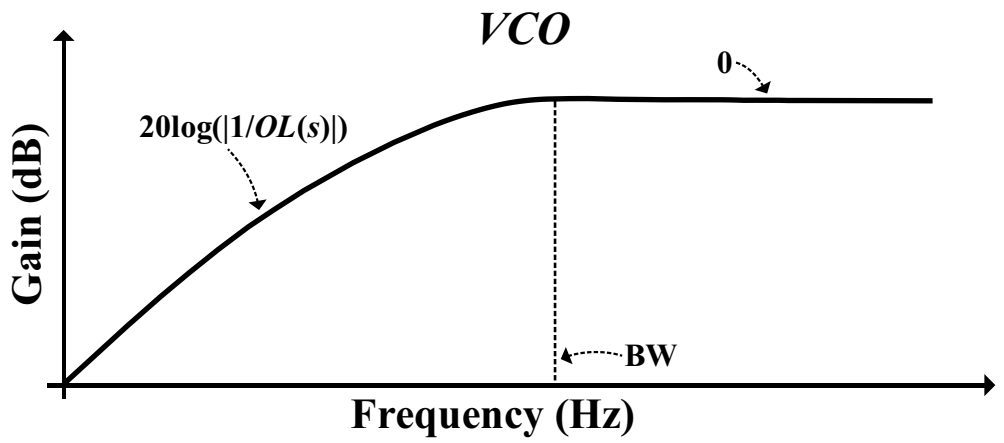
Building block	**(Noise) transfer function**	
	$f \ll$ **PLL BW**	$f \gg$ **PLL BW**
Input reference clock	N	$N \cdot OL(s) = G(s)$
Frequency divider	N	$N \cdot OL(s) = G(s)$
PFD and CP	$\dfrac{N}{K_{\text{PFD-CP}}}$	$\dfrac{N \cdot OL(s)}{K_{\text{PFD-CP}}} = \dfrac{G(s)}{K_{\text{PFD-CP}}}$
VCO	$\dfrac{1}{OL(s)}$	1
Loop filter	$\dfrac{K_{\text{VCO}}}{s} \cdot \dfrac{1}{OL(s)}$	$\dfrac{K_{\text{VCO}}}{s}$

Based on the summarized transfer functions in Table 8, Figure 38 shows the same thing in the frequency domain for the intuitive understanding of the transfer functions of each building blocks. As shown in Figure 38(a), the transfer functions for the reference clock, the frequency divider, and the PFD and CP show the shape of the low pass filter. Figure 38(b) also clearly shows the transfer functions for the VCO is a high pass filter. For the loop filter, Figure 38(b) indicates that the transfer function is similar to the band pass filter. This is because, at the origin, the term K_{VCO}/s provides one pole and the $1/OL(s)$ term

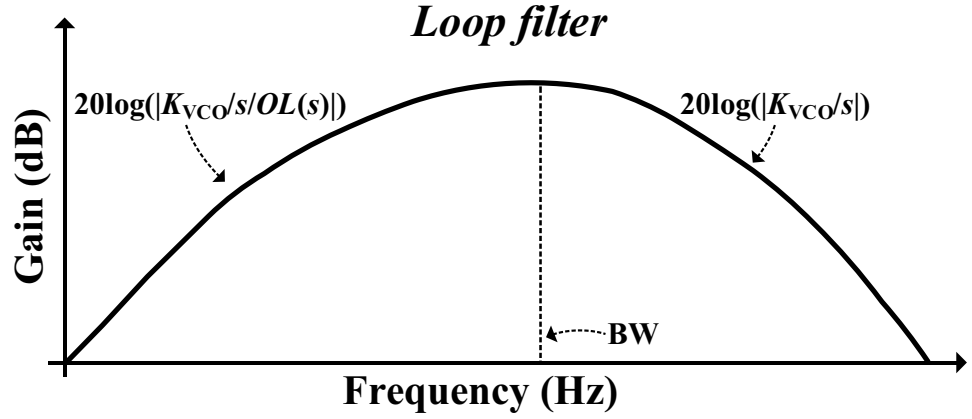
provides two zeros. Thus, at the very low frequencies, the slope is approximately +20dB/dec with a plus sign. Beyond the bandwidth of the PLL, the transfer function only has K_{VCO}/s, which means one pole, the slope would be −20dB/dec. Thus, the shape of the transfer function seems like a band pass filter.



(a)



(b)



(c)

Figure 38. Transfer functions for (a) the reference clock, the frequency divider, and the PFD and the CP (b) the VCO (c) the loop filter

Transfer Function with MATLAB

In order to clearly present the transfer functions, MATLAB was employed to replot Figure 38 neatly, as shown in Figure 39.

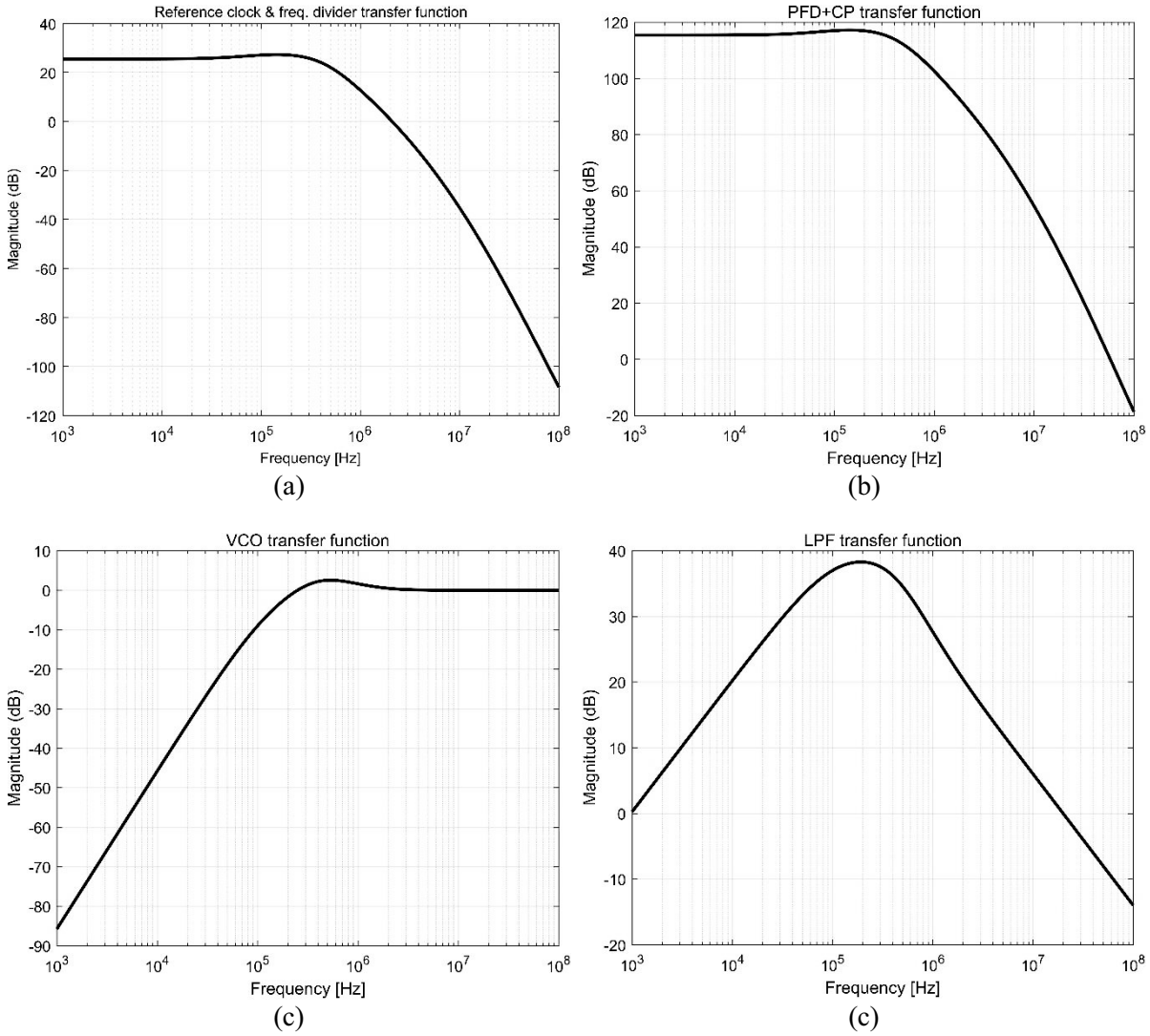


Figure 39. Plotted transfer functions using MATLAB; (a) the reference clock and the frequency divider; (b) the PFD and the CP; (c) the VCO; (d) the loop filter

The parameters for this MATLAB simulation are shown in Table 9. The graphs from the MATLAB clearly show the transfer functions. Note that the PFD and the CP transfer function more amplifies the noise than the reference clock within the PLL bandwidth. It implies that by increasing $K_{PFD\text{-}CP}$, the noise of the PFD and the CP can be suppressed at the expense of the power consumption.

Table 9. Parameters for the MATLAB

f_{REF}	f_{PLL}	I_{CP}	K_{VCO} (rad/V/s)	$K_{PFD\text{-}CP}$
200 MHz	3750 MHz	200 μA	2π·20 MHz	$I_{CP}/2\pi$

2.3.2 Phase Noise Analysis

Since phase noise is the most important specification, it must be well estimated and designed. With the output-referred noise of each building block and the transfer function derived in the previous section, phase noise of the fractional-*N* CP PLL can be investigated.

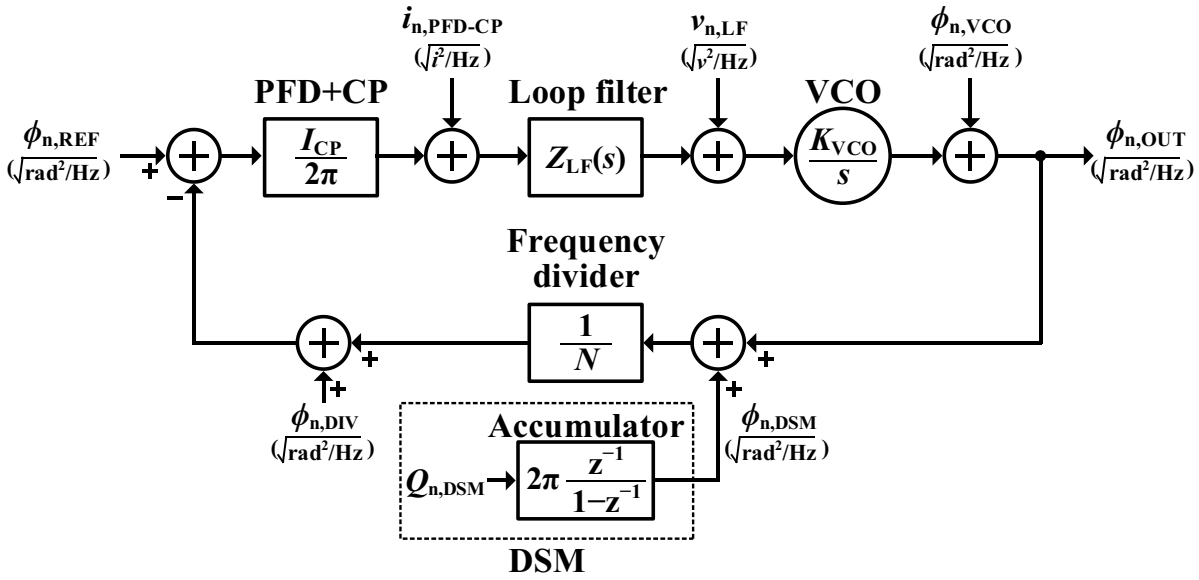


Figure 40. Linearized noise modeling of the fractional-*N* PLL

Figure 40 shows the linearized phase noise modeling of the fractional-*N* PLL with the DSM, i.e., delta-sigma PLL [30]. In the above figure the noise sources are denoted in red; $\phi_{n,REF}$, $i_{n,PFD-CP}$, $v_{n,LF}$, $\phi_{n,VCO}$, $\phi_{n,DSM}$, $\phi_{n,DIV}$, and $\phi_{n,OUT}$ are the reference noise, the current noise from the PFD and the CP, the voltage noise from the loop filter, the VCO phase noise, the quantization noise from the DSM in the phase domain, the frequency divider phase noise, and the output phase noise of the PLL, respectively. Since each noise source is reflected differently to output phase noise depending on its own noise transfer function (NTF), derived in the previous session, we will examine each noise source's contribution to the output phase noise one by one in the following with the help of the MATLAB. For the MATLAB simulations, the parameters of the PLL are set as shown in Table 9.

Reference Noise ($\phi_{n,REF}$)

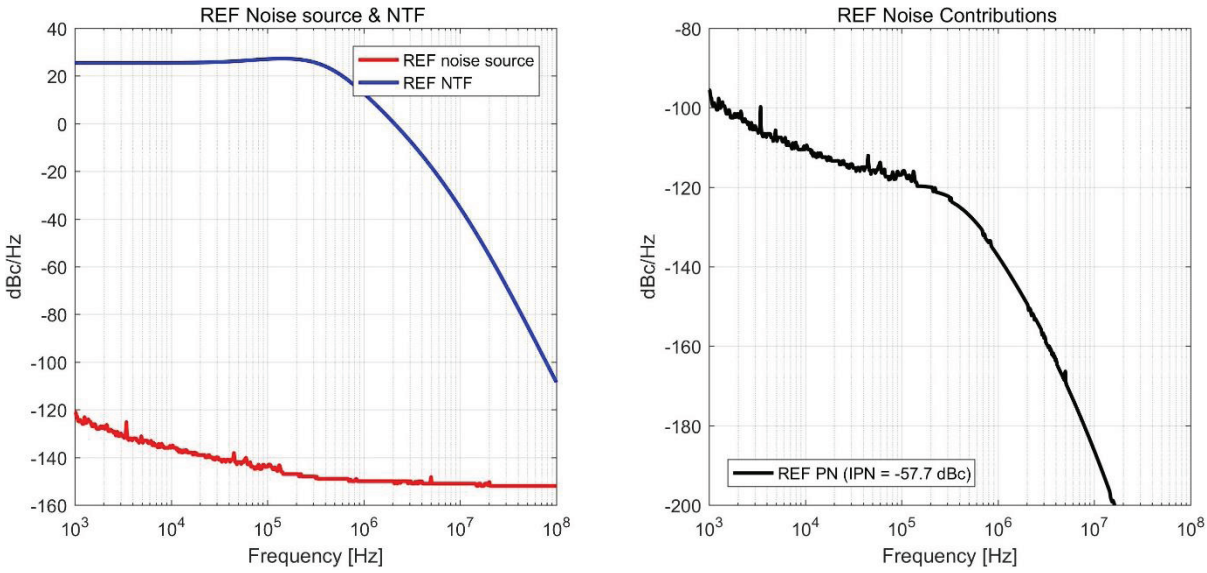
In the practical design of the PLL, the reference clock is implemented as a crystal oscillator (XO). Thus, the XO and a driver that carries a signal from the XO to the PFD are the dominant noise sources of the reference clock. For the MATLAB simulation, the measured phase noise with the 200 MHz reference frequency from the signal generator (Holzworth HS9002A) was used as the reference noise. Then, by multiplying the reference noise and the square of the NTF of the reference clock, MATLAB plots the reference noise, the reference NTF, $NTF_{REF}(s)$, and the output-referred reference phase noise, $S_{n,OUT,REF}$, as shown Figure 41, where the $NTF_{REF}(s)$ and $S_{n,OUT,REF}$ are

$$NTF_{REF}(s) = 20\log_{10}\left(N \cdot \frac{OL(s)}{1+OL(s)}\right) \tag{39}$$

and

$$S_{n,OUT,REF} = 20\log_{10}(\phi_{n,REF}) + NTF_{REF}(s) \tag{40}$$

respectively.



(a) (b)

Figure 41. (a) the noise (red) and the NTF (blue) of the reference clock. (b) the output-referred reference noise

Figure 41(a) shows the noise source in red ($20\log_{10}(\phi_{n,REF})$) and the NTF in blue (dB). As already discussed in Table 8, the NTF of the reference clock shows flat shape at the in-band frequencies and roll-off at the out-band frequencies as follows.

$$NTF_{\mathrm{REF}}(s) \approx \begin{cases} 20\log_{10}(N) & \text{for } f \ll \text{PLL BW} \\ 20\log_{10}\left(N \cdot G(s)\right) & \text{for } f \gg \text{PLL BW} \end{cases} \tag{41}$$

Since N is 18.75, the value of the NTF at the in-band is 25.46 dB (= $20\log_{10}(18.75)$). Figure 41(b) shows the output-referred reference phase noise, $S_{\mathrm{n,OUT,REF}}$, i.e., when $\phi_{\mathrm{n,REF}}$ is shaped by the $NTF_{\mathrm{REF}}(s)$ as expressed in Equation (40).

PFD and CP Noise ($i_{n,PFD-CP}$)

According to S_{UP} and S_{DN}, the CP dumps a net current into the loop filter by turning on the switches between the loop filter and the current source of the CP. However, when the switches are on, not only the net current but also noise component flow into the loop filter as shown in Figure 42.

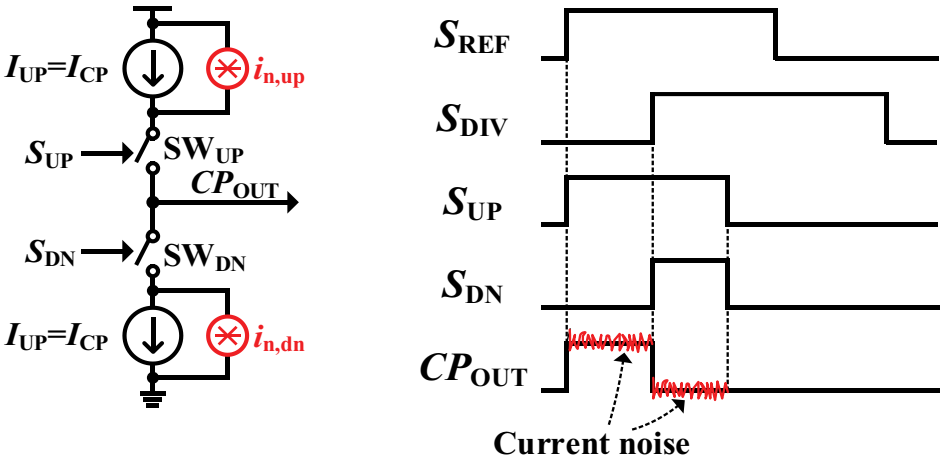
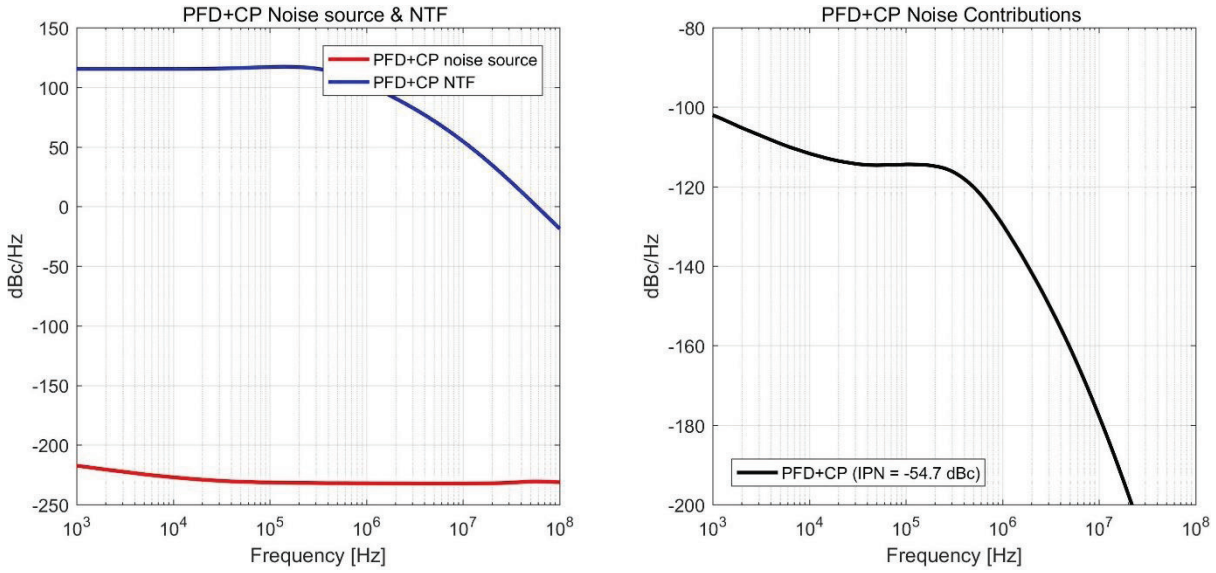


Figure 42. Injection of charge pump noise when SW_{UP} and SW_{DN} are on



(a) (b)

Figure 43. (a) the noise (red) and the NTF (blue) of the PFD and the CP. (b) the output-referred reference noise

Figure 43 (a) shows the noise source in red and the NTF in blue. To have a CP noise, the CP was simply implemented in Cadence. Then, the noise of the CP, $i_{n,PFD-CP}$, was obtained from the schematic simulation results. Then, by using the $i_{n,PFD-CP}$ and the NTF of the PFD and the CP, MATLAB plots the

$i_{n,PFD\text{-}CP}$, the NTF of the PFD and the CP, $NTF_{PFD\text{-}CP}(s)$, and the output-referred phase noise, $S_{n,OUT,PFD\text{-}CP}$, as shown in Figure 43. The $NTF_{PFD\text{-}CP}(s)$ and $S_{n,OUT,PFD\text{-}CP}$ are calculated as

$$NTF_{PFD\text{-}CP}(s) = 20\log_{10}\left(\frac{N}{K_{PFD\text{-}CP}} \cdot \frac{OL(s)}{1+OL(s)}\right) \tag{42}$$

and

$$S_{n,OUT,PFD\text{-}CP} = 20\log_{10}(\phi_{n,PFD\text{-}CP}) + NTF_{PFD\text{-}CP}(s) \tag{43}$$

respectively. Figure 43(a) shows the noise source in red ($20\log_{10}(\phi_{n,PFD\text{-}CP})$) and the NTF in blue. As already discussed in Table 8, $NTF_{PFD\text{-}CP}(s)$ shows flat shape at the in-band frequencies and roll-off at the out-band frequencies as follows.

$$NTF_{PFD\text{-}CP}(s) \approx \begin{cases} 20\log_{10}\left(\frac{N}{K_{PFD\text{-}CP}}\right) & \text{for } f \ll \text{PLL BW} \\ 20\log_{10}\left(\frac{G(s)}{K_{PFD\text{-}CP}}\right) & \text{for } f \gg \text{PLL BW} \end{cases} \tag{44}$$

Since N is 18.75 and the $K_{PFD\text{-}CP}$ is 200 μA/2π, the value of the NTF, $NTF_{PFD\text{-}CP}$(s), at the in-band is 115.40 dB (= $20\log_{10}(N/K_{PFD\text{-}CP})$). Note that the gap between $NTF_{PFD\text{-}CP}$(s) and NTF_{REF}(s) at the in-band is $20\log_{10}(K_{PFD\text{-}CP})$. When the $K_{PFD\text{-}CP}$ increased, the level of the $NTF_{PFD\text{-}CP}$(s) at the in-band decreases, and thus, suppressed the output-referred noise of the PFD and the CP. Figure 43(b) shows the output-referred phase noise of the PFD and the CP, $S_{n,OUT,PFD\text{-}CP}$, i.e., when $\phi_{n,PFD\text{-}CP}$ is shaped by the $NTF_{PFD\text{-}CP}(s)$ as expressed in Equation (43).

Loop Filter Noise ($v_{n,LF}$)

The passive loop filter also contributes to the noise because the loop filter contains resistors having the thermal noise, which adds noisy voltage to the control voltage of the VCO. Therefore, when the loop filter is designed, using a too large resistor should be avoided since the thermal noise depends on the resistance, as shown in the below definition of the thermal noise of a resistor.

$$v_{n,Rx} = \sqrt{4 \cdot T_0 \cdot k_B \cdot Rx} \tag{45}$$

where T_0, k_B, and Rx are the absolute temperature of Rx in kelvins, Boltzmann constant (joules/kelvin), and resistance, respectively. "x" is just an index number to distinguish resistors. Figure 44 shows the 4th order loop filter with the noise sources based on the definition in Equation (45). From Figure 44, to figure out how much amount of each resistor's voltage noise is transferred to the control voltage, V_{TUNE}, each noise source is investigated separately since the location of the resistors is different [27], [31].

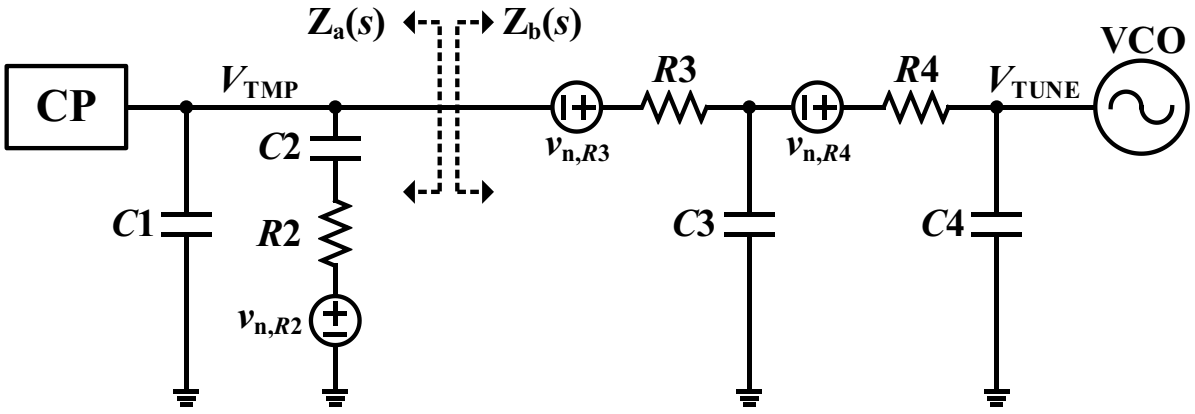


Figure 44. The 4th order loop filter with the noise sources

In the above figure, for the easy calculation, in the loop filter, the impedance $Z_a(s)$ and $Z_b(s)$ are defined when looking only left side from V_{TMP} to ground and only right side from V_{TMP} to ground, respectively. Then, $Z_a(s)$ and $Z_b(s)$ can be calculated as follows.

$$Z_a(s) = \left(\frac{1}{C1s}\right) || \left(R2 + \frac{1}{C2s}\right) \tag{46}$$

$$= \frac{1 + R2C2s}{(C1 + C2)s + R2C1C2s^2} \tag{47}$$

$$Z_b(s) = \frac{1 + (R3C3 + R4C4 + R3C4)s + R3C3R4C4s^2}{(C3 + C4)s + C3C4R4s^2} \tag{48}$$

In addition, the transfer function from V_{TMP} to V_{TUNE} can be pre-defined as

$$TF_{TMP}(s) = \frac{1}{1+(R3C3 + R4C4 + R3C4)s + R3C3R4C4s^2} \tag{49}$$

In the following, each noise source is analyzed by using $Z_a(s)$, $Z_a(s)$, and $TF_{TMP}(s)$.

Analysis for the *R*2 (x=2)

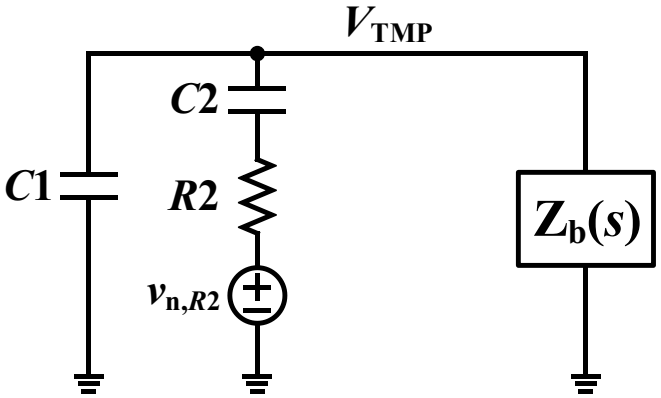


Figure 45. Simplified loop filter for the *R*2 noise calculation

The simplified loop filter for the noise calculation of *R*2 is shown in Figure 45. The effect of $v_{n,R2}$ on V_{TUNE}, i.e., the transfer function from $v_{n,R2}$ to V_{TUNE}, is

$$TF_{R2}(s) = \frac{\left(\frac{1}{C1s}||Z_b(s)\right)}{R2 + \frac{1}{C2s} + \left(\frac{1}{C1s}||Z_b(s)\right)} \cdot TF_{TMP}(s) \tag{50}$$

Analysis for the *R*3 (x=3)

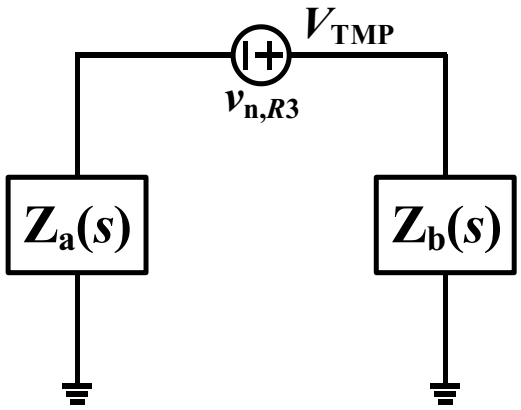


Figure 46. Simplified loop filter for the *R*3 noise calculation

The simplified loop filter for the noise calculation of $R3$ is shown in Figure 46. The effect of $v_{n,R3}$ on V_{TUNE}, i.e., the transfer function from $v_{n,R3}$ to V_{TUNE}, is

$$TF_{R3}(s) = \frac{Z_b(s)}{Z_a(s) + Z_b(s)} \cdot TF_{TMP}(s) \tag{51}$$

Analysis for the $R4$ (x=4)

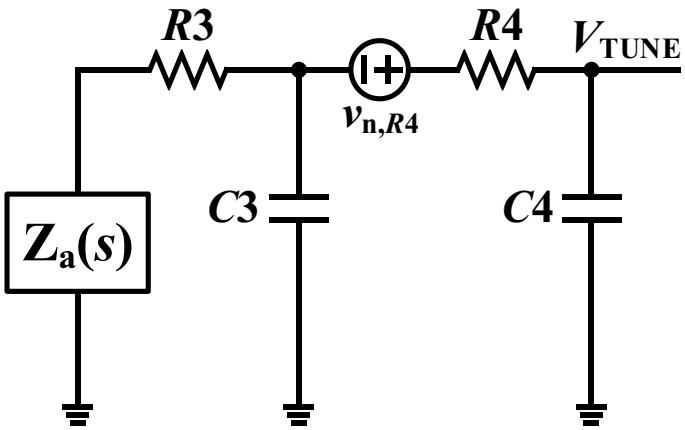


Figure 47. Simplified loop filter for the $R4$ noise calculation

The simplified loop filter for the noise calculation of $R2$ is shown in Figure 47. The effect of $v_{n,R4}$ on V_{TUNE}, i.e., the transfer function from $v_{n,R4}$ to V_{TUNE}, is

$$TF_{R4}(s) = \frac{\frac{1}{C4s}}{R4 + \frac{1}{C4s} + \left(\frac{1}{C3s} || (Z_a(s) + R3)\right)} \tag{52}$$

Add All Noise Source in V_{TUNE}

After the three noise sources are translated to the V_{TUNE} by using its own transfer function, the translated voltage noises can be converted to the output-referred phase noise, $S_{n,OUT,Rx}$ (x = 2,3, or 4), with the help of NTF of the loop filter, $NTF_{LF}(s)$, as discusses in Table 7. The $NTF_{LF}(s)$, $S_{n,OUT,R2}$, $S_{n,OUT,R3}$, and $S_{n,OUT,R4}$ are represented as

$$NTF_{LF}(s) = 20\log_{10}\left(\frac{K_{VCO}}{s} \cdot \frac{1}{1+OL(s)}\right) \tag{53}$$

$$S_{n,OUT,R2} = 20\log_{10}\left(\frac{v_{n,R2}}{\sqrt{2}} \cdot TF_{R2}(s)\right) + NTF_{LF}(s), \tag{54}$$

$$S_{\mathrm{n,OUT},R3} = 20\log_{10}\left(\frac{v_{\mathrm{n},R3}}{\sqrt{2}} \cdot \mathrm{TF}_{R3}(s)\right) + NTF_{\mathrm{LF}}(s), \tag{55}$$

and

$$S_{\mathrm{n,OUT},R4} = 20\log_{10}\left(\frac{v_{\mathrm{n},R4}}{\sqrt{2}} \cdot \mathrm{TF}_{R4}(s)\right) + NTF_{\mathrm{LF}}(s), \tag{56}$$

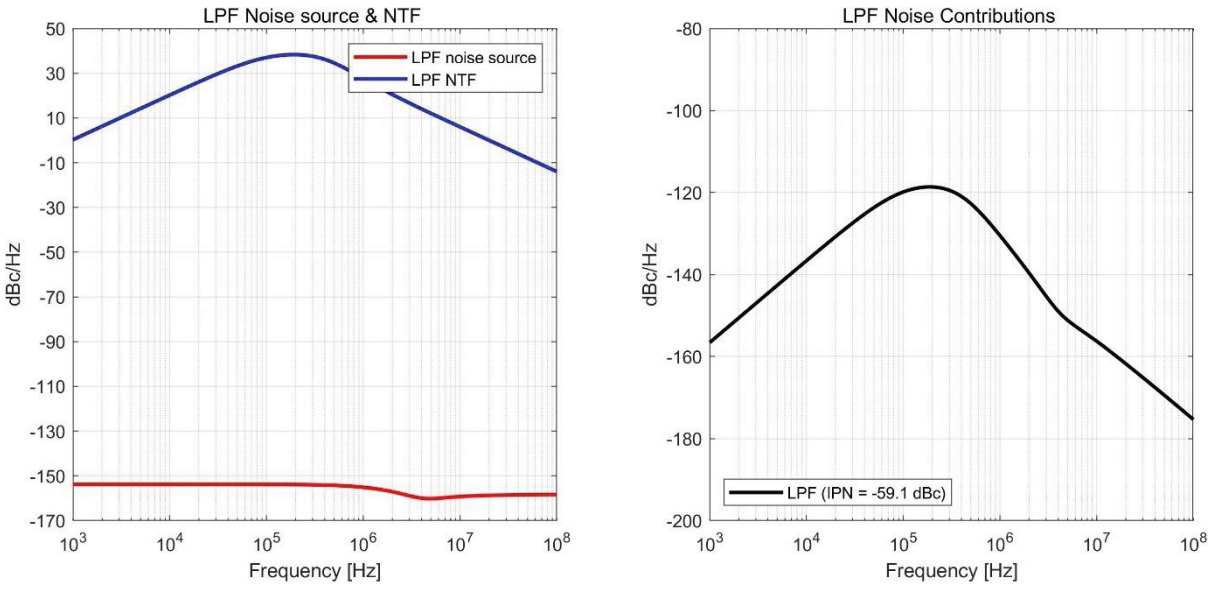
respectively. Therefore, the output-referred noise of the loop filter, $S_{\mathrm{n,OUT,LF}}$, due to $R2$, $R3$, and $R4$, can be calculated as follows.

$$S_{\mathrm{n,OUT,LF}} = 10\log_{10}\left(10^{\frac{S_{\mathrm{n,OUT},R2}}{10}} + 10^{\frac{S_{\mathrm{n,OUT},R3}}{10}} + 10^{\frac{S_{\mathrm{n,OUT},R4}}{10}}\right) \tag{57}$$

Table 10. Loop filter parameters

***C*1**	***R*2**	***C*2**	***R*3**	***C*3**	***R*4**	***C*4**
11.46 pF	8.835 kΩ	261.39 pF	8.835 kΩ	2.75 pF	8.835 kΩ	2.75 pF

Using the MATLAB, to figure out the loop filter noise transfer function and the level of the noise from the above theoretical calculation, a simple loop filter was designed with the parameters shown in Table 10 along with the parameters in Table 9.



(a) (b)

Figure 48. (a) the noise (red) and the NTF (blue) of the loop filter. (b) the output-referred reference noise

Figure 48(a) shows the noise source in red and the NTF in blue. As already discussed in Table 8, $NTF_{\mathrm{LF}}(s)$ shows similar shape with the band pass filter because the NTF of the loop filter can be approximated as follows.

$$NTF_{\mathrm{PFD\text{-}CP}}(s) \approx \begin{cases} 20\log_{10}\left(\dfrac{K_{\mathrm{VCO}}}{s}\cdot\dfrac{1}{OL(s)}\right) & \text{for } f \ll \text{PLL BW} \\ 20\log_{10}\left(\dfrac{K_{\mathrm{VCO}}}{s}\right) & \text{for } f \gg \text{PLL BW} \end{cases} \tag{58}$$

Figure 48(b) shows the output-referred phase noise of the loop filter, $S_{\mathrm{n,OUT,LF}}$, i.e., when $v_{\mathrm{n},R2}$, $v_{\mathrm{n},R3}$, and $v_{\mathrm{n},R4}$ are shaped by $\mathrm{TF}_{R2}(s)$ along with $NTF_{\mathrm{LF}}(s)$, $\mathrm{TF}_{R3}(s)$ along with $NTF_{\mathrm{LF}}(s)$, and $\mathrm{TF}_{R2}(s)$ along with $NTF_{\mathrm{LF}}(s)$, respectively. As shown, the output-referred loop filter noise also shows the shape of the band pass filter since the input-referred noise of the loop filter is almost flat as shown in red line.

VCO Noise ($\phi_{n,VCO}$)

The VCO is a unique building block whose noise is high pass filtered by the PLL. The phase noise of the free-running VCO can be modeled by the Lesson's Equation as follows when the flicker noise is not considered [32].

$$L(\Delta f) = 10\log_{10}\left[\frac{2kT}{P_{sig}} \cdot \left(\frac{f_0}{2Q\Delta f}\right)^2\right] \tag{59}$$

where $L(\Delta f)$ is the VCO phase noise at the offset frequency of Δf. Note that phase noise of the VCO shows the slope of −20 dB/dec as clearly shown in the above equation.

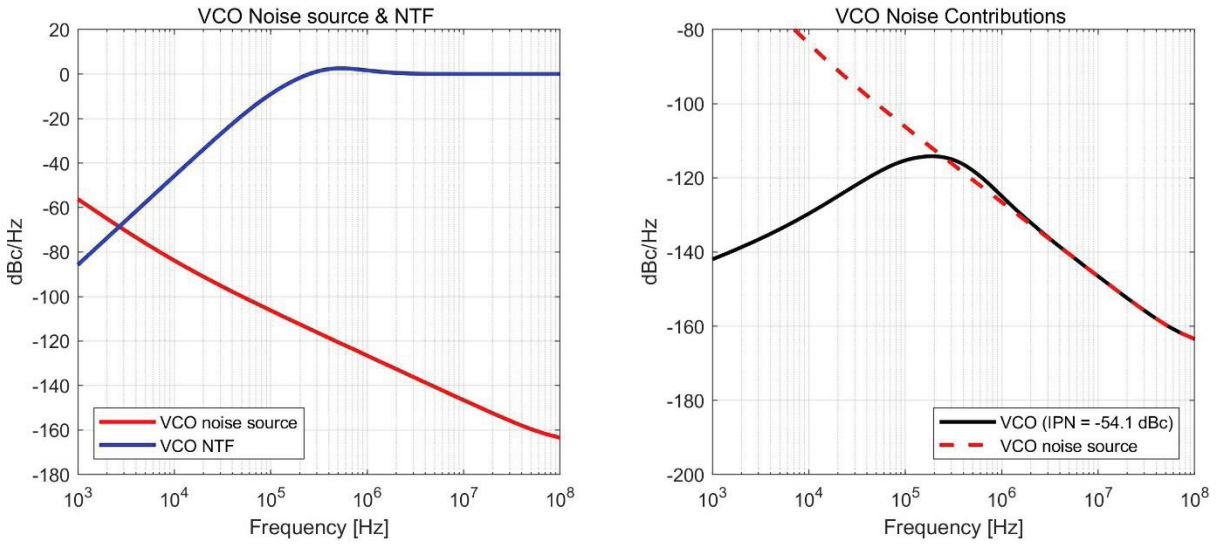
For the MATLAB simulation, an *LC* VCO was simply designed to oscillate at 3.75 GHz and simulated to obtain the free-running phase noise of the VCO. Then, by using the VCO's phase noise and NTF of the reference clock, MATLAB plots the VCO phase noise, the VCO's NTF, $NTF_{VCO}(s)$, and the output-referred VCO phase noise, $S_{n,OUT,VCO}$, as shown, where the $NTF_{VCO}(s)$ and $S_{n,OUT,VCO}$ are

$$NTF_{VCO}(s) = 20\log_{10}\left(\frac{1}{1+OL(s)}\right) \tag{60}$$

and

$$S_{n,OUT,VCO} = L(\Delta f) + NTF_{VCO}(s) \tag{61}$$

respectively.



(a) (b)

Figure 49. (a) the noise (red) and the NTF (blue) of the VCO. (b) the output-referred phase noise of the VCO

Figure 49(a) shows the noise source in red ($L(\Delta f)$) and the NTF in blue. As already discussed in Table 8, $NTF_{\mathrm{VCO}}(s)$ shows the shape of the high pass filter because the NTF of the loop filter can be approximated as follows.

$$NTF_{\mathrm{VCO}}(s) \approx \begin{cases} 20\log_{10}\left(\dfrac{1}{OL(s)}\right) & \text{for } f \ll \text{PLL BW} \\ 20\log_{10}(1) & \text{for } f \gg \text{PLL BW} \end{cases} \tag{62}$$

Figure 48(b) shows the output-referred phase noise of the VCO, $S_{\mathrm{n,OUT,VCO}}$ with the free-running VCO's phase noise. As shown, at the high offset frequencies, the phase noise of the VCO is directly reflected to the output of the PLL, since the $NTF_{\mathrm{VCO}}(s)$ at the out-band is almost zero ($20\log_{10}(1) = 0$).

DSM Noise ($\phi_{n,DSM}$)

The noise of the DSM, $\phi_{n,DSM}$, can be estimated by

$$\phi_{n,DSM}^2(f) = \frac{(2\pi)^2}{12 \cdot f_{REF}} \cdot \left(2\sin\left(\frac{\pi \cdot f}{f_{REF}}\right)\right)^{2(n-1)} \tag{63}$$

where n is the order of the DSM [31], [33]. The below shows the derivation process of $\phi_{n,DSM}(f)$ from the quantization noise at the output of the n^{th} order DSM. First, let's revisit Equation (21), as below.

$$Y(z) = X(z) + Q(z)\cdot(1 - z^{-1})^n \tag{64}$$

In Equation (64), X(z) is the desired division number and the high pass shaped quantization noise, $Q(z)\cdot(1-z^{-1})^n$, makes Y(z) to be noisy. Therefore, at the PLL output, the frequency fluctuations amount will be

$$Q(z)\cdot(1 - z^{-1})^n \cdot f_{REF} \tag{65}$$

Then, we need to figure out the effect of the frequency fluctuation on the phase noise. By assuming that the quantization error, Q(z), is uniformly distributed, the error power can be represented as

$$\frac{(\text{Unit step size})^2}{12} = \frac{1}{12} \tag{66}$$

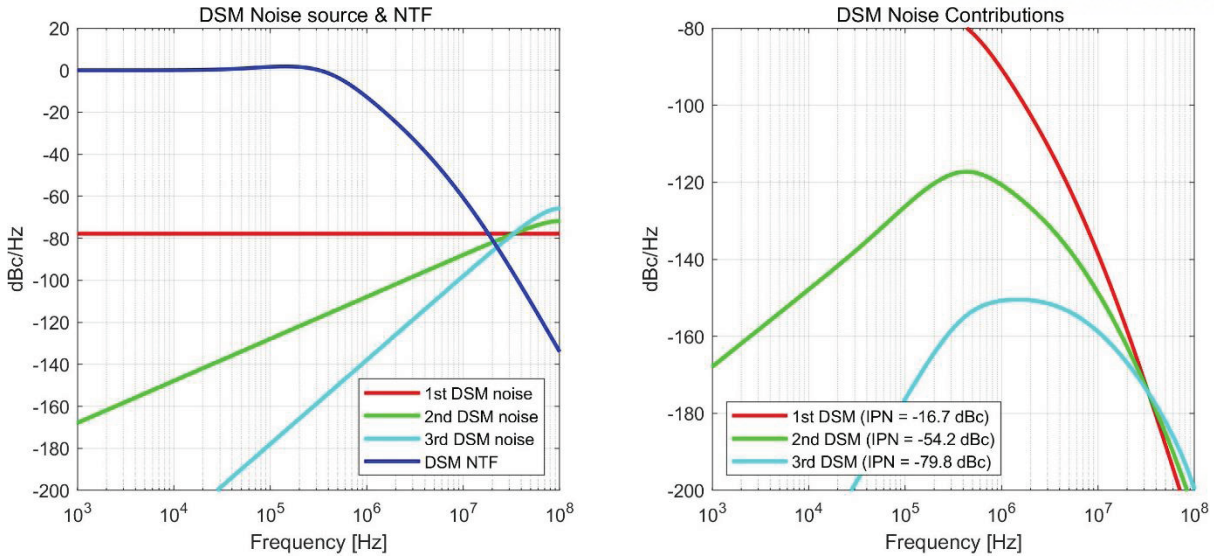
where the unit step is one. Since the quantization error power spreads over the operating frequency of the DSM, f_{REF}, the power spectral density (PSD) of the Q(z) will be

$$\text{PSD of } Q(z) = \frac{1}{12 f_{REF}} \tag{67}$$

By using Equation (65) and (67), the PSD of the frequency fluctuation, $S_f(z)$ at the PLL output will be

$$S_f(z) = \frac{1}{12 f_{REF}} \left|(1 - z^{-1})^n \cdot f_{REF}\right|^2 = \frac{f_{REF}}{12} \left|(1 - z^{-1})\right|^{2n} \tag{68}$$

Finally, by converting Equation (68) to the phase domain, Equation (63) can obtained [30],[33].



(a) (b)

Figure 50. (a) the noise of 1st order DSM (red), 2nd order DSM (green), 3rd order DSM (light blue), and the NTF (blue). (b) the output-referred phase noise of 1st order DSM (red), 2nd order DSM (green), and 3rd order DSM (light blue)

Figure 50(a) shows the NTF in blue, the phase noise of 1st order DSM in red, 2nd order DSM in green, 3rd order DSM in light blue. The NTF of the DSM, $NTF_{\mathrm{DSM}}(s)$, and the output-referred phase noise of the DSM can be written as

$$NTF_{\mathrm{DSM}}(s) = 20\log_{10}\left(\frac{OL(s)}{1+OL(s)}\right) \tag{69}$$

and

$$S_{\mathrm{n,OUT,DSM}} = 20\log_{10}(\phi_{\mathrm{n,DSM}}) + NTF_{\mathrm{DSM}}(s) \tag{70}$$

respectively. In Figure 50(a), the $NTF_{\mathrm{DSM}}(s)$ show the low pass filter characteristics since the $NTF_{\mathrm{DSM}}(s)$ is also approximated as follows.

$$NTF_{\mathrm{REF}}(s) \approx \begin{cases} 20\log_{10}(1) & \text{for } f \ll \text{PLL BW} \\ 20\log_{10}\left(OL(s)\right) & \text{for } f \gg \text{PLL BW} \end{cases} \tag{71}$$

Note that at the low offset frequencies, the phase noise of the DSM is directly reflected to the output of the PLL, since the $NTF_{\mathrm{DSM}}(s)$ at the in-band is almost zero ($20\log_{10}(1) = 0$). In addition, it is clear as the order of the DSM increases, the noise of the DSM is more shaped. Another notation is phase noise of the 1st DSM shows no slope, this is because when the quantization noise in the frequency domain is

translated to the phase domain, additional pole is introduced. As a summary, n^{th} order DSM's quantization noise in phase domain has a slope of −20(n−1) dB/dec. Figure 50(b) shows the output-referred phase noise of the DSM, $S_{n,OUT,DSM}$ according to the order of the DSM. As the order of the DSM increases, the smaller phase noise will be appeared into the $S_{n,OUT,DSM}$. Therefore, to minimize noise from the DSM, proper selection of the DSM order is important.

Frequency Divider Noise ($\phi_{n,DIV}$)

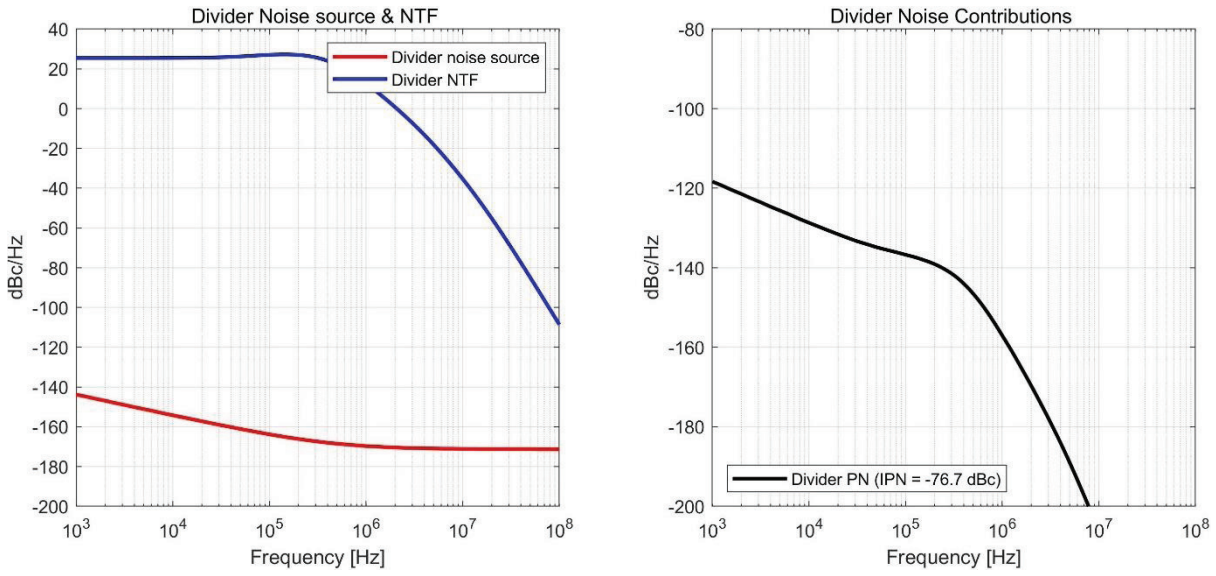
The frequency divider also has noise components which could degrade overall phase noise performance. For the MATLAB simulation, the frequency divider is simply designed based on the dual-modulus divider. Then, the simulated phase noise was used as the frequency divider noise source. Then, by using the frequency divider noise and the square of the NTF of the divider, MATLAB plots the phase noise of the divider, the frequency divider NTF, $NTF_{DIV}(s)$, and the output-referred frequency divider phase noise, $S_{n,OUT,DIV}$, as shown , where the $NTF_{DIV}(s)$ and $S_{n,OUT,DIV}$ are

$$NTF_{DIV}(s) = 20\log_{10}\left(N \cdot \frac{OL(s)}{1+OL(s)}\right) \tag{72}$$

and

$$S_{n,OUT,DIV} = 20\log_{10}(\phi_{n,DIV}) + NTF_{DIV}(s) \tag{73}$$

respectively.



(a) (b)

Figure 51. (a) the noise (red) and the NTF (blue) of the frequency. (b) the output-referred frequency divider phase noise

Figure 51(a) shows the noise source in red ($20\log_{10}(\phi_{n,DIV})$) and the NTF in blue. As already discussed in Table 8, the NTF of the frequency divider is the same as the NTF of the reference clock. Thus, it shows a flat shape at the in-band frequencies and roll-off at the out-band frequencies as follows.

$$NTF_{\mathrm{DIV}}(s) \approx \begin{cases} 20\log_{10}(N) & \text{for } f \ll \text{PLL BW} \\ 20\log_{10}\left(N \cdot G(s)\right) & \text{for } f \gg \text{PLL BW} \end{cases} \tag{74}$$

Since N is 18.75, the value of the NTF at the in-band is 25.46 dB (= $20\log_{10}(18.75)$). Figure 51(b) shows the output-referred frequency divider phase noise, $S_{\mathrm{n,OUT,DIV}}$, i.e., when $\phi_{\mathrm{n,DIV}}$ is shaped by the $NTF_{\mathrm{DIV}}(s)$ as expressed in Equation (73).

Estimated Phase Noise at the PLL Output

By adding the derived each noise source from the building blocks of the PLL, output phase noise of the PLL can be esimated based on the MATLAB.

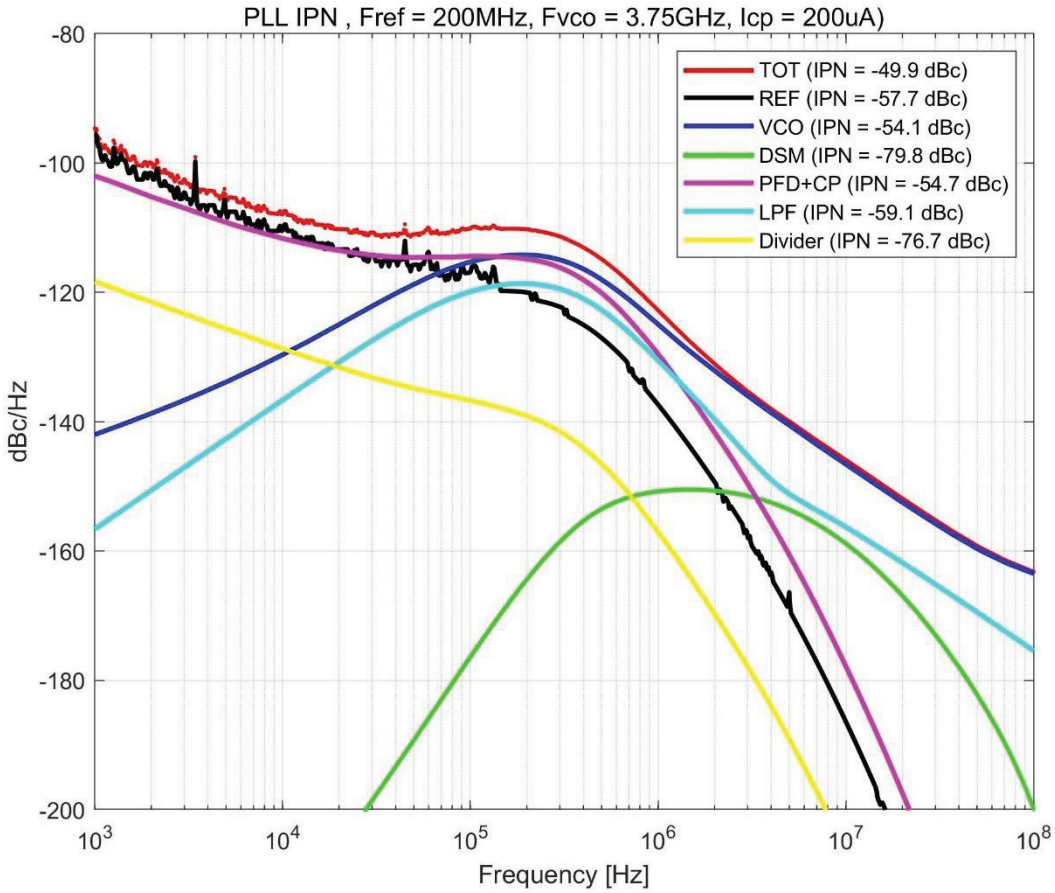


Figure 52. Estimated phase noise at the output of the PLL by adding each noise sources

Based on MATLAB, Figure 52 shows the estimated phase noise at the output of the PLL by adding the derived output-referred noise of each building block. The order of the DSM is assumed as three. The estimation shows that the double sideband (DSB) IPN of −49.9 dBc. As shown, the in-band phase noise is saturated by the phase noise of the reference clock, the PFD, and the CP. The out-band phase noise is limited by the phase noise of the VCO. It means that if phase noise of the reference clock or the PFD and the CP is relatively high, it is better to have low bandwidth to suppress the in-band phase noise. Meanwhile, if the phase noise of the VCO is relatively high, it is better to design the PLL to have high bandwidth to suppress the VCO noise.

2.3.3 Stability

Since a PLL is a negative feedback system consisting of a PFD, a CP, an LF, a VCO, and a frequency divider, it is important to secure stability not to make the system oscillate or fail to lock. For the stability analysis of the PLL, the transfer functions of each building block are re-used to configure open loop gain of the PLL, $OL(s)$, as follows, then through the $OL(s)$, stability of the PLL can be analyzed by the number of poles and zeros along with their locations.

$$OL(s) = K_{\text{PFD-CP}} \cdot Z_{\text{LF}}(s) \cdot \frac{K_{\text{VCO}}}{s} \cdot \frac{1}{N} \tag{75}$$

In general CP PLLs, the "Type" and the "Order" of the PLL are determined by the poles in the open loop gain of the PLL. First, the type of PLL depends on the number of poles at the origin, i.e., DC. For the general type-I PLL, it has one pole at the origin, which comes from the VCO. In case of the general type-II PLL, it has two poles at the origin, which come from the VCO and the loop filter. Second, the order of PLL is determined by only the number of poles in the open loop gain. For the stability analysis here, the type-II 3rd order PLL will be analyzed since it is the most basic structure of the PLL. In the type-II 3rd order PLL, the transfer function of the loop filter, $Z_{\text{LF}}(s)$, and $OL_{\text{3rd\_PLL}}(s)$ can be defined as

$$Z_{\text{LF}}(s) = \frac{1+R2C2s}{(C1+C2)s+R2C1C2s^2} \tag{76}$$

and

$$OL_{\text{3rd\_PLL}}(s) = K_{\text{PFD-CP}} \cdot \frac{K_{\text{VCO}}}{s} \cdot \frac{1}{N} \cdot \frac{1+R2C2s}{(C1+C2)s+R2C1C2s^2} \tag{77}$$

respectively. In the $OL_{\text{3rd\_PLL}}(s)$, the location of poles and zero is as follows.

$$\omega_{\text{P1}}=0,\ \omega_{\text{P2}}=0,\ \omega_{\text{P3}} = \frac{C1+C2}{R2C1C2}\left(\approx \frac{1}{R2C1}\right),\ \omega_{\text{Z1}} = \frac{1}{R2C2} \tag{78}$$

As shown, there are two poles at the origin, which means that the phase is -180° when the loop starts from DC. Therefore, the loop has the zero, ω_{Z1}, to raise the phase around the unit frequency of the loop, thereby to secure the phase margin. Note that ω_{P3} can be approximated as $1/R2C1$ since $C2$ is much larger than $C1$. Since there are many references that already calculate the exact value of phase margin

according to the value of $C1$, $C2$, and $R2$. Thus, in this thesis, the change in the bode plot according to the adjustment of the value of $C1$, $C2$, and $R2$ is intuitively shown in the following.

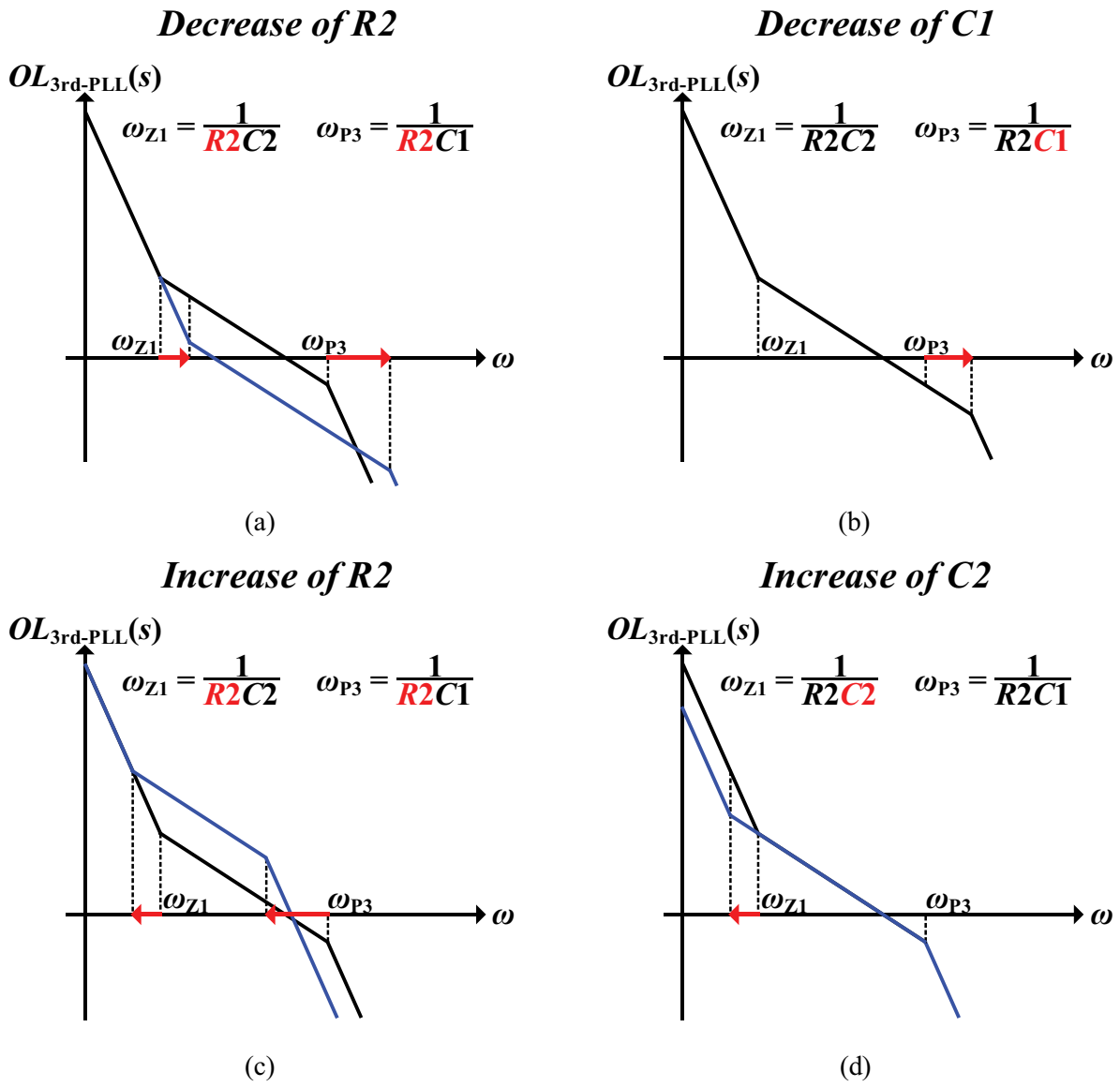


Figure 53. The bode plot with the fixed value of $K_{PFD\text{-}CP}$, K_{VCO}, and N; (a) when $R2$ is decreased, (b) when $C1$ is decreased, (a) when $R2$ is increased, (b) when $C2$ is increased

Let's assume that the value of $K_{PFD\text{-}CP}$, K_{VCO}, and N are fixed. Then, Figure 53(a), (b), (c), and (d) show when $R2$ is decreased, $C1$ is decreased, $R2$ is increased, and $C2$ is increased, respectively. In the case of (a) and (c), when the value of $R2$ is changed, not only the location of ω_{Z1} and ω_{P3}, but also the unity gain frequency also moves. This is because the value of $R2$ is coupled to both ω_{Z1} and ω_{P3}. Therefore, if you want to change the value of $R2$ for the change of the phase margin or the unity gain frequency, it should be done very carefully. In the case of (b) and (d), when the value of $C1$ or $C2$ is changed, the

unity gain frequency is not moved. Therefore, if someone wants to improve the phase margin without any change in the unity gain frequency, there are two options as shown. First one is to push the ω_{P3} by decreasing the value of $C1$ as in Figure 53(b). The second one is to pull the ω_{Z1} by increasing the value of $C2$ as in Figure 53(d). This tendency also can be applied to more higher order type-II PLLs such as type-II 5^{th} or 4^{th} order PLLs.

3. Fundamentals of *LC* VCO

In modern RF communication systems, the increasing demands on *LC* VCO such as low power consumption, low phase noise, and wide frequency tuning range force the RF designers to maximize the performance of *LC* VCO in a given technology. Thus, to fairly compare the performance of each *LC* VCO, Figure of Merit (FOM) was introduced, since the performance metrics of *LC* VCO is all in the trade-off relationship. The FOM of the VCO, FOM_{VCO}, is defined as [34]

$$FOM_{\mathrm{VCO}} = L_{\mathrm{VCO}}(\Delta f) + 10\log_{10}\left(\frac{P}{1\ \mathrm{mW}}\right) - 20\log_{10}\left(\frac{f_0}{\Delta f}\right), \tag{79}$$

where Δf, f_0, and P are the offset frequency, the oscillation frequency of the VCO, and the power consumption, respectively. If the frequency tuning range is also considered, the FOM with tuning range, $FOMT_{\mathrm{VCO}}$, is defined as

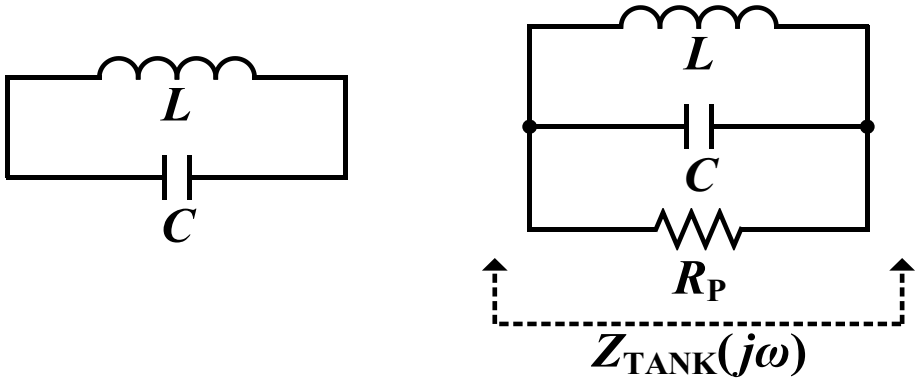
$$FOMT_{\mathrm{VCO}} = L_{\mathrm{VCO}}(\Delta f) + 10\log_{10}\left(\frac{P}{1\ \mathrm{mW}}\right) - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) - 20\log_{10}\left(\frac{\mathrm{FTR}}{10}\right). \tag{80}$$

To optimize the FOM_{VCO} even with the trade-offs, understanding the basics and the characteristics of *LC* VCO is a starting point. Thus, the fundamentals of *LC* VCO are introduced in the following.

3.1 *LC* Resonator of *LC* VCO

3.1.1 Basics of *LC* Tank

Design of an *LC* tank is generally starting point of the *LC* VCO design since the *LC* tank not only determines the oscillation frequency of the VCO but also significantly affect the level of the phase noise.



(a) (b)

Figure 54. Simplified *LC* tank without (a) losses (ideal *LC* tank) (b) with losses

Figure 54(a) and (b) show the ideal *LC* tank and practical *LC* tank, respectively. As shown, the *LC* tank consists of an inductor and a capacitor in parallel. In Figure 54(b), additional resistor, R_P, is connected in parallel to represent losses, which come from the metal wire line, etc. Even though the simplified *LC* tank in Figure 54 cannot fully represent the practical one, it can give an insight into the characteristics and behavior of the *LC* tank. In the one-port view, the tank impedance in Figure 54(b) can be represented as

$$Z_{\mathrm{TANK}}(j\omega) = \left(\frac{1}{j\omega C}\right) || (j\omega L) || (R_P) \tag{81}$$

$$= \frac{1}{\frac{1}{R_P} + j\left(\omega L - \frac{1}{\omega C}\right)} \tag{82}$$

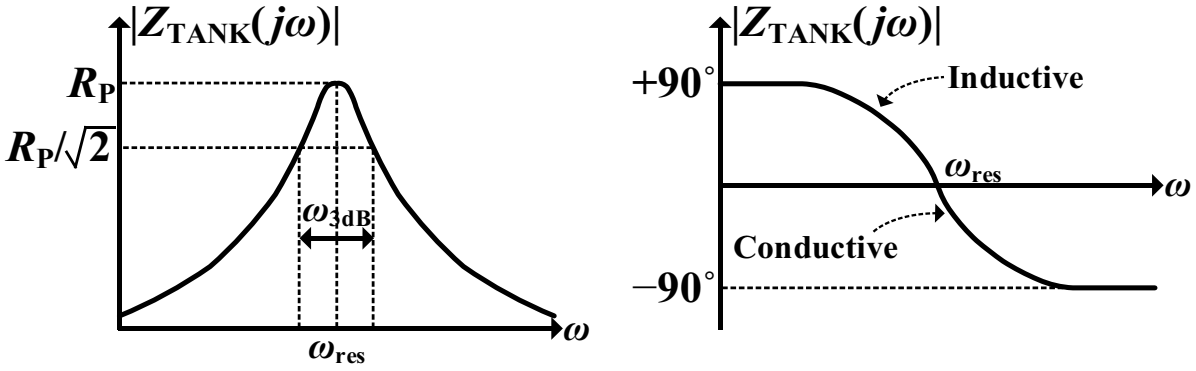
In Equation (82), when the imaginary part, i.e., reactive part, goes to zero at one specific frequency, that frequency is called as the resonance frequency of the *LC* tank, ω_{res}, which is calculated as

$$\omega_{\mathrm{res}} = \frac{1}{\sqrt{LC}} \tag{83}$$

and at the resonance frequency, the impedance of the tank will be

$$Z_{\mathrm{TANK}}(j\omega) = R_{\mathrm{P}} \tag{84}$$

Based on the above equations, the magnitude and the phase response of the tank impedance can be drawn as follows.



(a) (b)

Figure 55. (a) Magnitude of $Z_{\mathrm{TANK}}(j\omega)$ (b) phase of $Z_{\mathrm{TANK}}(j\omega)$

As shown in Figure 55(a) and (b), before reaches ω_{res}, the magnitude of the tank impedance increases and the phase of the tank is larger than zero. This is because the impedance of the inductor is dominant since it is smaller than the impedance of the capacitor. After ω_{res} is passed, the magnitude of the tank impedance decreases and the phase of the tank is smaller than zero, since the impedance of the capacitor is dominant.

Along with the resonance frequency, quality (Q)-factor is one of the important metrics since it indicates the ratio of the restored energy in the tank to the dissipated energy in the tank, which means that through Q-factor, the losses can be estimated. The definition of the Q-factor for the oscillating resonator is

$$Q = 2\pi \frac{\text{Eenergy stored}}{\text{Eenery dissipated per cycle}} \tag{85}$$

In addition, from the 3-dB bandwidth of Figure 55(a), the Q-factor can be defined as

$$Q = \frac{\omega_{\mathrm{res}}}{\omega_{\mathrm{3dB}}}, \tag{86}$$

which means that if the *LC* tank has a high Q-factor, the magnitude of the *LC* tank has a sharp response

around the resonance frequency. In other words, the sharper response means that the frequency filtering ability of the *LC* tank is improved. Thus, if we have a high Q-factor, *LC* VCO can achieve better phase noise performance. The Q-factor also can be defined for each passive component such as an inductor and a capacitor.

$$Q_{\text{Inductor}} = \frac{R_{\text{P}}}{j\omega L} = \frac{j\omega L}{R_{\text{S}}} \tag{87}$$

$$Q_{\text{Capacitor}} = R_{\text{P}}(j\omega C) = \frac{1}{R_{\text{S}}(j\omega C)} \tag{88}$$

where R_{S} is a series resistor which also represents the loss of each passive component. For general *LC* VCO operating at several GHz, Q-factor of the inductor dominates the Q-factor of the tank. This is because, at GHz range, the Q-factor of the capacitor is fairly larger than that of the inductor. In the following session, detail of the inductor along with the Q-factor will be detailed.

3.1.2 Integrated Inductor

As mentioned in the previous session, since the Q-factor of the inductor dominates the Q-factor of the *LC* tank, understanding Q-factor of the inductor is important. The Q-factor of the inductor shows different behavior according to the operating frequency.

At low frequencies

When the operating frequency is lower than several GHz, e.g. 10 − 20 GHz, the series resistance of the inductor is almost constant. Thus, the Q-factor of the inductor follows Equation (87).

At high frequencies

When the operating frequency is pretty high, the series resistance is not anymore constant and it starts to increases as the frequency goes up. The major cause is called a skin effect which is caused by an eddy current.

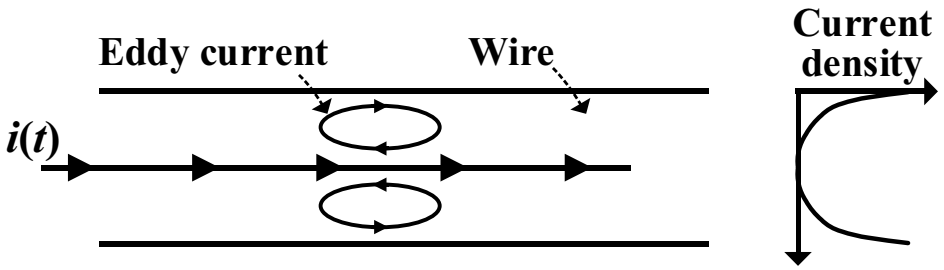


Figure 56. Effect of eddy current effect on series resistance

Figure 56 shows when the eddy current is occurred at high frequencies. As shown, the eddy current makes current loop within the wire. The eddy current is induced by the magnetic field variation due to the $i(t)$, which is the AC current. As shown, the eddy current makes low and high current density at the center of the wire and at the outside of the wire, respectively. It means that the reduced current path. Therefore, the effective series resistance increases. The eddy current is the main cause of the skin effect. In other words, the skin effect is the AC current tends to avoid flowing inside of the conductor and limits itself to flow near the "skin" of a wire. By the Maxwell's equation, the magnetic field is generated by change of the electric field, the skin effect apparently appears as the frequency increases. By the skin effect, the skin depth is defined, which is a depth that the current can flow from the surface of a conductor.

$$Skin\ depth = \delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{89}$$

where ρ, f, and μ are the resistivity of the metal, the frequency of the current, and the permeability of the material, respectively. As shown clearly in the above equation, as the frequency goes up, the skin depth decreases, and thus, increases the series resistance. In addition, when the inductor uses multiple turns, the eddy current can be induced by the magnetic field from the nearby turns of the inductor. Thus, it also prevents the current from flowing the whole area of the inductor. This phenomenon is called a proximity effect and it also significantly increases the series resistance. As a summary, up to a certain frequency, Q-factor increases as the frequency increases. Eventually, when the skin effect, the proximity effect, and the substrate lose appear, the tendency of the Q-factor starts to change, i.e., Q-factor decreases as the frequency increases.

Therefore, when the *LC* VCO is designed at the very high frequencies such as millimeter-wave bands, the inductor should be carefully designed since the series resistance could significantly degrade Q-factor of the inductor, and thus, the phase noise of the VCO.

3.1.3 Integrated capacitor

In the design of the integrated circuits (ICs), the capacitor is one of the basic and important components. Basically, capacitor stores energy in the electric field, which is formed between two nodes. In modern IC applications, three kinds of the capacitor are widely used; a metal-insulator-metal capacitor (MIM), metal-oxide-metal (MOM) capacitor, and a MOS capacitor. Since the three capacitors have different characteristics, the proper capacitor should be used according to the purpose. In the following, each capacitor's characteristics will be investigated.

Metal-insulator-metal (MIM) capacitor

Figure 57 shows the structure of the MIM capacitor in the general CMOS process [35]. The MIM capacitor consists of two metal plates at the top and the bottom, and a dielectric layer between the top and bottom metal. The top and bottom plate are usually called as the capacitance top metal (CTM) and the capacitance bottom metal (CBM), respectively. For high density, the dielectric layer is made by a high-k dielectric. Both metals, i.e., nodes, are connected to the thick metal for connection to the other circuits. For the MIM capacitor, to insert the dielectric layer between two metal plates, additional fabrication masks are required to define the top and the bottom plate. Therefore, the additional mask inevitably increases the fabrication cost. As shown, the bottom layer of the MIM capacitor is close to the top metal, i.e., thick metal, thus, the bottom plate has low parasitic capacitance compared to other capacitors. Also, the MIM cap has good linearity and robustness to a bias voltage and temperature variations. In addition, the MIM capacitor has high density, i.e., the capacitance per area, which means that effectiveness of the capacitor (Usually, about 2 fF/μm^2). However, for the MIM capacitor, it is hard to implement a unit capacitor having small capacitance.

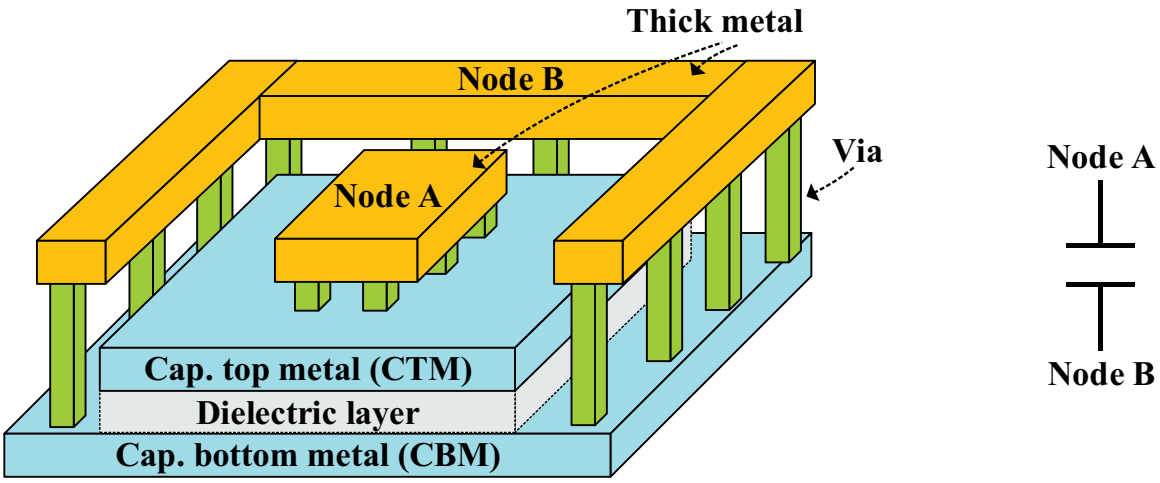


Figure 57. Structure of MIM capacitor

Metal-oxide-metal (MOM) capacitor

Figure 58 shows the structure of the MOM capacitor in the general CMOS process [35]. The MOM capacitors started to be used in deep-sub micron technology, such as 65-nm CMOS process. In the MOM capacitor, the parasitic capacitance between metal interconnections is used. Therefore, a unit capacitance of the MOM capacitor can be small compared to the MIM capacitor. To increase the density, multiple layers can be stacked as shown in Figure 58, which stacks three layers. However, generally, the density is about 0.5 fF/μm^2, which is much smaller than the MIM capacitor. The MOM capacitor can be extensively used with low fabrication cost since no additional fabrication mask is required for the generation of the MOM capacitor. However, when the large capacitance is required, the MOM capacitor should spend a lot of area due to the low density, which could increase the cost. The MOM capacitor is also robust to a bias voltage and temperature variations. However, different from the MIM capacitor, the MOM capacitor has somewhat higher parasitic capacitance at the bottom metal layers since the bottom plate is closer to the substrate than the MIM capacitor. In addition, several geometries can be used such as a parallel plate, interdigitated (with or without via stack), rotative, and fractal. (The below figure uses the interdigitated structure.)

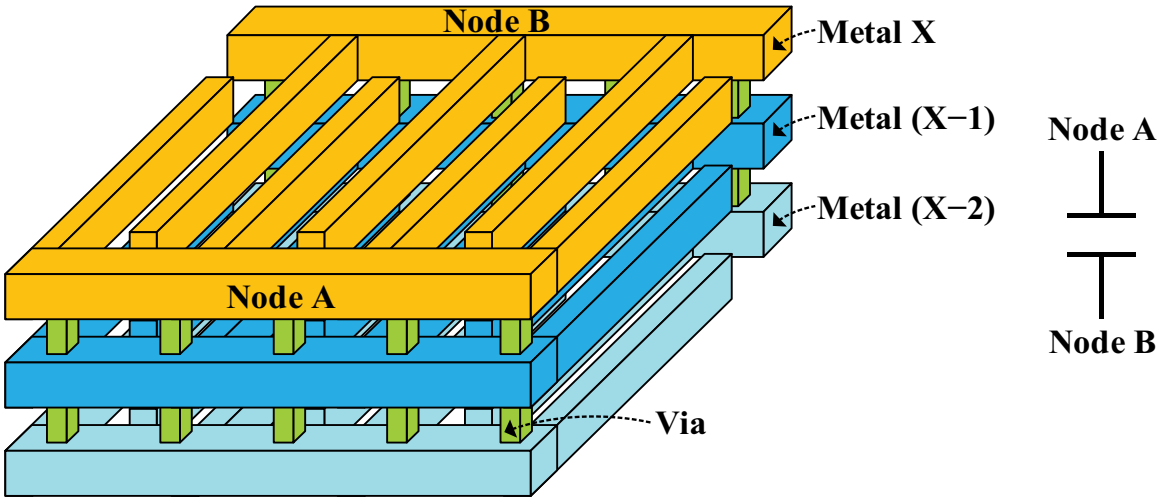
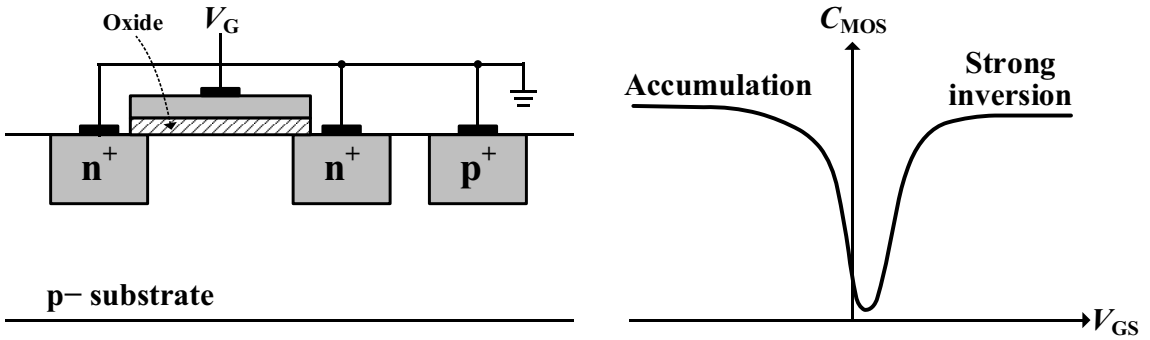


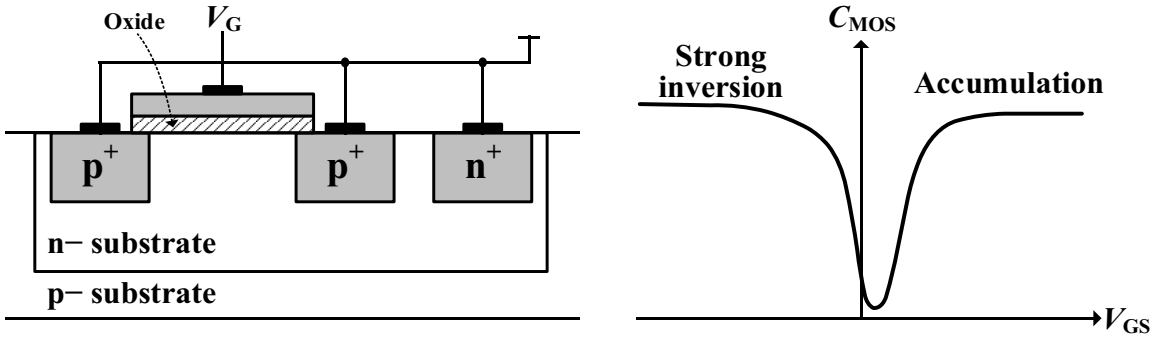
Figure 58. Structure of MOM capacitor

Metal-oxide-semiconductor (MOS) capacitor

MOS capacitor exploits the transistor's structure itself to configure the MOS capacitor. Figure 59(a) and (b) show the NMOS-based capacitor and PMOS-based capacitor, respectively. As shown, the gate oxide is used as a dielectric material. The gate and the connected source, drain, and body are used for the conductor, which locates at the upper and lower part of the oxide, respectively. In case of the NMOS-based MOS capacitor, when V_{GS} is large with a minus sign, the holes are accumulated at the channel and the MOS capacitor can provide a large capacitance, where it is called the accumulated region of the transistor. In the same manner, when V_{GS} is large with a plus sign, the electrons are clustered at the channel and the MOS capacitor can provide a large capacitance, where it is called as strong inversion region of the transistor. As shown in the graph of Figure 59(a) and (b), the MOS capacitor is sensitive to the bias voltage between the two conductors and it is not monotonous over the V_{GS}. Moreover, the MOS capacitor has a high non-linearity and the capacitance is not accurate compared with the MIM or MOM capacitors. In addition, if thin-ox transistors are used for the MOS capacitor, it has a high leakage current, meanwhile, the thin-ox-based MOS capacitor can provide higher density than others, such as approximately 10 fF/μm^2. This is because the oxide thickness is thinner compared to the MIM or MOM capacitors. Therefore, the MOS capacitor is useful only for non-critical applications, such as the miller compensation capacitor, bypass capacitor for supply and bias, etc.



(a)



(b)

Figure 59. Structure of MOS capacitors with their capacitance over a bias voltage, V_{GS},; (a) using NMOS transistor (b) using PMOS transistor

Based on the discussions about the three kinds of capacitors, the below table summarizes the characteristics of each capacitor in terms of capacitance density, quality, robustness to the bias voltage and the temperature (VT), cost, accuracy, and the leakage current. In summary, the circuit designers should use a proper capacitor among three kinds of capacitors based on each capacitor's characteristics and the targeted applications.

Table 11. Characteristics of each capacitors; MIM, MOM, and MOS capacitor

	MIM Capacitor	**MOM capacitor**	**MOS capacitor**
Density	Moderate (~2 fF/μm^2)	Low (~0.5 fF/μm^2)	High (~10 fF/μm^2)
Quality	Good	Good	Moderate
Robustness to VT	Good	Good	Bad
Cost	High	Low	Low
Accuracy	Good	Good	Bad
Leakage current	Good	Good	Bad

3.2 Design Considerations

In this session, several design points to be considered are detailed. First, to guarantee the oscillation of the VCO, the start-up condition will be dealt with. After that, topologies of the *LC* VCO will be investigated to provide guidelines for using the appropriate topology for each application. Finally, the operating region will be introduced.

3.2.1 Start-up Condition

The start-up condition of the *LC* VCO can be explained from two viewpoints. The first viewpoint is a "Barkhausen's criteria", which explains two conditions that a linear feedback system can start oscillation [28].

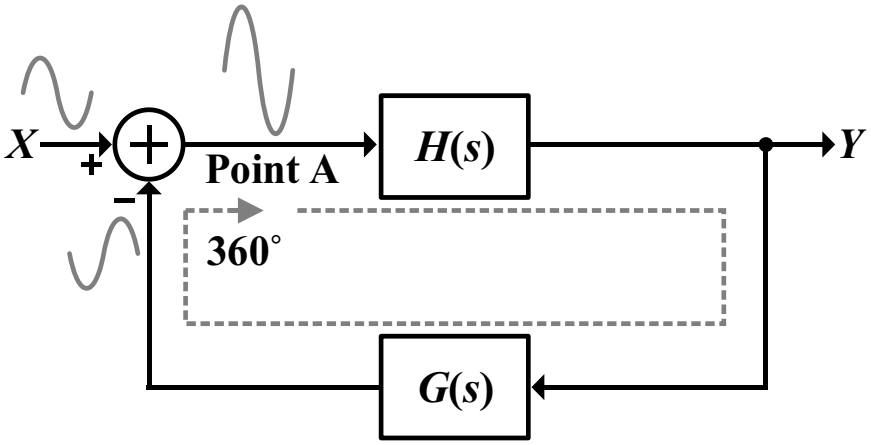


Figure 60. Feedback system with a feedforward gain of $H(s)$ and a feedback gain of $G(s)$

Figure 60 shows the linear feedback system having a feedforward gain of $H(s)$ and a feedback gain of $G(s)$. In this system, the Barkhausen's criteria can be expressed in mathematically as follows.

$$|H(s{=}j\omega_0) \cdot G(s{=}j\omega_0)| = 1 \tag{90}$$

$$\angle\big(H(s{=}j\omega_0) \cdot G(s{=}j\omega_0)\big) = -180° \tag{91}$$

where ω_0 is the oscillation frequency that satisfies the Barkhausen's criteria. As shown, when the loop gain is unity at ω_0 and the phase shift is -180°, the feedback system can start the oscillation. Here, the phase shift of -180° through $H(s)$ and $G(s)$ means that the total phase shift should be multiple of 2π, this is because there is a minus sign when the feedback signal goes to the input of the system. Then, as shown in Figure 60, the signal's amplitude can continue to increase. Note that the Barkhausen's criteria is not a sufficient condition but a necessary condition.

Then, now the Barkhausen's criteria can be applied to the *LC* VCO. Figure 61 shows how we can derive the start-up condition of *LC* VCOs through the Barkhausen's criteria. At the oscillation frequency, which is defined as

$$\omega_0 = \frac{1}{\sqrt{(L/2)\cdot 2C}} = \frac{1}{\sqrt{LC}}, \tag{92}$$

the parallel impedance of the inductor and the capacitor becomes infinite, thereby only the parallel resistor remains at the drain of the transistors, M_1 and M_2. Thus, at ω_0, each transistor with the resistor as a load impedance, $R_P/2$, behaves like a common source amplifier. Each common source (CS) amplifier (M_1 and $R_P/2$, and M_2 and $R_P/2$) contributes phase shift of -180° with the gain of $-g_m \cdot R_P/2$. This means that the phase condition of the Barkhausen's criteria can be satisfied since when the signal moves from node *X* to node *Y* and from node *Y* to node *X*, the phase shift is -360° through the two CS amplifiers. Then, the only remain condition is the open loop gain. If the loop gain of the *LC* VCO is greater than one or equal to one, the VCO can start to oscillate by the Barkhausen's criteria.

$$\left(\frac{g_m \cdot R_P}{2}\right)^2 \geq 1. \tag{93}$$

Equation (93) can be reconfigured as below. From Equation (94), it is clear to ensure the start-up of the *LC* VCO, we need large R_P, i.e., an inductor with high Q-factor, and large transconductance of the transistor.

$$R_P \geq \frac{2}{g_m}. \tag{94}$$

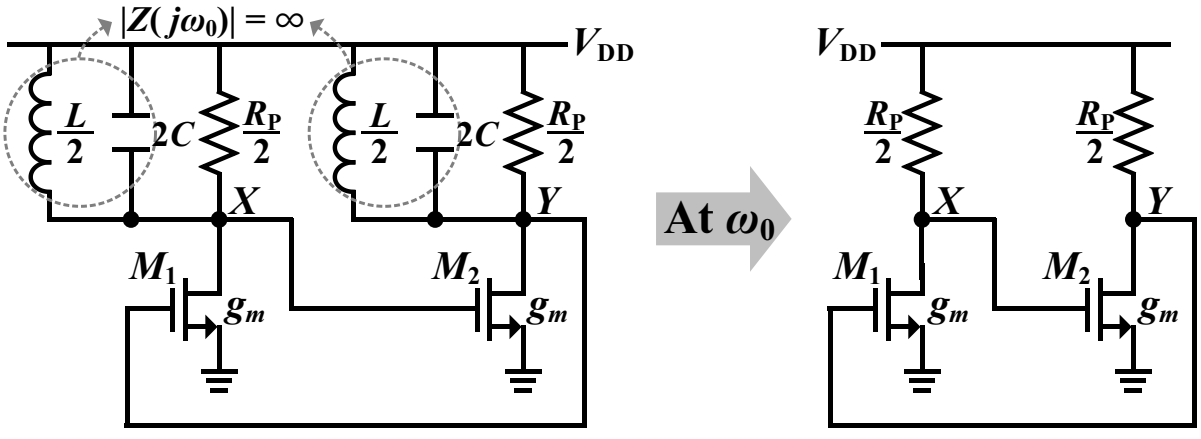
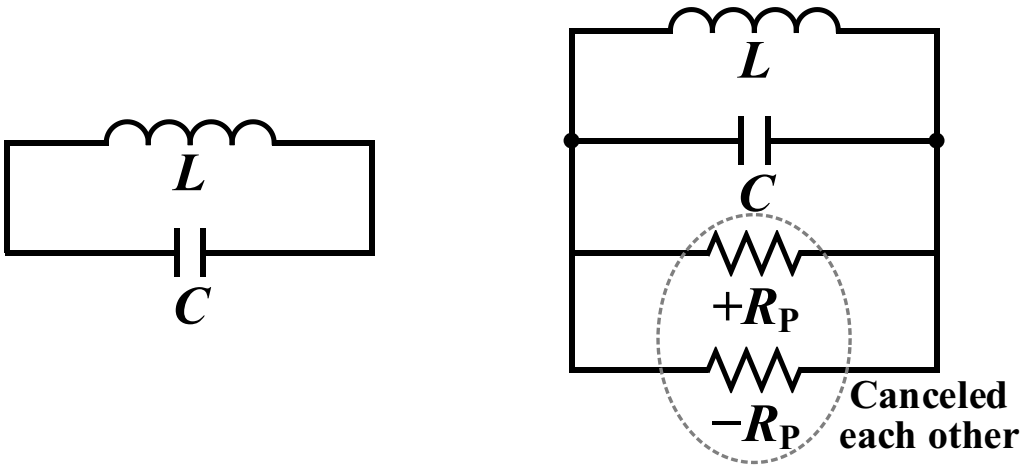


Figure 61. *LC* VCO when the Barkhausen's criteria is applied

As mentioned, there are two approaches to estimate the start-up condition of an *LC* VCO. Using a second viewpoint, the same result from the Barkhausen's criteria can be derived. Before going into further, let's revisit the *LC* tank as shown in Figure 62.



(a) (b)

Figure 62. (a) Ideal *LC* tank (b) usage of negative impedance to make a noisy tank similar to an ideal tank

As common sense, if there is a parallel connection of an ideal inductor and an ideal capacitor as shown in Figure 62(a), the *LC* tank can oscillate at its natural frequency infinitely since there are no noisy components which dissipate the energy. However, in the real *LC* tank, there is a noisy component, which is modeled as R_P in Figure 62(b). Then what if a resistor having the same magnitude with R_P but with opposite sign is connected to the *LC* tank in parallel? As shown in Figure 62(b), $+R_P$ and $-R_P$ are canceled each other, and the real *LC* tank can sustain the oscillation similar to the ideal *LC* tank.

By applying the concept that explained along with Figure 62, the start-up condition of the *LC* VCO can be investigated with Figure 63. As explained above, at the frequency of ω_0, $Z_{TANK}(s=j\omega_0)$ is reduced to R_P. The impedance seen by the cross-coupled transistor pair, Z_{TR}, is generally known as $-g_m/2$ [28], which is easy to calculate with the small signal analysis. Therefore, if Z_{TR} can cancel the energy dissipation part of the *LC* tank, the VCO can start to oscillate and maintain the oscillation since the energy loss by the R_P is compensated by the cross-coupled transistor pair. The impedance cancellation between $Z_{TANK}(s=j\omega_0)$ and Z_{TR} can be mathematically expressed as

$$Z_{TANK}(s=j\omega_0)||Z_{TR} \le 0 \tag{95}$$

$$\Rightarrow R_P||\left(-2/g_m\right) \le 0 \tag{96}$$

$$\Rightarrow R_P \geq \frac{2}{g_m} \tag{97}$$

As shown, the start-up condition, derived from the Barkhausen's criteria (Equation (94)), and the condition, derived from the one-port view (Equation (97)), show the same result. Both results imply that if the value of R_P is large, the value of g_m can be small. It means that if the LC tank has a small loss, the energy to be compensated by the g_m is also small.

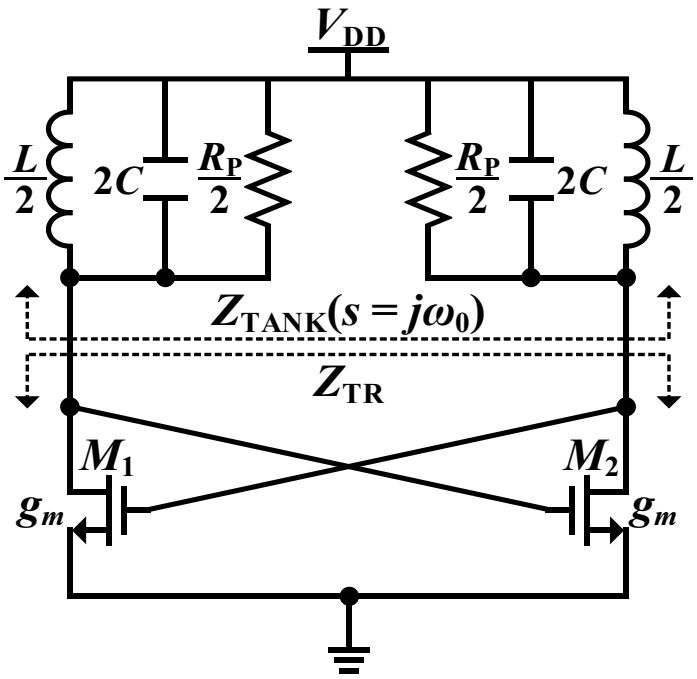


Figure 63. An LC VCO for analyzing the start-up condition by the one-port view

3.2.2 Topologies of *LC* VCO

To improve the performance of the *LC* VCO in terms of phase noise and power efficiency, a lot of research has been made and new structures are proposed [36] − [40]. However, in this subChapter, we will focus on the most basic two topologies of the *LC* VCO, which is the most widely used configuration; NMOS-type cross-coupled VCO and CMOS-type cross-coupled VCO.

NMOS-type cross-coupled *LC* VCO

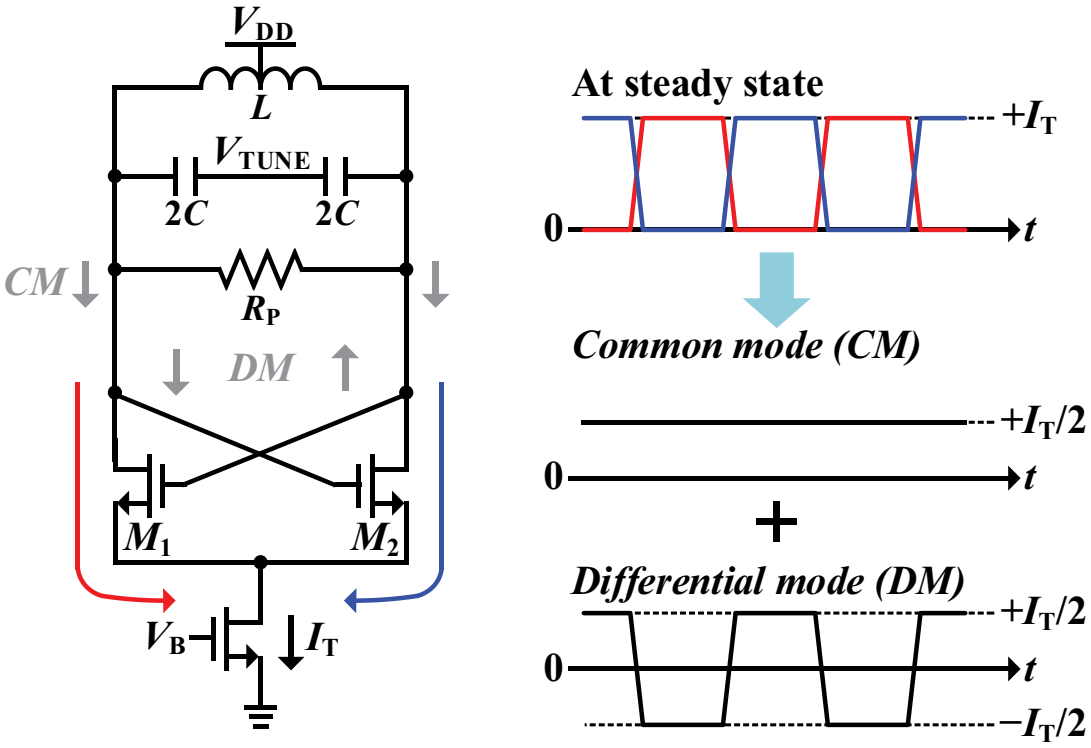


Figure 64. Architecture of the NMOS-type cross-coupled *LC* VCO with current waveform in steady state

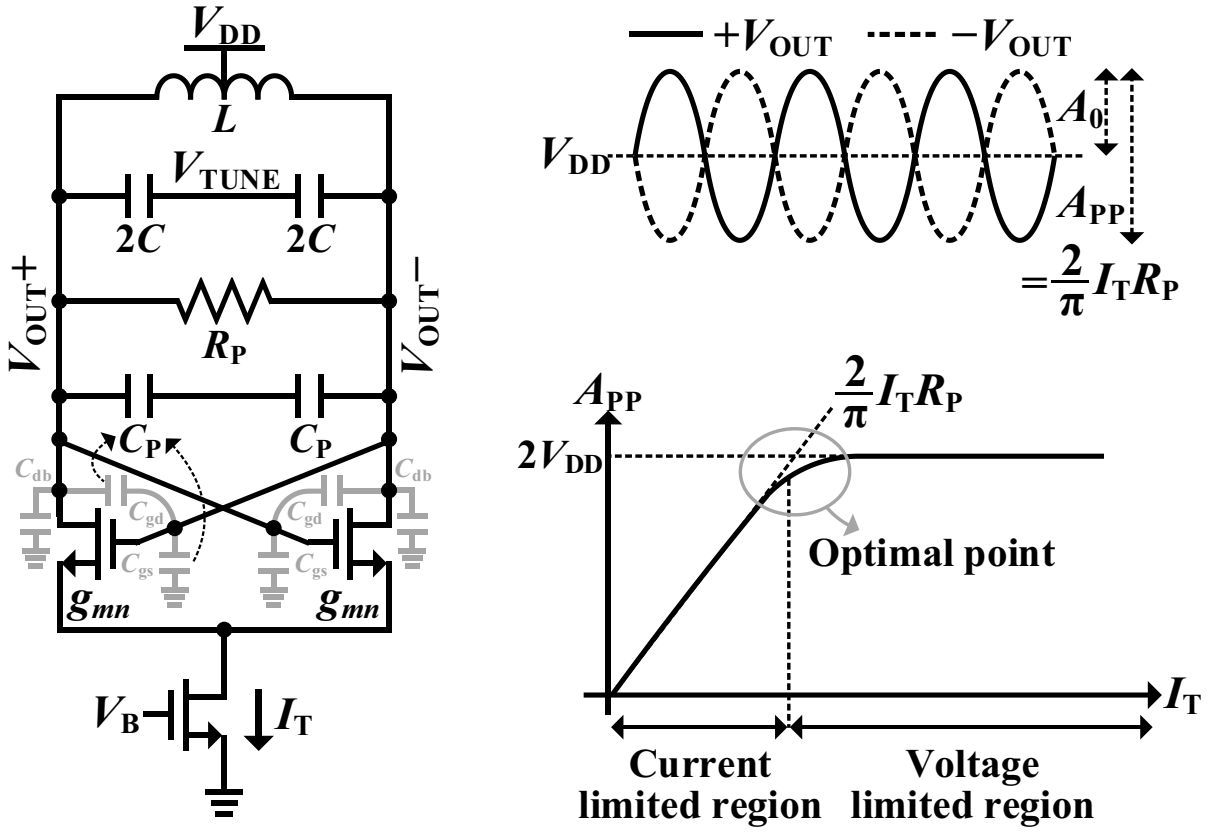
Figure 64 shows the basic structure of the NMOS-type cross-coupled *LC* VCO, which consists of an *LC* tank, two NMOS transistors, and a transistor for a tail current. As shown, when the VCO reaches the steady-state, the tail current, I_T, will be steered on one side and on the other side at the resonance frequency. Note that both transistors operate essentially in class-B since they are off for half of the period and on for the remaining half period. The current at the steady state can be decomposed into the common mode current and the differential mode current as shown in Figure 64. Except for the common mode current, when only the differential mode current is considered to be injected to the *LC* tank at the resonance frequency of the *LC* VCO, and from here, the amplitude of the VCO output signal can be found. If the differential mode current is decomposed by using the Fourier Series, the current can be expressed as

$$\frac{2}{\pi}\cdot I_{\mathrm{T}}\sum_{k=1,3,5,\ldots}^{\infty}\frac{1}{k}\sin(k\cdot 2\pi f) \tag{98}$$

Since the *LC* tank rejects the harmonics, only the fundamental tone can be injected to the *LC* tank and the current makes the swing of the VCO with the parallel resistor, R_{P}. Thus, each single-ended output of the VCO, $V_{\mathrm{OUT}}+$ and $V_{\mathrm{OUT}}-$, can be represented as shown below, with the halved R_{P} for each single-ended output.

$$V_{\mathrm{OUT}}+(\text{or } V_{\mathrm{OUT}}-)=\frac{R_{\mathrm{P}}}{2}\cdot\frac{2}{\pi}\cdot I_{\mathrm{T}}\cdot\sin(2\pi f)=A_0\sin(2\pi f) \tag{99}$$

where A_0 is the amplitude with the value of $R_{\mathrm{P}}\cdot I_{\mathrm{T}}/\pi$ and the peak-to-peak swing, A_{PP}, is $2\cdot R_{\mathrm{P}}\cdot I_{\mathrm{T}}/\pi$, as shown in the swing of the VCO in Figure 65(b). Since the swing of the VCO depends on the tail current, the most straightforward way to increase the swing is to increase the tail current. The swing cannot be controlled by changing R_{P} since it is usually determined by the integrated inductor of the *LC* tank.



(a) (b)

Figure 65. (a) VCO with parasitic capacitors (b) swing of the VCO according to the tail current

Figure 65(b) shows what could be the maximum swing of the *LC* VCO. Before the peak-to-peak swing reaches to $2V_{DD}$, the swing of the VCO increases along with the increase of the tail current. This region is called a current limited region since the maximum swing is limited by the current. However, when the peak-to-peak is close to $2V_{DD}$, the swing does not increase even if the bias current is further increased. This region is called a voltage limited region since in this region the only way to increase the swing is to increase the supply voltage. Generally, it is known that the optimal bias point for the tail current is at the edge of the current limited region. At the optimal bias point, we can have the best phase noise since when the swing is increased the phase noise is also improved at the expense of the power. However, after the optimal bias point, there is no more improvement of the phase noise and only the power is wasted.

Figure 65(a) shows the parasitic capacitors of the NMOS-type cross-coupled *LC* VCO. Here, for simplicity, only C_{gs}, C_{gd}, and C_{db} are considered. Then, the effect of the C_{gs}, C_{gd}, and C_{db} can be modeled as C_P, which can be calculated as

$$C_P = C_{gs} + C_{db} + 4C_{gd} \tag{100}$$

Therefore, when the parasitic capacitance is reflected, the oscillation frequency will be

$$\omega_0 = \frac{1}{\sqrt{L(C+C_P/2)}}, \tag{101}$$

CMOS-type cross-coupled *LC* VCO

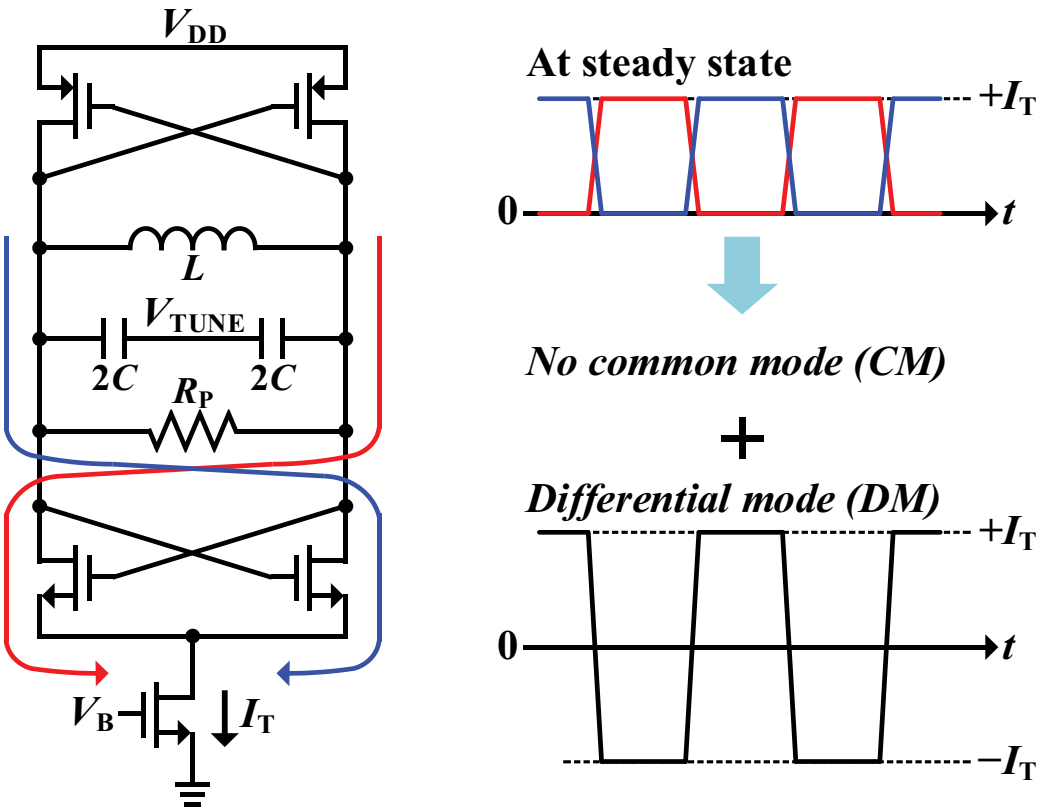


Figure 66. Architecture of the CMOS-type cross-coupled *LC* VCO with current waveform in steady state

Figure 66 shows the basic structure of the CMOS-type cross-coupled *LC* VCO, which consists of an *LC* tank, two NMOS transistors, two PMOS transistors, and a transistor for a tail current. Note that for a fair comparison with the NMOS-type cross-coupled *LC* VCO, the *LC* tank, the tail current, and the supply are the same. In addition, in the CMOS-type architecture, all transistors operate in class-B, i.e., for the half period left bottom NMOS and right top PMOS are on and others are off. For the remaining half period, right bottom NMOS and left top PMOS are on and others are off. When the VCO reaches the steady-state, the tail current, I_T, will be steered alternately in the direction denoted in red and then steered in the direction denoted in blue at the resonance frequency. Note that the steered current already flows differentially through the *LC* tank, which means that it only has differential mode current and there is no common mode current as shown in Figure 66. Therefore, different from the NMOS-type VCO, the amplitude of the differential mode current is twice in amplitude. In the same manner, when only the differential mode current is considered along with the *LC* tank, the amplitude of the VCO output signal can be found. If the differential mode current is decomposed by using the Fourier Series, the current can be expressed as

$$\frac{4}{\pi}\cdot I_{\mathrm{T}}\sum_{k=1,3,5,\ldots}^{\infty}\frac{1}{k}\sin(k\cdot 2\pi f) \tag{102}$$

Following to the same mechanism in the NMOS-type VCO, each single-ended output of the VCO, $V_{\mathrm{OUT}}+$ and $V_{\mathrm{OUT}}-$, can be represented as shown below, with the halved R_{P} for each single-ended output.

$$V_{\mathrm{OUT}}+(\text{or } V_{\mathrm{OUT}}-) = \frac{R_{\mathrm{P}}}{2}\cdot\frac{4}{\pi}\cdot I_{\mathrm{T}}\cdot\sin(2\pi f) = A_0\sin(2\pi f) \tag{103}$$

where A_0 is the amplitude with the value of $2\cdot R_{\mathrm{P}}\cdot I_{\mathrm{T}}/\pi$ and the peak-to-peak swing, A_{PP}, is $4\cdot R_{\mathrm{P}}\cdot I_{\mathrm{T}}/\pi$, as shown in the swing of the VCO in Figure 67(b). Since the swing of the VCO depends on the tail current, the most straightforward way to increase the swing is to increase the tail current, the same mechanism as did in the NMOS-type cross-coupled *LC* VCO.

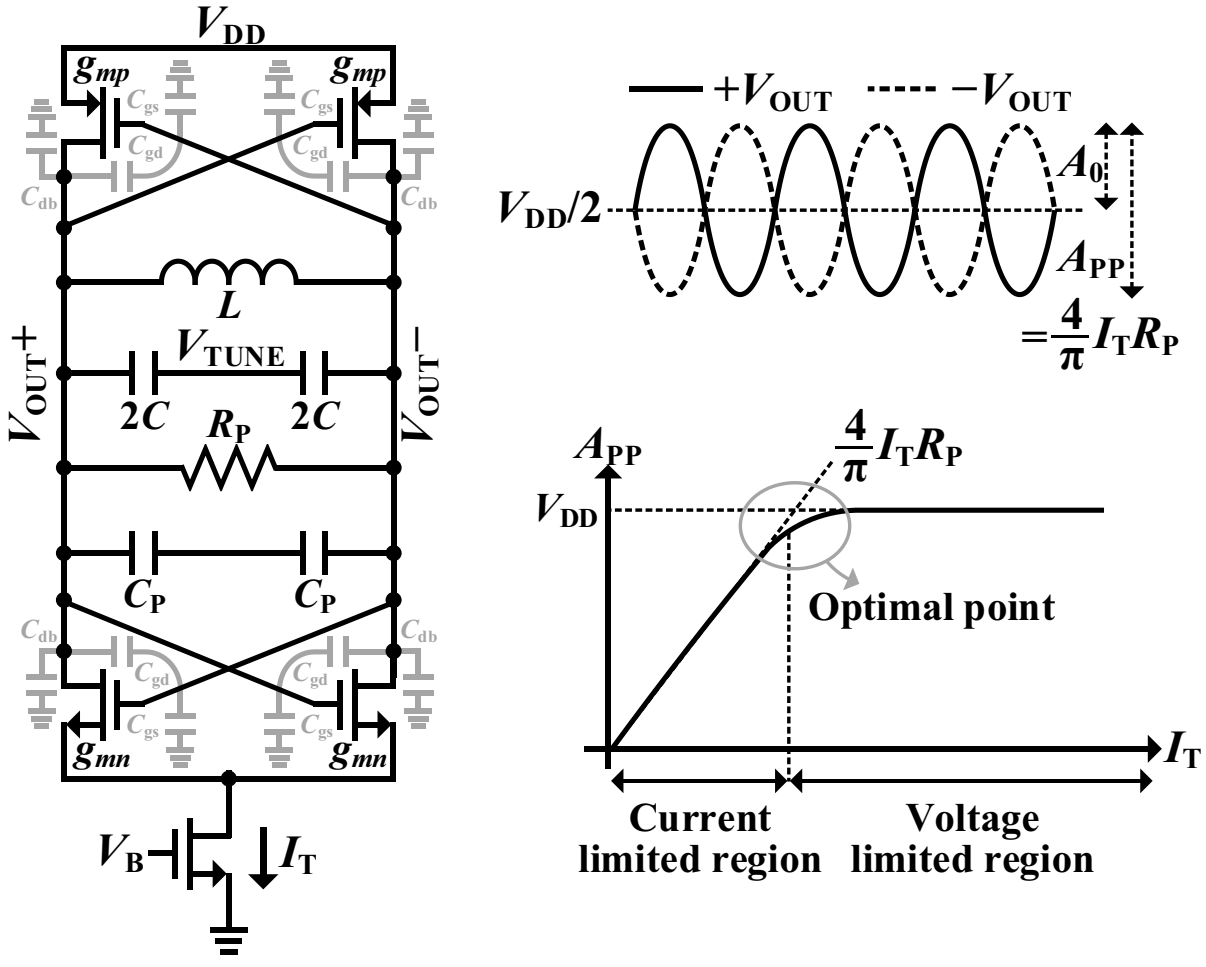


Figure 67. (a) VCO with parasitic capacitors (b) swing of the VCO according to the tail current

Figure 67(b) shows what could be the maximum swing of the *LC* VCO. Before the peak-to-peak swing reaches to V_{DD}, the swing of the VCO increases according to the tail current. This is the current limited region in the CMOS-type cross-couple *LC* VCO. However, when the peak-to-peak is close to V_{DD}, the swing does not increase even if the bias current is raised more. This region is the voltage limited region. For the CMOS-type cross-coupled *LC* VCO, the optimal bias point for the tail current is at the edge of the current limited region.

Figure 67(a) shows the parasitic capacitors of the CMOS-type cross-coupled *LC* VCO. Here, for simplicity, only C_{gs}, C_{gd}, and C_{db} are considered and assume that the parasitic capacitors of the NMOS transistor and the PMOS transistor are the same. Then, the effect of the C_{gs}, C_{gd}, and C_{db} can be modeled as C_P, which can be calculated as

$$C_P = 2\left(C_{gs} + C_{db} + 4C_{gd}\right) \tag{104}$$

Comparison between NMOS-type and CMOS-type cross-coupled *LC* VCO

Previously, each type of *LC* VCO was investigated in terms of maximum swing, parasitic capacitance when the *LC* tank, the supply voltage, and the tail current are same. Based on the observation, the phase noise and the FOM_{VCO} can be compared as shown in Figure 68 [41], [42].

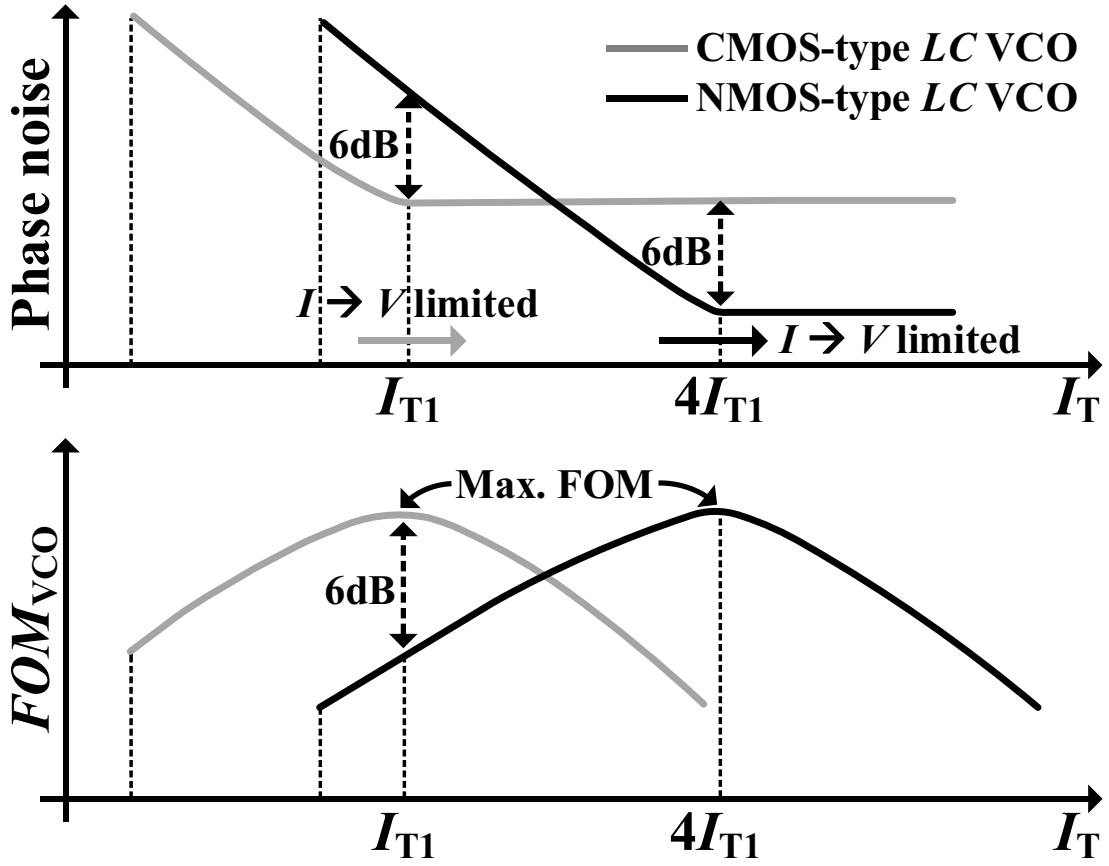


Figure 68. Comparison between NMOS-type and CMOS-type cross-coupled *LC* VCO in terms of phase noise and FOM_{VCO}

As shown, CMOS-type *LC* VCO saturates much earlier than the NMOS-type *LC* VCO by 4 times in terms of the tail current. This is because the maximum swing of the CMOS-type is half that of the NMOS-type, and the current injected into the *LC* tank is doubled in the CMOS-type VCO when the tail current is same for both types of VCOs. Intuitively, the NMOS-type *LC* VCO can achieve lower phase noise by 6 dB since the NMOS-type can make twice larger swing than the CMOS-type VCO, i.e., 20log(2) = 6 dB. However, the maximum achievable FOM_{VCO} is same for both architecture since the NMOS-type spends more power than the CMOS-type VCO, i.e., power efficiency is twice better for the CMOS-type VCO. Therefore, what type of VCO to use will be determined by which application where the VCO will be used. For example, if the target application requires low-power consumption, CMOS-type *LC* VCO can be a better choice, since, up to some point of the tail current, CMOS-type

VCO can provide better phase noise with low-power consumption than the NMOS-type VCO. If the target application requires low phase noise performance, NMOS-type VCO is the better choice since the NMOS-type VCO can provide better phase noise performance at the expense of the power consumption. In addition, since the CMOS-type *LC* VCO provides doubled transconductance by the NMOS and PMOS transistors, the CMOS-type is approximately twice more advantageous for the start-up condition. However, the CMOS-type has more parasitic capacitance and noise sources.

In summary, the characteristics of the NMOS-type and the CMOS-type *LC* VCO are summarized in the below Table 12.

Table 12. Comparison between NMOS-type and CMOS-type *LC* VCO

	NMOS-type	**CMOS-type**
Negative impedance by the cross-coupled transistor	$-2/g_{mn}$	$-2/(g_{mn}+ g_{mp})$
Parasitic capacitance	$C_{gs}+C_{db}+4C_{gd}$	$2(C_{gs}+C_{db}+4C_{gd})$
Peak-to-peak voltage swing	$2/\pi\cdot(R_P\cdot I_T)$	$4/\pi\cdot(R_P\cdot I_T)$

3.3 Phase Noise

In this subsession, two basic theories regarding the phase noise model of *LC* VCOs are briefly introduced. The first one is the well-known Lesson's equation and the second one is an impulse-sensitive function (ISF).

3.3.1 Linear-Time Invariant Model: Lesson's equation

The Lesson's equation is one of the famous one tried to predict the phase noise of *LC* VCOs [32]. However, the Lesson's equation assumes two things; 1. the VCO is a linear system, 2. the only noise source is an *LC* tank. Even though the two assumptions cannot be applicable in real VCO, still the equation can predict the overall tendency of the phase noise in *LC* VCOs. The below shows the derivation of the Lesson's equation.

First, the LC tank impedance at the offset frequency of $\Delta\omega$ can be written as

$$|Z_{\mathrm{TANK}}(\omega_0+\Delta\omega)| = \frac{j(\omega_0+\Delta\omega)L}{1-(\omega_0+\Delta\omega)^2LC} \tag{105}$$

where ω_0 is the resonance frequency of the *LC* tank and Equation (105) can be approximated as below

$$Z_{\mathrm{TANK}}(\omega+\Delta\omega) \approx j\cdot\frac{\omega_0 L}{2\left(\frac{\Delta\omega}{\omega_0}\right)} \tag{106}$$

Since the Q-factor of the *LC* tank is $R_{\mathrm{P}}/(\omega_0 L)$, using Equation (106) can be rewritten as

$$|Z_{\mathrm{TANK}}(\omega+\Delta\omega)| \approx R_{\mathrm{P}}\cdot\frac{\omega_0}{2Q\Delta\omega} \tag{107}$$

In the Lesson's equation, the only noise source is from the *LC* tank, which is the current noise of the parallel resistor of R_{P} as follows.

$$\frac{\overline{i_n^{\,2}}}{\Delta f} = \frac{4kT}{R_{\mathrm{P}}} \tag{108}$$

Then, when this current noise is injected to the *LC* tank, the voltage noise at the offset frequency of $\Delta\omega$ can be calculated by multiplying the Equation (107) and (108), as follows.

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z_{\mathrm{TANK}}(\omega+\Delta\omega)|^2 = \frac{4kT}{R_{\mathrm{P}}} \cdot \left(R_{\mathrm{P}} \cdot \frac{\omega_0}{2Q\Delta\omega}\right)^2 = 4kTR_{\mathrm{P}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{109}$$

When the Equation (109) is divided by the signal power, P_{sig}, the phase noise can be calculated as follows and that is the Lesson's equation.

$$L(\Delta\omega) = 10\log_{10}\left[\frac{2kT}{P_{\mathrm{sig}}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{110}$$

Note that in the above equation, different from the Equation (109), the $4kT$ term is changed to $2kT$ in Equation (110), because approximately half of the noise is attributed to the phase noise and the remaining half of the noise is amplitude noise, which is rejected by the limiting mechanism of the *LC* VCOs. However, the Lesson's equation cannot predict the flicker noise part, which shows the slope of −30 dB/dec at the low offset frequencies, the Lesson's equation was improved to include a $1/f^3$ region along with a flat region in the phase noise as shown below.

$$L(\Delta\omega) = 10\log_{10}\left[\frac{2kT}{P_{\mathrm{sig}}} \cdot \left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \cdot \left(1+\left(\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right)\right] \tag{111}$$

where $\Delta\omega_{1/f3}$ is a corner frequency of flicker noise. The Lesson's equation indicates that the key factors to improve phase noise are the high Q-factor of the *LC* tank and the signal power. Intuitively both are reasonable since if the Q-factor is high, it means that the better frequency selection mechanism of the *LC* tank. In addition, when the signal power is high, it means the improved signal-to-noise ratio (SNR).

3.3.2 Linear-Time Variant Model: Impulse-Sensitive Function

As an improved model for prediction of phase noise in *LC* VCOs, Hajimiri presented an impulse sensitive function, which is a linear time variant (LTV) model [43]. In this model, we assume that there is a current noise source expressed as an impulse and that current noise is injected to the *LC* tank, as shown in Figure 69. In this figure, the current noise source is represented as $I_n(t)$ and the noise changes according to the time.

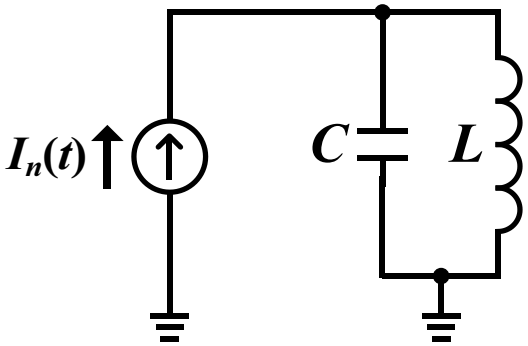


Figure 69. Simplified model for ISF theory with current noise source

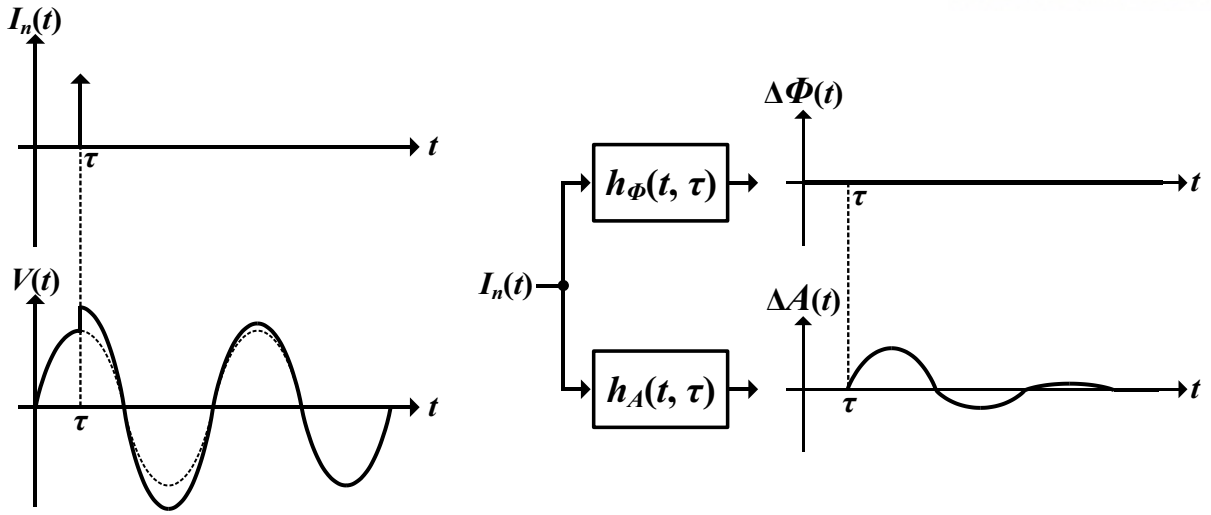
Then, when the current noise is injected to the *LC* tank, the *LC* tank responses as a distorted amplitude and an excess phase, which are represented as $A(t)$ and $\Phi(t)$, respectively, as shown in the below equation.

$$V(t)=A(t)\cdot\sin(2\pi f_0 t+\Phi(t)) \tag{112}$$

Since the impulse of current noise is composed of high-frequency components, all the current noise will inject into the capacitor by dumping a charge Δq onto the capacitor. This is because meanwhile the inductor is regarded as an open circuit, the capacitor is considered as short circuits. Therefore, the instantaneous change in the voltage can be given by

$$\Delta V=\frac{\Delta q}{C_{\text{Total}}} \tag{113}$$

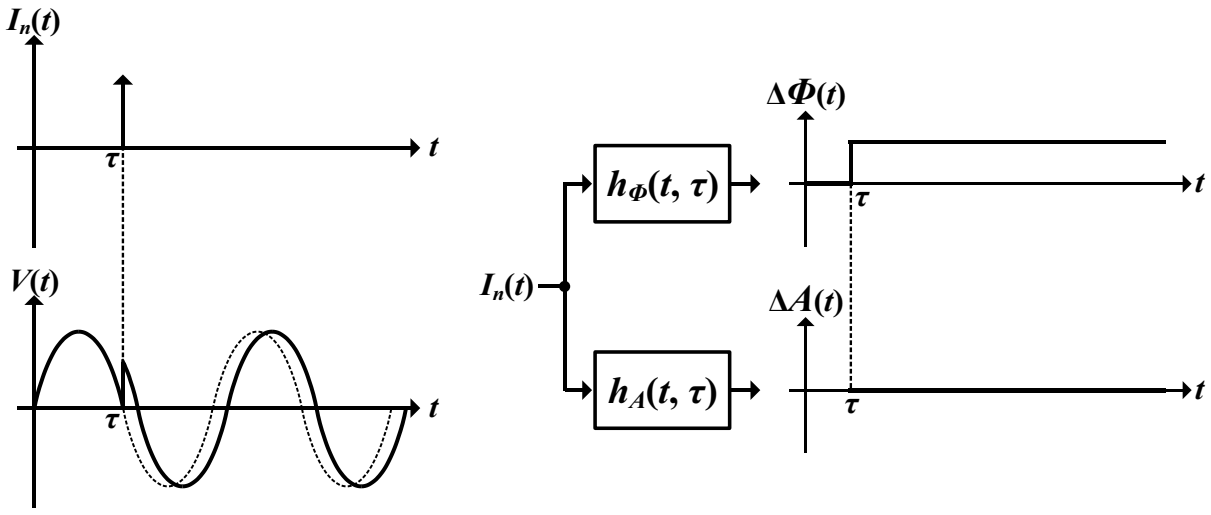
where C_{Total} and Δq are the capacitor seen by the current noise source and the injected charge to the C_{Total} by the current noise, respectively. The effect of ΔV on the phase of the *LC* VCO is different according to the time that the current noise is injected, $\boldsymbol{\tau}$, and the reason is intuitively shown in Figure 70(a) and (b)



(a) (b)

Figure 70. (a) Impulse response of the output signal of *LC* VCOs when the impulse is happened at the peak of the output signal. (b) Impulse response results of (a) in terms of the amplitude and the phase

As shown in Figure 70(a), if the current noise is injected when the VCO output signal is the peak, the noise only changes the amplitude of the output signal and the phase is not distorted. Therefore, the results of the impulse response can be divided into the amplitude variations and the phase variations as shown in Figure 70(b). In this case, there is no phase distortion and only the amplitude is changed. However, as time goes by, the amplitude variation reaches to zero, since the VCO follows the trajectory, which is called a limit cycle.



(a) (b)

Figure 71. (a) Impulse response of the output signal of *LC* VCOs when the impulse is happened at the zero-crossing point of the output signal. (b) Impulse response results of (a) in terms of the amplitude and the phase

However, as shown in Figure 71(a), if the current noise is injected at the zero-crossing point of the VCO output signal, the noise deviates the phase of the output signal from the ideal position whereas the amplitude is not distorted. Therefore, as shown in Figure 71(b), In this case, there is no amplitude distortion and only the phase is changed. Unfortunately, in case of the phase distortion, it cannot be recovered whereas the amplitude variation can recover it by the limit cycle. Thus, as shown in Figure 71(b), the distorted phase deviation remains.

The key observation from the previous two cases is that the *sensitivity* of the VCO to the current noise injection is a periodic function of time. In one period, there are points having zero the sensitivity and points showing peak sensitivity. In addition, the phase distortion is a linear function of the current noise injection. Therefore, this model is regarded as a kind of linear time-variant system. In addition, the impulse response for the phase distortion can be written as

$$h_{\Phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\mathrm{Max}}} u(t-\tau) \tag{114}$$

where q_{Max} and $u(t-\tau)$ are C_{Total} multiplied by the peak voltage of the VCO signal for the normalization and the unit step function at the time of τ, respectively. Here, the function $\Gamma(\omega_0\tau)$ is the Impulse Sensitivity Function (ISF), which is a periodic function in time and captures the nature of the time variant of the oscillation systems.

As an example of the ISF, when there is a perfect sine wave as shown in Figure 72, the ISF is a kind of cos wave. Note that the ISF has the same period as $V(t)$.

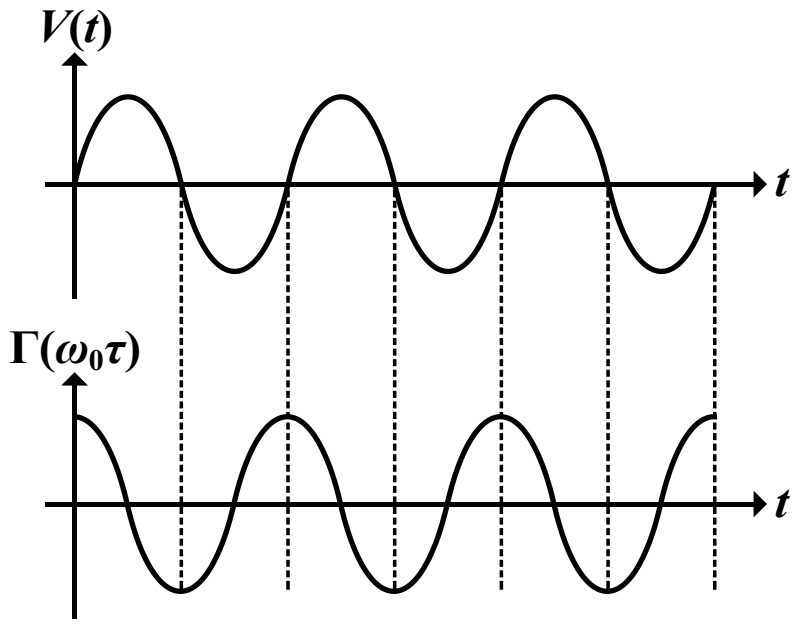
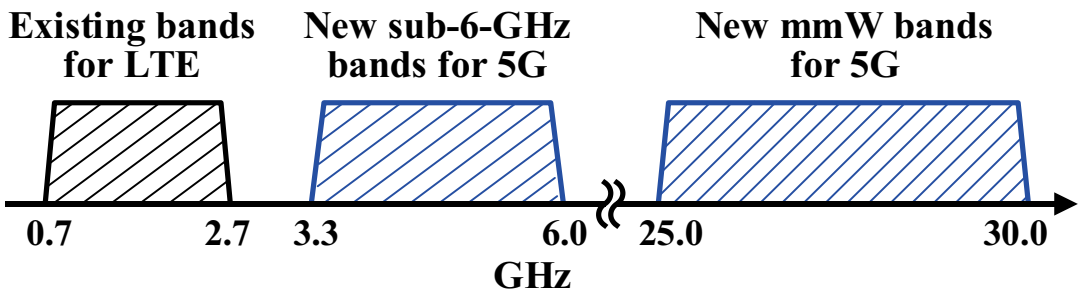


Figure 72. Impulse sensitivity function of a sine wave

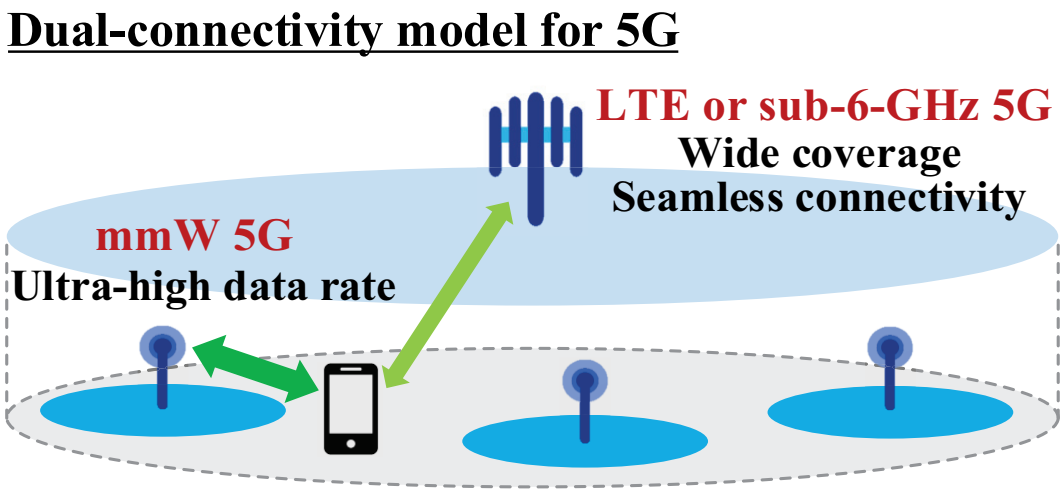
4. Design of Low Phase Noise Frequency Synthesizers for 5G

4.1 Objective and Motivation

For the past several decades, mobile communication systems have evolved gradually from 2G to 4G to satisfy the increasing demand of users for high data rates. Recently, the demand for ultra-fast mobile communications has become unprecedentedly strong due to the emergence of new technologies that require high data throughput, such as virtual reality (VR), augmented reality (AR), and massive Internet of Things (IoT). As the next generation mobile system to satisfy this demand, 5G mobile communications attract a lot of attention, and they are targeted to support data rates greater than 10 Gb/s. To achieve such high data rates, it is important to use high-order modulations, such as 64 or 256 QAM [2], [44]. Thus, one of the most challenging tasks to design wireless transceivers for 5G systems is the generation of millimeter-wave (mmW)-band local oscillation (LO) signals having an ultra-low integrated phase noise (IPN) over a wide integration range, i.e., bandwidth. As an example, to meet the error-vector magnitude (EVM) requirements of 64 QAM, an LO signal must have the IPN less than −30 dBc [3], [4].



(a)



(b)

Figure 73. (a) Frequency spectrum of existing bands and new bands for 5G; (b) dual connectivity; one of the promising models of 5G systems

In Figure 73(a), frequency spectrum is shown, which are required by cellular systems, including existing bands for 4G long-term evolution (LTE) from around 700 MHz to 2.7 GHz [5], [7] and new frequency bands for 5G systems, including bands below 6 GHz and mmW bands. During the evolution of mobile communications, the key principle of the industry has been to operate with past standards and spectrums, which is called as backward compatibility or an interoperability. Based on this principle, mobile devices with backward compatibility easily can enter the markets of different countries, where the transition of networks to newer access technologies is still ongoing. This trend is expected to continue for 5G systems. In addition, to overcome the limited coverage of mmW signals and improve the robustness of communications even in non-line-of-sight (NLOS) environments, a realistic model of 5G systems is the dual-connectivity between LTE (or sub-6-GHz 5G) and mmW-band 5G, as shown in Figure 73(b). In this model, which is based on the concept of small cells [8], [9], LTE (or sub-6-GHz 5G) using spectrum below 6 GHz will evolve in a way that it provides wide coverage and seamless connectivity, while mmW-band 5G enables ultra-high-bandwidth communications [9]. Therefore, considering the interoperability with existing standards and the dual connectivity of the practical 5G model, it is important for 5G transceivers to support multiple frequency bands in an efficient manner.

Recently, many researches have been to develop phase-locked loops (PLLs) that directly synthesize signals in mmW bands [10]−[16]. However, those architectures have several intrinsic problems. First, they cannot achieve a very low IPN. Lastest PLL's phase noise is plotted and summarized in [17] by normalizing the values of the phase noises to the same frequency. According to the survey, PLLs that generate mmW signals directly have much inferior performances of phase noise than PLLs that generate relatively low output frequencies, such as 3 – 5 GHz. The main reason of this trend is the decrease in the quality factor (Q-factor) of the *LC* tank of voltage-controlled oscillators (VCOs), which occurs at high frequencies, such as in the mmW-band [18], [19]. The second problem of the direct mmW PLLs is their limited frequency-tuning range. Since the portion of the parasitic capacitance in the *LC* tank increases for the same resonance frequency, the VCOs that generate mmW signals cannot obtain a wide frequency-tuning range [20]. Third, when PLLs are required to generate LO signals for the lower frequency bands below 6 GHz, they must divide the output frequencies again, necessitating additional circuits and power.

Another possible way for the generation of an mmW-band LO signal is to generate an output frequency in the GHz-range, i.e., around 4 GHz, from a PLL and then increase the frequency to higher bands by a frequency multiplier having low noise. In the frequency range of 3 − 5 GHz, the tank of *LC* VCOs can have a higher Q-factor and a lower portion of parasitic capacitance. Thus, a GHz-range PLL can have better performances in terms of phase noise and frequency-tuning range. In addition, in this architecture, low-frequency bands can be generated naturally by the PLL without the use of additional circuits and power. Thus, if we want to achieve low phase noise, a wide frequency-tuning range, and low power consumption simultaneously, it is obvious that the latter architecture is a much better choice

for generating LO signals for 5G transceivers.

In this proposed work, an LO generator was designed, which can provide ultra-low IPN signals in multiple frequency bands, i.e., mmW bands and bands below 6 GHz. Based on the second approach above, the proposed LO generator uses a combination of a high figure-of-merit (FOM) GHz-range PLL and low phase-noise injection-locked frequency multipliers (ILFMs) [21]. To further reduce the IPN, we also propose an ultra-low phase noise reference-frequency doubler (RFD). The proposed RFD increases the reference frequency, which suppresses the level of the in-band phase noise and the delta-sigma-modulator (DSM) noise of the PLL. Consequently, the LO signal at 28 GHz from the proposed LO generator can achieve an ultra-low IPN that can satisfy the requirements of 5G systems.

The rest of this paper is organized as follows. Chapter 4.2 introduces the overall architecture of the proposed LO generator. Chapter 4.3 presents design considerations and the implementation of the proposed RFD. Chapter 4.4 and 4.5 present the designs of the cascaded GHz-PLL and ILFMs, respectively. The experimental results are presented in Chapter 4.6, and conclusions are presented in Chapter 4.7.

4.2 Overall Architecture of the Proposed LO Generator

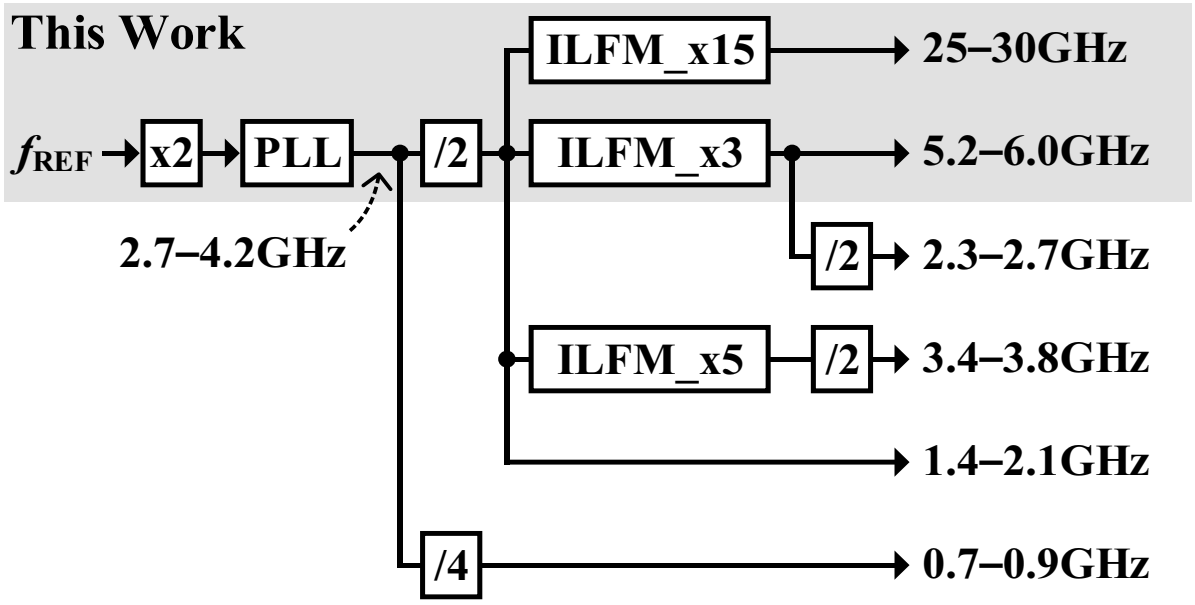


Figure 74. The proposed LO plan for 5G, using a reference-frequency doubler (RFD), a fractional-*N* PLL, and ILFMs

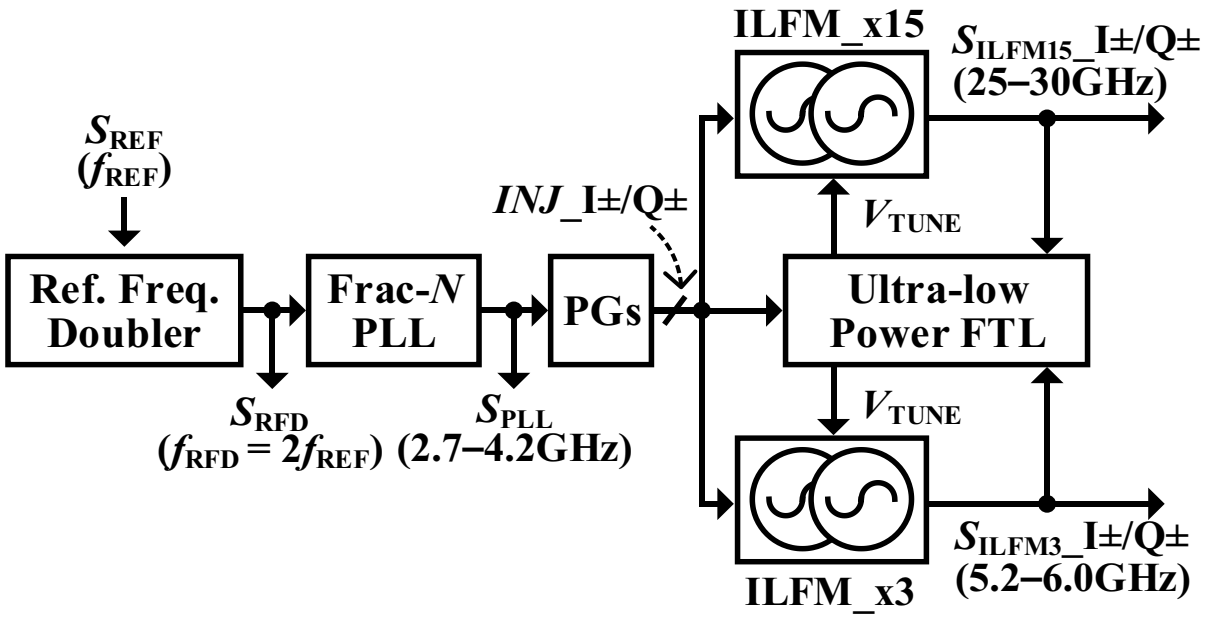


Figure 75. The proposed LO generator's overall architecture with the proposed frequency plan

Figure 74 shows the proposed LO plan that can concurrently support existing bands and new mmW bands. A fractional-*N* PLL in cooperation with a low-noise RFD and a VCO having a high Q-fractor generates ultra-low phase-noise signals in the GHz range. After that, ILFMs increase these frequencies

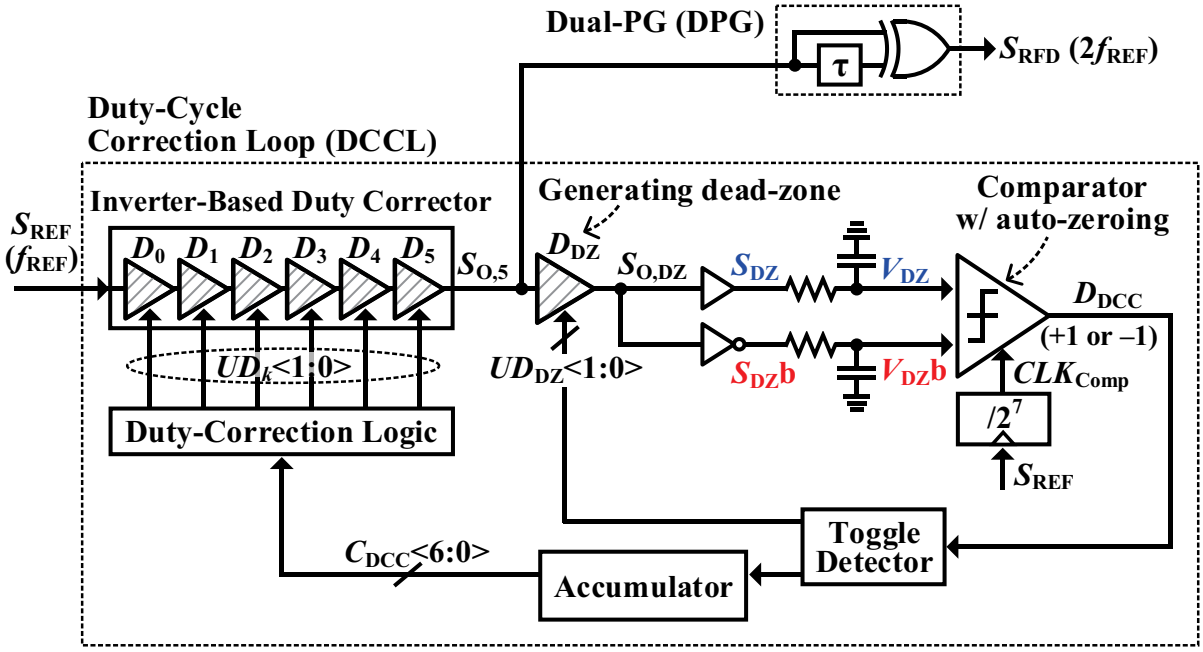
in GHz range to higher frequencies in mmW bands without degrading the total IPN. In this design, the frequency bands marked in the dotted box in Figure 74 were implemented to verify the feasibility of the approach. Figure 75 shows the proposed multi-band LO generator's overall architecture, which consists of an RFD, a GHz-range fractional-*N* PLL, and two ILFMs. First, the reference frequency, f_{REF}, is doubled by the RFD. Due to this increase in the reference frequency of the PLL, the in-band phase noise and the quantization noise of the DSM of the PLL can be suppressed significantly. When the PLL generates an output signal with a low phase noise, S_{PLL}, either ILFM_x15 or ILFM_x3 increases the frequency of S_{PLL} to the target frequency band without degradation in phase noise. If one of the two ILFMs is selected to be used, the four signals in quadrature relation as outputs of the divide-by-2 divider after the PLL are transferred to pulse generators (PGs), which generate injection pulses that are injected to the quadrature VCOs (QVCOs). A low-power frequency-tracking loop (FTL) [45] was used to keep correcting the frequency drifts of QVCOs of ILFMs and to ensure low IPN of their output signals (S_{ILFM15}_I±/Q± or S_{ILFM3}_I±/Q±) despite PVT variations. Since the two ILFMs share one FTL, the additional burden such as power consumption or silicon area for designing multiple ILFMs is reduced greatly. The detailed designs of the ILFMs and the FTL are presented in Chapter 4.5.

4.3 Design of Low-Noise Reference-Frequency Doubler (RFD)

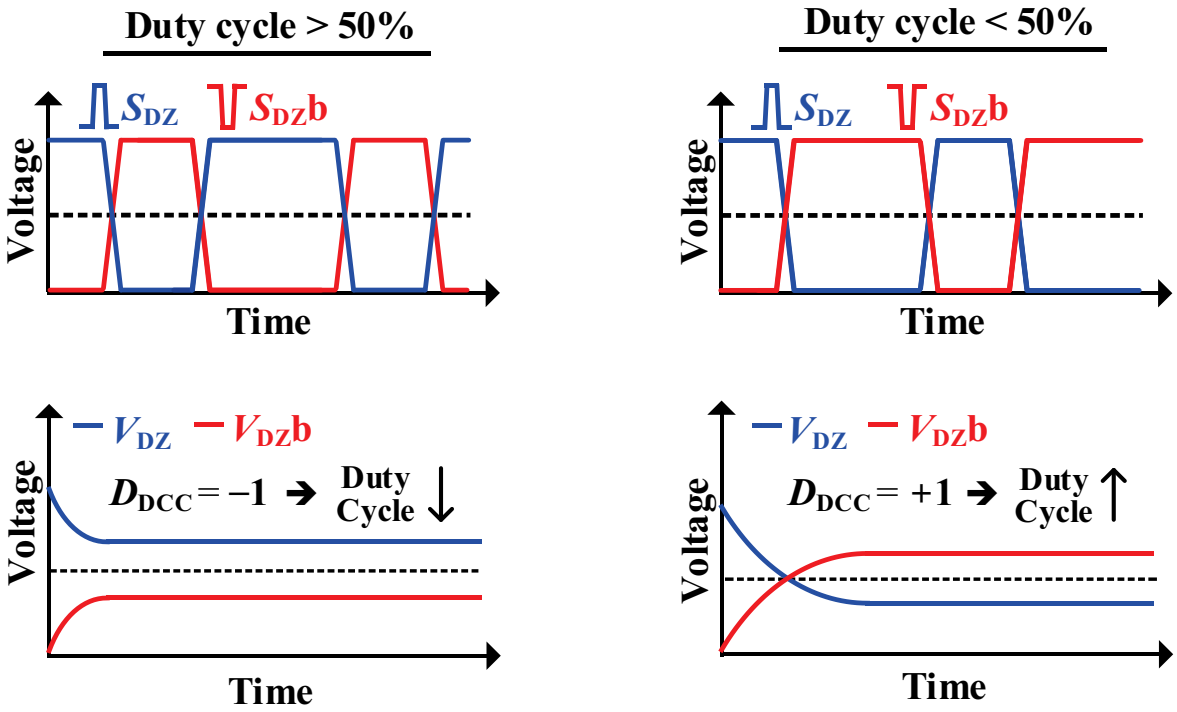
Doubling the reference frequency, f_{REF}, is the same as inserting new rising edges exactly in the middle of between two rising edges of S_{REF}, and two methods can be used to generate these new edges. The first method uses only the rising edges of the original clock. After generating a long delay using an even number of delay cells, the extent of the delay is regulated by a delay-locked loop (DLL). When the DLL is in the stead-state, i.e., in the locked condition, the total delay of the delay cells is fixed at the period of the reference clock, T_{REF}; thus, a rising edge from the middle of the delay cells is located exactly in the middle of two consecutive rising edges of the original rising edges. In general, the jitter of a new edge increases in proportion to the delay amount from the reference edge. In this case, the new rising edge must undergo a large amount of delay, i.e., $T_{REF}/2$, which inevitably causes a huge increase in the output jitter. Besides, the delay cells of the DLL should make a total delay of T_{REF}, thereby consuming a significant amount of power. The second method to double the f_{REF} is to create new rising edges from the falling edges of the original clock signal. Generally, reference signals from crystal oscillators have a duty cycle that is sufficiently close to 50%. So, if we create new rising edges from the falling edges of the reference clock, only a slight adjustment in the timing is required rather than generating a $T_{REF}/2$ delay. In this case, the new rising edges are supposed to experience much shorter delays from the original edges than occurred in the first case; thus, a much lower RMS jitter is available, even when a smaller amount of power is required.

According to the foregoing discussion, the better strategy for designing an RFD to double f_{REF}, in terms of noise and power consumption, is to exploit both rising and falling edges of S_{REF}. In Figure 76(a), schematics of the proposed RFD are shown, which includes the duty-cycle correcting loop (DCCL) and the dual-PG (DPG). In the RFD, the DCCL has the function of continuously calibrating the duty cycle of $S_{O,5}$ in the background. Then, the DPG gathers the rising and falling edges of $S_{O,5}$, thereby generating the output signal, S_{RFD}, which has a frequency of $2f_{REF}$. The DCCL captures the duty cycle deviation of $S_{O,5}$ from the DC level comparison between the complementary signals, S_{DZ} and S_{DZ}b, i.e., V_{DZ} and V_{DZ}b. (The role of one delay cell, D_{DZ}, is explained later in this section.) Since the RC filters that follow S_{DZ} and S_{DZ}b have a pole at a very low-frequency, compared to f_{REF}, the levels of V_{DZ} and V_{DZ}b become almost constant. If the duty cycle moves away from 50%, the level of either V_{DZ} or V_{DZ}b must be higher than the other. Then the comparator can determine the direction of the duty cycle, i.e., whether it should be increased or decreased. As shown in the left part of Figure 76(b), when the duty cycle of $S_{O,5}$ (or $S_{O,DZ}$) is larger than 50%, the level of V_{DZ} is higher than that of V_{DZ}b, and the following comparator outputs the D_{DCC} of –1 to reduce the duty cycle. However, when the duty cycle of $S_{O,5}$ (or $S_{O,DZ}$) is less than 50%, as shown in the right part of Figure 76(b), the level of V_{DZ} is lower than that of V_{DZ}b, and the value of D_{DCC} becomes +1 to increase the duty cycle. Since the proposed DCCL uses DC voltages (i.e., DC levels of S_{DZ} and S_{DZ}b) to extract the error information in the duty cycle, the comparator can operate at a very low frequency, which is $f_{REF}/128$; thus, it only requires a

narrow bandwidth and low power (i.e., 40 μW). Then, according to D_{DCC}, the accumulator updates the seven-bit digital code, C_{DCC} <6:0>, to correct the duty cycle of $S_{O,5}$.



(a)



(b)

Figure 76. Proposed reference-frequency doubler using a DPG and a DCCL: (a) overall architecture; (b) duty-cycle detection principle of the DCCL

In the overall architecture of Figure 76(a), the duty cycle is calibrated by interworking of a duty corrector having six delay cells, D_ks (k = 0 − 5), where each delay cell including two inverters, an additional delay cell generating a dead zone, D_{DZ}, and the duty-correction logic (DCL). Figure 77 describes a delay cell of the inverter-based duty corrector, D_k. It consists of two inverters, each of which includes a slow and a fast PMOS and a slow and a fast NMOS. Since the size ratio, i.e., W/L, of the fast transistor is 2^{k+1} times that of the slow transistor, the drain current ratio of the fast transistor is also 2^{k+1} times that of the slow one. When the fast transistor is selected, the transition of edges is so fast that the amount of the delay of edges is minimized. However, when the slow transistor is selected, the transition of edges becomes slow; thus, the amount of the delay increases so that the duty cycle can be changed effectively. When the code of C_{DCC} <6:0> is delivered, the DCL decodes it into six two-bit codes, i.e., UD_k<1:0>, where k is from 0 to 5. According to UD_k<1:0> from the DCL, D_k can have one of three configurations. Figure 78(a) shows the first configuration, when UD_k<1:0> has the value of '00', both the fast PMOS and the fast NMOS are used for two inverters. In this case, the duty cycle does not change, since the delay amount when passing through the inverter is the same for both the rising and falling edges of the signal. When UD_k<1:0> is '01', as shown in Figure 78(b), the first inverter is configured with the fast PMOS and the slow NMOS, meanwhile the second inverter includes the slow PMOS and the fast NMOS. In this case, the rising edges of $S_{IN,k}$ are delayed in the first inverter, whereas the falling edges of $\overline{S_{IN,k}}$ are in the second inverter. As a result, the rising edges of $S_{IN,k}$ will be more delayed than the falling edges, thereby the duty cycle decreases. When UD_k<1:0> is '10', as shown in Figure 78(c), the falling edges of $S_{IN,k}$ is more delayed than rising edges, which increases the duty cycle.

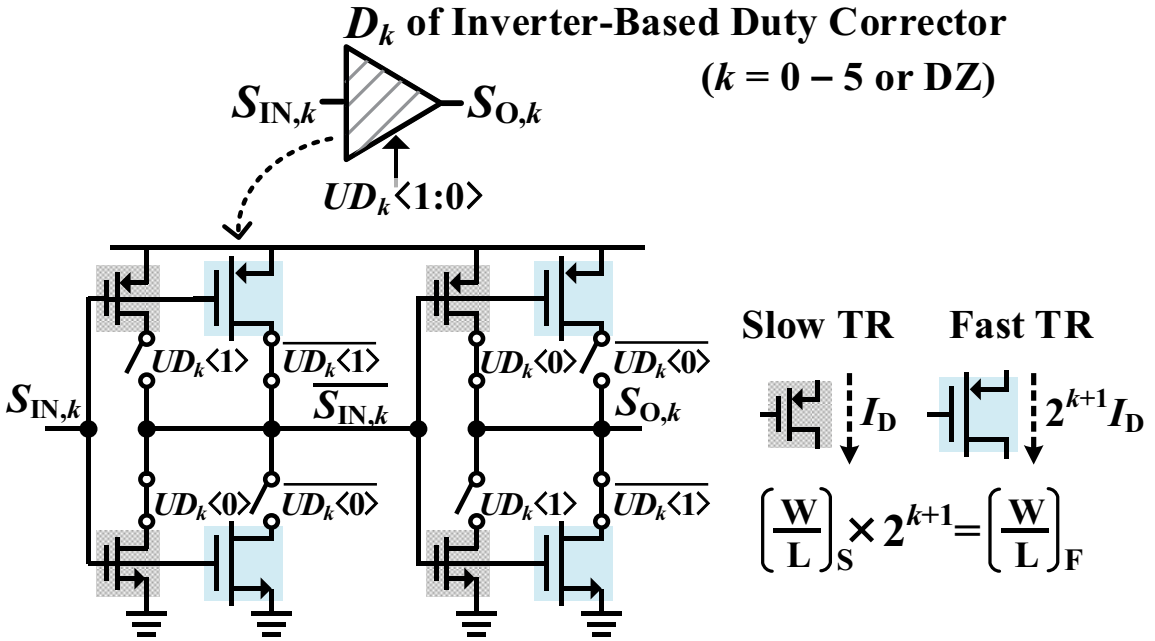


Figure 77. Delay cell (D_k) of the inverter-based duty corrector, consisting of two inverters that have slow and fast transistors

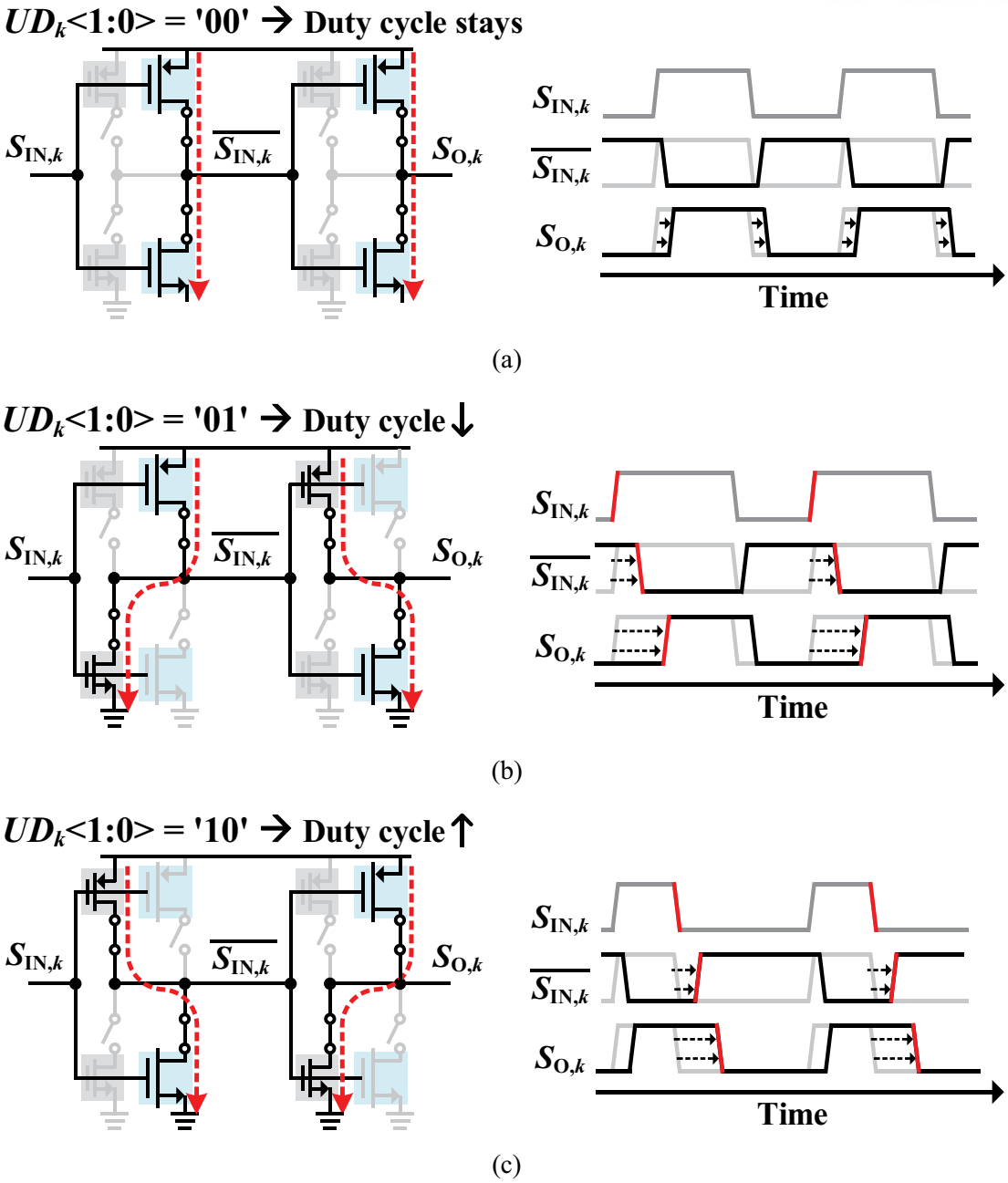


Figure 78. Changes of the duty cycle of $S_{O,k}$ according to UD_k<1:0>,: (a) when UD_k<1:0> is '00'; (b) when UD_k<1:0> is '01'; (c) when UD_k<1:0> is '10'

As shown above, the magnitude of the change in the duty cycle depends on the amount of the delay through a slow current path. Figure 77 shows that the size of the fast transistors increases by a factor of two as the value of k increases by one, while the size of the slow transistors remains the same. Since the capacitance seen by the output of D_k is dominated by the gate capacitance of the fast transistors of the next delay cell, i.e., D_{k+1}, the delay of D_k by the slow transistors is almost doubled as k increases. In practice, the ratio of the increase in the amount of the delay is smaller than two (due to other parasitic capacitors), but no problem occurs as long as the increase in the delay is monotonous throughout the

delay-cell chain. To minimize redundant delays, which also can reduce additional noise originated from the delay, the DCL was designed not to have '01' or '10' in UD_k<1:0>s if it is not necessary.

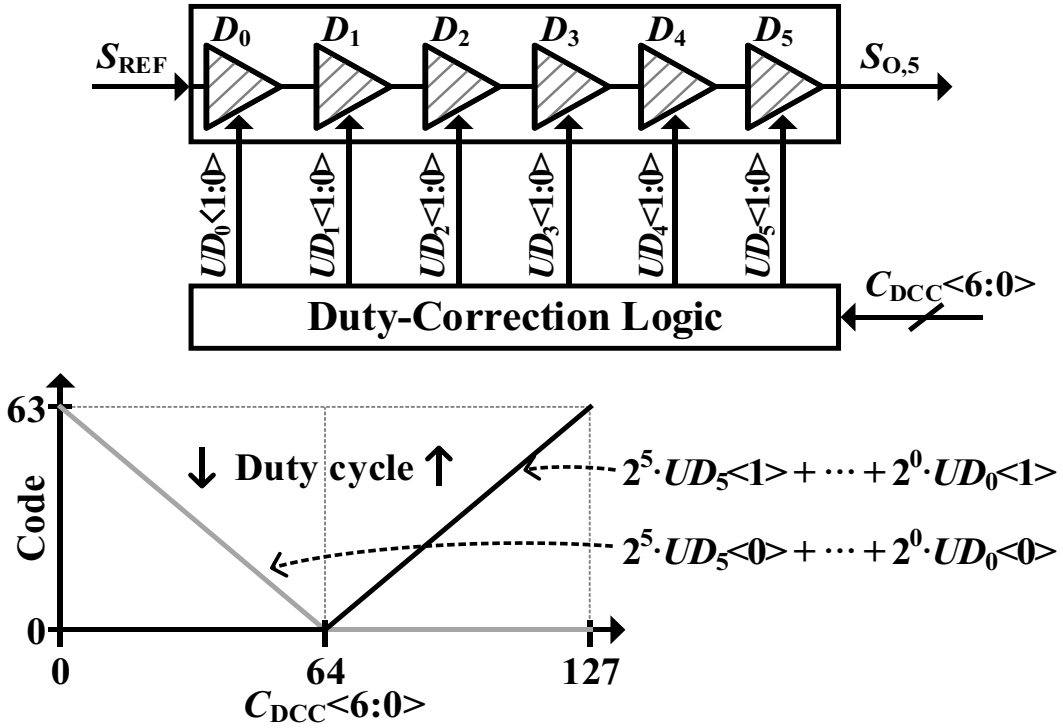


Figure 79. Algorithm of the duty-correction logic (DCL) to decode C_{DCC}<6:0> to minimize redundant delay and thus added noise

As shown in Figure 79, when C_{DCC}<6:0> is 64, no correction of the duty cycle is necessary, and all UD_k<1:0>s become '00'. When the duty cycle must be increased, corresponding to the value of C_{DCC}<6:0>, some of the UD_k<1>s are set to '1', while all UD_k<0>s are '0'. However, in order to decrease the duty cycle, some of UD_k<0>s are set to '1', while all UD_k<1>s are '0'. In this manner, the total delays that the rising edges and falling edges undergo can be minimized.

In Figure 76, the additional delay cell of D_{DZ} is used to generate a dead zone. The step size of D_{DZ} is between that of D_0 and D_1. The purpose of the dead zone is to prevent the periodic toggling at $S_{O,5}$ caused by the change in C_{DCC}<6:0> at steady state, which could cause unwanted spurious tones. Figure 80 shows the changes of the duty cycles of $S_{O,5}$ and S_{DZ} by the operation of the DCCL. During the coarse tuning (binary search), the control bits of the dead-zone cell, UD_{DZ}<1:0>, are set to '00' to ensure that $S_{O,5}$ and $S_{O,DZ}$ have the same duty cycles. In this phase, C_{DCC}<6:0> is simultaneously updated by D_{DCC}, so that the DCL and the inverter-based duty corrector can calibrate the duty cycle of $S_{O,5}$ accurately. When the duty cycle is sufficiently close to 50%, D_{DCC} is supposed be toggled between +1 and −1. During this duty-cycle-tracking phase, when the continuous toggling of D_{DCC} is detected, the code of UD_{DZ}<1:0> is forced to toggle between '01' and '10', instead updating C_{DCC}<6:0>.

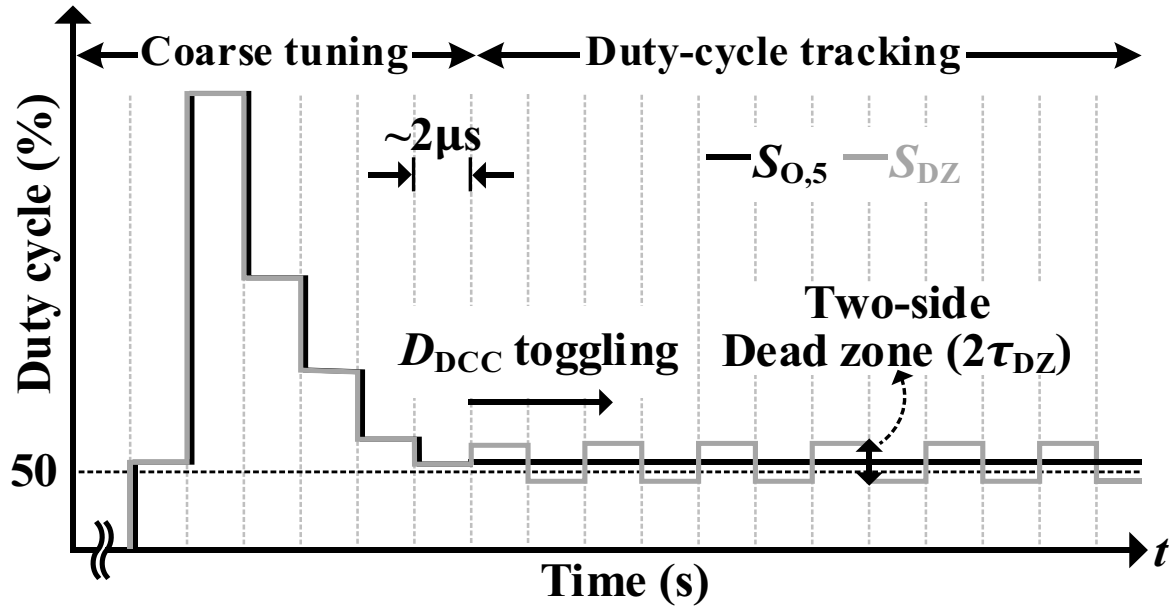


Figure 80. Changes of the duty cycles of $S_{O,5}$ and S_{DZ}, according to the operation of the DCCL

By intentionally varying $S_{O,DZ}$, $S_{O,5}$ can be kept constant; thus, the spur can appear at the operating frequency of the DCCL can be minimized. If the duty cycle of $S_{O,5}$ varies due to any environmental changes, the comparator would produce consecutive +1s or −1s. Then, UD_{DZ}<1:0> is reinitialized to '00', and C_{DCC}<6:0> is updated again to readjust the duty cycle of $S_{O,5}$ to be close to 50%. Since the error in the duty cycle of $S_{O,5}$ within the dead zone cannot be corrected, the resolution of the DCCL is determined by the size of the dead zone. To evaluate the variation of the dead zone, and, thus, the resolution of the DCCL, Monte-Carlo simulation was performed with 2,000 samples. As shown in Figure 81, the average and the 3-sigma standard deviation of the size of the dead zone were 0.21% and 0.015% with respect to the 50% duty cycle, respectively.

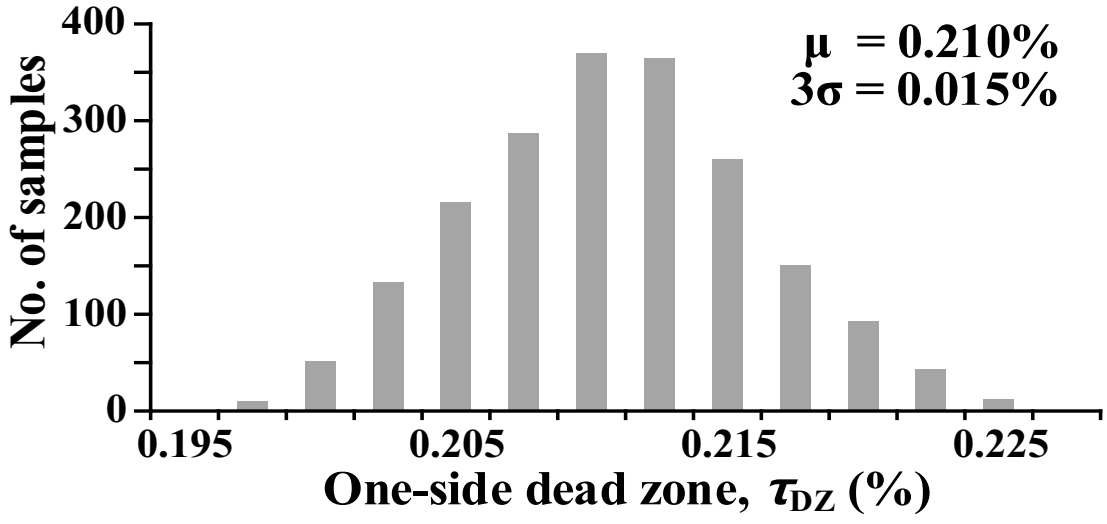


Figure 81. Monte-Carlo simulation of the size of dead zone

When a 3-sigma value is assumed, the level of the reference spur at the RFD output (or S_{RFD}) can be estimated to be less than −45 dBc [46]. Figure 82 shows the comparator in the RFD, consisting of a one-stage pre-amplifier and a following sampling latch. The technique called as an auto-zeroing was used to remove the input offset of the pre-amplifier [47]. From post-layout simulations, the resolution of the comparator was less than 100 μV, which corresponds to a duty-cycle error of 0.0083%, indicating that the comparator's input offset does not limit the resolution of the duty-cycle correction of the proposed DCCL.

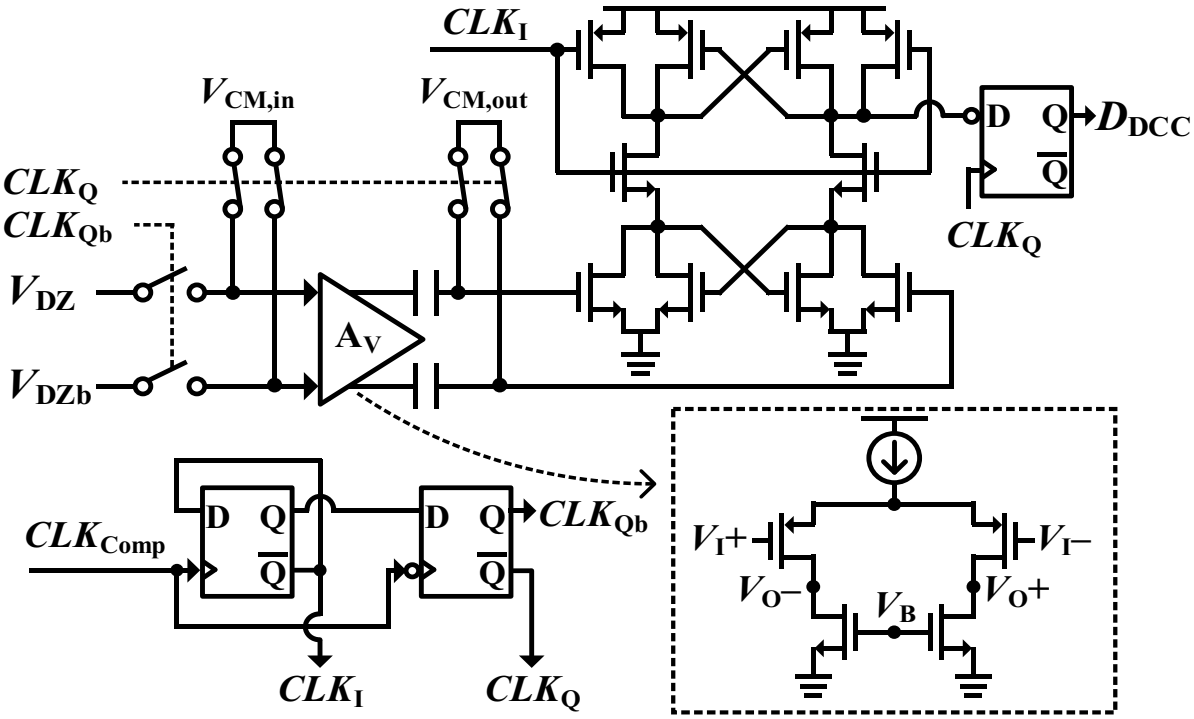
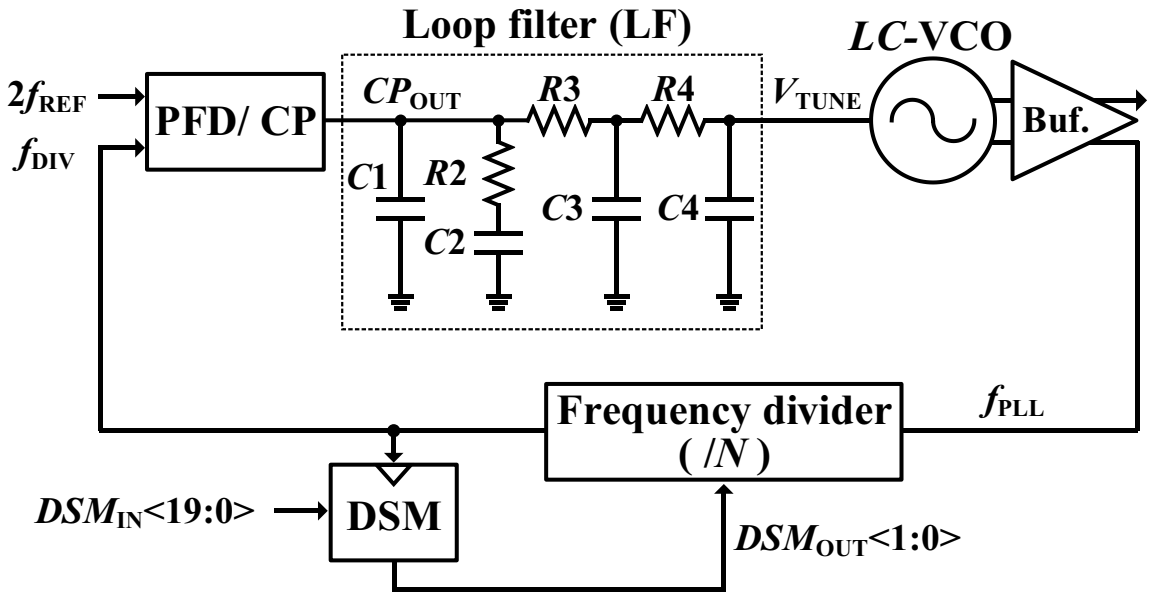


Figure 82. Comparator in the RFD with the auto-zeroing technique

4.4 Design of Low IPN Fractional-*N* PLL and Building Blocks



Values of Loop components

*C*1	*C*2	*R*2	*R*3	*C*3	*R*4	*C*4
12 pF	262 pF	11 kΩ	7 kΩ	2.7 pF	7 kΩ	2.7 pF

Figure 83. Overall architecture of the implemented fractional-*N* PLL

Figure 83 shows the overall architecture of the fractional-*N* PLL that generates low-IPN signals around 3 – 4 GHz, using the $2f_{REF}$-reference clock generated from the preceding RFD. The PLL is based on a conventional 5th-order and type-II PLL architecture with a 3rd-order 1-2 MASH DSM. The loop bandwidth of the PLL was designed to be 500 kHz; this wide loop bandwidth is helpful in further suppressing the phase noise of the VCO. The reason we can use this relatively wide loop bandwidth is that the proposed RFD provides the PLL with a frequency-doubled reference clock with very low phase noise. Due to this high reference frequency, the divider can have reduced division number, thereby suppressing the increase in the in-band noise from loop-building blocks, such as a charge pump (CP), a phase-frequency detector (PFD), and a divider. In addition, the quantization noise, Q-noise, from the DSM will be suppressed naturally. The PLL has a 4th-order passive loop filter. In this type of loop filter, the characteristics are determined mainly by *R*2, *C*1, and *C*2. The values of the passive components are listed in the table. To filter out high-frequency noise coupled through the long metal line from the loop filter to the VCO's control voltage, V_{TUNE}, an additional 2nd-order RC filter was placed right before the V_{TUNE} node of the VCO in the layout. This 2nd-order RC filter, consisting of *R*3, *C*3, *R*4, and *C*4, also provides an additional rejection to the level of the reference spur and can be used to calibrate the phase margin of the loop.

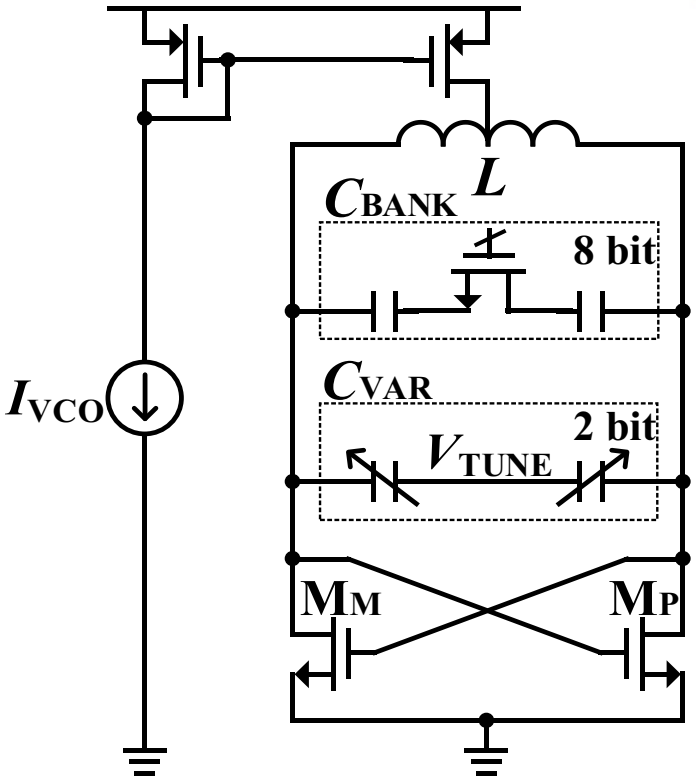


Figure 84. NMOS-type cross-coupled *LC* VCO

Figure 84 shows that the designed NMOS-type cross-coupled *LC* VCO [48], [49] to achieve low phase noise with a large output swing. To ensure its reliability, the core transistors of the VCO, i.e., M_P and M_M, were designed with thick-oxide transistors having 70-μm width and 280-nm length. We used an eight-bit capacitor bank with metal-oxide-metal (MOM) capacitors to increase the frequency-tuning range. We also used a two-bit varactor bank to fine tune the frequency, and it controlled the voltage-to-frequency gain (K_{VCO}). The inductance of the two-turn inductor of the *LC* tank is 1.2 nH, and the loaded Q is 16.6 at 3.9 GHz. The PFD has a typical rising edge-triggered tri-state topology, and it includes two D-flip flops (DFFs), an AND gate, and delay cells that provide a reset delay to prevent the dead-zone effect. According to a two-bit control signal, the reset delay can change between 150 and 450 ps with steps of 100 ps. As shown in Figure 85, the CP is based on a current-steering topology [28] for higher switching speed and to improve the linearity, and the CP current, I_{CP}, is 200 μA. One of the major causes of the reference spur in the PLLs using a current-steering CP is the skew between the PFD's output signals, i.e., *UP* (or *DN*) and *UPb* (or *DNb*), which control the main and the dummy switches of the CP. To minimize the skews between *UP* and *UPb* and *DN* and *DNb*, inverter-based latches are used between the PFD and the CP. The CP includes two OP amps, i.e., OP_1 and OP_2. First, the unit gain OP amp of OP_1 is used to fix the voltage of node *X* at that of the CP output, CP_{OUT}. Since the voltages at nodes *X* and CP_{OUT} are the same, the voltages at nodes *Y* and *Z* do not fluctuate despite the toggling between *UP* and *UPb* or *DN* and *DNb*, which enhances the switching speed and the linearity of the CP.

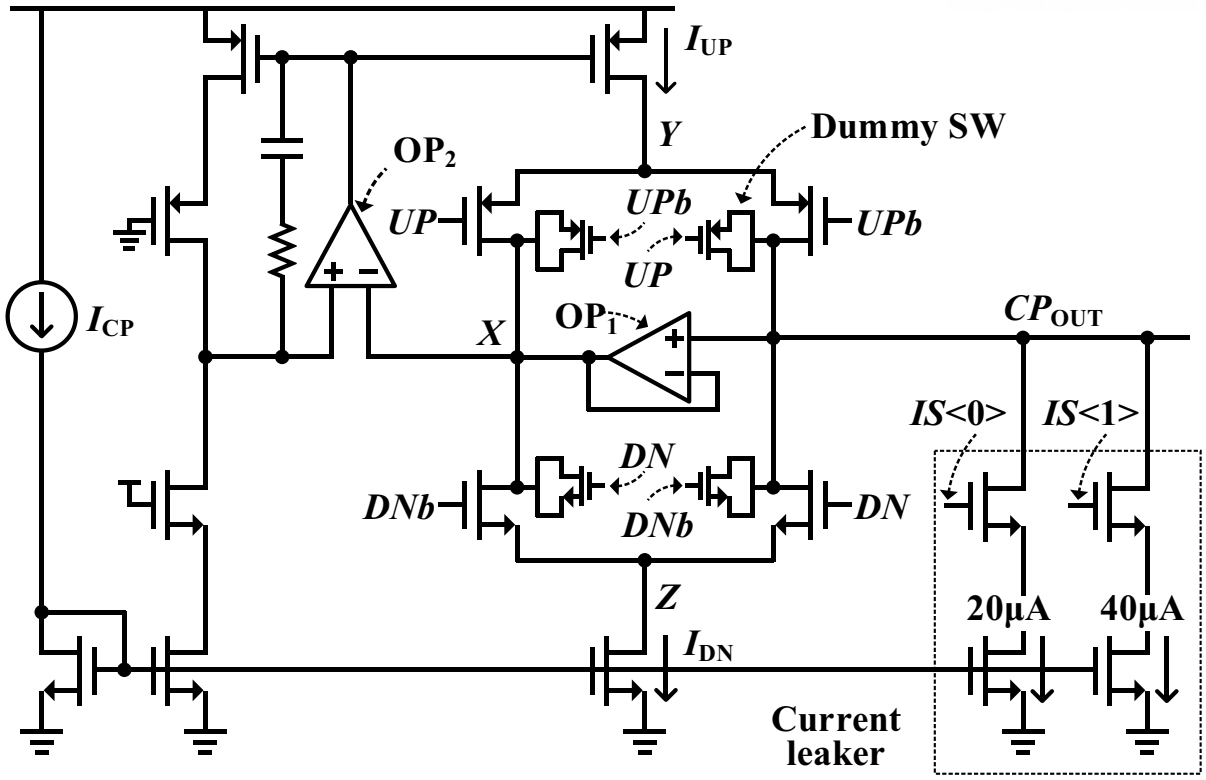


Figure 85. Schematics of the current-steering charge pump (CP)

Second, OP_2 is used to implement a dynamic bias control scheme, and it can reduce the mismatch between the up current, I_{UP}, and the down current, I_{DN}, [50]. According to the results of the post-layout simulations, the mismatch between I_{UP} and I_{DN} can be restricted to less than 0.1% across the ranges of CP_{OUT} from 0.38 to 0.95 V. In general, the linearity of the CP tends to be degraded near the point at which the phase difference between S_{REF} and the feedback signal close to zero. To enable the CP to operate in a linear region by shifting the operating point, optional sinking current sources are reserved at CP_{OUT}. Considering the maximum change of the DSM code, the period of the VCO's output signal, the period of the reference clock, and the division number of the PLL, the required current range is from 28.5 to 44.4 μA. By a two-bit control signal, IS<1:0>, the amount of the sinking current can be changed from 20 to 60 μA.

Figure 86 shows the schematics of a 20-bit 3rd-order 1-2 MASH DSM, which can provide a 3rd-order noise-shaping of the quantization noise. Since the DSM generates a two-bit output signal, DSM_{OUT}<1:0>, it causes smaller phase shifts than the 1-1-1 MASH DSM that generates a three-bit output signal. To add a dithering effect, the output of a 15-bit pseudo-random binary sequence (PRBS) generator is connected to the LSB of the DSM code, DSM_{IN}<19:0>.

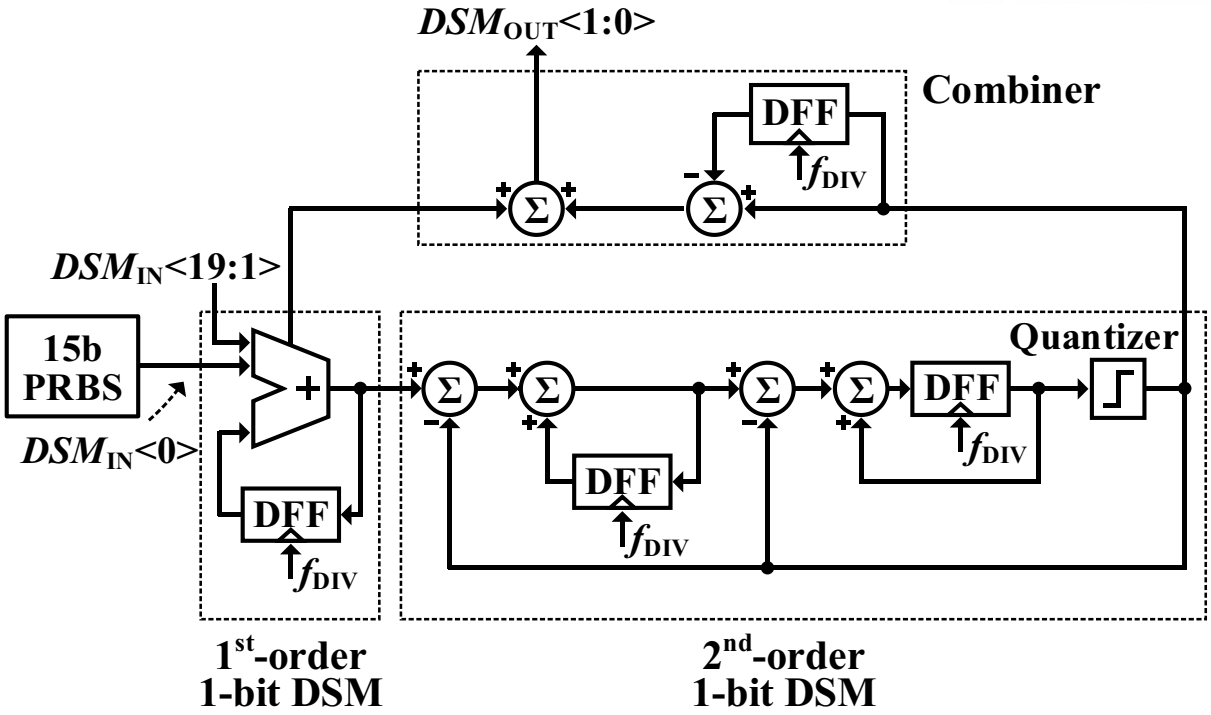


Figure 86. 3rd order 1-2 MASH DSM with a 15bit PRBS generator

4.5 Design of Low IPN Fractional-*N* PLL and Building Blocks

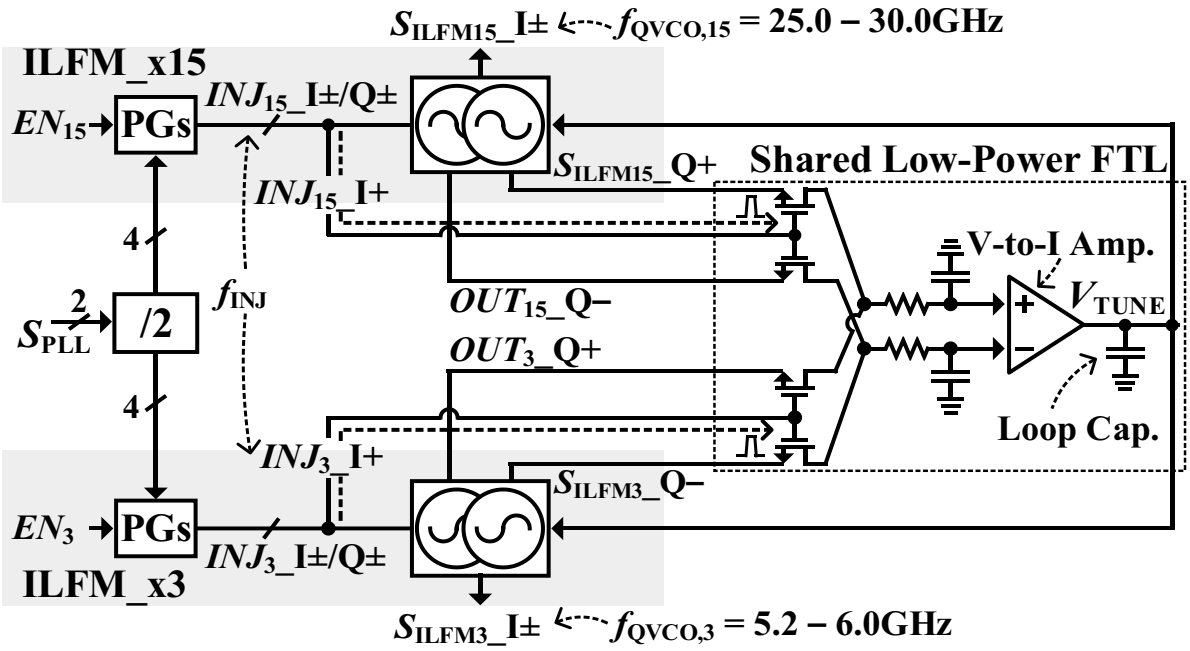


Figure 87. Schematics of two ILCMs and the frequency-tracking loop (FTL)

In this work, we implemented two ILFMs. As shown in Figure 87, ILFM_x15 has a multiplication factor of 15 to generate a mmW-band LO signal, and ILFM_x3 has a multiplication factor of three to generate a signal in a 5–6 GHz frequency band. By dividing the differential output signals of the PLL by two, a pulse generator provides quadrature injection signals, INJ_{15}_I±/Q± (or INJ_3_I±/Q±) to ILFM_x15 (or ILFM_x3). As generally known, an ILFM can have a low-phase noise performance only when the VCO's free-running frequency, $f_{QVCO,M}$, is close enough to the target frequency, $M \cdot f_{INJ}$, where f_{INJ} is the frequency of the inejction singal and M is the multiplication number in ILFM [51]. Therefore, the frequency difference, f_{DEV}, between $f_{QVCO,M}$ and $M \cdot f_{INJ}$, should be maintained to be small regard to the ILFM's lock range, f_{LOCK}. However, since the ILFM operates in a mmW, f_{LOCK} typically is limited to less than 3% of the VCO's free-running the frequency [52], [53]. Thus, for the robust operation along with a low phase noise performance even with the environmental variations, an ILFM operating at mmW must have a carefully designed FTL, which can track the frequency deviation of the VCO and calibrate the real-time frequency drifts. In this work, we used an ultra-low power FTL, as was presented in [52]. Also, the FTL was designed to be shared by the two ILFMs to reduce the area of the silicon and design redundancy. Figure 88 shows the operational principle of the FTL, i.e., how the FTL calibrates the $f_{QVCO,M}$ of an ILFM and minimizes f_{DEV}. As an example, we assumed the case in which ILFM_x15 is used. To detect f_{DEV}, the FTL detects and compares the overlapped area of INJ_{15}_I+ and OUT_{15}_Q+ with that of INJ_{15}_I+ and OUT_{15}_Q– at the moment of injection of INJ_{15}_I+. If $f_{QVCO,15}$ deviates from $15f_{INJ}$, the quadrature relationship in the output signals of the QVCO is distorted momentarily, i.e.,

INJ_{15}_I+ locates much closer to either OUT_{15}_Q+ or OUT_{15}_Q−, making the two areas to be different. After that, the value of the two areas are changed to the corresponding DC voltages, V_{AQ}+ and V_{AQ}−, and the loop monitors the voltages in real time. Since the FTL operates only at a low frequency by monitoring the averages of phase deviations, the power consumption of the FTL was less than 900 μW. Although we used two QVCOs in this work, the occupied area was not large this is because the size of the inductors in both ILFM_x3 and ILFM_x15 were small. (The number of turns of the inductor in ILFM_x3 was three and the inductor of ILFM_x15 is inherently small due to the high oscillation frequency.) The V-to-I amplifier is designed based on a two-stage operational transconductance amplifier (OTA). The role of the first stage in the OTA is a kind of a level shifter, and the OTA's second stage includes a cascode load to boost the gain and minimize mismatches in current. When the layout is drawn, the inter-digitation was used to improve the differentiality. The mmW QVCO of ILFM_x15 is based on the DC-coupled CMOS-type architecture with a six-bit cap-bank and a varactor.

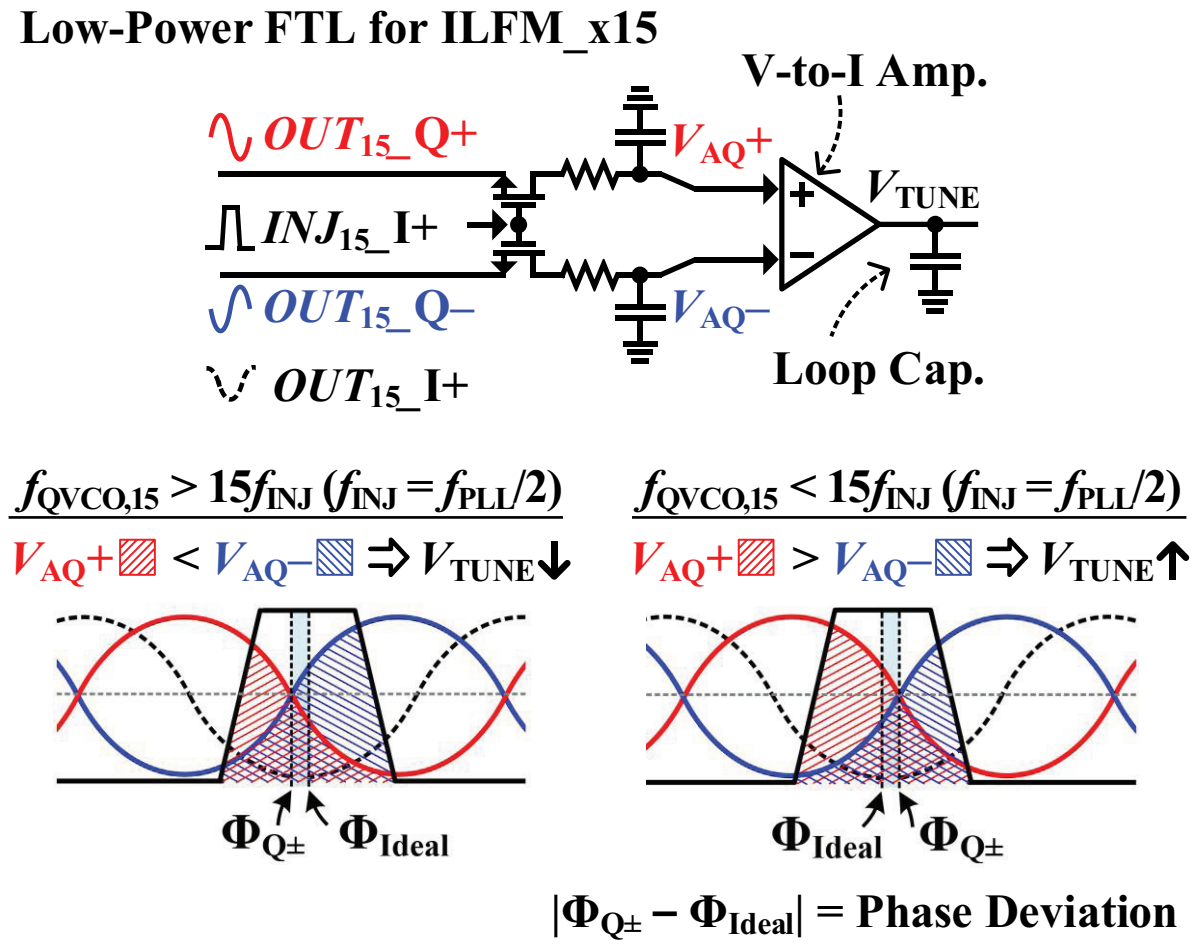
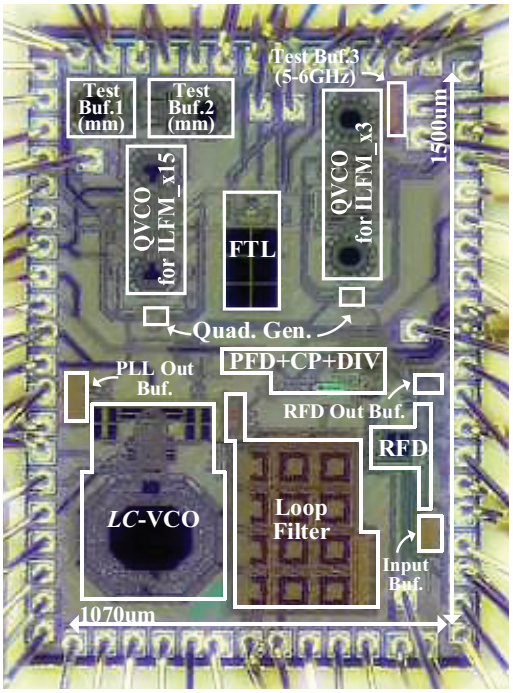


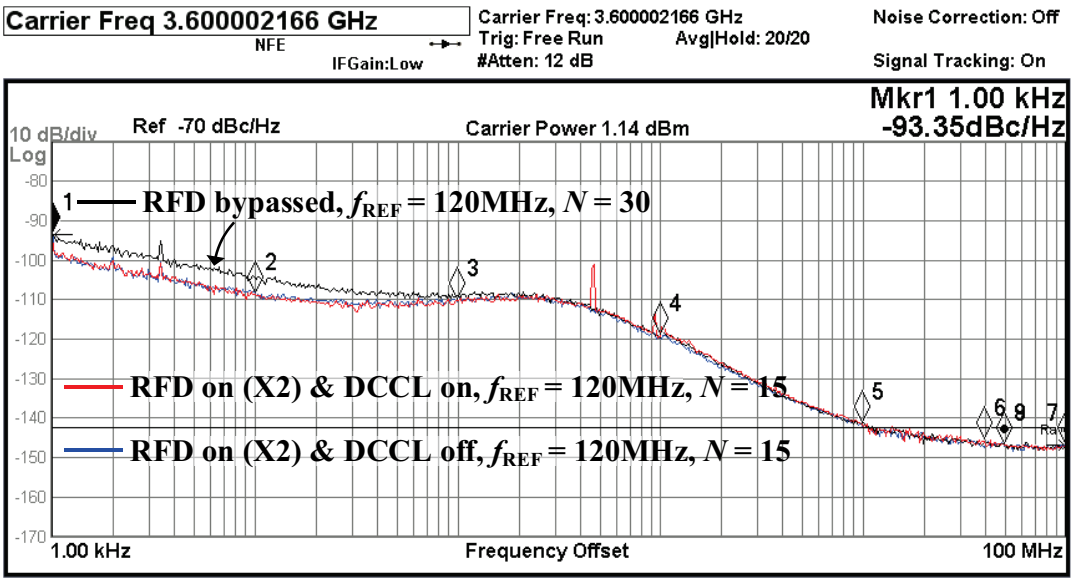
Figure 88. Principle of the FTL when the multiplication factor is 15

4.6 Experimental Results



Power Consumption (mW)		
RFD		2.5
PLL (20.1)	*LC*-VCO	6.0
	PFD+CP	2.2
	Divider+DSM	3.0
	VCO buf.+Quad. gen.	8.9
ILFM x15 (13.8)	QVCO	10.4
	PGs	2.5
	FTL	0.9
ILFM x3 (12.5)	QVCO	9.1
	PGs	2.5
	FTL	0.9
Total	(RFD+PLL+ILFM_x15)	36.4
	(RFD+PLL+ILFM_x3)	35.1

Figure 89. Chip micrograph and power break-down table



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	2	1.00 kHz	-93.35dBc/Hz			
2	N	2	10.0 kHz	-108.62dBc/Hz			
3	N	2	100 kHz	-110.08dBc/Hz			
4	N	2	1.00 MHz	-119.20dBc/Hz			
5	N	2	10.0 MHz	-141.44dBc/Hz			
6	N	2	40.0 MHz	-145.67dBc/Hz			
7	N	2	100 MHz	-146.96dBc/Hz			
8	N	2	50.0 MHz	-146.76 dBc/Hz	Integ Noise	100 MHz	185.2 fs
9	N	2	50.0 MHz	-146.76 dBc/Hz	Integ Noise	100 MHz	-50.57 dBc

Figure 90. Phase noises measurement when the integer-*N* mode PLL operates at 3.6GHz in three cases

The proposed multi-band quadrature LO generator was fabricated in a 65-nm CMOS technology. As shown in Figure 89, the active silicon area was 0.95 mm^2, and the total power consumption was 36.4 mW when a 29.22 GHz signal was generated from ILFM_x15. Figure 90 shows the measured phase noises of a 3.6-GHz output signal when the PLL operated in the integer-*N* mode. The black line is the measured phase noise when the RFD was bypassed and *N* was set to 30, and the red and blue line is the phase noises when the RFD was enabled and *N* was set to 15. When the reference frequency was doubled by the RFD, the in-band phase noise of the PLL decreased significantly, thereby resulting in much lower IPN and jitter, which were −50.5 dBc and 185 fs, respectively. The phase noises shown in red and blue were measured when the DCCL of the RFD was turned on and off, respectively. There is little difference between the two graphs, which indicated that the additional noise due to the operation of the DCCL was insignificant.

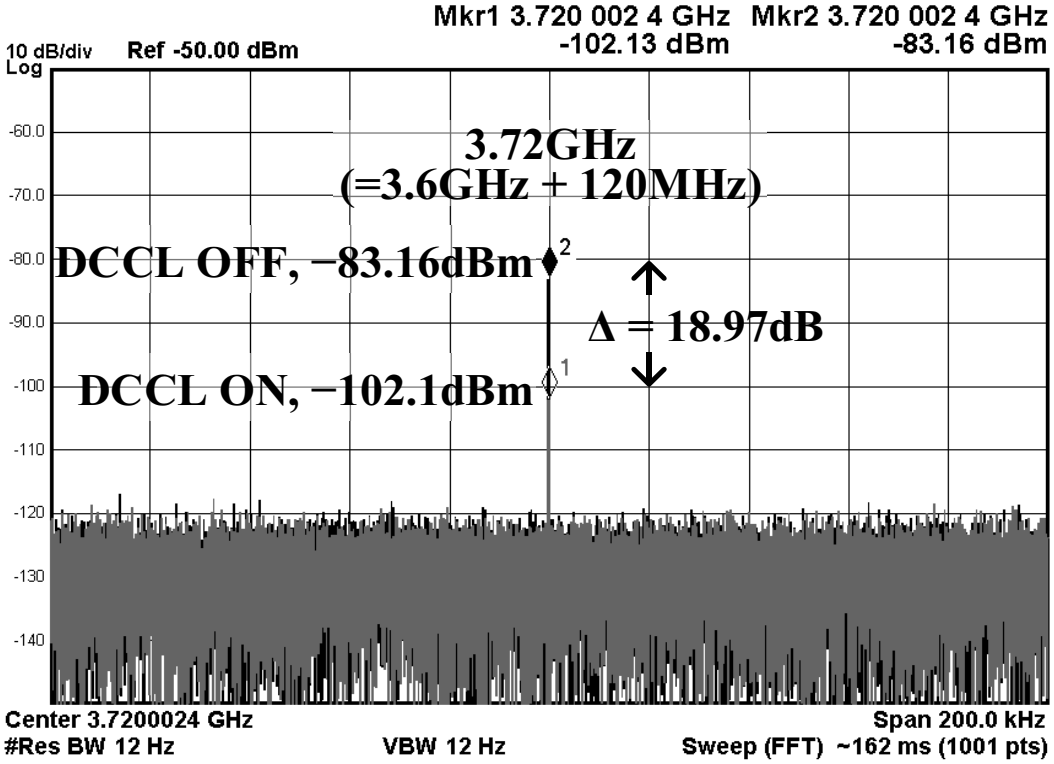
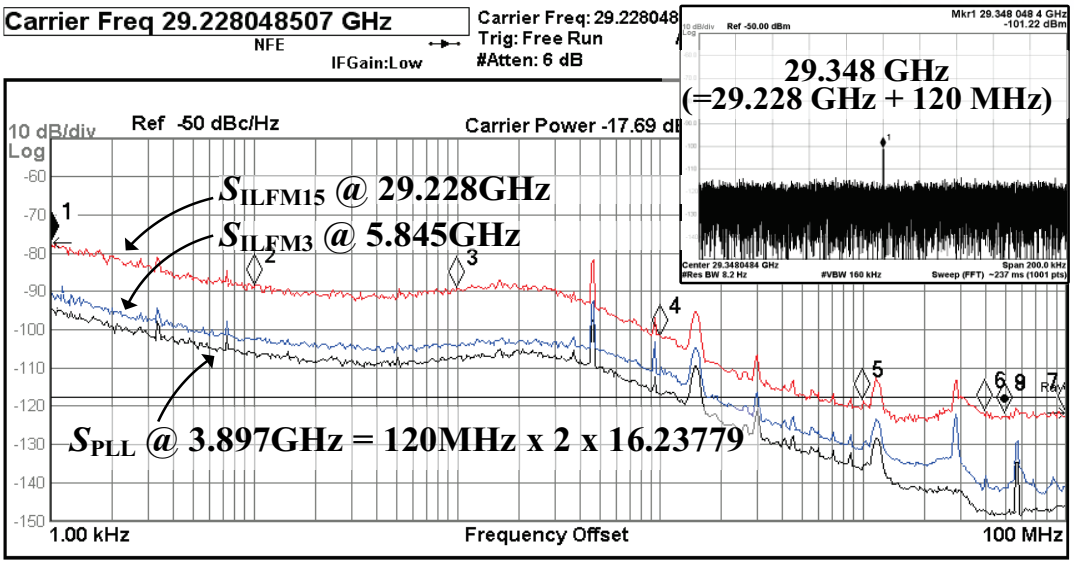


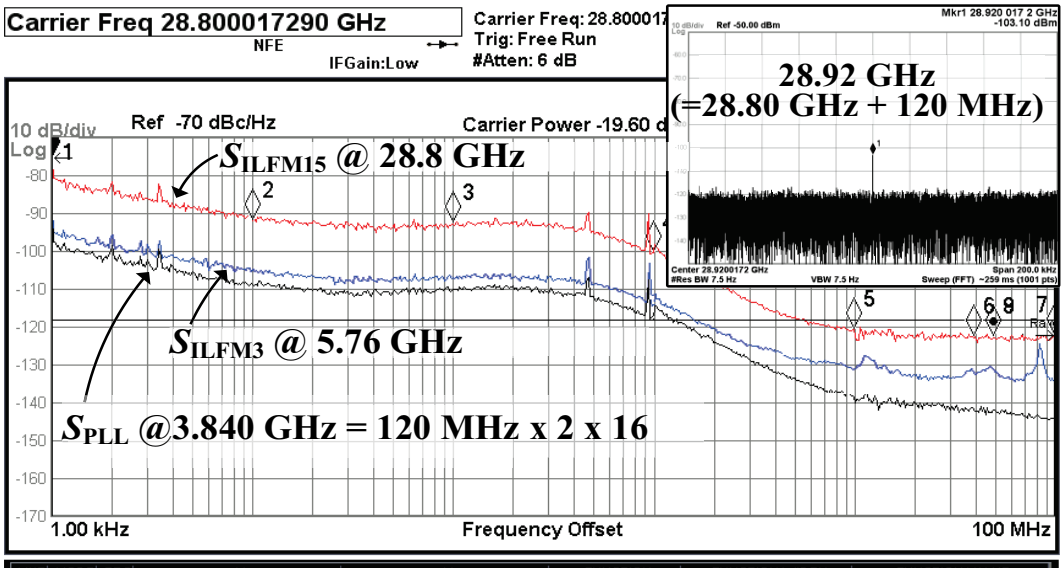
Figure 91. Measured level of the reference spur reduction at the output of the PLL when DCCL is turned on

Figure 91 shows that the continuous duty-cycle calibration of the DCCL resulted in a great reduction in the level of the reference spur even though the difference in the noise when the DCCL was turned on and off was negligible. The measurements show that the level of the spur at 120 MHz was improved by 18.9 dB at the PLL output when the DCCL was turned on. The phase-noise graph (red line) has a spurious tone at 468.8 kHz because the DCCL of the RFD operates at this frequency.



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	2	1.00 kHz	-77.15dBc/Hz			
2	N	2	10.0 kHz	-88.66dBc/Hz			
3	N	2	100 kHz	-89.43dBc/Hz			
4	N	2	1.00 MHz	-101.95dBc/Hz			
5	N	2	10.0 MHz	-118.72dBc/Hz			
6	N	2	40.0 MHz	-121.29dBc/Hz			
7	N	2	100 MHz	-121.82dBc/Hz			
8	N	2	50.0 MHz	-122.24 dBc/Hz	Integ Noise	100 MHz	206.2 fs
9	N	2	50.0 MHz	-122.24 dBc/Hz	Integ Noise	100 MHz	-31.45 dBc

Figure 92. Phase noises measurement when the fractional-*N* mode PLL with output of the ILFM_x3 and ILFM_x15



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	2	1.00 kHz	-75.49dBc/Hz			
2	N	2	10.0 kHz	-91.89dBc/Hz			
3	N	2	100 kHz	-92.75dBc/Hz			
4	N	2	1.00 MHz	-100.33dBc/Hz			
5	N	2	10.0 MHz	-120.69dBc/Hz			
6	N	2	40.0 MHz	-122.68dBc/Hz			
7	N	2	100 MHz	-122.38dBc/Hz			
8	N	2	50.0 MHz	-122.80 dBc/Hz	Integ Noise	100 MHz	172.3 fs
9	N	2	50.0 MHz	-122.80 dBc/Hz	Integ Noise	100 MHz	-33.14 dBc

Figure 93. Phase noises measurement when the integer-*N* mode PLL with output of the ILFM_x3 and ILFM_x15

In Figure 92 the measured phase noises of the PLL in the fractional-*N* mode along with the output signals of ILFM_x15 and ILFM_x3. When ILFM_x15 was used to generate a 29.22-GHz output signal, the measured IPN was −31.4 dBc and the measured RMS jitter was 206 fs. For ILFM_x3, the IPN of the 5.84-GHz signal was –44.1 dBc. Figure 93 shows the measured phase noises of the output signals of ILFM_x15, ILFM_x3, and the PLL in the integer-*N* mode. In these measurements, the measured IPN and RMS jitter of the 28.8 GHz signal generated from ILFM_X15 were −33.1 dBc and 172 fs, respectively. In Figure 92 and Figure 93, both measurements of the level of the reference spur at the 120 MHz offset at the output of ILFM_x15 were regulated to less than –83 dBc. In addition, the differences in the levels of phase noises between the PLL and ILFM_x3 (or ILFM_x15) was very close to 20log(*M*), which means that the noise contributed by the ILFMs was almost insignificant. Table 13 compares the performance of the proposed multi-band LO generator with the performances of state-of-the-art mmW fractional-*N* frequency synthesizers. As shown in Table 13, this work is capable of providing frequencies for the multiple-band and concurrently achieving the best IPN, the lowest in-band phase noise, the lowest level of the reference spur, and FOM_{JIT}.

Table 13. Performance comparison with state-of-the-art mm-band ILFMs

	This work	**ISSCC'15 [10]**	**ISSCC'17 [11]**	**JSSC'14 [13]**	**JSSC'16 [16]**
Process	65nm CMOS	32nm SOI	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	RFD + GHz-PLL +ILFMs	Analog/Digital Hybrid PLL	All-Digital PLL	All-Digital PLL	20GHz SS-PLL + 60GHz QILO
Type	Fractional-*N*	Fractional-*N*	Fractional-*N*	Fractional-*N*	Integer-*N*
Quad/Multi. Freq. Bands	YES/YES	NO/NO	NO/NO	NO/NO	YES/NO
Output Freq. (GHz)	25.0 – 30.0 5.2 – 6.0 2.7 – 4.2	13.1 – 28.0	50.2 – 66.5	56.4 – 63.4	55.6 – 65.2
Ref. Freq, f_{REF} (MHz)	120	104.5	100	100	40
Jitter$_{RMS}$ @f_O (GHz) (Integ. Range)	206fs @29.22 (1k – 100MHz)	1.03ps* @22.25 (10k–100MHz)	258fs @65.35 (1k – 40MHz)	590fs @61.87 (10k – 10MHz)	290fs @60.5 (10k – 40MHz)
IPN @f_O (GHz) (Integ. Range)	–31.4 @29.22 (1k – 100MHz)	–19.8* @22.25 (10k–100MHz)	–22.5 @65.35 (1k–40MHz)	–15.8 @61.87 (10k–10MHz)	–22.2* @60.5 (10k – 40MHz)
IPN (dBc) Norm. to 28GHz (Integ. Range)	–31.8 (1k–100MHz)	–17.8* (10k–100MHz)	–29.9 (1k–40MHz)	–22.7 (10k–10MHz)	–28.8* (10k – 40MHz)
In-band noise (@10kHz) (dBc/Hz) @f_O (GHz)	–88.6 @29.22	–71.0 @22.25	–78.7 @65.35	–75.0 @61.87	–78.5 @60.5
Reference spur (dBc)	–83.5	NA	NA	–74	–73
Power Cons. (P_{DC})	36.4 (x15 mode)	31.0	46.0	48.0	32.0
Active Area (mm^2)	0.95	0.24	0.45	0.48	1.08 w/ pads
FOM_{JIT} (dB)**	–238.1	–224.8	–235.1	–227.8	–235.7

* Calculated from the measurement results ** $FOM_{JIT}=10\log(\sigma_t^2 \cdot P_{DC})$ (dB)

4.7 Conclusions

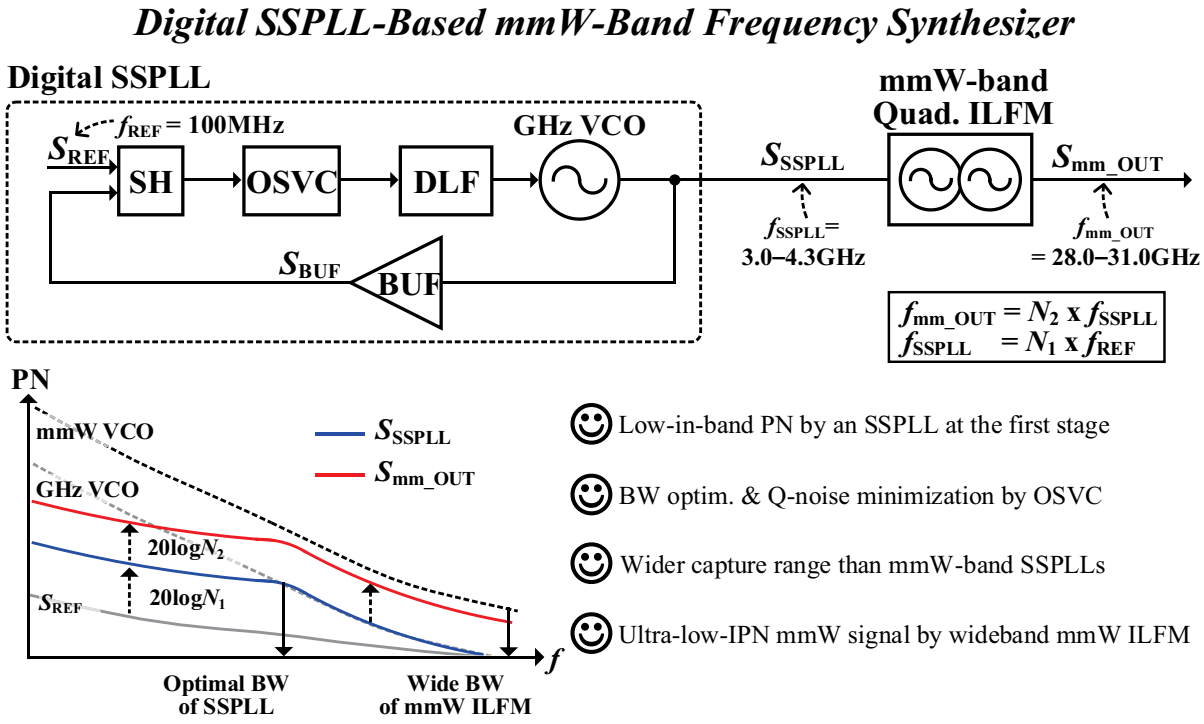
We presented an ultra-low-IPN multi-band LO generator that concurrently can support existing cellular bands below 6 GHz and new mmW bands for 5G. First, using an RFD and an *LC* VCO with a high Q-factor, a fractional-*N* PLL generated a low-phase noise signal in the GHz range. Then, the following ILFMs increased the output frequency of the PLL to higher-frequency bands without the degradation in phase noise. The ILFMs shared one low-power FTL that continuously corrected the frequency drifts of the QVCOs, thereby preventing the degradation of the IPN of the ILFMs. The fractional-*N* mode PLL and the following ILFM_x15 generated a 29.22-GHz signal that had measured IPN and RMS jitter values of −31.4 dBc and 206 fs, respectively. When ILFM_x3 was enabled, it generated a 5.76-GHz signal that had an IPN, measured as −44.1 dBc. The IPNs were low enough to comply with the EVM requirement of 64 QAM. The value of the reference spur was less than –83 dBc at the 120-MHz offset from 29.22 GHz.

5. Design of −40 dBc IPN mmW Frequency Synthesizer using digital SSPLL

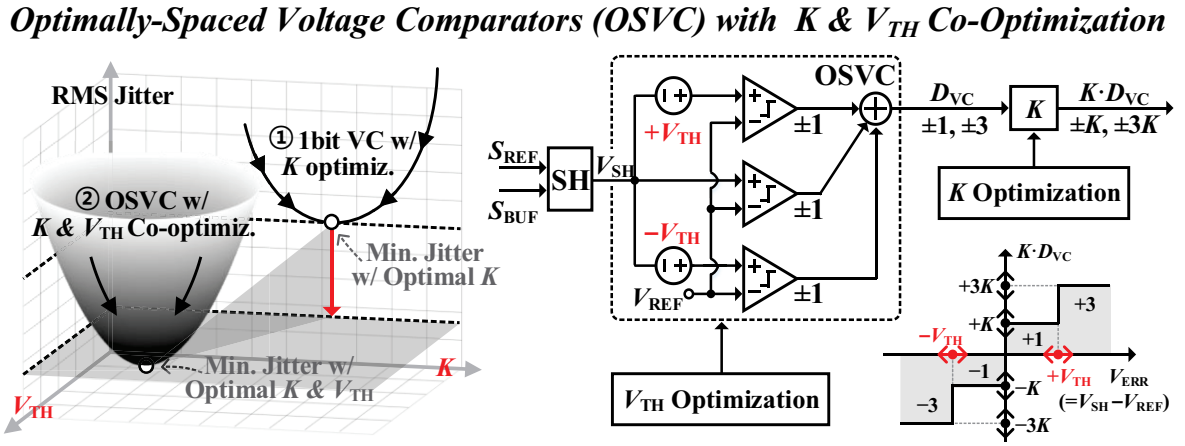
5.1 Objective and Motivation

Recently, since 5G systems require a high-data rate, an LO generator in the 5G transceivers (TRXs) must generate millimeter-wave (mmW)-band signals with an ultra-low phase noise (PN) performance. In addition, as the technology advances, a direct-conversion receiver is introduced to replace a mixer in the receiver chain. For the sampling operation, the direct RF-sampling TRXs needs a high-frequency clock signal, which must have extremely low integrated PN (IPN) [6]. Therefore, for those applications, the signals at the mmW-bands must have a low RMS jitter performance such as less than 100 fs. To achieve such a low RMS jitter, recently, [6] used the charge-pump PLL architecture and achieved a very low RMS jitter, less than 60 fs at 14 GHz. However, the reference frequency, f_{REF}, was 500 MHz to suppress the in-band phase noise from the building blocks of the PLL as much as possible. Such high reference frequency indicates that the architecture in [6] is not practical. To avoid the use of such a high f_{REF} for the minimization of the in-band phase noise, sub-sampling PLLs (SSPLLs) emerged as the solution. However, it is challenging for the SSPLL to generate the mmW-band signals directly, i.e., direct-mmW SSPLL, since the capture range of the SSPLL is rapidly narrowed as the osillation frequency increases due to the sampling operation. Thus, the reliable operation of the SSPLL operating at mmW-bands is difficult. To secure the capture range, [14] proposed to use a prescaler after the VCO. However, as like the CP PLL, it increases the in-band phase noise and also the power consumption due to the frequency divider, i.e., prescaler. In addition, an mmW VCO having a low Q-factor is a bottleneck to suppress out-band phase noise. Along with the analog SSPLLs, digital SSPLLs also have been developed by using ADCs [55] since the digital SSPLL is not suffered from a PVT-sensitive loop gain and a huge loop filter area. However, digital SSPLLs have another problem such as the quantization noise (Q-noise), which degrades overall IPN. Therefore, digital SSPLLs require high-performance ADCs that concurrently have high-sampling frequencies, fine resolutions, and wide dynamic ranges. Thus, more power consumption and larger silicon area are required.

5.2 Overall Architecture of the Proposed SSPLL-based Frequency Synthesizer



(a)



(b)

Figure 94. (a) mmW-band frequency synthesizer based on the digital SSPLL using the OSVC (b) the concept of an OSVC-based digital SSPLL with V_{TH} and K co-optimization (bottom)

This work proposes a digital SSPLL-based 28 − 31GHz frequency synthesizer (FS) that can achieve 76fs-RMS jitter and –40 dBc IPN by using the reference frequency of 100 MHz. As shown in Figure 94(a), as the first stage, the digital SSPLL generate GHz-range output signals, thereby, to secure a wide capture range. For the implementation of the digital SSPLL, the optimally-spaced voltage comparators (OSVC) is proposed to overcome the trade-off regarding the Q-noise in the conventional

digital SSPLLs. For the Q-noise minimization in the proposed OSVC, only three simple 1bit voltage comparators (VCs) are needed instead of high-performance ADC requiring a high resolution and multiple bits. Thus, the proposed work can save significant power and silicon area. Since a bandwidth of the injection-locked frequency multiplier (ILFM) following the digital SSPLL is greater than 200 MHz, the out-band phase noise of the mmW-band signal also is determined by a high-Q VCO of the GHz-range SSPLL rather than the low-Q VCO of the mmW in the ILFM. Consequently, this work can generate mmW-band output signals having ultra-low IPN and RMS jitter.

In the design of TDC-based digital PLLs, it is important to minimize the Q-noise while minimizing the power consumption. As a solution, [56] presents to use a simple BBPD instead of a complicate TDC along with the loop gain optimization of the PLL by controlling the error-correction gain, K, in the background. Even though [56] exhibits excellent power and area efficiency, it has a limitation in terms of the Q-noise minimization. This is because of a lack of information by BBPD, which only has binary information regarding the phase error. To address this limitation, [57] presented a solution, which uses three BBPDs connected in parallel and optimize the spacing between the time thresholds between BBPDs as well as K. Since to defince the thresholds is more suitable for voltage domain rather than the time domain, we apply the concept in [57] to the design of the ditial SSPLL, which is the proposed OSVC-based digital SSPLL. Figure 94(b) shows the output jitter of a 1bit-VC-based digital SSPLL. As shown, if the K is optimized by the background calibration, it can achieve a low RMS jitter performance by effectively suppressing the Q-noise. The figure also shows the OSVC-based ditial SSPLL can achieve a better RMS jitter by co-optimizing the voltage threshold value between VCs, V_{TH}, and K. In the conceptual diagram of an OSVC-based digital SSPLL shown in Figure 94(b), a sample-and-hold (SH) circuit samples the level of S_{BUF} and outputs V_{SH}, which is V_{SH} is compared with V_{REF} by the three VCs having different input offsets, i.e., $+V_{TH}$, 0, and $-V_{TH}$, which had been inserted intentionally. Then, the voltage error, V_{ERR}, is converted one of the four values of D_{VC}. Lastly, the OSVC can minimize instantaneous phase errors more precisely and the Q-noise, concurrently, with the optimized V_{TH} and K. Since the delta-sigma-based DACs (ΔΣDACs), which can provide a fine resolution, can be used to calibrate V_{TH}, the concept of the OSVC is more effective in the voltage domain than the time domain.

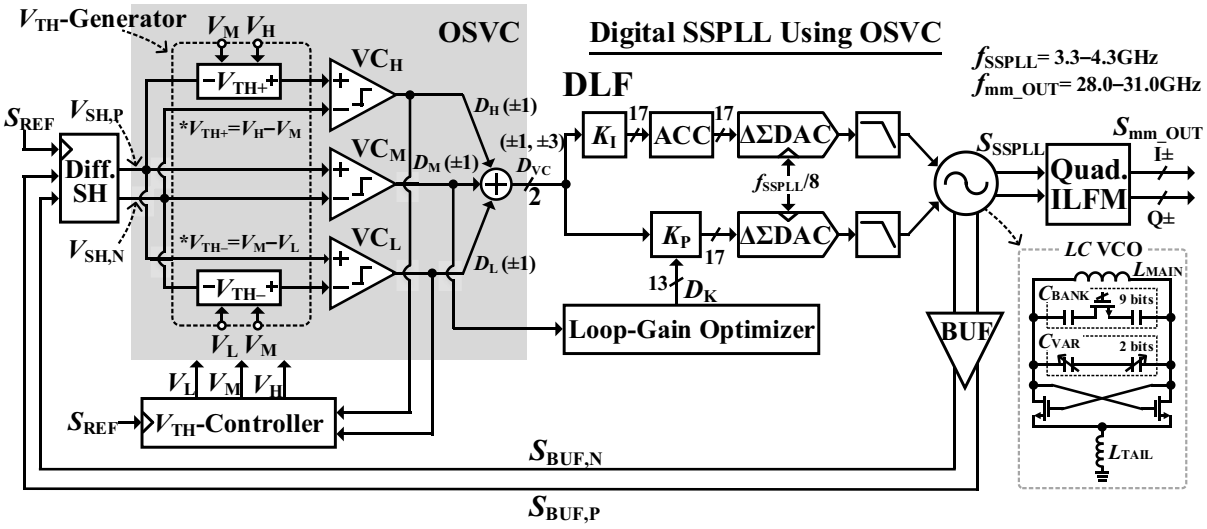
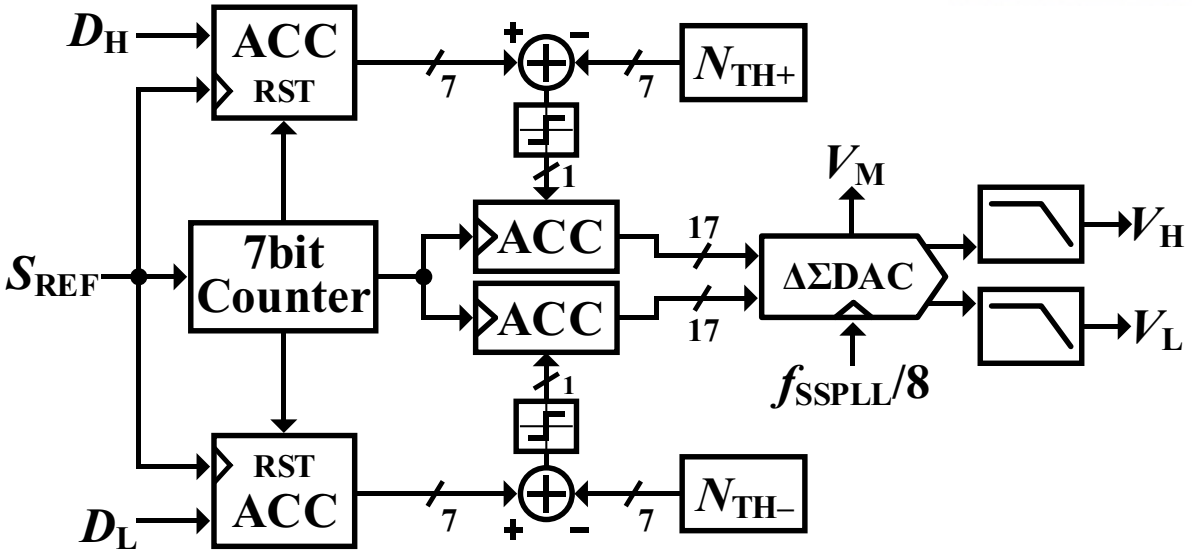
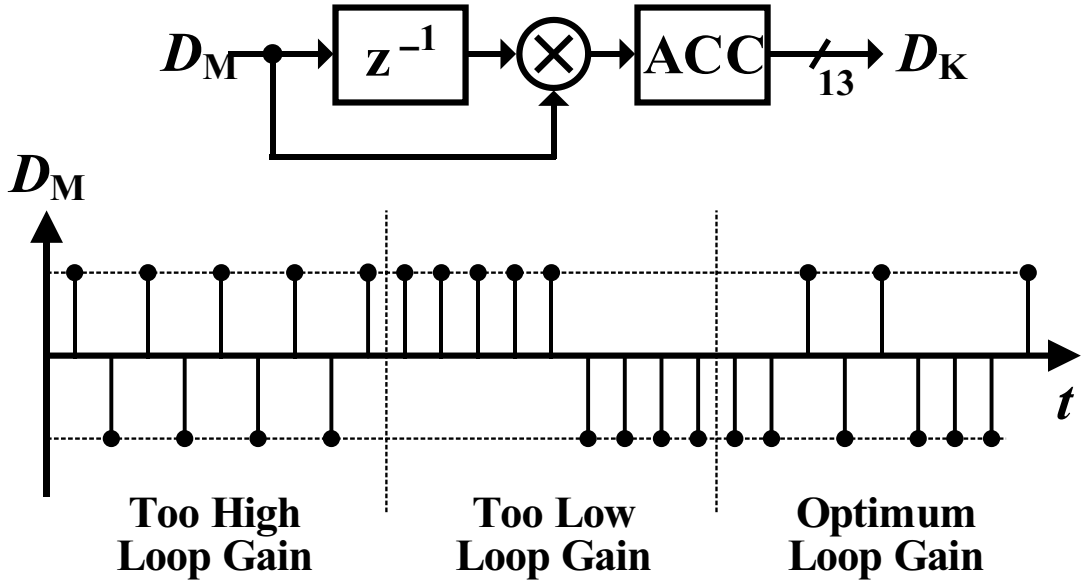


Figure 95. Overall architecture of the mmW-band frequency synthesizer

Figure 95 shows the overall architecture of the mmW-band frequency synthesizer, including the OSVC-based digital SSPLL and the mmW ILFM [21]. In the digital SSPLL, the three voltage comparators quantizes the difference between $V_{SH,P}$ and $V_{SH,N}$, which are the differentially sampled voltages by the SH. The quantized output values of VC_H, VC_M, and VC_L are D_H, D_M, and D_L, respectively. As shown, the OSVC has four decision values in D_{VC} by placing the offset voltage of V_{TH+} to the positive input of VC_H and that of V_{TH-} to the negative input of VC_L. As shown in Figure 96(a), two input offset voltages should be adjusted independently by using the three voltages provided by the V_{TH}-controller, V_H, V_M, and V_L to optimize V_{TH+} and V_{TH-} even with the presence of the intrinsic input offsets of the VCs. By referring [57], the value of V_H and V_L can be optimized by the V_{TH}-controller; when the the optimal values of N_{TH+} and N_{TH-} are compared with the accumulated values of D_H and D_L, respectively. The the combination of a ΔΣDAC and the low-pass filters allows V_H and V_L to have a high resolution, i.e., effectively 10 fs in time domain. V_M is the reference value and it is the half of DAC supply voltage. Note that, if the output of ΔΣDAC is monotonous, the input offsets of the three voltages comparator and the non-linearity of the ΔΣDAC have no problem due to the continuously optimized and back-ground calibrated values of V_{TH+} and V_{TH-}. The digital loop filter consists of the proportional (P) and the integral (I) paths. As shown, the VCO is controlled separately by both paths to minimize a latency, which could degrade the jitter performance. As shown in Figure 96(b), by ensuring zero autocorrelation of D_M [56], the loop-gain optimizer can keep adjusting the P-path gain, K_P, to be optimum. The settling time of K_P is less than 750μs at the worst case.



(a)



(b)

Figure 96. (a) the schematics of the V_{TH}-controller and (b) loop-gain optimizer

5.3 Operation of the Proposed SSPLL-based Frequency Synthesizer

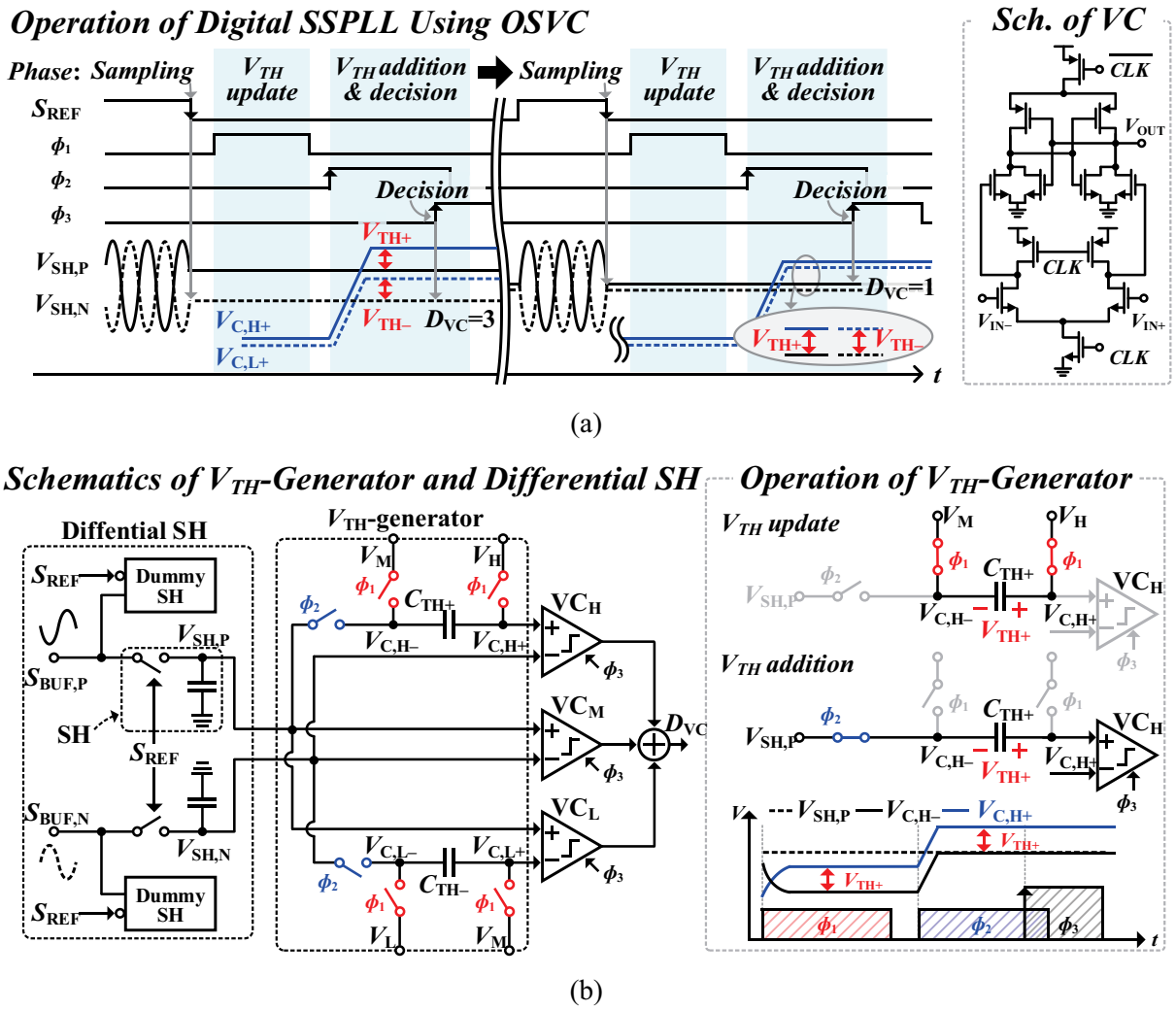


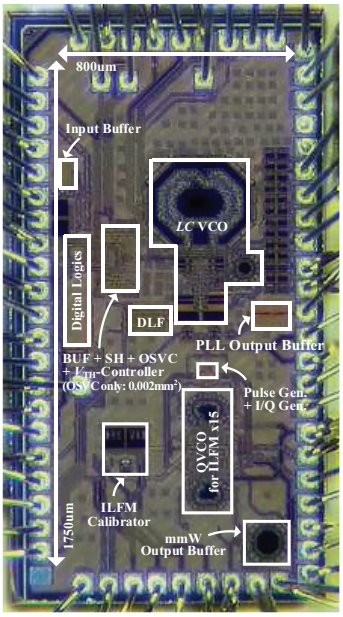
Figure 97. (a) Operation of the proposed digital SSPLL using the OSVC (b) the schematics and operation of the OSVC

Figure 97(a) and (b) shows the operation of the proposed OSVC-based SSPLL in the time domain and the schematics of the differential sample-and-hold circuits and the following V_{TH}-generator, respectively. The overall operation is as follows. First, the sampling of $V_{SH,P}$ and $V_{SH,N}$ is happend by the sample-and-hold circuit at the falling edge of S_{REF}. Second, in *'V_{TH} update'* phase, i.e., during ϕ_1, the voltage difference across C_{TH+} (or C_{TH-}) is redefined by the outputs of the V_{TH}-generator, V_H and V_M (or V_M and V_L), to update the value of V_{TH+} (or V_{TH-}). Third, in *'V_{TH} addition'* phase, i.e., during ϕ_2, the connection between $V_{C,H-}$ (or $V_{C,L-}$) and $V_{SH,P}$ (or $V_{SH,N}$) is rebuilt to add V_{TH+} (or V_{TH-}) to the input of VC_H (or VC_L). Finally, in *'Decision'* phase, i.e., at the rising edge of ϕ_3, decisions are happened by the three voltage comparators to provide D_{VC}. Note that, in the design of the V_{TH}-generator, the sizes of the switches and that of the input transistors of the voltage comparators are minimized and optimized to minimize the

charge-sharing effect, which is usually occurred by the parasitic capacitors. If the charge-sharing effect is severe, it could degrade the gain of the sample-and-hold circuits. The voltage comparators were implemented based on a double-tail regenerative topology.

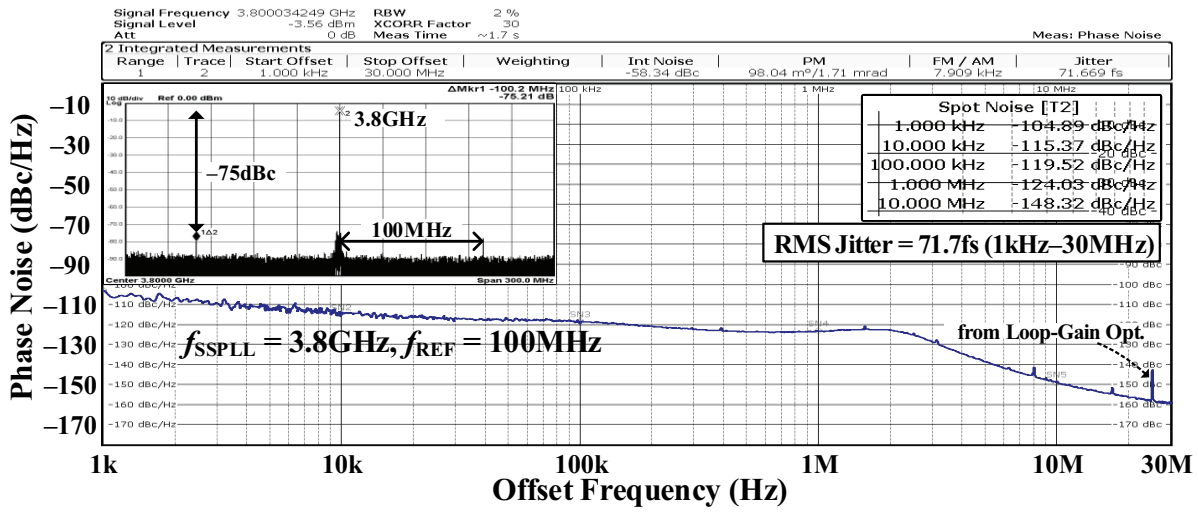
5.4 Experimental Results

The proposed mmW frequency synthesizer based on the OSVC-based SSPLL and the ILFM was fabricated in 65nm CMOS technology. The die photograph is shown in Figure 98 along with the power breakdown table. The total power consumption was 41.8 mW and the occupied area was 0.32 mm^2. Figure 99(a) and (b) show the measure phase noise of the OSVC-based SSPLL when the output signal at 3.8 and 3.9 GHz, respectively. The measurement results show that the proposed OSVC-based SSPLL achieved very low in-band phase noise, i.e., less than –114 dBc/Hz at the 10 kHz offset at both cases. Therefore, both cases at 3.8 and 3.9 GHz, the achieved IPN was less than −58 dBc and the measured RMS jitter was also less than 72 fs.

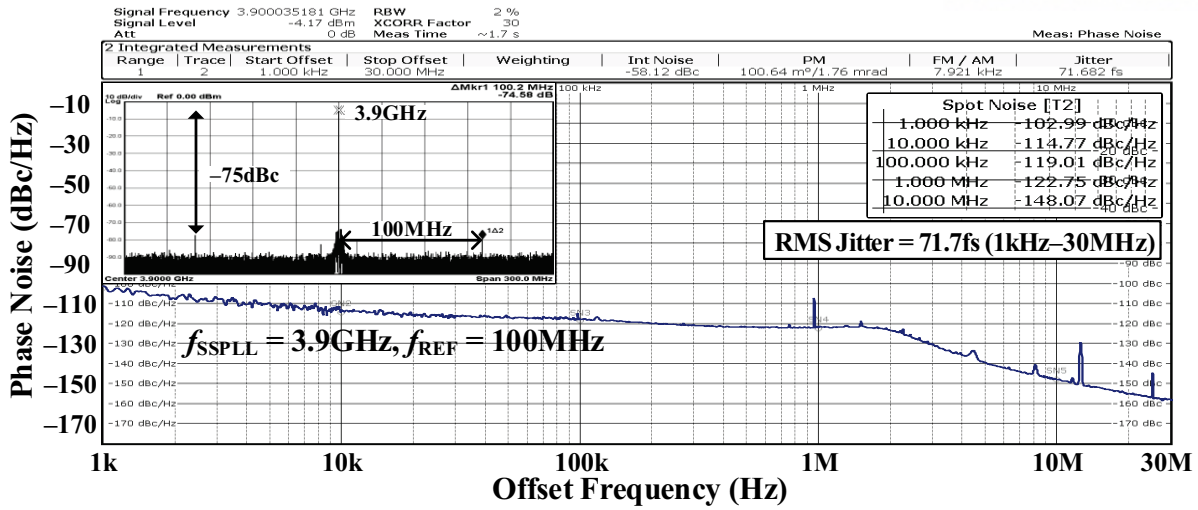


Power Consumption (mW)		
PLL (19.1)	GHz *LC* VCO	8.0
	BUF (Before SH) + SH	7.0
	Digital Logics (Loop-gain Opt., etc.) + V_{TH}-Controller + DLF	4.0
	OSVC	0.1
ILFM /2 x 15 (22.7)	Pulse Gen. + I/Q Gen.	11.4
	mmW-Band QVCO	10.4
	ILFM Calibrator	0.9
Total		41.8

Figure 98. Die photograph and power-breakdown table



(a)



(b)

Figure 99. When the reference frequency, f_{REF}, was 100MHz, (a) measured phase noises and spectrums of 3.8 GHz-output signals of the OSVC-based digital SSPLL (b) measured phase noises and spectrums of 3.9 GHz-output signals of the OSVC-based digital SSPLL

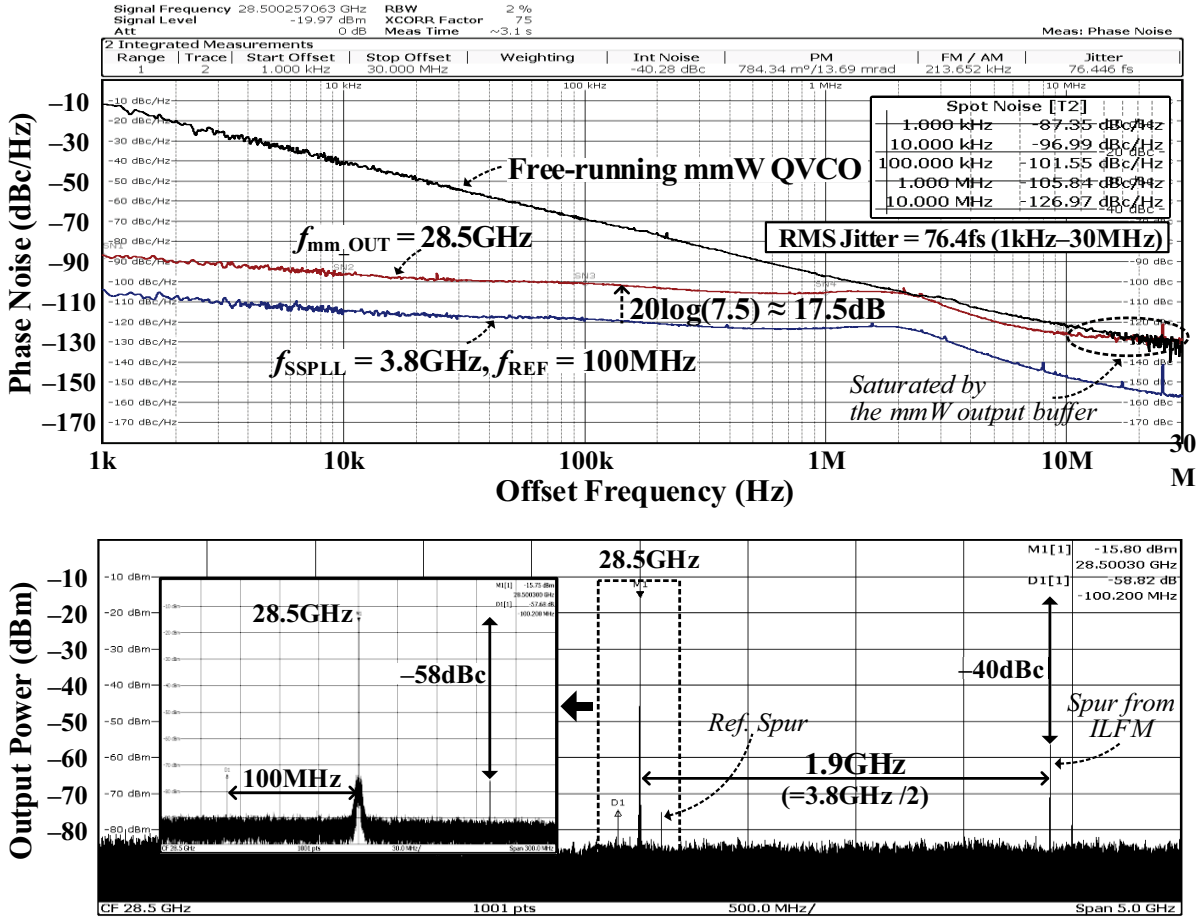


Figure 100. Measured phase noise and spectrum of the 28.5GHz signal of the proposed mmW-frequency synthesizer

Figure 100 shows the measured phase noise and spectrum when the proposed mmW-frequency synthesizer operates at 28.5 GHz. The mmW output signal was generated; First, after divide the 3.8 GHz signal of the SSPLL by 2 for the quadrature signal generation. Then, using the 1.9 GHz signal, the PG can generate injection pulses and transfer those to the ILFM. Then, the mmW-band ILFM multiplies a factor of 15 to the 1.9 GHz signal to generate 28.5 GHz signal. As shown in Figure 100, the mmW FS of this work achieved –40.3 dBc IPN and 76fs-RMS jitter at 28.5 GHz. It also shows the phase noise of the frequency synthesizer's output signal at 28.5 GHz follows that of the SSPLL's output at 3.8 GHz with a constant gap of 17.5 dB, which corresponds to the 20log(7.5). Table 14 compares the performance of the proposed OSVC-based digital SSPLL with the performances of state-of-the-art SSPLLs. As shown in Table 14, the proposed digital SSPLL achieved the lowest RMS jitter among the state-of-the-art SSPLLs. Also, this work achieved FOM_{JIT} of −250.1 dB, which is the competitive value among the SSPLLs.

Table 14. Comparison with state-of-the-art SSPLLs

	This work	**JSSC'18 D. Liao**	**ISSCC'15 [55] Z. Chen**	**ISSCC'15 T. Siriburanon**	**ISSCC'18 A. Sharkia**
Process	65nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	Digital SSPLL	Analog SSPLL	Digital SSPLL	Digital SSPLL	Analog SSPLL
Topology	OSVC-based	SS-PD based	ADC-based	ADC-based	SS-PD based
Type	Integer-*N*	Fractional-*N*	Fractional-*N*	Integer-*N*	Integer-*N*
f_{SSPLL} (GHz)	3.1–4.3	2.39–2.46	2.6–3.9	2.2	4.6–5.6
f_{REF} (MHz)	100	50	49.15	100	100
$Jitter_{RMS}$ (fs) @f_O (GHz) (Integ. Range)	72 @3.8 (1 k–30 MHz)	169 @2.397 (10 k–30 MHz)	226 @2.68 (1 k–100 MHz)	380 @2.2 (10 k–40 MHz)	185 @5.0 (10 k–50 MHz)
Ref. spur (dBc) @f_O (GHz)	–75 @3.8	–72 @2.397	–60 @2.68	–74 @2.2	–64 @5.0
Power Cons. (P_{DC}) (mW)	19.1	21.0	11.5	4.2	1.1
Active Area (mm^2)	0.21	0.43	0.23	0.15	0.01
FoM_{JIT} (dB)**	–250.1	–242.2	–242.3	–242.2	–254.2

Table 15 compares the performance of the proposed mmW frequency synthesizer using OSVC-based digital SSPLL and the ILFM with the performances of state-of-the-art mmW-band frequency synthesizers. As shown this work achieved 76 fs RMS jitter and the IPN of −40.4 dBc, respectively, which are the lowest value among the mmW frequency synthesizers. In addition, this work achieved the best $FOM_{JIT,N}$ (normalizing FOM_{JIT} to f_{REF}) and the best FOM_{JIT} among the state-of-the-art mmW frequency synthesizers.

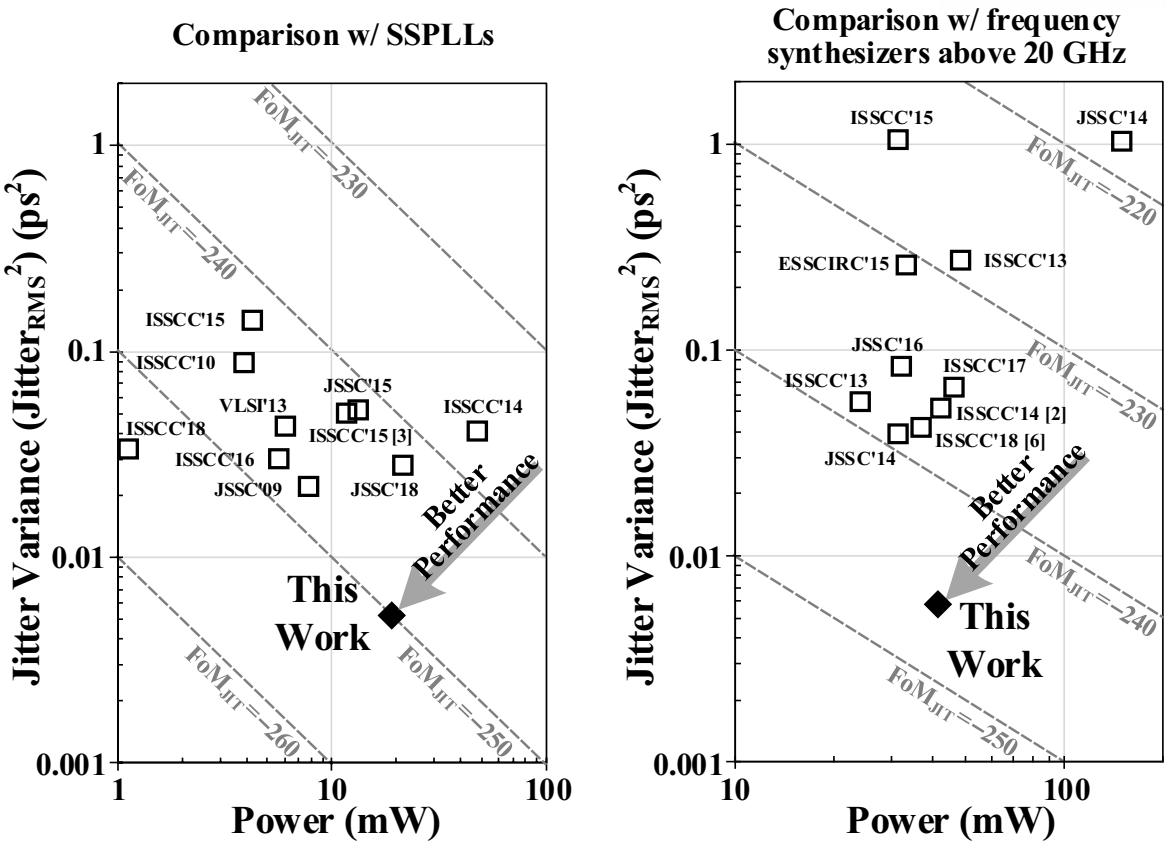
Table 15. Comparison with state-of-the-art mmW-band frequency synthesizers

	This work	**ISSCC'14 [14] V. Szortyka**	**ISSCC'17 [11] A. Hussein**	**ISSCC'18 [21] H. Yoon**	**JSSC'16 [16] T. Siriburanon**
Process	65nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	GHz-Digital SSPLL + ILFM	60GHz SS QPLL	All-Digital PLL	RFD + GHz-PLL + ILFMs	20GHz SSPLL + 60GHz QILO
Type	Integer-*N*	Integer-*N*	Fractional-*N*	Fractional-*N*	Integer-*N*
Quadrature	YES	YES	NO	YES	YES
f_{OUT} (GHz)	28.0–31.0	53.8–63.3	50.2–66.5	25.0–30.0	55.6–65.2
f_{REF} (MHz)	100	40	100	120	40
$Jitter_{RMS}$ (fs) @f_O (GHz) (Integ. Range)	76 @28.5 (1 k–30 MHz)	230 @62.64 (1 k–100 MHz)	258 @65.35 (1 k–40 MHz)	206 @29.22 (1 k–100 MHz)	290 @60.5 (10 k–40 MHz)
IPN (dBc) Norm. to 28GHz (Integ. Range)	–40.4 (1 k–30 MHz)	–30.8 (1 k–100 MHz)	–29.9 (1 k–40 MHz)	–31.8 (1 k–100 MHz)	–28.8* (10 k–40 MHz)
In-band noise (@10kHz) (dBc/Hz) Norm. to 28GHz	–97.1	–88.1*	–86.1	–89.0	–85.2
Ref. spur (dBc) @f_O (GHz)	–58 @28.5	–40 @62.64	NA	–83 @29.22	–73 @60.5
Power Cons. (P_{DC}) (mW)	41.8	42.0	46.0	36.4	32.0
Active Area (mm^2)	0.32	0.16	0.45	0.95	1.08 w/ pads
FoM_{JIT}(dB)**	–246.1	–236.5	–235.1	–238.1	–235.7
$FoM_{JIT,N}$ (dB)***	–270.7	–268.5	–263.3	–262.0	–267.5

*Calculated from measurements

**$FoM_{JIT}=10\log(\sigma_t^2 \cdot P_{DC})$ dB

***$FoM_{JIT,N}=10\log(\sigma_t^2 \cdot P_{DC}/(f_{OUT}/f_{REF}))$ dB (K. M. Megawer, ISSCC'18)



(a) (b)

Figure 101. (a) Benchmarking FOM_{JIT} for SSPLLs and (b) benchmarking FOM_{JIT} for frequency synthesizers of which the output frequencies are above 20 GHz (right)

Figure 101(a) and (b) show the benchmarking FOMs of recent SSPLLs and frequency synthesizers operating above 20 GHz, respectively. According to the benchmarks in Figure 101, the proposed digital SSPLL achieved the lowest RMS jitter among all state-of-the art SSPLLs, and the proposed mmW-band frequency synthesizer achieved not only the lowest RMS jitter but also the best FOM_{JIT} among all mmW-band frequency synthesizers operating above 20 GHz.

5.5 Conclusions

In this work, we presented a mmW-band frequency synthesizer that can generate 28 – 31 GHz output signals with less than –40-dB IPN by cascading a GHz-range digital SSPLL having an ultra-low phase noise and a mmW-band ILFM having a wide noise-rejection bandwidth. Using the sub-sampling operation and the effect of the Q-noise reduction due to the proposed OSVC, the digital GHz-range SSPLL at the first stage can achieve a very low in-band phase noise. In addition, a high-Q *LC* VCO at a GHz range help suppressing the out-band phase noise of the SSPLL. Since the OSVC uses only three 1-bit VCs, it requires small power and small silicon area, although it can achieve the significant effect to reduce the Q-noise. At the second stage, the ILFM adds little intrinsic in-band noise, and it also provides a very wide VCO-noise-reduction bandwidth. Therefore, it can multiply GHz-range input frequencies to mmW-band output frequencies with the least increase in the RMS jitter, resulting in ultra-low RMS jitter and IPN of –40 dBc and 76 fs, respectively.

6. Design of Wideband and Low Phase Noise Quadrature LO-Generator

6.1 Objective and Motivation

Cellular transceivers today need to support multiple standards from 2G to 4G in different networks all over the world in order to be competitive globally. To meet this demand, the frequency range of local oscillation (LO)-signals of transceivers must be substantially wide. LO-signals must also satisfy the stringent phase noise requirements of each standard. Thus, the design of a wideband LO-signal generator (LO-generator) for a multi-standard cellular transceiver is very challenging.

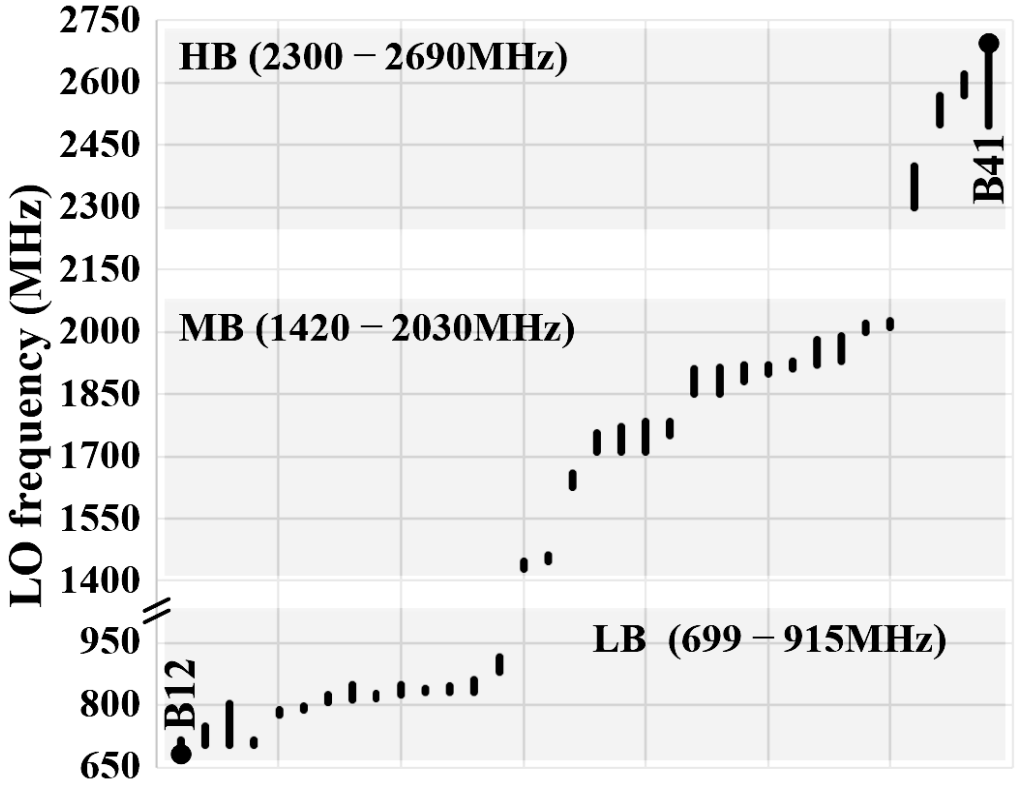


Figure 102. Frequency range for multi-standard cellular transceivers

Figure 102 shows the frequencies of LO-signals (LO-frequencies) for recent cellular transceivers that support multiple standards, such as 2G GSM, 3G WCDMA, and 4G LTE [5]. To obtain wideband LO-frequencies from 699 to 2690 MHz in an efficient manner, a cellular transceiver must have an adequate plan for the generation of LO-frequencies (LO-plan). Figure 103 shows the most popular LO-plan for cellular transceivers, which consists of divide-by-2 and divide-by-4 dividers after voltage-controlled oscillators (VCOs). One of the main reasons for the popularity of this LO-plan is that dividers with a division ratio of 2 or a multiple of 4 can easily generate quadrature signals that are essential for transceivers using I/Q modulations [58]–[60]. However, when this conventional LO-plan is used, the minimum requirement of the frequency-tuning range (FTR) of VCOs must increase to more than 63% to cover the minimum and the maximum frequencies, as marked by the dashed circles in Figure 103.

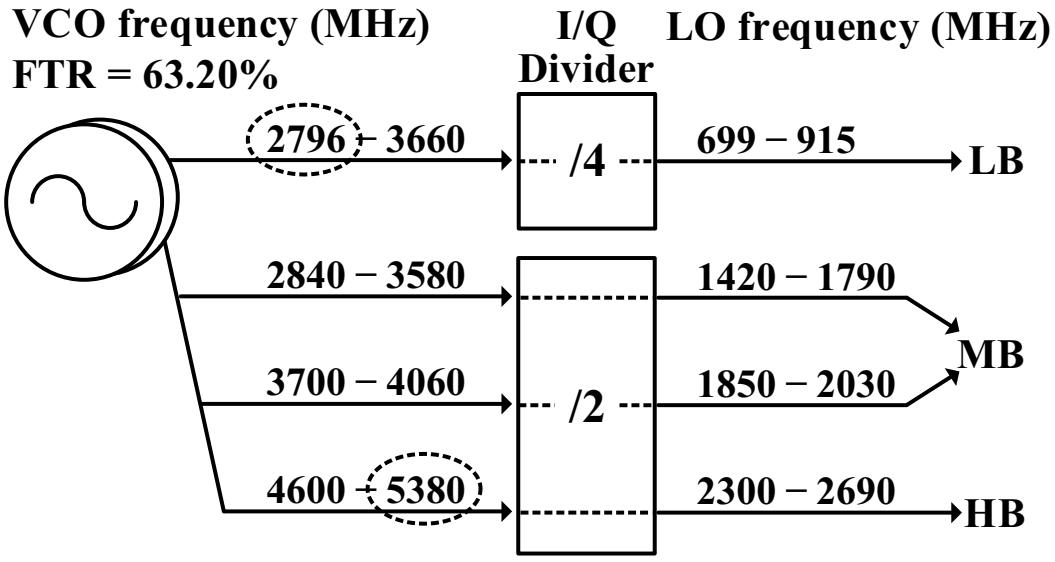


Figure 103. Conventional LO-plan for multi-standard cellular transceivers, where the required FTR of VCOs is 63%

Even though a divide-by-8 divider can be added to the LO-plan of Figure 103, the required FTR still must be larger than 55%. Moreover, if we want to prepare an additional margin considering possible frequency shifts due to process-voltage-temperature (PVT) variations, the FTRs of the VCOs must be extended up to 70 or 80%. Since a typical low phase noise *LC*-VCO, as noted, can hardly achieve a FTR of more than 60%, the conventional LO-plan inevitably asks for a transmitter (TX) and a receiver (RX) to include multiple VCOs [61]–[66]. If a transceiver must use multiple chains of TXs and RXs for carrier-aggregation (CA) [67], [68], the number of required VCOs soars. Since an *LC*-VCO is an area-hungry circuit due to its high-quality passive components, the integration of a large number of VCOs causes a significant increase in silicon area and cost.

In recent years, many attempts have been made to design wideband *LC*-VCOs with FTRs greater than 80% [69]–[73]. The VCOs of [69], [70] used techniques involving transformers to switch the bands of resonant frequencies. Reference [71] proposed an active inductor in the resonant tank, allowing its effective inductance to be varied. In [72], [73], a switch across the loop of the inductor shifted its resonant band when it was on or off. However, all of these methods inevitably degraded the quality factor (Q-factor) of *LC*-tanks. Thus, it is very difficult for VCOs that use these methods to satisfy the stringent phase noise requirements of cellular standards, such as spot noise at 400-kHz and 20-MHz offsets for GSM [74]–[77].

In addition to the efforts to extend the FTRs of *LC*-VCOs, structural ideas on wideband LO-generation have been reported in [78]–[89]. References [78]–[83] used quadrature VCOs (QVCOs), in which two differential *LC*-VCOs were coupled in a crosswise fashion. Since a QVCO can intrinsically generate quadrature signals at VCO frequencies, when it is used with quadrature dividers or single

sideband (SSB) mixers, the required FTR can be reduced significantly. However, a QVCO includes two *LC*-tanks; thus, LO-generators using QVCOs bring no advantages in minimization of silicon area. In [84], [85], more than 67% FTRs were obtained from two *LC*-VCOs. Then wideband LO-frequencies were generated using chains of typical divide-by-2 dividers. However, two *LC*-VCOs were still required, and the use of a large number of dividers, 6 or 7 in series, causes high power consumption. References [86], [87] used poly-phase filters (PPFs) to generate quadrature phases. However, the use of passive *RC*-filters for PPFs reduces the levels of the signals. Moreover, the accuracy of quadrature phases from PPFs is too sensitive to PVT variations. References [88], [89] used injection-locked ring oscillators (ILROs) to generate wideband LO-signals. Using a multi-stage ring VCO, an ILRO can operate as a quadrature divider without restricting its division ratio to a particular value, 2 or any multiple of 4. With various options on division ratios, the required FTR can be minimized to a reasonable level that can be covered by one *LC*-VCO. However, the operation and the performance of ILROs are very vulnerable to PVT variations due to its narrow lock range. Thus, the phase noise is degraded as input frequencies deviate from the specific harmonic frequency of the free-running oscillator of the ILRO [90]. Furthermore, if the deviation is out of the lock range, the divider cannot acquire the division ratio targeted. Thus, for reliable operation, ILRO-based wideband LO-generators must include dedicated PVT calibrators [89].

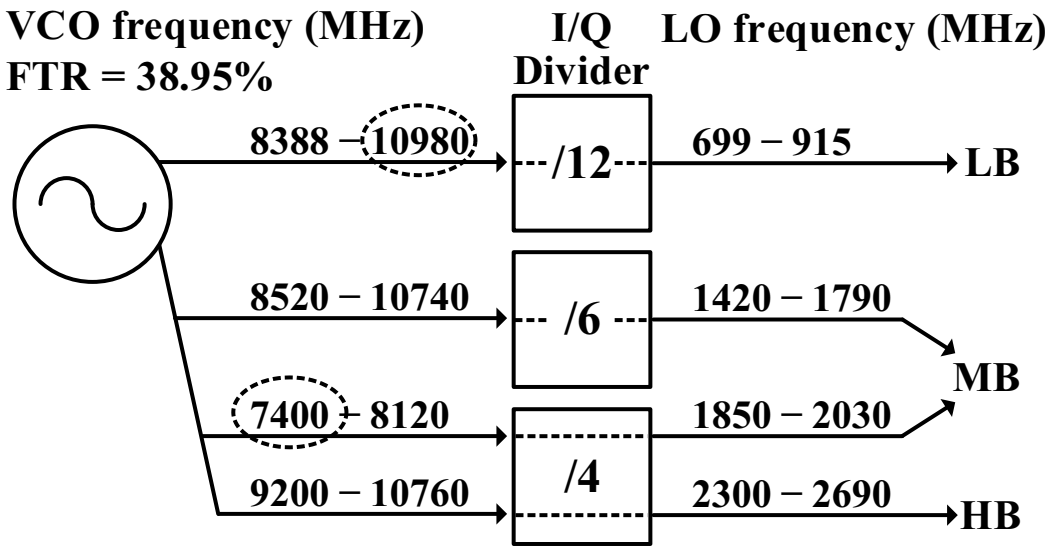


Figure 104. New LO-plan using divide-by-12, divide-by-6, and divide-by-4 dividers, where the required FTR of a VCO is 39%

In this work, we proposed a wideband and low phase noise quadrature LO-generator using a single *LC*-VCO and simple frequency dividers. Using divide-by-6, divide-by-4, and divide-by-12 dividers, the new LO-plan, shown in Figure 104, can minimize the required FTR to less than 39%, which can be

easily covered by one *LC*-VCO. The key building block of this new LO-plan is a quadrature divide-by-6 divider that can generate accurate I/Q signals. To implement the quadrature divide-by-6 circuit, we proposed a fully differential divide-by-3 divider with 50% duty cycle that can address limitations in conventional architectures, which are discussed in Chapter 6.2. Using the proposed divide-by-3 divider followed by a conventional divide-by-2 divider, the divide-by-6 divider can generate precise I/Q signals. The idea of the proposed divide-by-3 divider was also used in the design of a new differential divide-by-2 circuit for the divide-by-4 and the divide-by-12 dividers of the LO-generator.

The proposed LO-generator was fabricated in a 40-nm CMOS process. Due to the relaxed requirement on the FTR by the new LO-plan, the LO-generator included a single *LC*-VCO. Additionally, the size of the tank-inductor was reduced because of the high VCO frequencies of the new LO-plan. Therefore, we were able to integrate the proposed LO-generator in a compact silicon area. With a high Q-factor due to its small FTR, the VCO achieved low phase noise; thus, LO-signals satisfied the stringent phase noise requirements of current cellular standards.

This Chapter consists of the following sections. Chapter 6.2 presents the architecture of the proposed LO-generator and implementation of the quadrature divide-by-6 divider, using the proposed differential divide-by-3 divider with 50% duty cycle. Chapter 6.3 presents the differential divide-by-2 divider for quadrature divide-by-4 and divide-by-12 dividers. The circuit details of other building blocks are covered in Chapter 6.4. Experimental results are presented in Chapter 6.5, and conclusions are drawn in Chapter 6.6.

6.2 Proposed LO-generator using the Quadrature Divide-by-6 Divider

6.2.1 Overall Architecture of the Proposed Quadrature LO-Generator

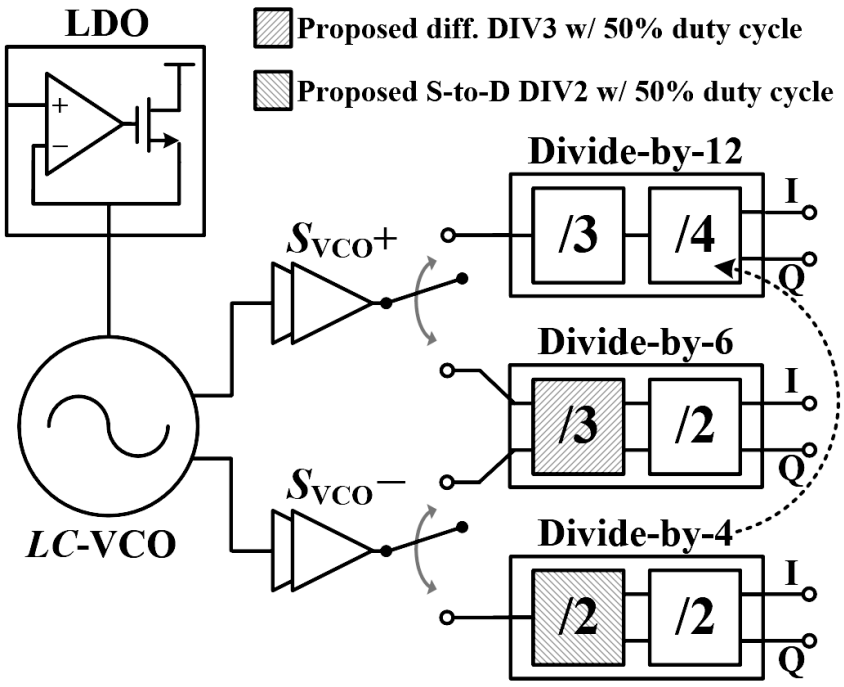


Figure 105. Overall architecture of the proposed LO-generator

Figure 105 shows the proposed wideband and low phase noise LO-generator for multi-standard cellular transceivers, which consists of an *LC*-VCO and three LO-dividers: divide-by-12, divide-by-6, and divide-by-4 dividers. Due to the proposed LO-plan, as shown in Figure 104, the FTR requirement was reduced to 39%, which can be covered by a single *LC*-VCO with a high Q-factor. The VCO is provided with its core current from an LDO, enhancing power-supply rejection (PSR) and current controllability. Through inverter-based VCO buffers, the differential output signals of the VCO, $S_{VCO}+$ and $S_{VCO}-$, are delivered to one of three LO-dividers. As shown in Figure 105, the divide-by-6 divider consists of the proposed differential divide-by-3 divider with 50% duty cycle and the following conventional divide-by-2 divider. The divide-by-4 divider used a new single to differential (S-to-D) divide-by-2 divider based on the idea of the proposed divide-by-3 divider, preceding the conventional divide-by-2 divider. This divide-by-4 divider was used following the conventional divide-by-3 divider in the divide-by-12 divider. All dividers were designed using true single-phase clock (TSPC) D-flip-flops (DFFs) [91]. It is generally noted TSPC DFF-based dividers have lower operating frequencies than current mode logic-based (CML-based) counterparts. However, due to recent scaling-down of CMOS technologies, TSPC-based dividers can now operate at frequencies of several tens of GHz. Moreover, they have lower power consumption without static current and occupy smaller area. They also are able to operate under a low supply voltage and have large output swings [92].

6.2.2 Limitations in Conventional Divide-by-3 Dividers

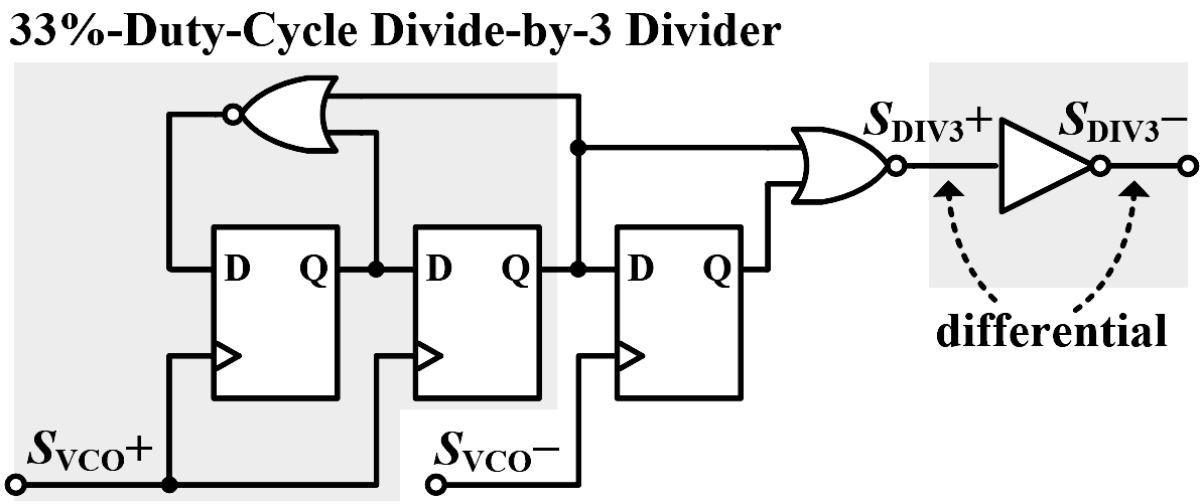


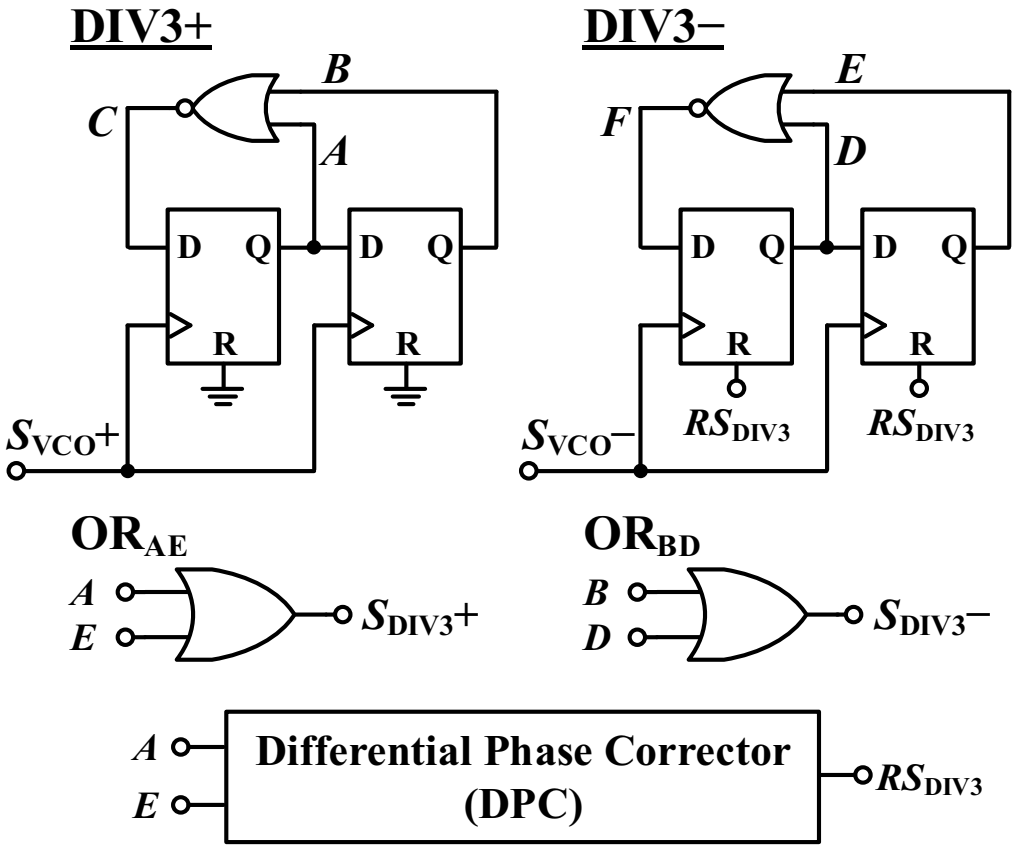
Figure 106. Conventional DFF-based divide-by-3 divider

Figure 106 shows a conventional DFF-based divide-by-3 divider [28]. The core of the divider consists of two DFFs, triggered by $S_{VCO}+$, and one NOR gate, but it generates 33% duty cycle. Using the additional DFF triggered by $S_{VCO}-$ and the following NOR gate, it can generate divided signals with 50% duty cycle. Since it has a single output, an inverter must be added after the NOR gate to obtain differential outputs of $S_{DIV3}+$ and $S_{DIV3}-$. However, the propagation delay of the inverter that generates $S_{DIV3}-$ must produce a phase error between the differential signals. Moreover, if the duty cycle of $S_{DIV3}+$ is not perfectly 50% due to some non-idealities of DFFs or NOR gates, $S_{DIV3}-$ cannot be the differential pair of $S_{DIV3}+$. Consequently, there must be an inevitable I/Q phase error between the quadrature signals after the following quadrature divide-by-2 divider. The effect of the propagation delay of the inverter becomes conspicuous at high frequencies. For example, when the VCO frequency is 10 GHz, the I/Q phase error due to the inverter becomes 6° even if its delay is minimized to only 10 ps. Even if the inverter delay is compensated by a pass-gate, it is impossible to match the delays of the inverter and the pass-gate perfectly over a wide range of VCO frequencies and various PVT conditions. While an architecture that uses a multi-stage ILRO can be considered to design differential divide-by-3 dividers [93]–[95], the operation of an ILRO is too sensitive to PVT variations due to its narrow lock range [90]. This problem is critical when the target range of LO-frequencies is very wide, as was the case in this work.

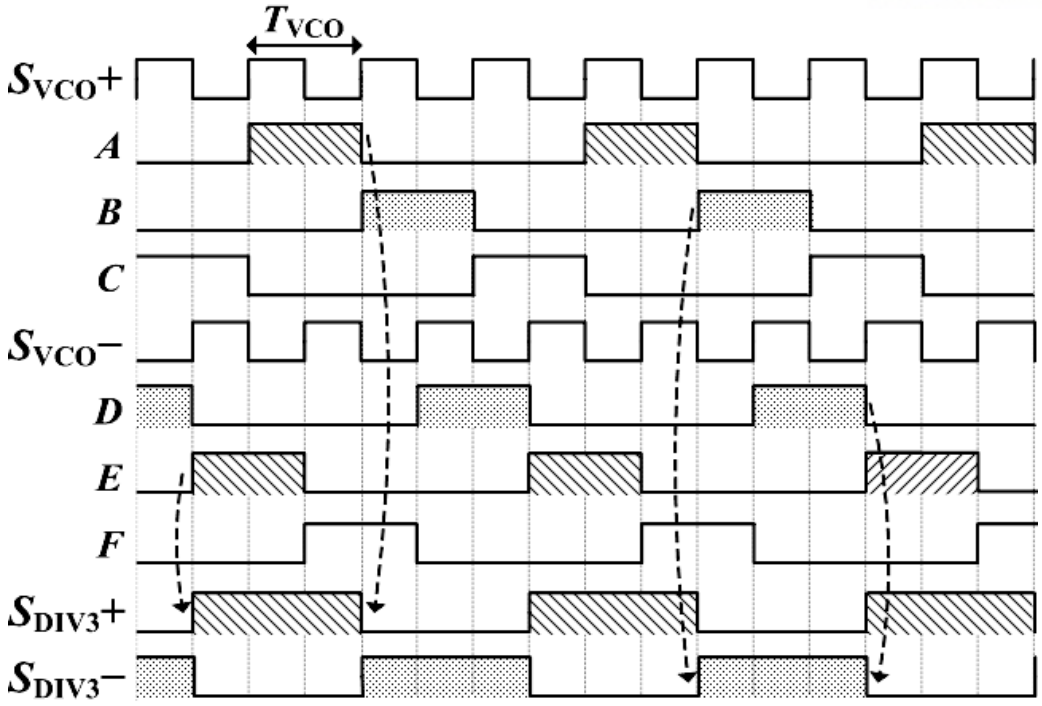
6.2.3 The Proposed Differential Divide-by-3 Divider with 50% Duty-Cycle

Figure 107(a) and (b) show the implementation and the timing diagrams of the proposed fully differential divide-by-3 divider with 50% duty cycle, respectively. The divider includes two identical divide-by-3 dividers with 33% duty cycle, DIV3+ and DIV3−, which are triggered by $S_{VCO}+$ and $S_{VCO}-$, respectively. As shown in Figure 107(b), the two dividers generate six signals having 33% duty cycle, $A - F$, in which the phases are spaced evenly in the order of A, F, B, D, C, E, and the difference of any two consecutive phases is 60°. Using two OR gates, OR_{AE} and OR_{BD}, that crossly combine the pulses of A and E and B and D, respectively, differential output signals with 50% duty cycle, $S_{DIV3}+$ and $S_{DIV3}-$, can be obtained. All rising and falling edges of $S_{DIV3}+$ and $S_{DIV3}-$ originate only from rising edges of $S_{VCO}+$ and $S_{VCO}-$, and no falling edges of $S_{VCO}+$ and $S_{VCO}-$ are used. Thus, the differential phase and 50% duty cycle become very accurate, even if the duty cycle of $S_{VCO}+$ or $S_{VCO}-$ deviates from 50%.

For the proposed divider to operate correctly as described above, signals $A - F$ must be lined up in the same order as in Figure 107(b). This implies that the detection of $S_{VCO}+$ by DIV3+ must precede that of $S_{VCO}-$ by DIV3− by one and half the VCO period, T_{VCO}, in other words, the rising edge of A must occur earlier than that of D by $1.5T_{VCO}$. However, due to the non-deterministic initial conditions, the sequence of Figure 107(b) could be disarranged. If this occurs, $S_{DIV3}+$ and $S_{DIV3}-$ would not become differential.



(a)



(b)

Figure 107. (a) Proposed divide-by-3 divider for differential outputs with 50% duty cycle (b) timing diagrams under normal operation

For the reliable operation of the divider in any environmental conditions, the proposed divider uses a differential phase corrector (DPC) that resets DIV3− until the sequence of the signals is correct, as shown in Figure 107(b). Figure 108(a) shows the implementation of the DPC. Considering sufficient set-up time for the dividers after being reset, the frequency of the DPC clock, CK_{DPC}, is reduced by a divide-by-4 divider, triggered by A. As shown in Figure 107(b), the level of E at the rising edge of A must be high under normal operation; E leads A by $0.5T_{VCO}$. Thus, by checking the level of E at the rising edge of A, the proposed DPC can detect any incorrect operations of the divider, and one DFF and one inverter are used to generate the detecting signal, S_{EA}b. In any abnormal cases, S_{EA}b becomes high, which generates a reset pulse, RS, at the rising edge of CK_{DPC}. To properly reset DIV3−, the timing of the falling edge of the reset pulse is important. It must present between the two consecutive rising edges of S_{VCO}−, where one rising edge is when A is high, and the other is when B is high, as marked in gray in Figure 108(b). However, since the period of S_{VCO}− for this LO-plan is very short, the falling edge of RS can easily fall out of the valid range due to the change of the pulse width of RS, τ_{PW}, or propagation delays of DFFs of the divide-by-4 divider, τ_{CK}, which are vulnerable to PVT variations. In this case, the proposed differential divide-by-3 divider will again fail to begin the correct operation. Therefore, the pulse of RS needs to pass the delay selector (DS) that controls the delay from the falling edge of RS to that of RS_{DIV3}, $N \cdot \tau_{DS}$. To set the proper delay, the DS increases N by one successively in every failure until there is no reset pulse generated from RS.

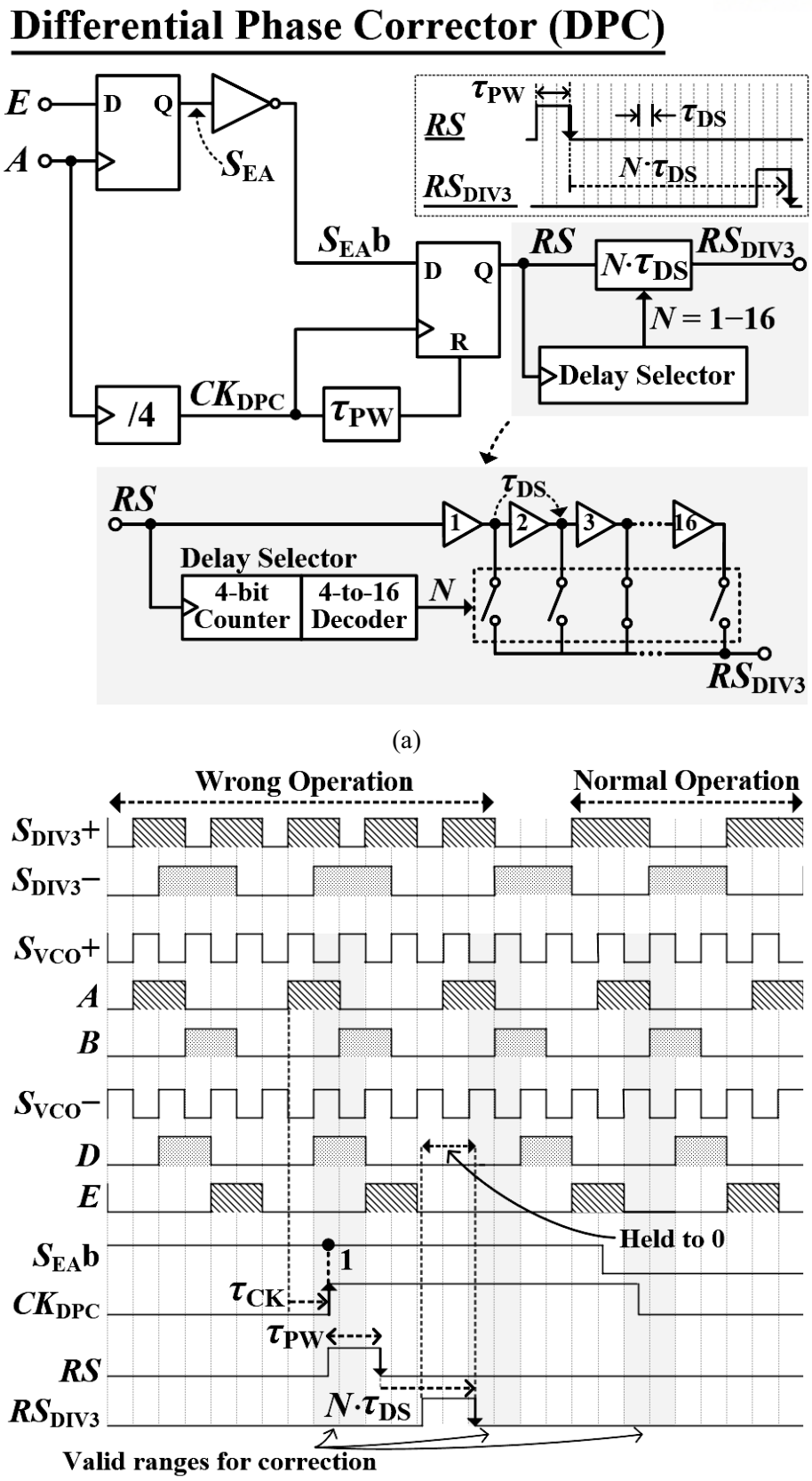


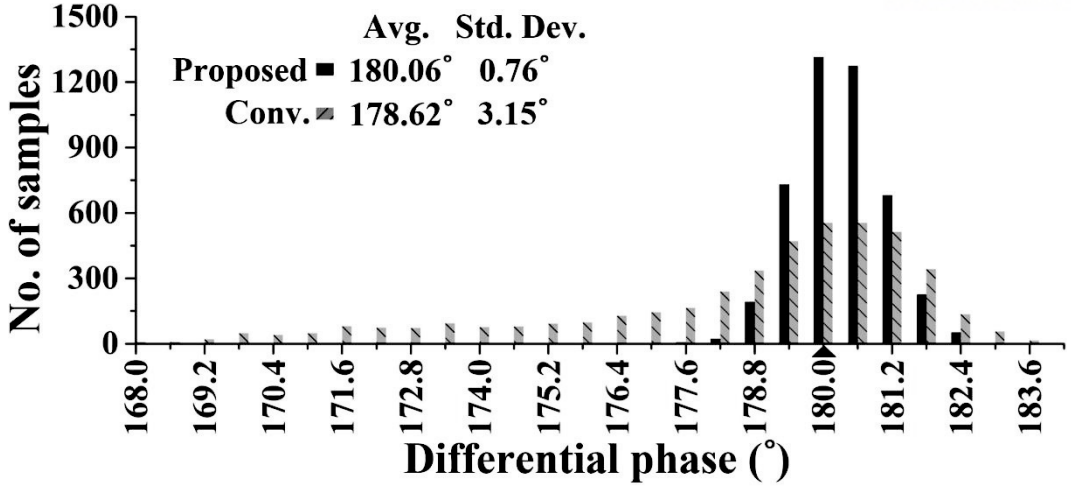
Figure 108. (a) Implementation of the differential phase corrector (DPC), (b) timing diagrams of the proposed divide-by-3 divider and the DPC

When $N \cdot \tau_{DS}$ becomes the appropriate amount, i.e., the falling edge of RS_{DIV3} is placed in the valid ranges, S_{EA}b will be detected as low at the next rising edge of CK_{DPC}; thus, RS is no longer generated, and the last value of N is maintained. The proper delay of $N \cdot \tau_{DS}$ varies according to the frequency of the VCO and propagation delays of DFFs in different process corners; thus, τ_{DS} and the maximum N, N_{MAX}, of the DS must be determined carefully to satisfy the following conditions. First, the step of the delay, τ_{DS}, must be smaller than the minimum VCO period. Second, the maximum delay, $N_{MAX} \cdot \tau_{DS}$, must be larger than twice the maximum VCO period, which is the distance between the valid ranges for correction. The second condition comes from the worst case scenario, where the falling edge of RS is located right after the end of the first valid range. In this case, to place the falling edge of RS_{DIV3} within the next valid range, the DS must be capable of providing the maximum delay, larger than $2T_{VCO}$. From these conditions, the boundaries can be set as:

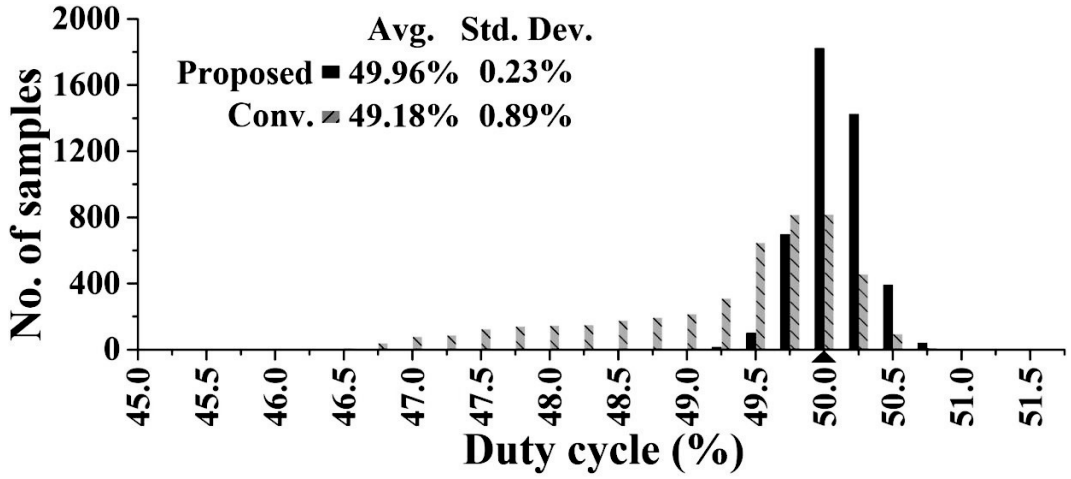
$$\tau_{DS} < \mathrm{Min}(T_{VCO}) \approx 90\mathrm{ps}, \tag{115}$$

$$N_{MAX} \cdot \tau_{DS} > \mathrm{Max}(2T_{VCO}) \approx 235\mathrm{ps}, \tag{116}$$

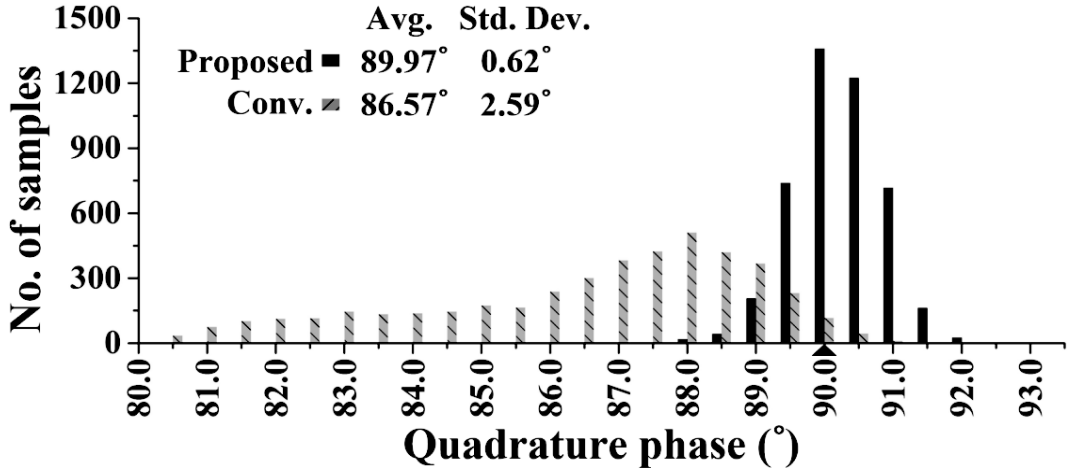
where T_{VCO} is the period of VCO signals with any VCO frequencies for the divide-by-6 divider, 8.5 – 11.0 GHz in this work. According to corner and temperature simulations, the designed τ_{DS} varies from 38 to 68 ps, which satisfied Equation (115) at any frequency. Then, N_{MAX} must be larger than seven according to Equation (116). Finally, considering a sufficient margin, N_{MAX} was designed as 16; thus, N can be from 1 to 16 using a four-bit counter. Therefore, the DPC can safely correct any wrong operations of the proposed differential divide-by-3 divider in any circumstances. Even in the worst-case scenario, the correction process is completed in less than 10 ns, and the proposed DPC consumes less than 100 μW.



(a)



(b)



(c)

Figure 109. Monte-Carlo simulations: (a) the differential phase and (b) the duty cycle of proposed and conventional divide-by-3 dividers in Fig. 5 (c) the quadrature phase of the divide-by-6 divider using proposed divide-by-3 divider

Figure 109(a) and (b) show the results of Monte-Carlo simulations, which compare the accuracy of the differential phase and the duty cycle of the output signals of the proposed divide-by-3 divider, respectively, with the conventional divider shown in Figure 106. Figure 109(c) compares the quadrature phases of the output signals of two divide-by-6 dividers: one using the proposed divide-by-3 divider and the other using the conventional divider. To obtain more realistic results, the simulation bench used the full circuits including the VCO, the LDO, and dividers. For each of nine simulation sets, three PVT corners, [TT, 1.1 V, 70 °C], [FF, 1.15 V, –30 °C], and [SS, 1.05 V, 120 °C], at each of three different VCO frequencies for the divide-by-6 plan, 8.5, 9.5 and 11.0 GHz, 500 samples were obtained through simulations with 3-sigma local mismatches (4,500 samples in total). For fair comparison, the conventional divide-by-3 divider was designed based on the same 33% duty cycle divider that was used for the proposed divide-by-3 divider. In addition, the delay of the last inverter of the conventional divider was accurately compensated by a pass-gate at the typical corner, [TT, 1.1 V, 70 °C], and at 9.5 GHz. As shown in Figure 109(a), the standard deviation of the differential phase of the proposed divide-by-3 divider was less than 0.8° from the average of 180.06°. On the other hand, the conventional divider had a much larger standard deviation, and it also had samples that largely deviated from 180°, which occurred due to a delay mismatch between the last inverter and the compensating pass-gate, and non-50% duty cycle, especially at [SS, 1.05 V, 120 °C/ 11.0 GHz]. In Figure 109(b), the duty cycle of the output signals of the proposed divider was also accurate with an average of 49.96% and a standard deviation of 0.23%. As shown in Figure 109(c), the quadrature phase of the I/Q signals from the divide-by-6 divider of the proposed LO-generator was very precise; thus, more than 95% of the samples were within ±1° errors from 90°. Phase noise of the proposed and the conventional dividers were close to each other, since they were based on the same 33% duty cycle divider. However, while the conventional divider had different phase noise at the differential outputs since one output was driven by an inverter, but the other was by a pass-gate, the proposed divider achieved the same phase noise at the differential outputs due to its fully symmetric topology.

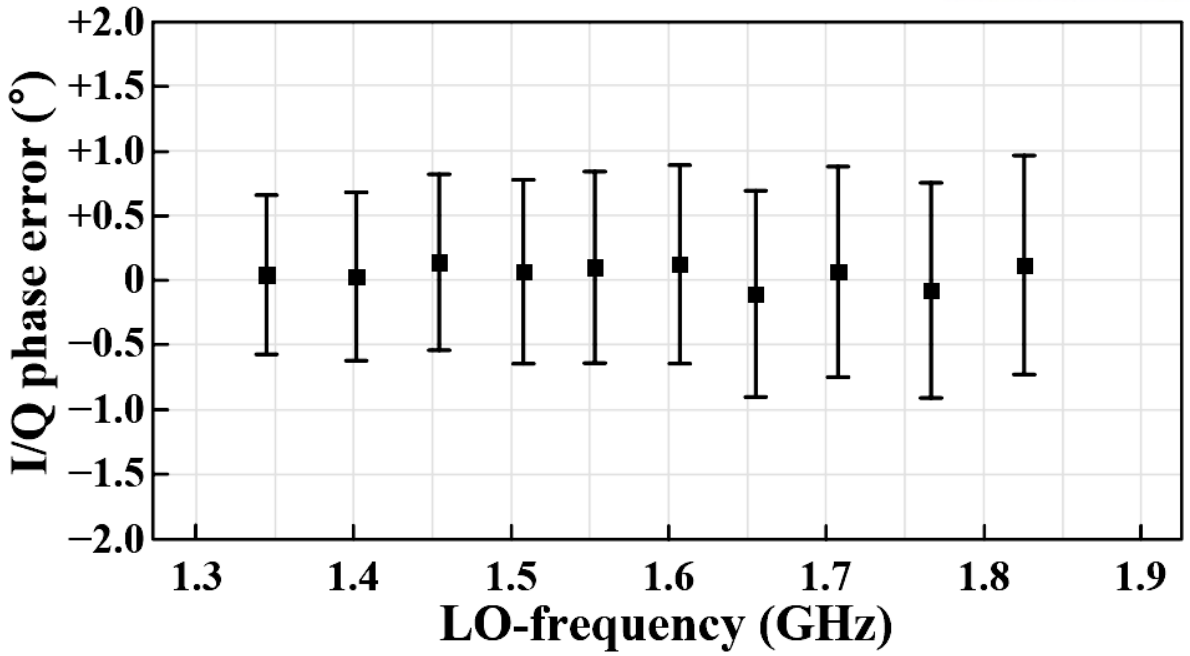


Figure 110. Monte-Carlo simulations: I/Q phase errors between quadrature signals of the proposed divide-by-6 divider over target frequencies

Figure 110 shows the results of Monte-Carlo simulations, which evaluate the phase accuracy of the quadrature signals from the proposed divide-by-6 divider over target frequencies. As in the simulation for Figure 109(c), 1,500 samples were obtained from the three extreme PVT corners at each frequency. The average of a phase error at each frequency was represented with a rectangle in the interval, bounded by the 5th and the 95th percentiles. According to the simulations, the phase errors were less than 1° in more than 90% of the samples at all target frequencies, and they were sufficiently low to achieve a good error-vector-modulation (EVM) performance [74].

6.3 Differential Divide-by-2 Divider For Quadrature Divide-by-4 and -12 Divider

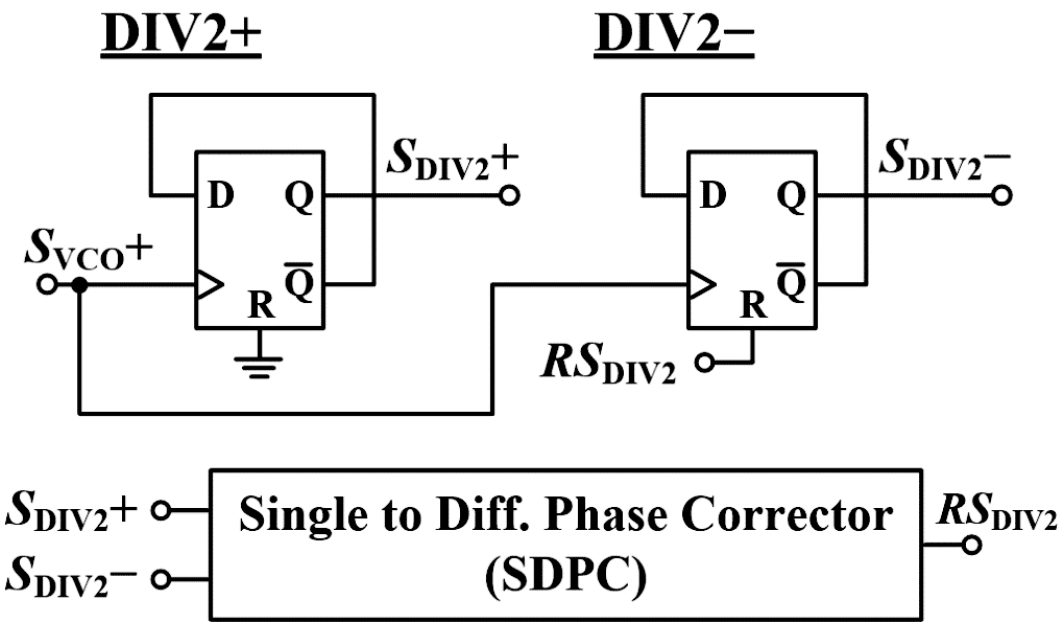


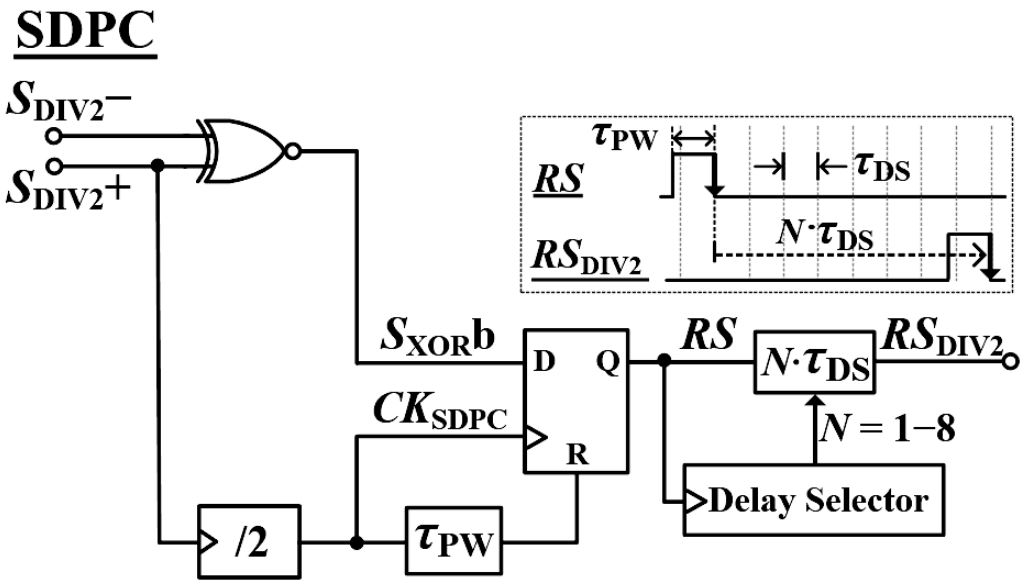
Figure 111. Proposed differential divide-by-2 divider

The design concept of the proposed divide-by-3 divider is generally applicable to any frequency dividers with arbitrary division ratios, and a new S-to-D divide-by-2 circuit for the divide-by-4 divider was also designed based on the same concept. This divide-by-4 divider was used for the divide-by-12 divider. As shown in Figure 111, the proposed S-to-D divide-by-2 divider consists of two conventional self-feedback DFFs, DIV2+ and DIV2–, that generate differential signals and a single to differential phase corrector (SDPC) that calibrates the relationship of the phases of the differential outputs. Figure 112(a) and (b) show the implementation and timing diagrams of the SDPC, respectively. When the proposed S-to-D divide-by-2 divider does not operate properly, the phases of the two outputs, $S_{DIV2}+$ and $S_{DIV2}-$, become in-phase, as shown in Figure 112(b). In this case, $S_{XOR}b$ becomes high, and a reset pulse, *RS*, is generated, which resets DIV2–. To control reset timing, the SDPC requires a DS, as does the DPC for the differential divide-by-3 divider. The DS increases *N* by one, every time *RS* is produced. The increase of *N* continues until the falling edge of RS_{DIV2} resets the DIV2– at the right timing, i.e., the falling edge of RS_{DIV2} occurs when $S_{DIV2}+$ is high, and thus no reset pulse, *RS*, is generated. The required τ_{DS} and N_{MAX} can be obtained from the following conditions:

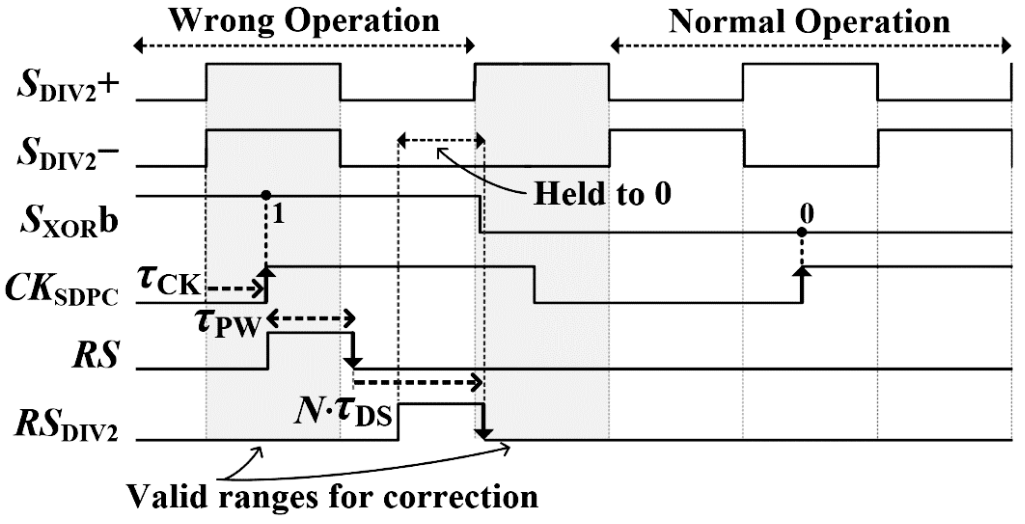
$$\tau_{DS} < \mathrm{Min}(T_{VCO}) \approx 92\mathrm{ps}, \tag{117}$$

$$N_{MAX} \cdot \tau_{DS} > \mathrm{Max}(T_{VCO}) \approx 135\ \mathrm{ps}, \tag{118}$$

where T_{VCO} is the period of the VCO signals for the divide-by-4 plan. Based on post corner simulations, τ_{DS} varies from 20 to 35 ps. Along with N_{MAX} of 8, conditions of Equation (117) and (118) are satisfied irrespective of any PVT variations. When this S-to-D divide-by-2 divider is used after the divide-by-3 divider for the divide-by-12 plan, a DS is not required. This is because the frequency of the input signals is so low that the presence of the falling edge of *RS* can be guaranteed within the first valid range after the rising edge of CK_{SDPC}.



(b)



(b)

Figure 112. (a) Implementation of the single to differential phase corrector (SDPC), (b) timing diagram of the proposed divide-by-2 divider and the SDPC

6.4 Other Building Blocks

6.4.1 Design of the *LC* VCO

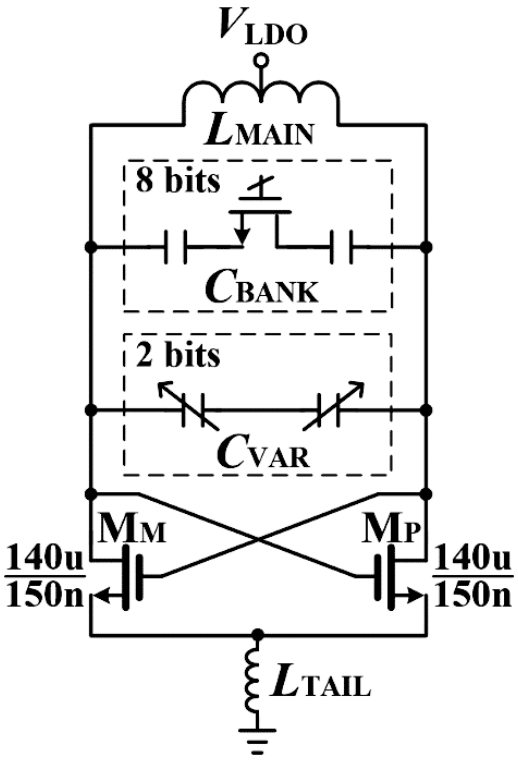


Figure 113. Low phase noise NMOS-type *LC*-VCO

Due to the proposed LO-plan, the required FTR of the VCO was reduced from 63% to 39%. The relaxation of the FTR of the VCO minimizes the required range of the variable capacitance that has to be covered by the capacitor bank. Along with small capacitive loading, the *LC*-VCO can maximize the loaded Q of the tank, which allows the VCO to achieve low phase noise. Figure 113 shows the topology of the *LC*-VCO in this work, which is based on a conventional NMOS-type, cross-coupled topology that can achieve low phase noise with a large swing of signals [48], [49]. To prevent gate-oxide breakdown due to a large swing of signals and reduce flicker noise, the core transistors of M_M and M_P were desinged using thick-oxide devices. In the new LO-plan, the VCO frequencies are much higher than those in conventional plans; thus, the inductance of the resonant tank can be reduced, and the VCO can be integrated in a small silicon area. Due to high VCO frequencies, the tank-inductor with a small inductance can still maintain a very high Q-factor. In this work, the inductor of the tank had an inductance of 240 pH and a Q-factor of 37 at 11 GHz. To satisfy the tight phase-noise requirements of the GSM standard, a tail inductor with an inductance of 130 pH and a Q-factor of 7 at 11 GHz was added [36]. The tail inductor occupied only 0.01 mm^2, and the Q-factor of 7 was sufficiently high for its functionality. The *LC*-VCO included an eight-bit capacitor bank and a two-bit varactor bank for coarse and fine frequency-tunings, respectively.

6.4.2 Design of the Low-Dropout Regulator

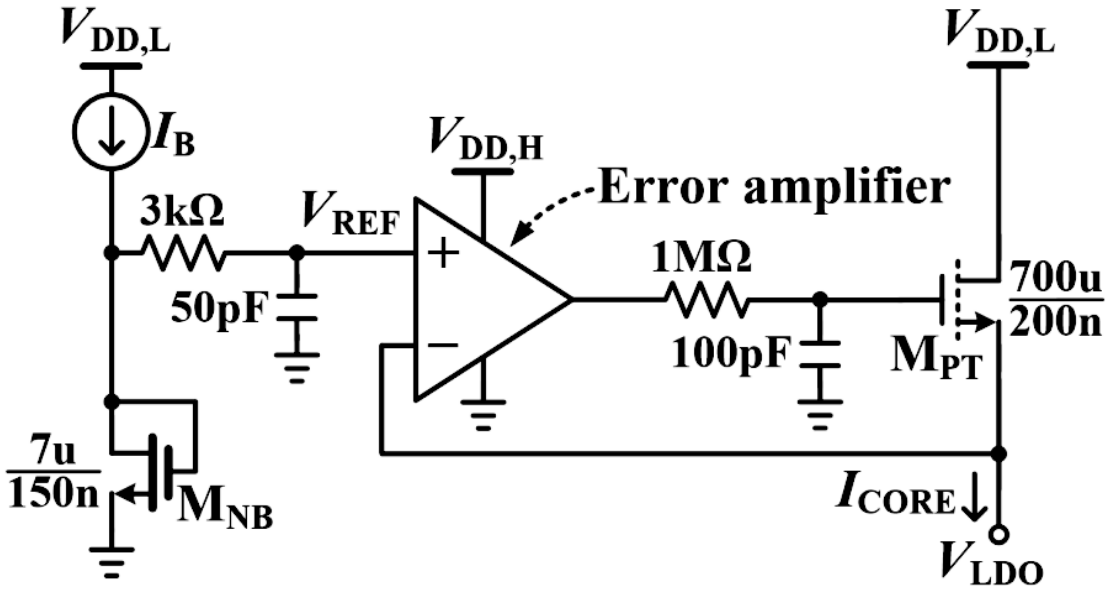


Figure 114. High PSR NMOS-type LDO

The core current of the *LC*-VCO, I_{CORE}, was sourced from the LDO at the top. As shown in Figure 114, the output voltage of the LDO, V_{LDO}, is supposed to be set to V_{REF}, which is defined by the diode-connected NMOS, M_{NB}, and the bias current, I_B. Since the aspect ratios of M_{NB} and M_M (or M_P) were designed as 1 to 20, I_{CORE} becomes 40 times I_B. We used an NMOS pass-transistor, M_{PT}, for the LDO to provide a high PSR (up to tens of MHz) while maintaining a high phase margin for a wide range of I_{CORE} [96]. The PSR of the LDO were –65 and –40 dB at the offsets of 10-kHz and 10-MHz, respectively. To reduce the headroom requirement, a native thin-oxide device was used for M_{PT}. The error amplifier was designed based on a folded-cascode topology, and two *RC*-filters were placed at its input and output to filter out thermal noise. The *RC*-filter at the input of the error amplifier had a pole frequency of 1.1 MHz by including a 3-kΩ resistor and a 50-pF MOS-capacitor. A 1-MΩ resistor and a 100-pF MOS-capacitor were used for the *RC*-filter at the output, and along with the output impedance of the error amplifier, they generated a pole with a frequency of 0.6 kHz. Due to these *RC*-filters having a low cut-off-frequency, the noise contribution of the LDO to the VCO's output was negligible. The dominant pole was present at the gate of M_{PT}, and the gain-bandwidth product and the phase margin of the regulating loop were 275 kHz and 65°, respectively. The supply voltage to the pass-transistor, $V_{DD,L}$, was 1.1 V, and that of the error amplifier, $V_{DD,H}$, was 1.8 V. V_{REF} was around 0.75 V, which generates an I_{CORE} of 11 mA, and the error amplifier consumed less than 200 μW. Figure 115 shows the schematic and the transistor sizes of a DFF that was used for the dividers. The DFF has a typical TSPC-topology [91] and includes two additional transistors, M_{RP} and M_{RN}, to pull down the node of Q to zero, when the node of R becomes high by the reset signal.

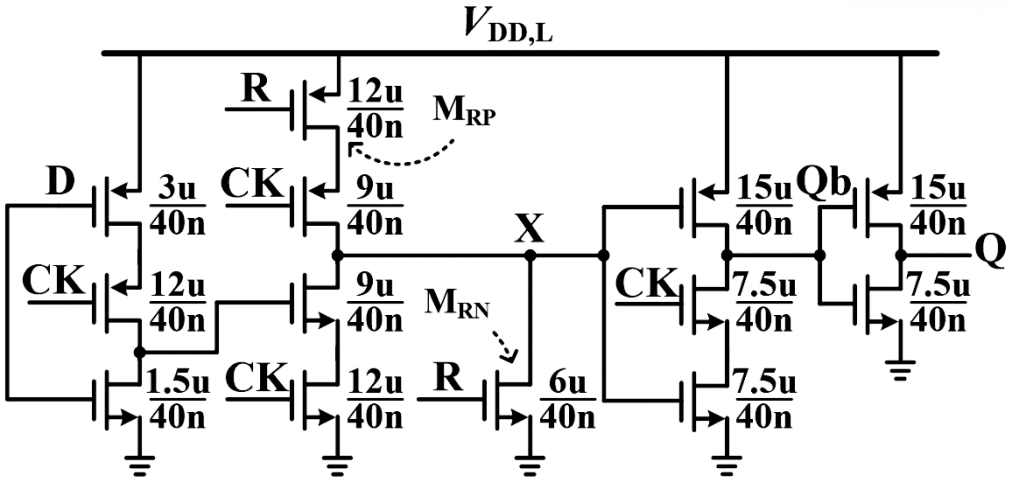


Figure 115. Schematic of a TSPC DFF, used for the dividers

6.5 Experimental Results

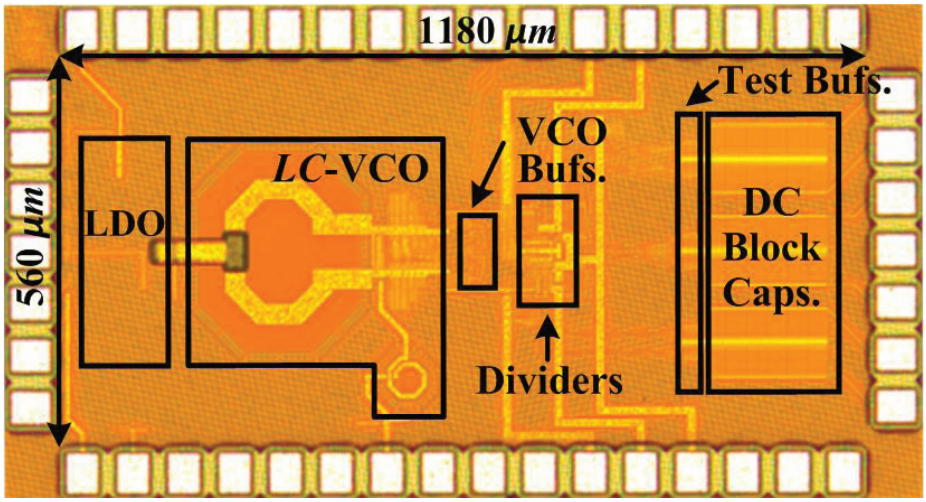


Figure 116. Chip micrograph of the proposed quadrature LO-generator

In this work, we proposed a single *LC*-VCO-based low phase noise and wideband quadrature LO-generator for multi-standard cellular transceivers that was fabricated in a 40-nm CMOS technology. Chips were tested on printed circuit boards (PCBs) after wire-bonding. Figure 116 shows the chip micrograph of the proposed LO-generator. The active area of the *LC*-VCO and the LO-dividers was 0.15 mm^2. For measurement, quadrature signals from the dividers were transferred to pads through on-chip test buffers and DC-blocking metal-oxide-metal (MOM) capacitors. The on-chip test buffers consisted of cascaded inverters, where their sizes increased gradually to drive 50Ω load impedance.

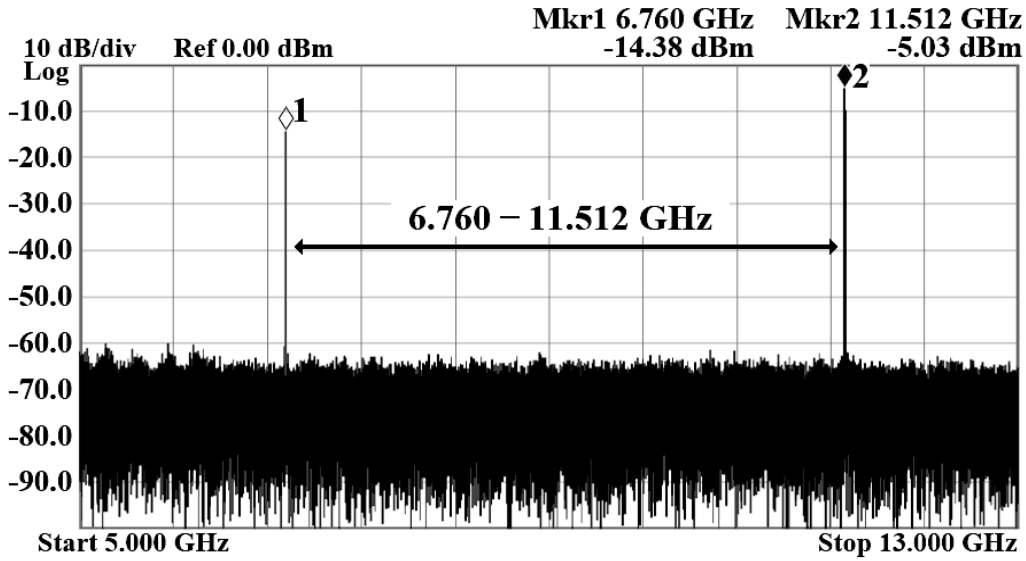
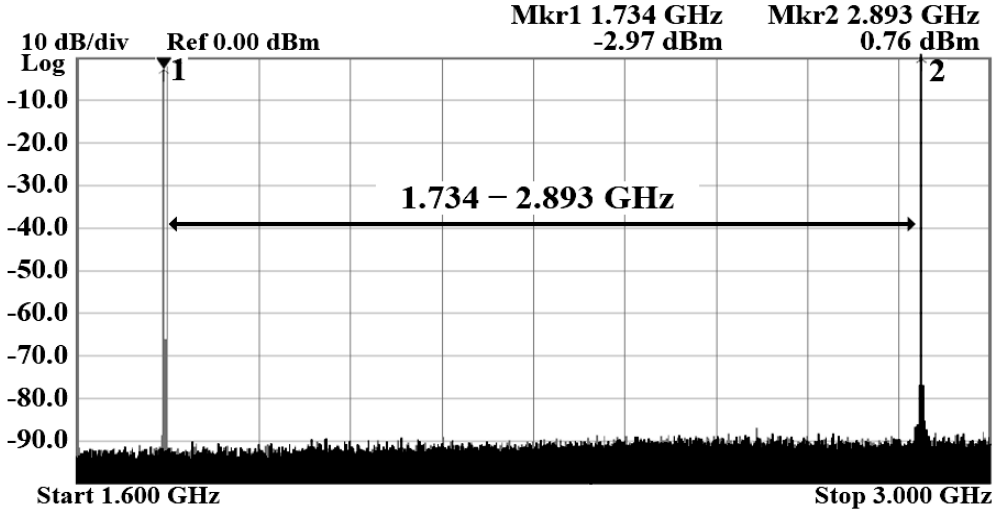
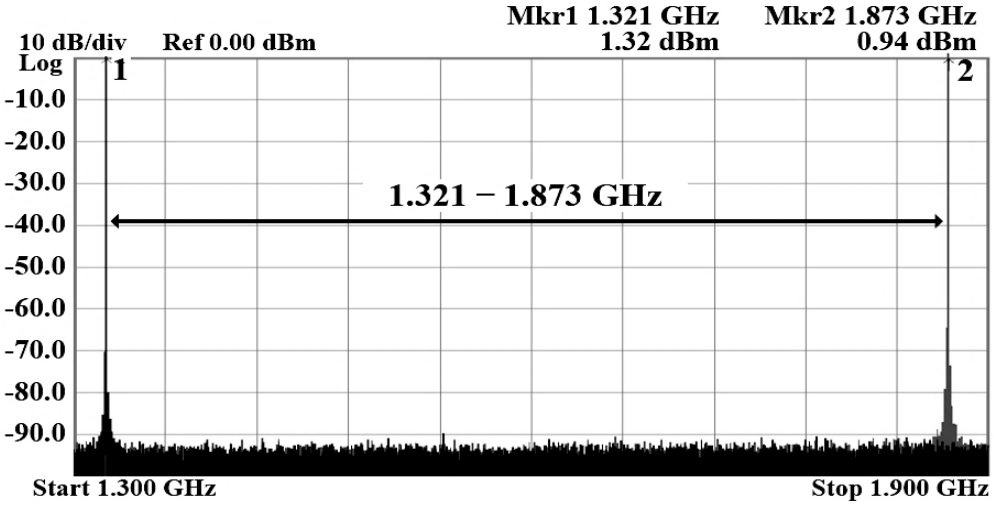


Figure 117. Measured spectrum of the VCO of the LO-generator

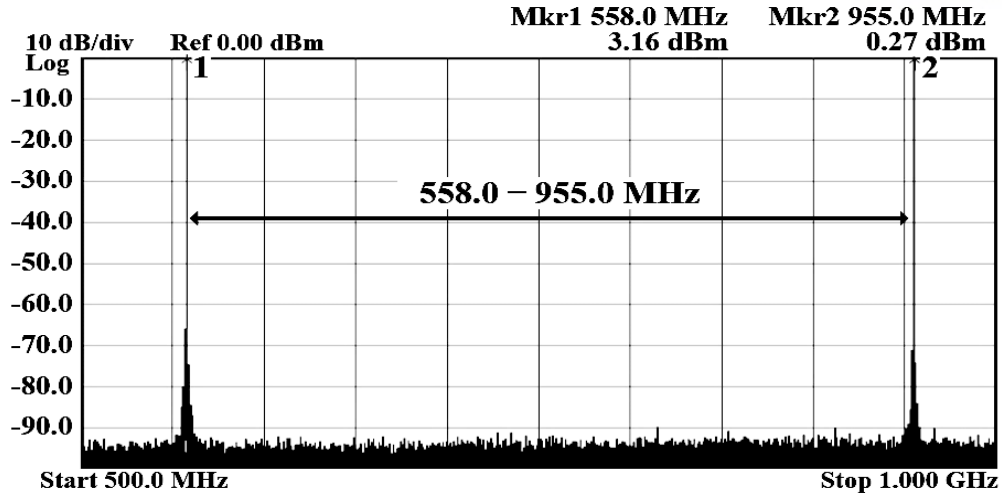
Figure 117 shows the measured spectrum of the VCO signals, where the frequency range was from 6.76 to 11.51 GHz. The corresponding FTR of the VCO was 52%, which is sufficient to cover the target FTR. To verify that all required LO-frequencies can be generated by the proposed LO-generator, the spectra of the outputs of each divider were measured. Figure 118(a), (b), and (c) show the spectra of signals from the divide-by-4, the divide-by-6, and the divide-by-12 dividers, respectively. As shown in Figure 118(a) – (c), the proposed LO-generator using a single VCO is capable of covering all LO-frequencies for recent multi-standard cellular transceivers, as shown in Figure 102. Figure 119(a) and (b) show the measured frequency ranges of the VCO signals and the LO-signals, respectively, when the eight bit code of the capacitor bank and the control voltage of the two bit varactor were swept.



(a)

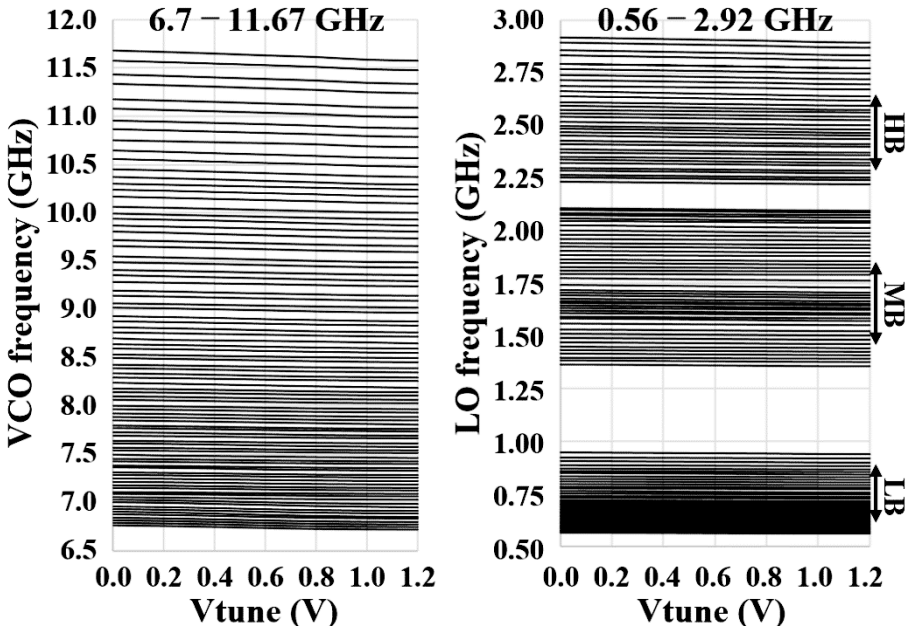


(b)



(c)

Figure 118. Measured spectra of the proposed LO-generator using (a) the divide-by-4 (b) the divide-by-6 and (c) the divide-by-12 divider

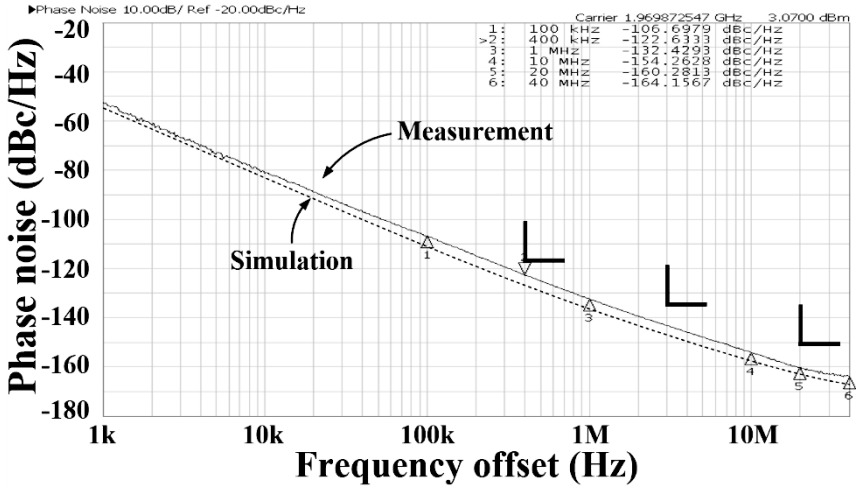


(a) (b)

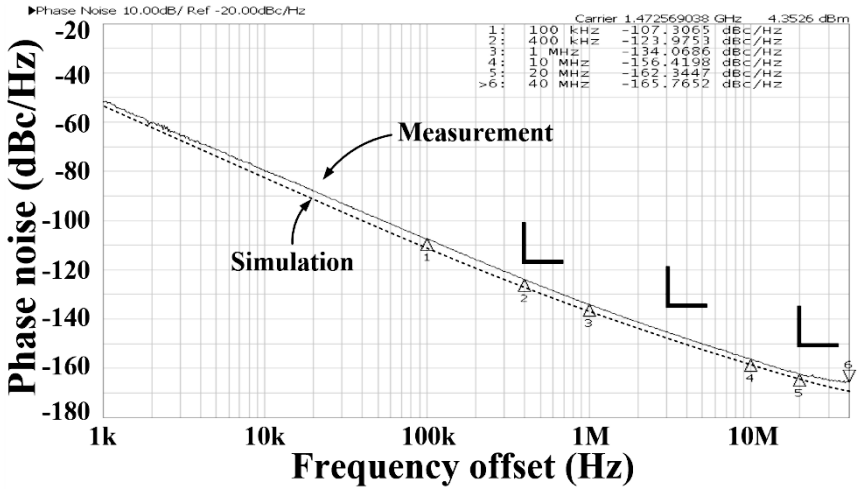
Figure 119. Measured frequency ranges of (a) the VCO and (b) the LO-generator

Figure 120(a) – (c) show the measured phase noise of the LO-signals from three dividers. The figures also show phase noise from post-layout simulations, observed at the outputs of the dividers, to evaluate the intrinsic performance of the dividers. In Figure 120(a) – (c), the most stringent spot noise requirements, which come from GSM, were marked: –118, –136, and –151 dBc/Hz at the offsets of 400 kHz, 3 MHz, and 20 MHz, respectively, for the mid-frequency band (MB), and –118, –136, –150, and –162 dBc/Hz at the offsets of 400 kHz, 3 MHz, 10 MHz, and 20 MHz, respectively, for the low-

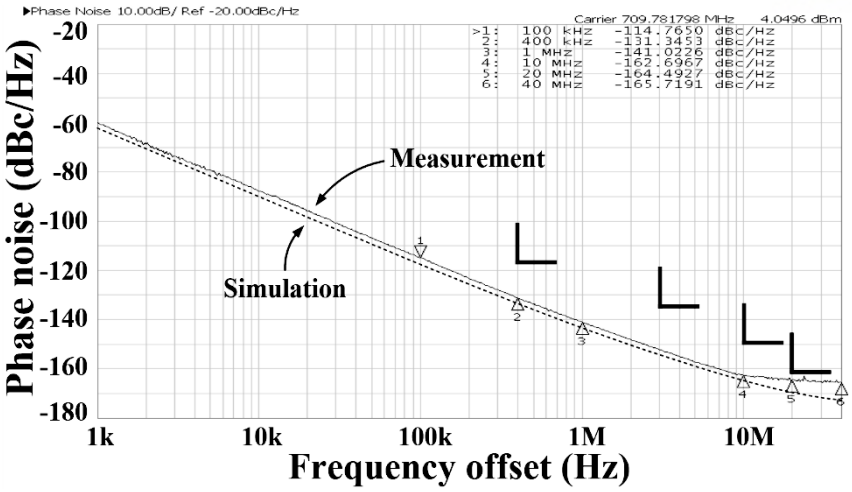
frequency band (LB) [74]–[77]. Figure 120(a) shows that the signal from the divide-by-4 divider with a 1.97-GHz LO-frequency achieved a phase noise of –132.4 dBc/Hz at the 1-MHz offset. Figure 120(b) shows that the signal from the divide-by-6 divider with a 1.47-GHz LO-frequency achieved a phase noise of –134.1 dBc/Hz at the 1-MHz offset. In Figure 120(c), the LO-signal from the divide-by-12 divider had a phase noise of –141.0 dBc/Hz at the 1-MHz offset from the 709-MHz LO-frequency. In this measurement, the VCO with the VCO buffer, and the divide-by-12 divider consumed 13.0 and 3.5 mW, respectively. As shown in Figure 120(a) – (c), phase noise of the proposed LO-generator was sufficiently low to satisfy the phase noise requirements of cellular standards. Figure 121 shows phase noise at the offsets of 400 kHz, 3 MHz and 10 MHz over all target LO-frequencies with the GSM requirements, indicated by the dotted lines. The high-frequency band (HB) is only used for LTE, where critical phase noise requirements are defined as integrated phase noise (IPN) rather than as spot noise.



(a)



(b)



(c)

Figure 120. Measured and simulated phase noise of LO-signals with frequencies of: (a) 1.95 GHz by divide-by-4, (b) 1.46 GHz by divid-by-6, and (c) 706 MHz by divide-by-12 (at offsets greater than 10 MHz, PN was saturated by the thermal noise of the on-chip test buffer)

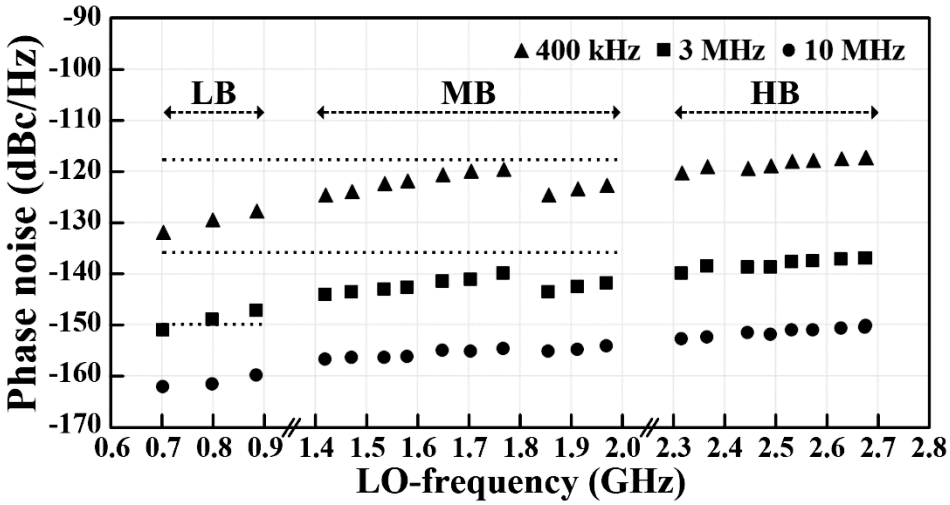
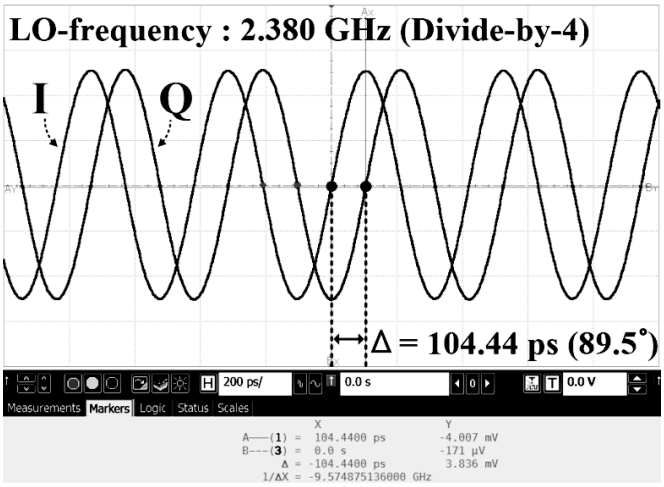


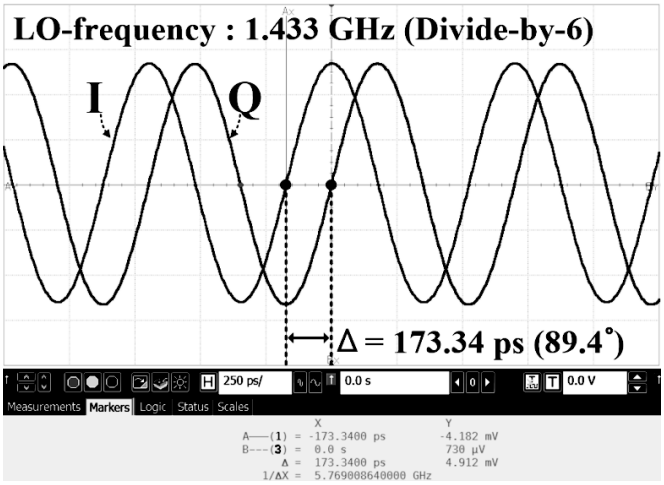
Figure 121. Phase noise at three offsets over LO-frequencies for all three bands

Figure 122(a)–(c) show the measured quadrature signals (I/Q signals). The most reliable method to evaluate an I/Q phase error is to measure the sideband rejection of the output of an on-chip quadrature mixer that receives the quadrature signals from the LO-generator [97]. However, since a quadrature mixer was not integrated in this work, I/Q phase errors were obtained from the signals, acquired through time domain measurements using an oscilloscope. To minimize potential phase errors due to any extrinsic causes in measurement, the lengths of the transmission lines and the bonding wires for quadrature signals were carefully matched when PCBs were implemented. Figure 122(a) shows the I/Q signals with a 2.38-GHz LO-frequency from the divide-by-4 divider with the phase difference of 89.5°. Figure 122(b) shows I/Q signals with a 1.433-GHz LO-frequency from the divide-by-6 divider with a

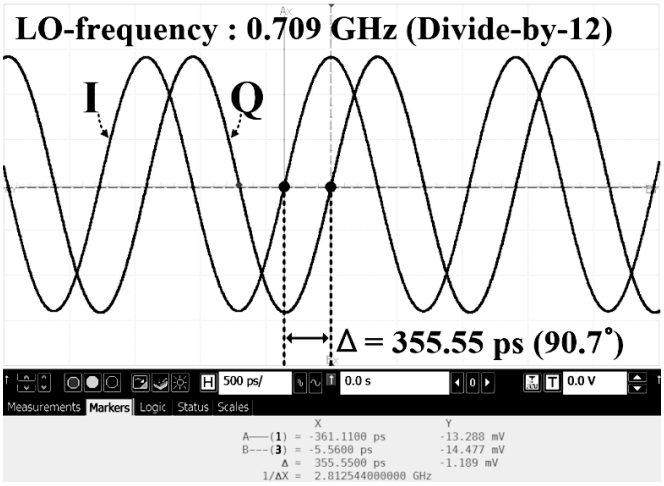
phase difference was 89.4°. In Figure 122(c), the I/Q signals with a 709-MHz LO-frequency were generated from the divide-by-12 divider, and the phase difference was 90.7°.



(a)



(b)



(c)

Figure 122. Measured quadrature (I/Q) signals: (a) Divide-by-4; (b) divide-by-6; (c) divide-by-12

Table 16 compares the performance of the proposed LO-generator with state-of-the-art wideband quadrature LO-generators. Reference [80], [84], [88], [89] show larger frequency ranges, since they targeted software-defined radio or cognitive radio applications. Compared to the architectures that used two *LC*-tanks, the proposed LO-generator occupies a smaller silicon area. It also had the lowest normalized phase noise while consuming low power, since the VCO was able to maximize its loaded Q due to the relaxed FTR, and the TSPC DFF-based LO-dividers achieved low phase noise, irrespective of variations in PVT. In addition, it had small I/Q phase errors over all target LO-frequencies, due to the proposed quadrature divide-by-6 divider using the differential divide-by-3 divider with 50% duty cycle.

Table 16. Performance comparison with state-of-the-art wideband quadrature LO-generators

	Process	**f_{LO} (GHz)**	**No. of *LC*-Tank**	**I/Q Gen. Method**	**Area (mm^2) (VCO+I/Q Gen.)**	**PN(dBc/Hz) @ f_{off} (f_{LO})**	**Norm. PN(dBc/Hz) @1MHz (1GHz)**	**Power (mW) (VCO+I/Q Gen.)**	**I/Q phase error.**
[78]	130 CMOS	1.8–6.0	2 (QVCO)	QVCO +SSB Mixer/ Quad. Dividers	1.28*	–130.4 @1.6MHz (1.87 GHz)	–130.8	23.3 – 35.0	N/A
[80]	90 CMOS	1.0–10.0	2 (QVCO)	QVCO +SSB Mixer/ Quad. Dividers	0.29	–120.0 @1MHz (1.75 GHz)	–124.9	31.0	N/A
[81]	130 CMOS	0.87–2.6	2 (QVCO)	QVCO +SSB Mixer/ Quad. Dividers	0.19	–126.5 @1MHz (1.70 GHz)	–131.1	27.8	< 2°
[83]	65 CMOS	5.8–9.4	2 (QVCO)	QVCO (No Divider)	0.35	–123.7 @1MHz (3.80 GHz)	–134.8	7.6 (VCO Only)	< 1.5°
[84]	40 CMOS	0.04–6.0	2	Quad. Dividers (7 Series Div2 Dividers)	0.21*	–149.0 @20MHz (3.60 GHz)	–134.1	30.0 (w/ PLL)	N/A
[88]	65 CMOS	4.9–11.1	1	ILRO/ Quad. Dividers	0.11	–122.3 @1MHz (1.61 GHz)	–126.4	22.0	< 4°
[89]	65 CMOS	0.01–6.6	1	ILRO/ Quad. Dividers	0.14*	–135.3 @3MHz (1.70 GHz)	–130.4	16.0 – 26.0 (w/ PLL)	N/A
This work	40 CMOS	0.56–2.92	1	Quad. Dividers Only	0.15	–141.0 @1MHz (0.71 GHz)	–138.0	16.5	< 1°
						–132.4 @1MHz (1.97 GHz)	–138.3	16.0	

***** Estimated from chip photographs

6.6 Conclusions

In this work, we presented a wideband and low phase noise quadrature LO-generator with a compact silicon area for multi-standard cellular transceivers. Using divide-by-6, divide-by-4, and divide-by-12 dividers, the new LO-plan reduced the required FTR of a VCO to less than 39%. Thus, the entire frequency range of 699 – 2690 MHz for current cellular transceivers, supporting multiple standards from 2G to 4G, was covered by one high-Q *LC*-VCO. Because of high VCO frequencies in the new LO-plan, the tank-inductor was allowed to have a small inductance, while maintaining a very high Q-factor. The loaded Q of the VCO was further enhanced since the capacitive loading of the capacitor bank was minimized by the reduced FTR requirement. As a result, the *LC*-VCO of the proposed LO-generator achieved low phase noise, as well as it occupied a small silicon area. To implement the quadrature divide-by-6 divider, we proposed a fully differential divide-by-3 divider with 50% duty cycle. Using the same idea, a differential divide-by-2 circuit was also proposed for divide-by-4 and divide-by-12 dividers. These LO-dividers, based on simple TSPC DFFs, generated the output signals with precise quadrature phases, and phase errors were regulated to less than 1° over all LO-frequencies.

7. Design of Wideband Dual-Mode *LC* VCO with a Switchable Core

7.1 Objective and Motivation

In global markets for cellular, recent transceivers are demanded to be compatible with different networks such as 2G, 3G, and 4G in worldwide sense by supporting multi-band and multi-mode standards in a single chip. A cellular transceiver design is becoming more difficult since the transceiver must cover a very wide frequency range. For example, if a transceiver covers the LTE band-12 and band-7 concurrently, it must operate at 700 MHz and also 2.5 GHz [98]. To accommodate this wide frequency range, a voltage-controlled oscillator (VCO) that oscillates over this wide frequency range is required for carrier frequencies of a local oscillator (LO). Between a ring VCO and an *LC*-VCO, the *LC*-based VCO is the only available option to satisfy the stringent phase noise requirement from the cellular standards. However, the intrinsic narrow frequency tuning range of the *LC*-VCO occurs a problem to secure a wide frequency tuning range to be used in cellular transceivers.

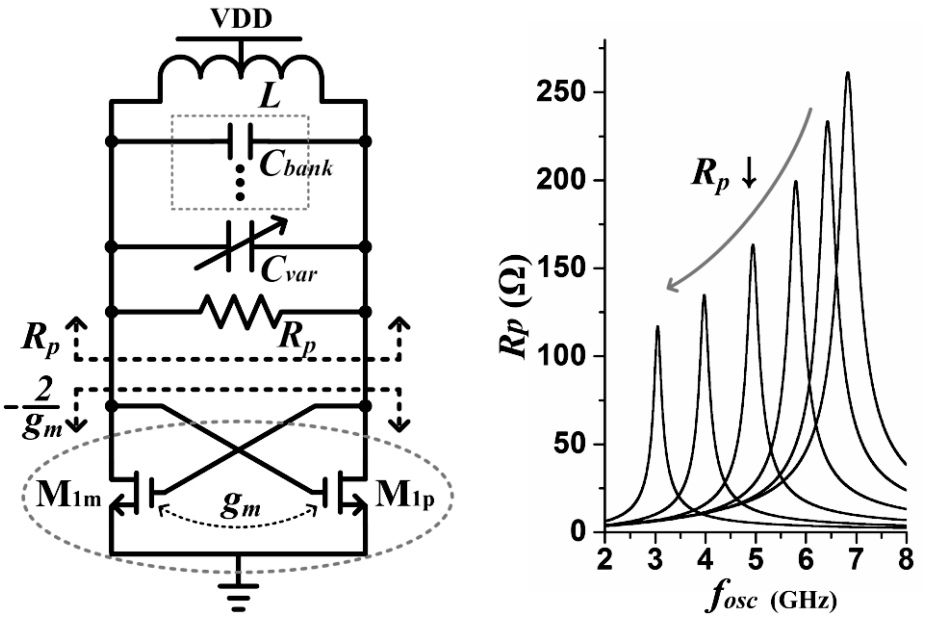
Recently, there have been many efforts to make a wide frequency tuning range of *LC*-VCOs. The first approach is to change the inductance in the *LC* tank by adopting transformers or switching inductance [72], [99]−[103]. However, this approach inherently degrades the Q-factor of the inductor, thereby, the degradation of the phase noise of the *LC* VCO. In addition, the occupied silicon area is increased since the inductor is the most area hungry passive component in ICs. Second, as a most typical approach, by turning on and off capacitors in the *LC* tank and by filling the gap between the digitized capacitor bank by varactors, the oscillation frequency can be controlled and the frequency tuning range can be extended [104]. However, this approach still has a problem. It has a natural trade-off between the start-up condition and the parasitic capacitors, which hinder the expansion of the frequency tuning range; At the low oscillation frequencies, start-up condition is hard to meet due to low the gain of the cross-coupled transistors. At high oscillation frequencies, parasitic capacitance from the cross-coupled transistors, the capacitor bank, and the varactor is a limit to increasing the maximum oscillation frequency.

To break this trade-off regard to the size of the core transistors, which has a direct connection with the start-up gain, the size of the core transistors can be switched to expand the frequency tuning range (FTR) of *LC*-VCOs. In the presented paper [105], a CMOS-type cross-coupled *LC*-VCO switched a core transistor. At the low oscillation frequencies, if the start-up gain is not enough, additional core transistors are shorted to the main core transistors to boost up the gain. However, since the phase noise of a CMOS-type cross-coupled *LC*-VCO has a limit to achieve low phase noise due to the limited output swing, this architecture is not suitable to meet the stringent phase noise requirements from cellular standards, especially for GSM. In addition, theoretically, the parasitic capacitance of the CMOS-type cross-coupled *LC*-VCO is twice larger than the NMOS-type cross-coupled *LC*-VCO, thereby, this architecture is hard to oscillate at high frequencies.

In this work, a new wideband *LC*-VCO based on the NMOS-type with switchable transconductance of the core transistors is presented. By shorting between the primary and the secondary cores through the switches between them, the low-frequency oscillation is allowed by the increased start-up gain, which is boosted by the increased transconductance of the core transistors. Moreover, *RC*-bias circuits, which control the DC voltage of the gates of the secondary cores can minimize the size of the switches between the primary and the secondary core while maintaining high transconductance of the secondary core. Since the capacitive loading to the VCO by the parasitic capacitance of the switches is reduced by the *RC*-bias circuits, the maximum oscillation frequency can be extended even when the switches are turned off. In the measurement results, it shows that the proposed VCO can achieve an FTR of 41%, i.e., from 3.36 to 5.1 GHz, with competitive phase noise performance, i.e., −123.1 dBc/Hz at the 1 MHz offset when the oscillation frequency is 4.21 GHz.

7.2 Frequency-Range Analysis of an *LC* VCO

A typical NMOS-type cross-coupled *LC*-VCO is shown in Figure 123(a). Since this architecture can achieve 6 dB lower phase noise in theoretically than the CMOS-type *LC*-VCO, this architecture is preferred when low phase noise performance is required by applications. However, as previously mentioned due to the intrinsic tradeoff, lower and upper oscillation frequency boundary, f_{osc}, is limited as explained in the following two sub-sessions.



(a) (b)

Figure 123. (a) NMOS-type cross-coupled *LC*-VCO (b) loaded R_p across the VCO's oscillation frequencies

7.2.1 Lower Boundary of the Oscillation Frequency by the Start-Up Condition

Theoretically, an ideal *LC* tank is assumed to oscillate infinitely without the loss of energy. However, in practice, since the integrated inductors and capacitors have a loss component, the *LC* VCO must have an active core, which sources energy into the tank to compensate for the energy loss to sustain the oscillation. The loss component in the *LC*-tank can be modeled as a resistor, R_p, connected to the *LC* tank in parallel as shown in Figure 123(a). R_p represents how much energy is dissipated due to the loss in the *LC* tank. Therefore, the transconductance, g_m, of the core transistors, M_m and M_p, can be decided by R_p, since R_p also represents how much energy is needed to compensate the loss component. The relationship between R_p and g_m to guarantee the start-up condition of the *LC*-VCO is as follows.

$$R_p > \frac{2\alpha}{g_m} \tag{119}$$

where α is a factor to have a margin by considering process-voltage-temperature (PVT) variations. Thus, the range of α should be greater than one [106]. Previously, R_p is assumed to include all loss components from the core transistors and the *LC*-tank. However, in practice, the value of R_p is mainly decided by the quality factor (Q-factor) of the inductor, Q_{ind}. This is because in the GHz-range Q-factor of the inductor is much lower than that of other components. Thus, effective R_p can be denoted as follows only considering the Q-factor of the inductor.

$$R_p = 2\pi \cdot f_{osc} \cdot L \cdot Q_{ind} \tag{120}$$

where L is the value of the inductor, i.e., inductance, in the *LC*-tank. Along with the definition of Q_{ind}, Equation (120) can be rewritten as

$$R_p = \frac{(2\pi \cdot f_{osc})^2 L^2}{R_s} \tag{121}$$

where R_s is the series resistance of the inductor representing loss component. The changes of R_p across the oscillation frequency was simulation as shown in Figure 123(b) by assuming that an inductor having 600 pH, whose Q-factor is 17 at 4 GHz and the capacitance is changed from 800 fF to 4 pF. In Figure 123(b), as the f_{osc} goes down, the magnitude of R_p decreases as we expected through Equation (121). It means that the start-up condition is hard to meet at low frequencies. Therefore, the minimum oscillation frequency, $f_{osc,low}$, of the *LC*-VCO is mainly limited by the start-up condition described in Equation (119) and it can be calculated as

$$f_{osc,low} = \frac{1}{2\pi}\sqrt{\frac{2\alpha \cdot R_s}{g_m L^2}} \tag{122}$$

7.2.2 Upper Boundary of the Oscillation Frequency by Parasitic Capacitance

Generally, the oscillation frequency, f_{osc}, of an *LC*-VCO can be represented as

$$f_{osc} = \frac{1}{2\pi\sqrt{L \cdot C_{total}}} \tag{123}$$

where C_{total} is the total capacitance including all capacitive components inside of the *LC*-VCO. Generally, a typical *LC*-VCO employs two types of capacitors to control f_{OSC}, which are a capacitor bank and varactors. Thus, C_{total} has C_{bank} and C_{var}, which are capacitance from capacitor banks and varactors, respectively. In C_{total}, C_{gs} and C_{gd} are also included, which are the parasitic capacitors between the gate and the source, and the gate and the drain of the core transistors, respectively. Thus, by considering the parasitic capacitors, C_{total} can be represented as [106]:

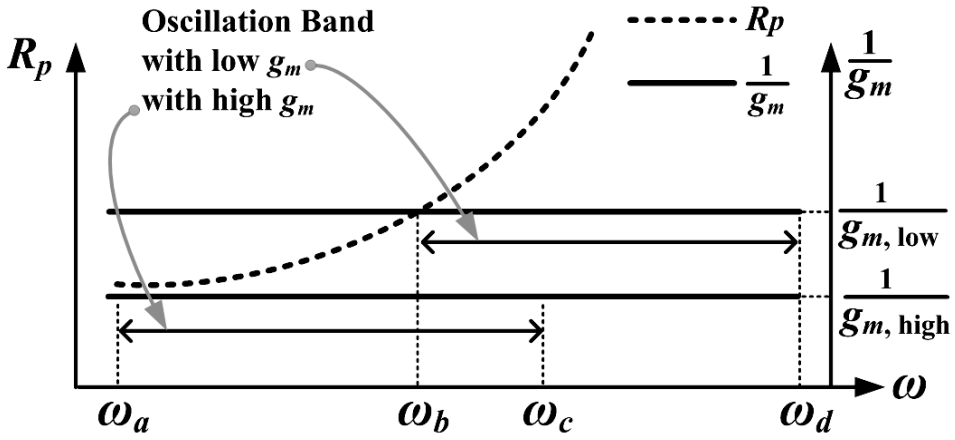
$$C_{total} = \frac{2C_{bank} + 2C_{var} + C_{gs} + 4C_{gd}}{2} \tag{124}$$

In Equation (124), except C_{gs} and C_{gd}, the value of C_{bank} and C_{var} can be changed to control f_{OSC}. When the maximum value of C_{bank} and C_{var} are used to generate low frequency, the portion of the parasitic capacitors is negligible, since they are relatively small compared to the value of C_{bank} and C_{var}. In contrary, when the VCO should oscillate at high frequencies, the parasitic capacitance is a major limitation, since the minimum C_{bank} and C_{var}, $C_{bank,min}$ and $C_{var,min}$, are so small and now those values are comparable to the parasitic capacitance. Therefore, the maximum limit of the oscillation frequency, $f_{osc,high}$, is limited by C_{gs}, C_{gd}, $C_{bank,min}$ and $C_{var,min}$ as

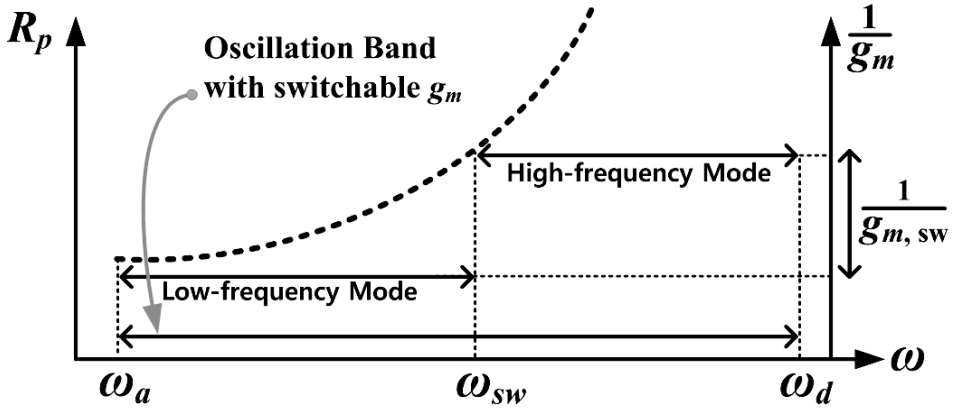
$$f_{osc,high} = \frac{1}{2\pi\sqrt{L \cdot \left(\frac{C_{gs} + 4C_{gd} + 2C_{bank,\,min} + 2C_{var,\,min}}{2}\right)}} \tag{125}$$

Therefore, to extend the $f_{osc,high}$ in Equation (125), the parasitic capacitance from the core transistor such as C_{gs} and C_{gd} should be minimized by designing the size of the core transistors to be optimal.

7.3 Proposed Dual-Mode *LC* VCO With a Switchable Gate-Biased Active Core



(a)



(b)

Figure 124. Oscillation bands according to different transconductance, g_m (a) when g_m is either small or high (b) when g_m is switchable

As we previously discussed, there is a trade-off when we want to extend the maximum and the minimum oscillation frequency. The g_m of the core transistors must be large enough to ensure the oscillation of the VCO in the low-frequency band. However, it induces large parasitic capacitance, which would hinder the high-frequency oscillation. On the other hands, to have small parasitic capacitance, if the g_m is minimized by reducing core transistor's size, the maximum frequency of the VCO can be extended at the expense of failure of the start-up in the low-frequency band. Figure 124(a) illustrates the aforementioned trade-off to extend the frequency tuning range. The value of R_p is plotted over the oscillation frequency in the dotted line as described in Equation (121). The value of $1/g_m$ is plotted using the solid line. When g_m is designed to be high by sizing up the core transistor, the minimum oscillation frequency of the VCO can be lowered to ω_a, but the large parasitic capacitance also lowers the maximum oscillation frequency to ω_c. On the contrary, when g_m is designed to be small by sizing

down the core transistor, the maximum oscillation frequency of the VCO can be raised to ω_d, but the small g_m also raises the minimum oscillation frequency to ω_b to satisfy the start-up condition.

To break up this trade-off, we proposed a g_m-switching technique, whose concept is intuitively drawn in Figure 124(b). First, when the VCO is supposed to operate in the low-frequency band, g_m is changed from a low value to a higher value to satisfy the start-up condition. Second, when the VCO is supposed to operate in the high-frequency band, g_m is changed from the high value to the low value by reducing the core transistor's size for small parasitic capacitance. As a result, the frequency tuning range of the VCO can widend from ω_a to ω_d.

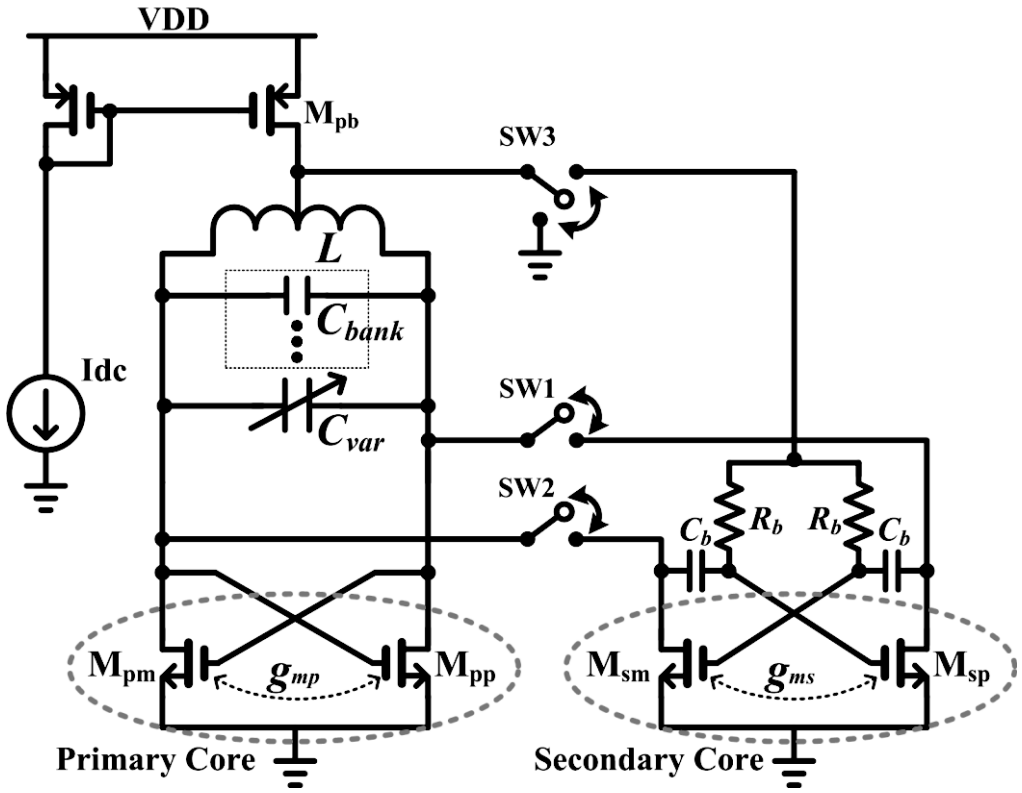
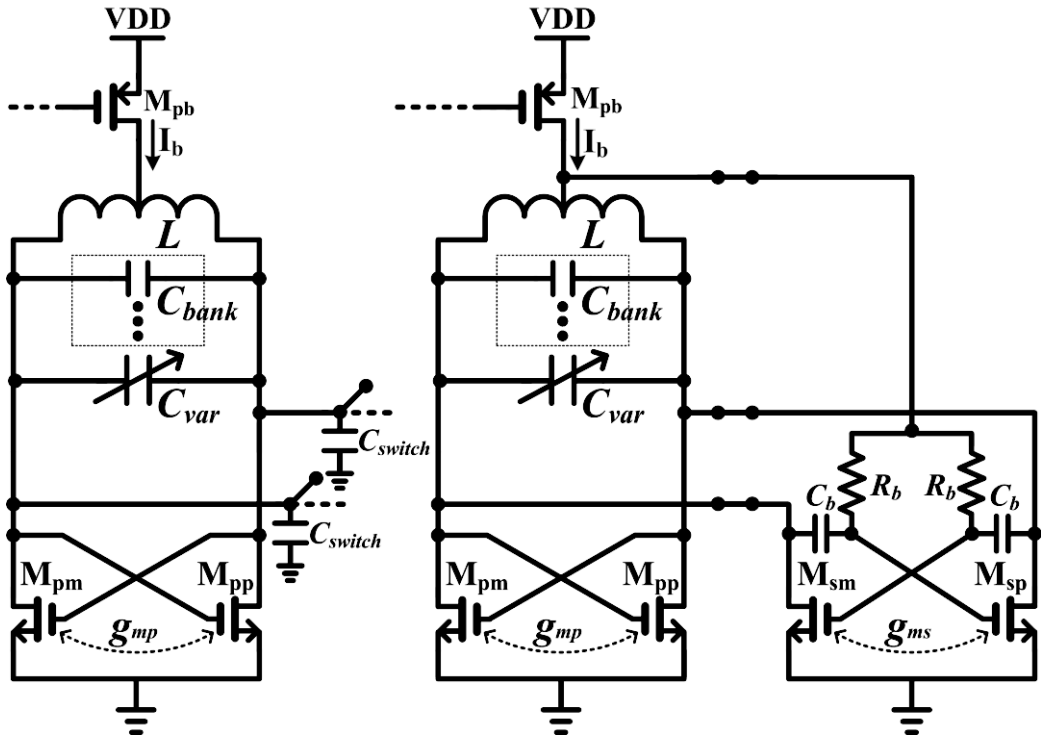


Figure 125. Overall architecture of the proposed *LC*-VCO with a switchable gate-biased active core

Figure 125 shows the overall architecture of the proposed wideband *LC*-VCO having a dual-mode. As shown in Figure 125, the proposed *LC*-VCO has two pairs of cross-coupled NMOS-transistors. The first one is the primary core transistors consisting of M_{pm} and M_{pp}. The second one is the secondary core transistors consisting of M_{sm}, M_{sp}, and the *RC*-bias circuits with R_b and C_b. The secondary core transistors can be shorted in parallel to the primary core transistors by the pass-gate switches, which are SW1 and SW2. In the VCO, there are a 6-bit capacitor-bank and a 2-bit varactor-bank and to to control the frequency of the VCO and to fill the frequency gap between the capacitor bank, respectively.

7.3.1 Proposed Dual-Mode VCO: HF and LF Modes



(a) (b)

Figure 126. Two operation modes of the proposed VCO (a) HF mode (b) LF mode

The proposed VCO can operate in two modes; high- and low-frequency mode, according to the target oscillation frequency. First, when the VCO oscillates in the high-frequency (HF) mode as described in Figure 126(a), the series switches such as SW1 and SW2 are open to disconnect between the primary and secondary core. Therefore, the differential signals of the primary core can not reach to the secondary core. In addition, to completely turn off the secondary core, after turning off the SW3, the bias voltage of the *RC*-bias circuit is grounded. In the HF mode, the operation of the *LC*-VCO is exactly the same as the conventional *LC*-VCOs. Since the switches are fully turned off, SW1 and SW2, the primary core can be completely isolated from the secondary core, thereby the parasitic capacitance from the secondary core transistors cannot load the *LC* tank. It means that it can help the VCO to oscillate at high frequencies. In addition, the size of the switches is designed to be small enough, which will be dealt with in the following session. Thus, the effect of the switch size, i.e., parasitic capacitance, on the oscillation frequency is negligible. Since the VCO in this mode operates as a typical NMOS-VCO, the g_m can be represented as follows as

$$g_{m.HM} = g_{mp} = \sqrt{2\mu_n C_{ox} \frac{W_p}{L_p} I_b} \tag{126}$$

where μ_n, C_{ox} ,W_p/L_p, and I_b are the mobility of electrons, gate-oxide capacitance, the aspect ratio of M_{pn} and M_{pp}, and the bias current of the VCO, respectively.

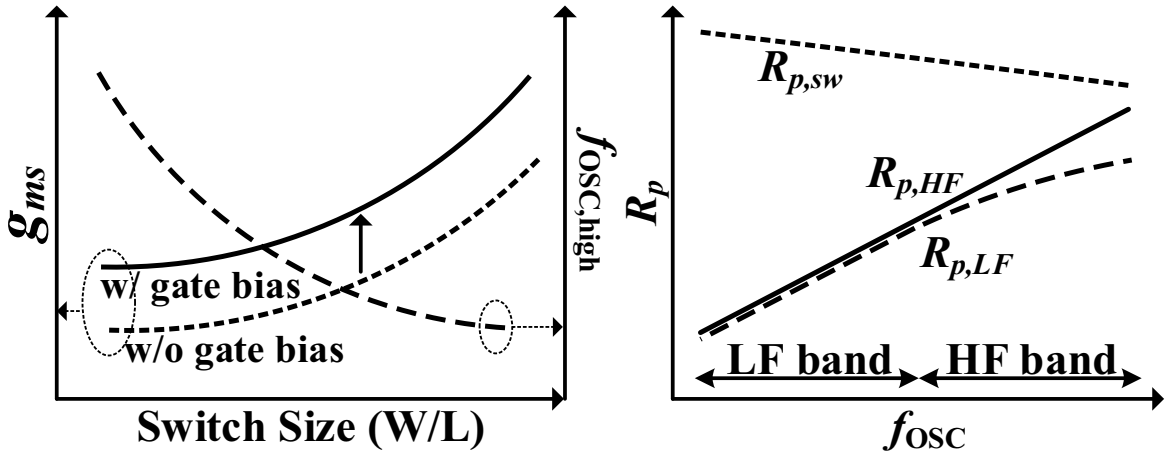
Second, when the *LC*-VCO oscillates in the low-frequency (LF) mode as described in Figure 126(b), the switches are shorted to connect the primary and the secondary core. In additon, the gate voltage of M_{sm} and M_{sp} has the same bias voltage of the primary core transistors. Therefore, the transconductance in the LH mode, $g_{m,LM}$, is boosted and it can be denoted as

$$g_{m,LM} = g_{mp} + g_{ms} = \sqrt{2\mu_n C_{ox} \frac{W_p}{L_p} I_b \cdot (1+\beta)}, \quad \beta = \frac{W_s / L_s}{W_p / L_p} \tag{127}$$

where W_s/L_s is the aspect ratio of M_{sm}, M_{sp}. When the tansconductance of the HF mode, i.e., Equation (126), and that of the LF mode, i.e., Equation (127), are compared, the total transconductnace increases $\sqrt{1+\beta}$ times in the LF mode when the I_b is the same. For example, if β is one, i.e., the size of the primary and the secondary core is the same, the $g_{m,LM}$ increases by $\sqrt{2}$ times $g_{m,HM}$. Therefore, the minimum oscillation frequency of the LF mode can be pushed down by 16 % than that of the HF mode described in Equation (122). In practice, the R_p of the tank is the function of between 2nd and 1st order of the f_{osc} rather 2nd order as denoted in Equation (121) because of the Q-factor from the capacitors. Therefore, in the LF mode, the minimum oscillation frequency of the *LC*-VCO can be further lowered by more than 20 %, theoretically.

7.3.2 Switch-Size Minimization by the Gate-Bias Technique

Even though the switches between the primary and the secondary core are opened to remove the parasitic capacitance from the secondary core, it also contributes the parasitic capacitance by the switch itself. Therefore, the size of the switches must be carefully designed not to lower the maximum oscillation frequency, which occurs another trade-off regarding the size of the switches.



(a) (b)

Figure 127. (a) g_{ms} and $f_{osc,high}$ over the size of the switch with and without the RC-gate bias circuits (b) R_p of the VCO according to the oscillation frequencies

In Figure 127(a), the dotted line shows $f_{osc,high}$ in the HF mode, and the solid lines represent transconductance of the secondary core in the LF mode. As shown and as explained in the previous sessions, to extend $f_{osc,high}$ in the HF mode, the switch's size must be minimized not to load the *LC* tank. However, switches with a small size have a large on-resistance, which results in a huge drop in DC voltage when the signal is transferred to the secondary core. Since the transconductance is mainly determined by the gate-bias voltage, whose voltage drop due to the small switches would reduce the transconductance of the secondary core. To solve this trade-off, the *RC* gate-bias circuit, having two resistors and capacitors, is empolyed in the secondary core as shown in Figure 126(b). Then, even when the size of the switch is small, the high transconductance of M_{sm} and M_{sp} can be secured since the gate-bias voltages are provided through the *RC* gate-bias circuit, which has the same value of the primary core. However, as shown in Figure 127(b), if the size of the switch is designed too small, R_p of the VCO could be decreased, which could occur hard start-up of the VCO and degradation of phase noise. Therefore, the size of switches must be carefully designed to be optimal, thereby not to degrade the R_p, i.e., the Q-factor, and to minimize the parasitic capacitance.

7.3.3 Phase Noise of the VCO

Two additional noise sources are should be considered when the proposed *LC*-VCO operates in the LF mode: the *RC*-bias circuits and the switches. First, the impact of the switches is negligible since they are inserted at core transistors' drain and they are carefully designed not to degrade the Q-factor of the *LC*-tank [105]. Second, regarding the *RC*-bias circuit, the capacitance and the resistance are 500 fF and 2 kΩ, respectively. Thus, the capacitor is seemed to be short since the pole frequency is much lower than the oscillation frequency of the VCO. Then, the resistor, R_b, is seemed to be in parallel with the R_p of the tank. By considering the effect of R_b, the phase noise of the *LC*-VCO can be predicted as [32],

$$PN \approx 10 \cdot log\left[\frac{kT}{V_{max}^{\ 2}} \cdot \frac{1}{(R_P \,||\, R_b) \cdot (C_{total}\omega_o)^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2\right] \tag{128}$$

where V_{max}, ω_o, and $\Delta\omega$ are the swing of the output signal, oscillation frequency, and a frequency offset, respectively. In the proposed work, R_b is designed to be much higher than R_p, thus the effect of R_b to the Q-factor of the *LC*-tank is insignificant. Figure 128 shows post-layout simulations to show the contribution to the total phase noise by the switches and R_b when the *LC*-VCO oscillates at 3.5 GHz. It was simulated under the various environments such as by sweeping the corner (SS/ TT/ FF) and temperature (-30/ 30/ 100 °C). As shown, the switch's noise contribution os bigger than the R_b. The worst case happens when the corner and the temperature are SS and −30 °C, respectively. In that case, the noise contribution of the switch is less than 7.5 % at both frequencies offsets of 100 kHz and 2 MHz, which degrades phase noise less than 0.32 dB.

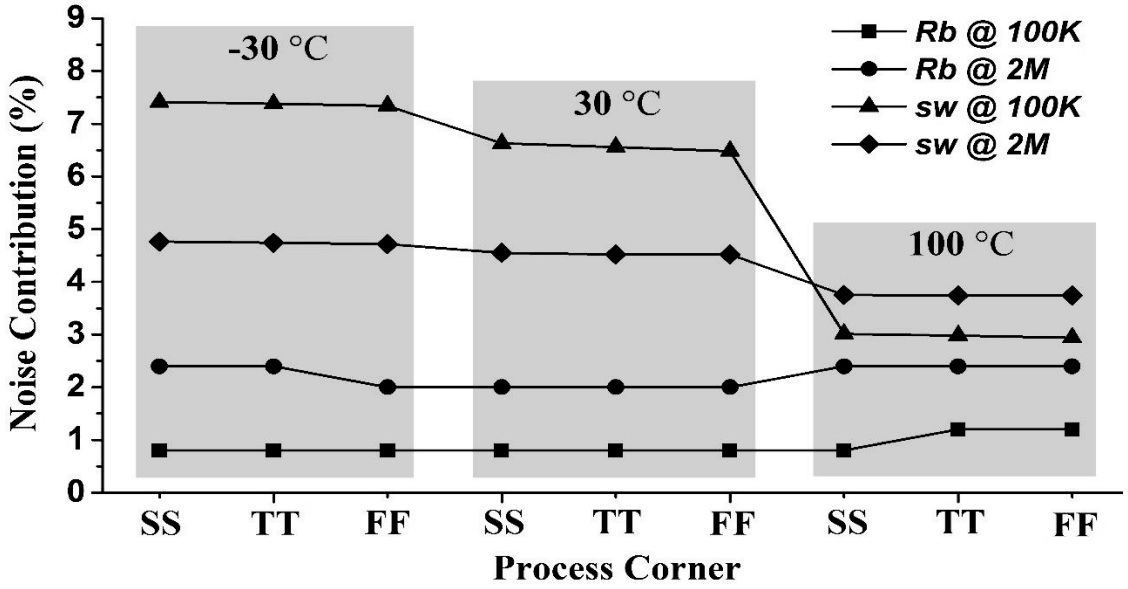


Figure 128. Noise contributions: the switches and the R_b at three corners and temperatures

7.4 Experimental Results

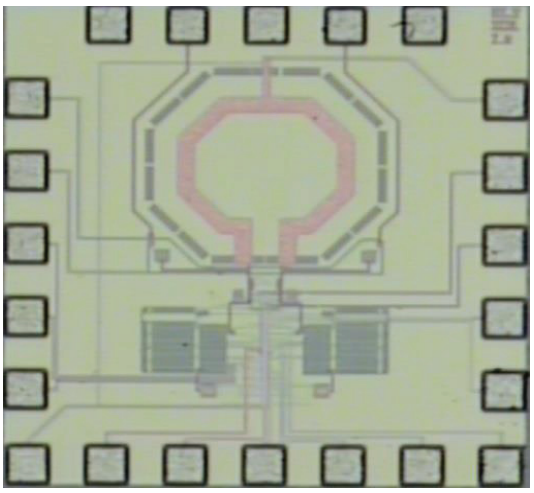
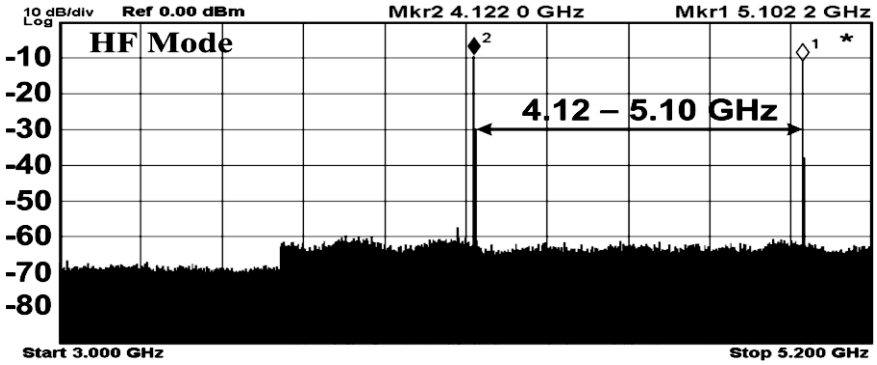
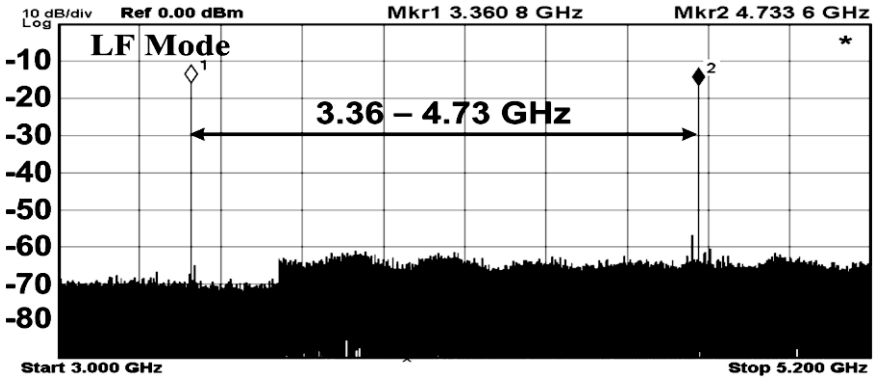


Figure 129. Photograph of the proposed VCO

Figure 129 shows a photograph of the proposed wideband VCO, which was fabricated in 65-nm CMOS technology. The occupied area was a 0.24 μm^2 and the total power consumption was 8.7 mW when the *LC*-VCO operates at 5 GHz.



(a)



(b)

Figure 130. Measured minimum and maximum oscillation frequency in (a) HF-Mode (b) LF-Mode

Figure 130(a) shows the swept output frequency of the VCO in both the HF mode and the LF mode. In this measurement, when all the capacitors in the capacitor bank were off and the V_{tune} was 1.2 V, the maximum oscillation frequency was 5.1 GHz. Figure 130(b) shows that the measured oscillation frequency range was from 3.36 to 4.73 GHz when the VCO operates in the LF mode. Compared to the HF mode, meanwhile the maximum oscillation frequency of the LF mode is decreased by 370 MHz by the parasitic capacitance, the minimum oscillation frequency was able to be lowered more than 700 MHz by the boosted transconductance from the secondary core.

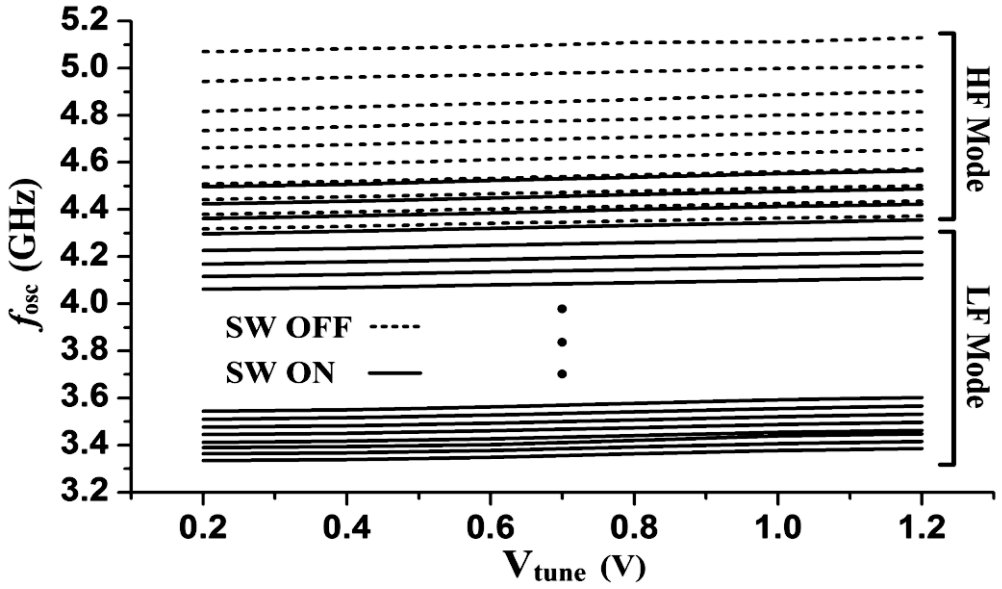


Figure 131. Measured frequency tuning range in the LF mode and the HF mode by sweeping the capacitor bank and the varactor

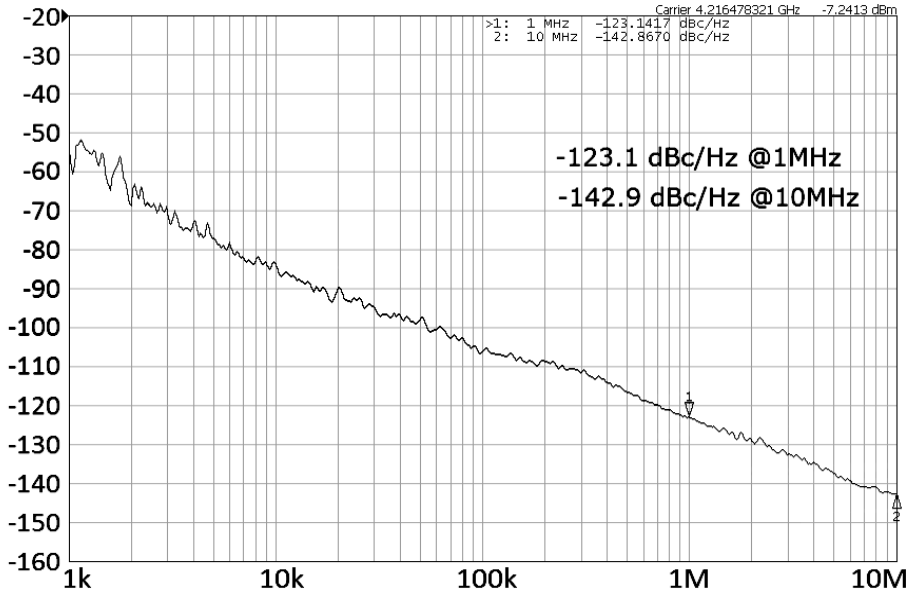


Figure 132. Measured phase noise in the LF mode when the VCO oscillates at the 4.21 GHz

Figure 131 shows the measured oscillation frequency of the proposed VCO by sweeping the control code of the capacitor bank and the control voltage the varactors, V_{tune}. By turning on or off the switches, the VCO can be operated at either the LF or the HF mode, respectively. From the measurement results, the measured FTR of the *LC*-VCO was from 3.36 to 5.10 GHz, which corresponds to the frequency tuning range of 41%. Figure 132 shows the measured single sideband (SSB) phase noise result when the VCO operates at 4.21 GHz, which is the maximum oscillation frequency when the *LC*-VCO is in the LF mode. This measurement is the worst case since as shown in Figure 127(b), in the LF mode, when the oscillation frequency goes higher, the R_p becomes degraded by the on-resistance of the switches, which also degrades the Q-factor. Figure 132 shows the measured spot phase noise was -123.1 and -142.9 dBc/Hz at the 1 and 10 MHz offsets, respectively. The time required for switching mode from LF (or HF) to HF (or LF) is mainly limited by the *RC* gate-bias circuits, which is approximately 10ns in the measurements.

7.5 Conclusions

In this proposed work, a new wideband *LC*-VCO having a dual-mode with a switchable transconductance of the main core transistors is proposed. To boost up the gain for the start-up of the *LC*-VCO when the lower oscillation frequency is required, the switches are shorted between the primary and the secondary core, which is called as the LF mode. On the other hand, in the HF mode, the switches are opened to isolate the primary core from the secondary core to reduce the capacitance loading. Therefore, the maximum oscillation frequency can be extended since there is no capacitive loading originated from the secondary core. Moreover, at the gates of the secondary core, the *RC* gate-bias circuits are employed to have a high transconductance even with the drop in the DC voltage at the gate of the secondary core by on-resistance from the switches. The performance summary is shown in Table 17. Table 18 shows the performance comparison with state-of-the-art wideband *LC*-VCOs. As shown in Table 18, the proposed VCO achieved a competitive FOMT of 198.4 while provides both low phase noise and a wide tuning range.

Table 17. Performance Summary

Power consumption (VCO core only)	8.7 mW at 5GHz
Oscillation frequency	3.361 − 5.102 GHz
Tuning range	41.1 %
Frequency-voltage gain (K_{VCO})	50 − 85 MHz/V
Phase noise (f_{osc} = 4.21 GHz, Δf = 1MHz)	−123.14 dBc/Hz

Table 18. Performance Comparison With Wideband *LC*-VCOs

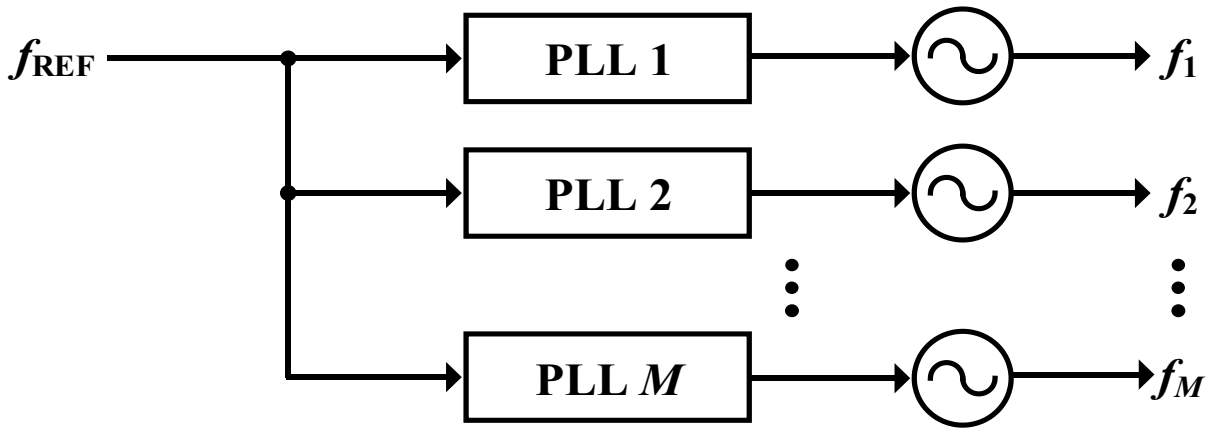
Reference	**[102]**	**[105]**	**[107]**	**[108]**	**This Work**
Process	350nm BiCMOS	130nm CMOS	90nm CMOS	130nm CMOS	65nm CMOS
FTR Range (Hz)	31% 3.8–5.2G	50.6% 3.1–5.2G	45% 4.5–7.1G	39% 3.8–5.6G	41.1% 3.36–5.10G
PN (dBc/Hz) @ $\Delta f/f_{osc}$ (Hz)	–110.0 @ 1M/5.2G	–117.0 @ 1M/3.8G	–108.5 @ 1M/5.63G	–119.21 @ 1M/4.28G	–123.14 @ 1M/4.21G
P_{DC} (mW)	6.4	5.2	14	5	8.7
***FOMT**	186.1	195.5	185.1	196.7	198.4

$$*\,\mathrm{FOMT} = -\mathrm{PN}(f_{off}) + 20\log\frac{f_o}{f_{off}} - 10\log\frac{\mathrm{P_{DC}}}{1\mathrm{mW}} + 20\log\frac{\mathrm{FTR}}{10} \quad [102]$$

8. Design of Multi-Clock Generator

8.1 Objective and Motivation

Modern system-on-chip (SoC) includes various modules, which perform a number of functions, such as memory, input/output (I/O) interfaces, microprocessors, and the power management. To simultaneously improve overall system performance with high energy efficiency, each module must operate at a unique optimum clock frequency. [109] – [114]. In addition, for optimizing the overall system performance and the energy efficiency, multiple clock frequencies, whose frequency can be changed dynamically with fine resolution, are required in advanced multicore processors [115]. When considering a solution that generates multiple clock frequencies, the prerequisite is to sustain low phase noise performance of the output signal of each clock, without excessively high power consumption and huge silicon area [113], [116]. Figure 133(a) shows the simplest architecture using multiple phase-locked loops (PLLs), which are connected in parallel. Since this approach requires multiple PLLs to operate simultaneously, a significant amount of power will be consumed and a large silicon area will be occupied, which conflicts with previous prerequisites. In contrast to this one-dimensional approach, [117] proposed a new architecture, which is shown in Figure 133(b). Here, only a single fractional-*N* PLL is used and there are subsequent frequency dividers having a fractional resolution. Each frequency divider includes a delta-sigma modulator (DSM) and a circuit to remove a quantization-noise (Q-noise), i.e., Q-noise canceler. Compared with the architecture in Figure 133(a), it overwhelms the previous one in terms of power consumption and silicon area since it has only one PLL.



(a)

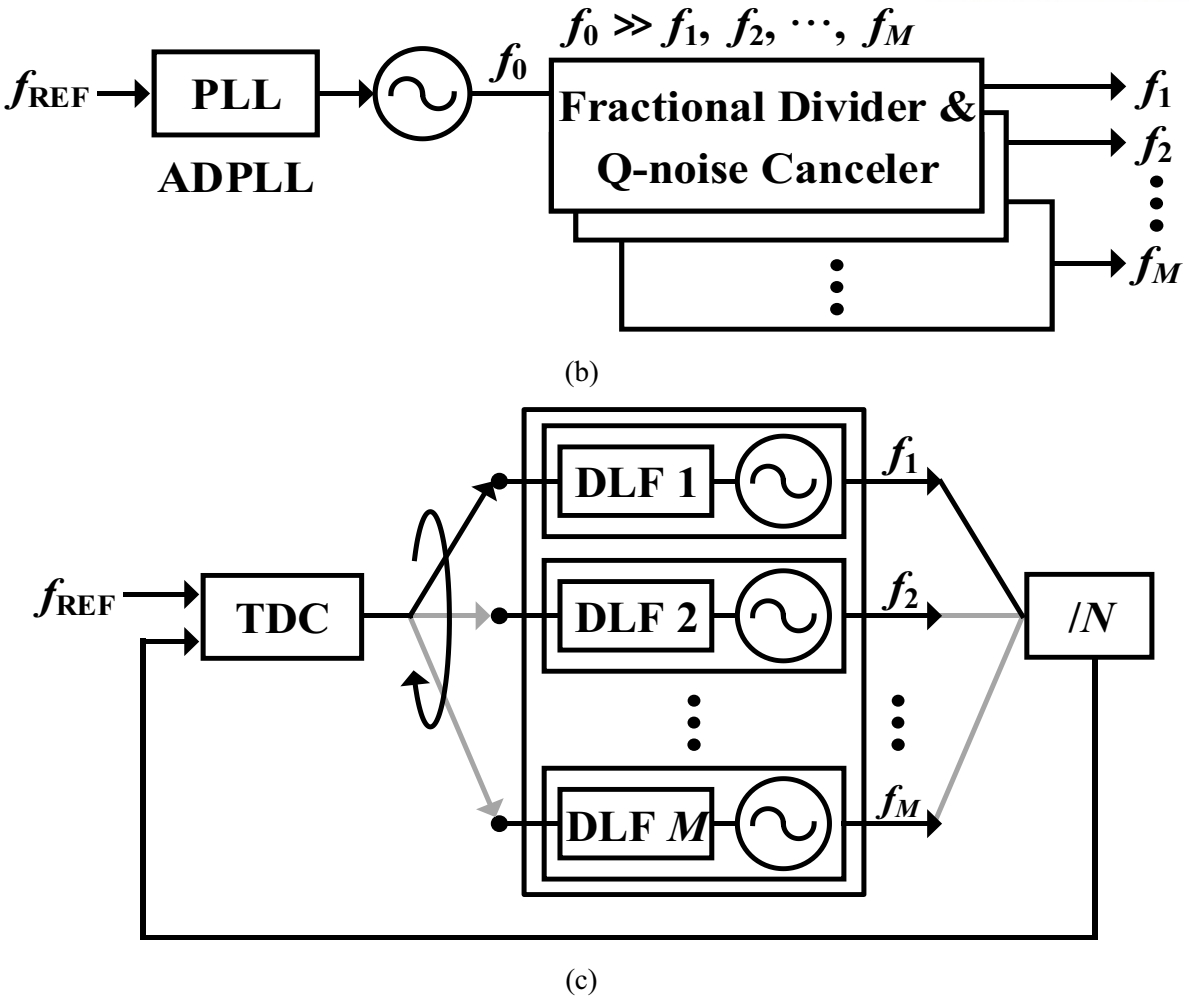
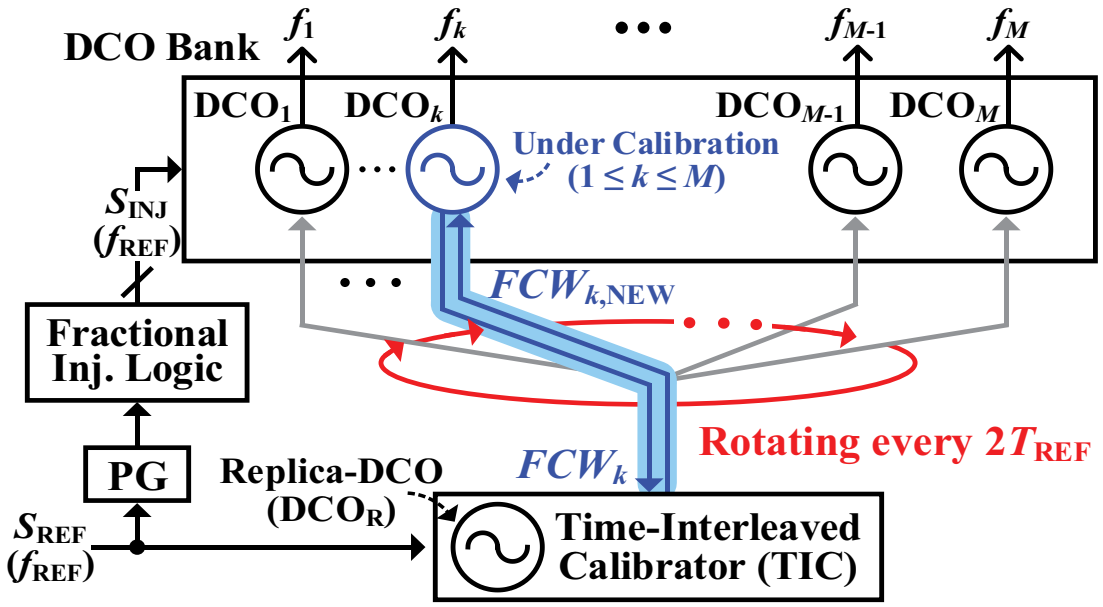


Figure 133. Conventional architectures providing multiple outputs with different operating frequency: (a) multiple PLLs in parallel; (b) a single PLL with subsequent multiple fractional dividers with a fractional resolution; (c) digital PLL includes multiple DCOs, which are corrected by a single TDC

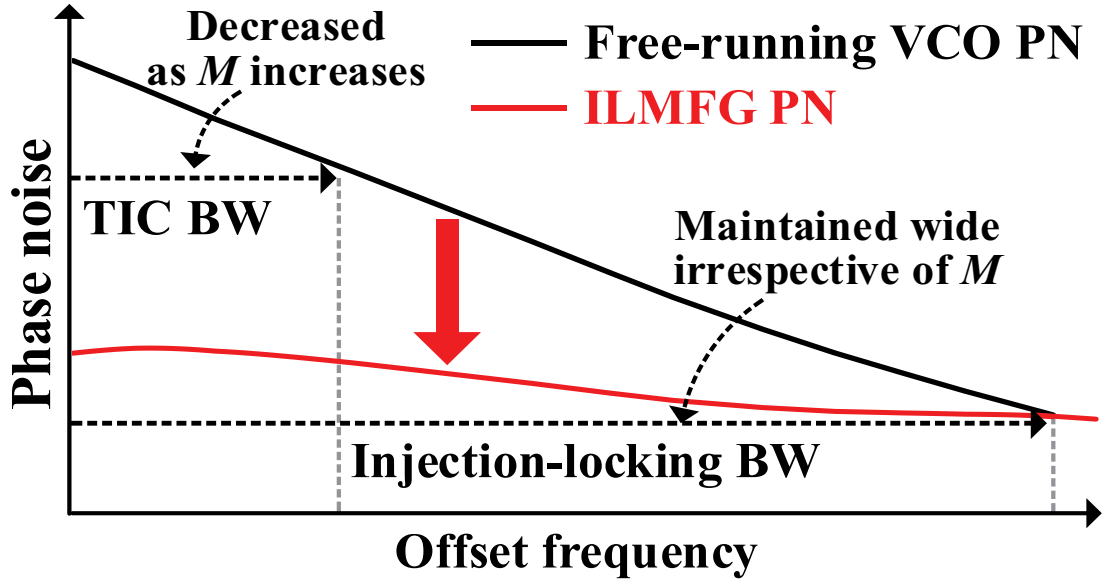
However, since the operating frequency of the output signal decrease as the frequency passes through the frequency dividers, the PLL operating frequency, f_0, by considering the division ratio of the divider, the operation frequency must be higher than the required frequencies. Therefore, additional power is consumed by the PLL. In addition, the Q-noise canceller along with the DSM increases the complexity of the design and the operation of the frequency dividing requires more power consumption. Alternatively, a multi-frequency generator can be designed in a digital fashion as in Figure 133(c), which includes a time-to-digital converter (TDC) and multiple pairs of a digitally-controlled oscillator (DCO) along with a digital loop filter (DLF). Only a single TDC is connected to the DCOs and it sequentially calibrates the frequency drifts of each DCO. Since the required number of TDC is only one to corrects all DCOs, this architecture has low complexity and small the power consumption compared to the architectures in Figure 133(a) and (b). However, when the number of DCOs, M, increases, it implies that the calibration period for each DCO is extended by M times. Thus, the effective comparison

frequency seen by each DCO should decrease accordingly, which means the narrowed loop bandwidth. Therefore, this degrades the phase noise and increases the settling (or locking) time.

In this work, we propose an all-digital injection-locked multi-frequency generator (ILMFG), which simultaneously generates multiple output clocks with an ultra-low-jitter, which operates at different clock frequencies [118]. The concept of the propose multi-frequency generator is illustrated in Figure 134(a). The ILMFG includes the DCO bank having multiple DCOs and a time-interleaved calibrator (TIC). The TIC sequentially calibrates each DCO's output frequency in the background with the help of the replica-DCO. Similar to the architecture of Figure 133(c), the bandwidth of the TIC cannot be widened, since the TIC calibrates the DCOs in a time-interleaved fashion. But, there are difference from the digital PLL with multiple DCOs shown in Figure 133(c), where the large M degrades the phase noise, the proposed multi-frequency generator in Figure 134(a) can stably provide ultra-low-jitter output signals regardless of the number of M. This is because the injection-lock bandwidth of the DCO can be kept very wide, regardless of M, since the injection pulse is continuously injected into all DCOs at every period of the reference clock, i.e., the bandwidth of the TIC and that of the injection-locking have no relationship. Thus, as drawn in Figure 134(b), the injection-locking can suppress the phase noise (or jitter) dramatically up to its bandwidth, which is typically wide [119], [120]. Here, the main purpose of the calibrator is not only to reject DCOs' noise but also to calibrate the frequency drifts in DCOs [46], [89], [90], [121], [122], [123], [124] – [127], which doesn't need to have wide bandwidth. Therefore, the bandwidth of the TIC need not be wide if that bandwidth can track the variations in the supply voltage or the temperature. In addition, the proposed clock generator can have a fractional resolution for the multiplication factor, by the fractional injection logic [128], which rotationally injects the injection pulses into the ring DCO's nodes.



(a)



(b)

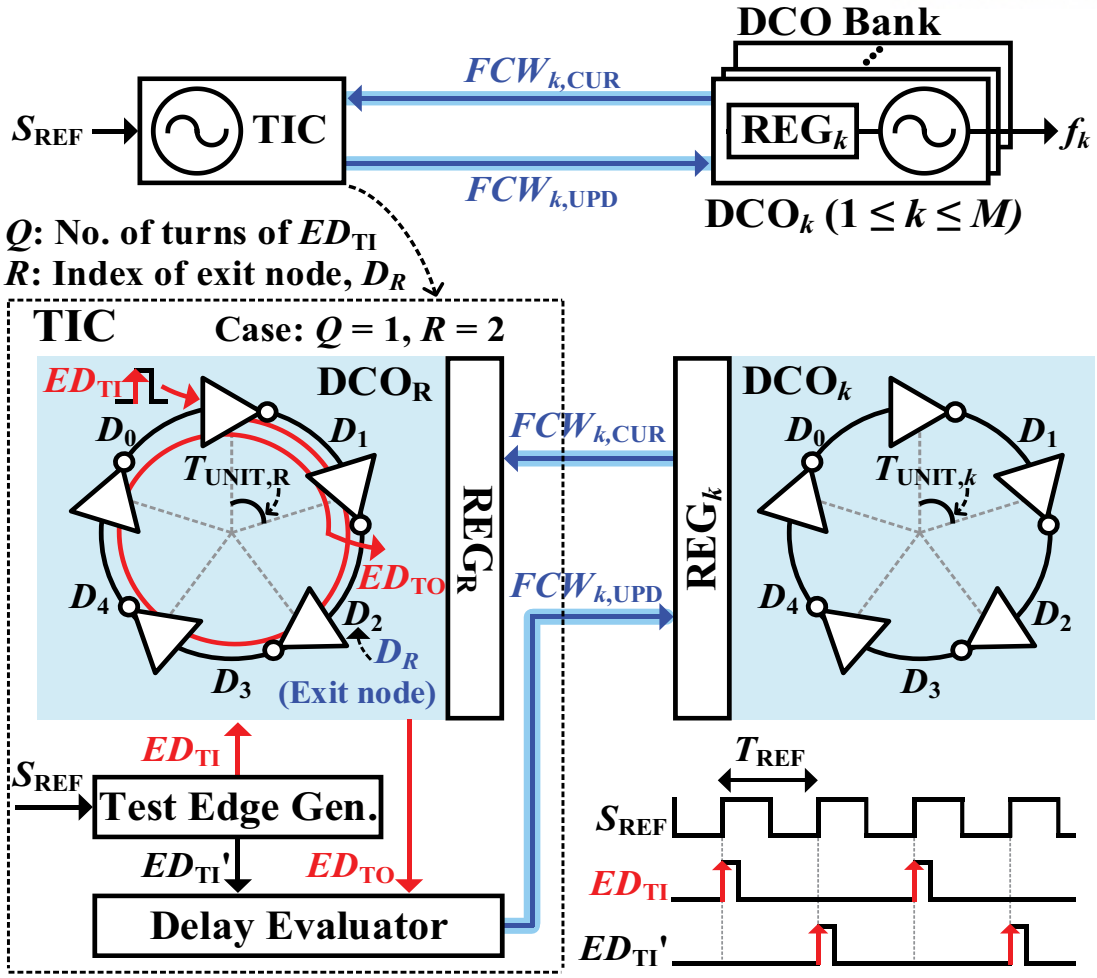
Figure 134. (a) Conceptual diagram of this work with the time-interleaved calibration (b) how the ILMFG can have low noise with the help of the injection locking

This Chapter is organized as follows. In Chapter 8.2, the concept of this work is introduced along with the proposed calibrator operating in the time-interleaved fashion. Chapter 8.3 explains the implementation of the ILMFG with its operation. Chapter 8.4 describes the effects such as phase noise and the spur, which is raised by the frequency mismatches between DCOs of the DCO bank and the replica-DCO. Chapter 8.5 and 8.6 present experimental results and the conclusions, respectively.

8.2 Concept of the Proposed Multi-Frequency Generator

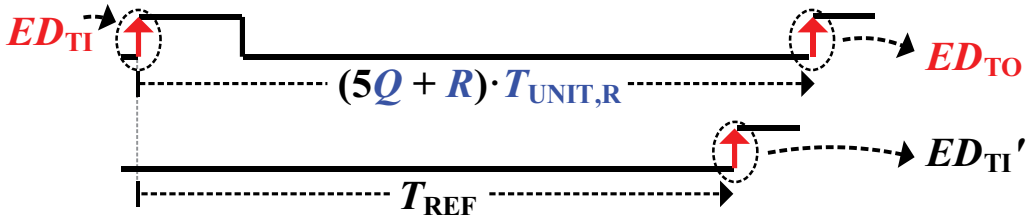
Figure 134(a) shows the proposed ILMFG, which has a DCO bank containing M identical ring-based DCOs, DCO_ks, the TIC having the replica-DCO, DCO_R, and a pulse generator (PG) followed by a fractional injection logic. Here, the range of k is between 1 and M. Each DCO_k it can have an independent output frequency, f_k, since it is controlled by its own frequency control word (FCW). The TIC sequentially shifts the target DCO to be calibrated every $2T_{REF}$, where T_{REF} is the period of S_{REF}. Since DCO_R is not injection locked by the pulses, if DCO_R shares the same FCW with the target DCO, the target DCO's free-running frequency can be evaluated in real time [129] – [131]. Regardless of which DCO is being calibrated by TIC, all the DCOs are injection locked by the injection pulses, S_{INJ}, which is generated from the rising edge of S_{REF}, i.e., the frequency of S_{INJ} equals f_{REF}. Thus, even when we have the narrowed bandwidth of the TIC by the increase of M, the bandwidth of the injection-locking is kept wide independent of the number of M. Thus, all DCOs can have very an ultra low jitter or phase noise. In summary, the proposed ILMFG has advantages as follows. First, the power efficiency of the proposed ILMFG increases corresponds to the value of M, since only a single calibrating loop is employed. Second, M output signals of the ILMFG can achieve ultra-low jitter, since the injection-locking bandwidth has no relationship with that of the TIC. In other words, the jitter of the DCOs can be greatly suppressed up to the injection-locking bandwidth even when the TIC's bandwidth is narrow due to the time-interleaved calibration. Thus, all DCOs in the DCO bank can achieve low phase noise performance even there are PVT variations. Third, point (node) of the DCOs, where the injection pulses to be injected, are controlled by the fractional injection logic [128]. Therefore, the output frequencies of the DCOs have a fractional frequency resolution, i.e., one tenth of f_{REF}. This resolution is much larger than the frequency step of typical fractional-N PLLs having DSM. But, this frequency resolution is sufficiently smaller than the required one by the advanced multicore processors in modern SoCs [115].

Figure 135(a) shows the operating principle of the ILMFG along with the TIC, i.e., how captures the deviation of the free-running frequency of each DCO, $f_{k,FR}$, from the target frequency, $f_{k,TAR}$. The DCO_k is designed based on inverters and it has five stages. DCO_k is connected to a register, REG_k, which remembers FCW for the DCO itself. The TIC includes a delay evaluator, a test-edge generator, and the DCO_R with a register, REG_R, which also remembers the FCW of DCO_R. As shown in the timing diagram in Figure 135(a), two consecutive edges are provided by the test-edge generator generates, i.e., the rising edges of ED_{TI}' and ED_{TI} are originated from the even and odd rising edges of S_{REF}, respectively. When DCO_k is calibrated, the operation of the TIC is as follows. First, if a DCO_k is selected to be calibrated, the current FCW of DCO_k, $FCW_{k,CUR}$, moves to REG_R. Then, the delay of the unit delay cell of DCO_k, $T_{UNIT,k}$, is copied to that of DCO_R, $T_{UNIT,R}$. Second, a test edge of ED_{TI} is injected to the initial node of the DCO_R, D_0. Then, ED_{TI} goes around the five delay cells, whose base is an inverter. When it finishes Q turns, the edge will exit at the node of D_R ($0 \le R \le 4$), with the name of the returning test edge, ED_{TO}.



(a)

Operation of Delay Evaluator



$f_{k,FR}$	Evaluation	$FCW_{k,UPD}$ =
$> f_{k,TAR}$	ED_{TO} leads ED_{TI}'	$FCW_{k,CUR} - 1$
$< f_{k,TAR}$	ED_{TO} lags ED_{TI}'	$FCW_{k,CUR} + 1$

(b)

Figure 135. (a) The TIC's operation (b) operation of the delay evaluator in two cases

Figure 135(a) shows an example when Q is 1 and R is 2, which is represented by the red line. The value of Q and the value R are already pre-determined when the target frequency of DCO_k is set. The total

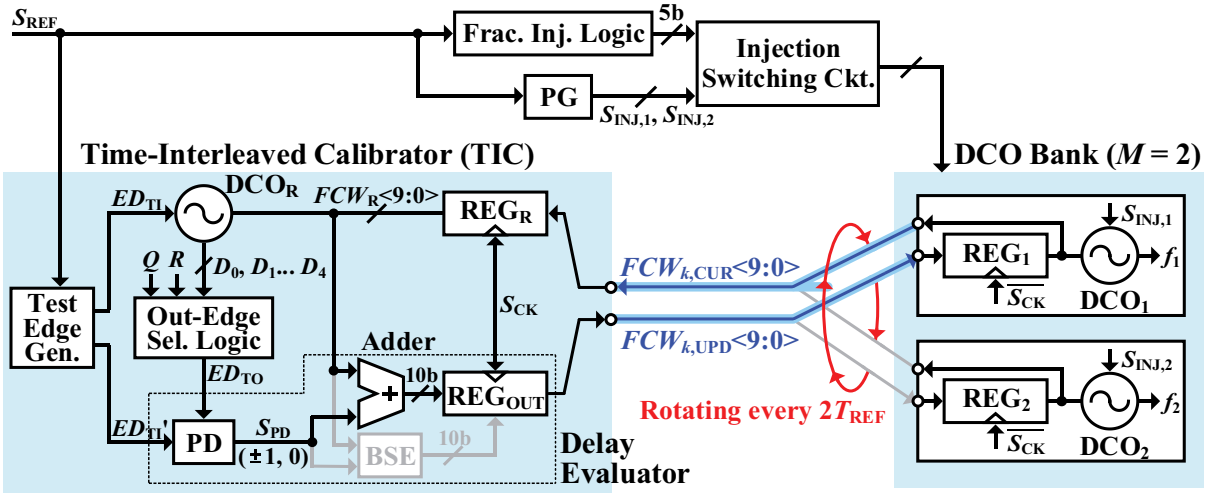
traveling time of the test edge can be represented as $(5Q + R)\cdot T_{\mathrm{UNIT,R}}$, because the DCOs consists of five stage, i.e., N_{DCO} is five. By comparing the traveling time with T_{REF}, i.e., examines which edge between ED_{TO} and ED_{TI}' first arrives, the amount of $T_{\mathrm{UNIT,R}}$, and thus, $T_{\mathrm{UNIT},k}$ can be calculated. Then, according to this evaluation's result, the delay evaluator provides the updated FCW, $FCW_{k,\mathrm{UPD}}$, to the REG_k. The table in Figure 135(b) shows how $FCW_{k,\mathrm{UPD}}$ is calculated. When $f_{k,\mathrm{FR}}$ is faster than $f_{k,\mathrm{TAR}}$, ED_{TO} comes first than ED_{TI}'. Then, $FCW_{k,\mathrm{UPD}}$ is replaced by $FCW_{k,\mathrm{CUR}}-1$ to slow down $f_{k,\mathrm{FR}}$. In the same manner, when $f_{k,\mathrm{FR}}$ is slower than $f_{k,\mathrm{TAR}}$, ED_{TO} comes later than ED_{TI}', and $FCW_{k,\mathrm{UPD}}$ is replaced by $FCW_{k,\mathrm{CUR}}+1$ to speed up $f_{k,\mathrm{FR}}$. Through this repetitive calibration, if the difference between $f_{k,\mathrm{FR}}$ and $f_{k,\mathrm{TAR}}$ close to zero, $FCW_{k,\mathrm{CUR}}$ settles since ED_{TI} and ED_{TI}' arrive almost at the same time. At this time, the $f_{k,\mathrm{FR}}$ can be calculated as:

$$f_{k,\mathrm{FR}} \approx \frac{1}{2N_{\mathrm{DCO}}\cdot T_{\mathrm{UNIT},k}} = \frac{(5Q+R)\,f_{\mathrm{REF}}}{10} = 0.1N_k \cdot f_{\mathrm{REF}} \tag{129}$$

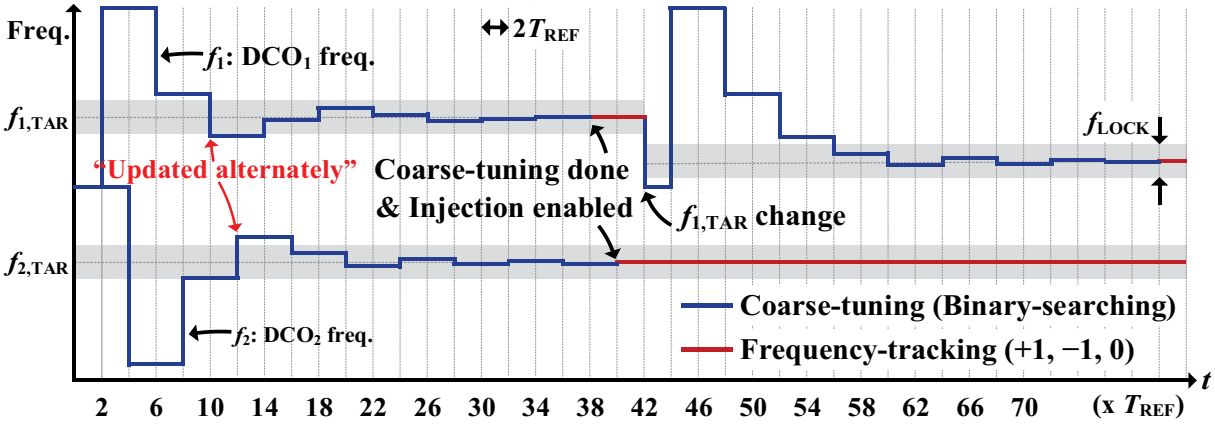
where N_k is the total number of unit delay cells that ED_{TI} has passed, i.e., $N_k = 5Q + R$.

8.3 Implementation of Highly-Digital Multi-Frequency Generator

8.3.1 Implementation of the Overall Architecture



(a)



(b)

Figure 136. The ILMFG: (a) Overall architecture (b) timing diagram

Figure 136(a) shows the overall architecture of the proposed ILMFG. As shown, it includes the TIC, the DCO bank, injection switching circuits, and a pulse generator along with a fractional injection logic. In this prototype, the number of DCO is fixed at two, i.e., M is two. However, M can be easily increased just by adding more DCOs to the DCO bank. The DCO has a 10-bit capacitor bank for controlling its output frequency and an injection transistor, which is implemented using NMOS, to receive injection pulses from the PG. The register of DCO_k, REG_k, stores $FCW_{k,CUR}$<9:0> and receives $FCW_{k,UPD}$<9:0> from the TIC. The TIC consists of a phase detector (PD), a binary-search engine (BSE), a 10-bit adder DCO_R, the test edge generator, and an out-edge selection logic. The TIC shifts the target DCO at every $2T_{REF}$. When DCO_k begins to be calibrated by the TIC, through the channel created between the TIC and the DCO_k, FCW_R<9:0> is initialized as $FCW_{k,CUR}$<9:0>. Since the same FCW is

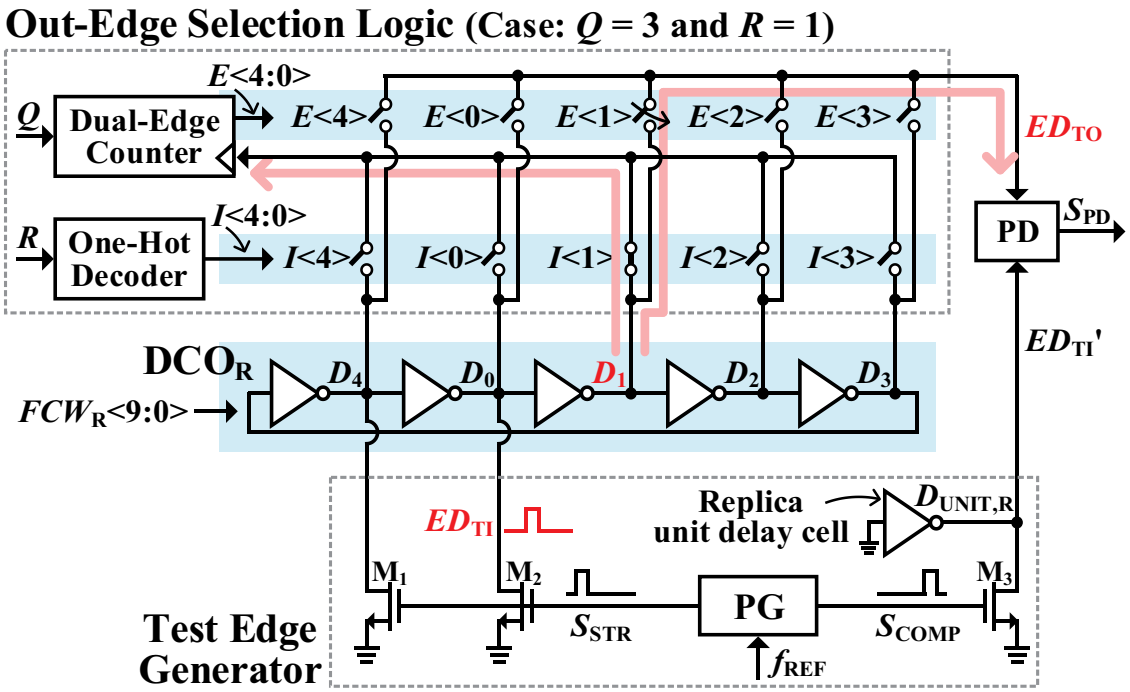
shared between the DCO_R of the TIC and DCO_k, they can have the same output frequency. ED_{TI} is then injected into the DCO_R, and the out-edge selection logic connects between the PD and D_R according to the value of R. When ED_{TI} completes the travel for $(5Q + R)\cdot T_{UNIT,R}$, the out-edge selection logic outputs ED_{TO} to the PD. After that, the PD compares the timings of ED_{TI}' and ED_{TO} and provides the output, S_{PD}, to the adder or the BSE. Based on the value of S_{PD}, $FCW_{k,UPD}$<9:0> of the REG_{OUT} is calculated and updated correspondingly. Finally, $FCW_{k,UPD}$<9:0> is transferred to REG_k to update $FCW_{k,CUR}$<9:0> for tracking the frequency deviation of DCO_k. For the PD, a dead zone was intentionally inserted [132]. Thus, if the timing difference between ED_{TO} and ED_{TI}' is within the dead zone, the PD outputs zero, thereby the toggling of $FCW_{k,CUR}$<9:0> can be avoided in the steady state. Therefore, spurious tones by the toggling can be prevented. In this prototype, the size of the dead zone was designed between the size of the LSB and the second LSB of the capacitor bank of the DCO.

How to update $FCW_{k,UPD}$<9:0> by using the information in S_{PD} depends on the calibration status. The timing diagram is shown in Figure 136(b) to explain the sequential operation of the proposed ILMFG and how both DCOs are calibrated together by the single TIC. During the coarse-tuning phase, the BSE only takes the polarity information in S_{PD}, which sequentially updates each bit of $FCW_{k,CUR}$<9:0> from the MSB to the LSB based on the binary search algorithm, to bring f_k briefly within the lock range of the injection, f_{LOCK}, which is denoted in gray. When this coarse-tuning phase finishes (e.g. in Figure 136(b), between $38T_{REF}$ and $40T_{REF}$), the injection switching circuit starts to inject pulses from the PG to the DCOs, based on the outputs of the fractional-injection logic. Therefore, now that both DCOs are injection locked, they can exactly generate their own target frequencies. Then the phase moves to the frequency-tracking phase. In this mode, the two injection-locked DCOs can continue to generate output signals with an ultra-low-jitter despite real-time environment variations, since the TIC keeps correcting the frequency drifts of DCO_1 and DCO_2 alternately. As shown in Figure 136(b), when the target frequency of DCO_1 (i.e., $f_{1,TAR}$) is suddenly changed at $42T_{REF}$, the coarse-tuning phase with the BSE again starts to bring DCO_1's free-running frequency (i.e., $f_{1,FR}$) swiftly within the locking range. Note that DCO_1 can start generating the changed $f_{1,TAR}$, almost as soon as the injection is enabled again, because the wide bandwidth of the injection-locking. It means that the frequency-acquisition time is mainly determined by the time spent by the coarse-tuning. Because the BSE update each bit of the 10 bits capacitor bank one-by-one, the frequency-acquisition time can be calculated as $10\cdot 2M\cdot T_{REF}$. In this prototype, T_{REF} is 6.67 ns and M is 2, thus, the frequency-acquisition time is approximately 266 ns. Note that if M increases, the frequency-acquisition time also extends as well. However, even when M is set to 10, the frequency acquisition time is still less than 1.4 μs. In addition, when M is set to 10, during the frequency-tracking phase, each DCO will be corrected every 133 ns, which is very still faster than the frequency drifts by the environmental variations.

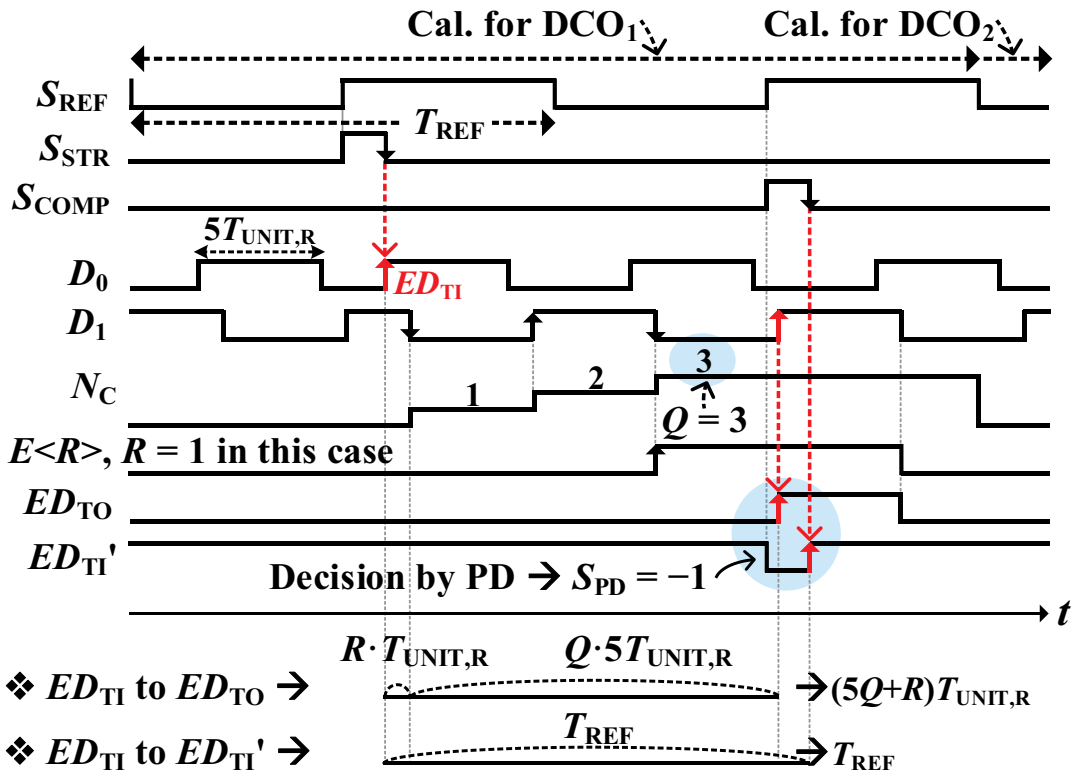
One critical disadvantage of the proposed calibration method is that the replica-DCO in the TIC consumes the same amount of the power as DCO_k. In particular, when M is relatively small such as two,

the power consumption of DCO_R accounts for a large portion in the total power consumption. To reduce this burden, the operation speed of the TIC can be slowed down in environments, where frequency drifts of the DCOs are not fast. For example, if the operation speed of the TIC slows down by eight times, each DCO_k will be calibrated every $32T_{REF}$ ($=8 \cdot 2M \cdot T_{REF}$). Then, the power consumed by the TIC is reduced accordingly. Even though the calibration speed is slowed down, there are no problems for the frequency tracking. This is because the slowed calibration speed is still much faster than the typical VT variations. For example, if M is designed as 10, each DCO is calibrated every 1.0667 μs when the calibration speed is lower by eight times than the normal mode.

8.3.2 Out-Edge Selection Logic and the Test Edge Generator



(a)

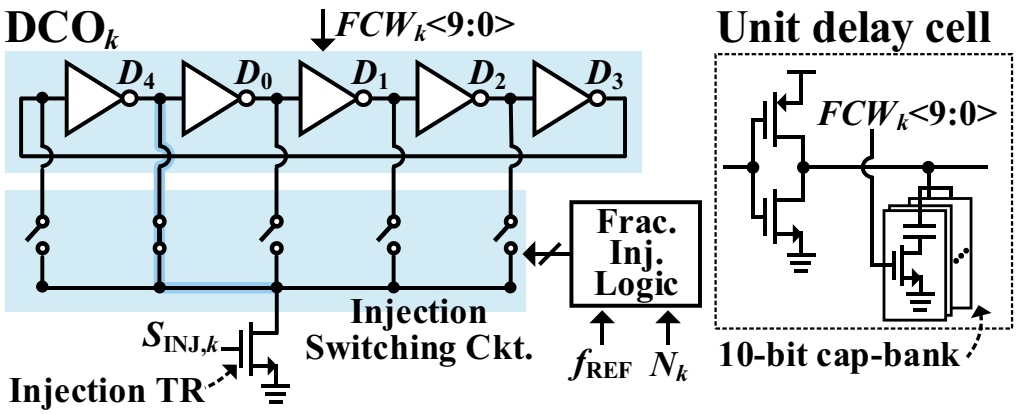


(b)

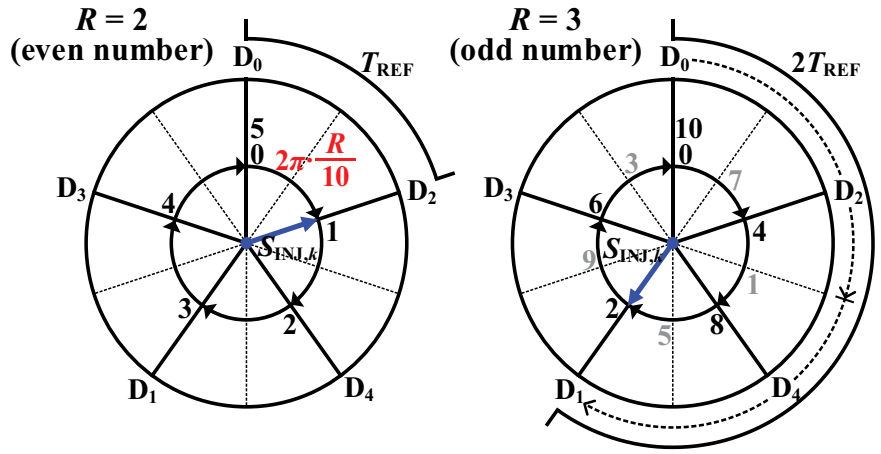
Figure 137. (a) schematics of the out-edge selection logic (b) example case when Q is 3 and R is 1: timing diagram in the normal mode

The schematics of the out-edge selection logic with the test edge generator and it's the timing diagram are shown in Figure 137(a) and (b), respectively. These figures illustrate an example case when the value of Q and R are three and one, respectively. It means that N_k is set to 16. As shown, the out-edge selection logic includes a one-hot decoder [133], a dual-edge counter, and 10 switches, which are shorted to the five output nodes of DCO_R. The test edge generator consists of a PG and three NMOS transistors, M_1, M_2, and M_3, whose the drains are shorted to the node of D_4, D_0, and the replica-unit delay cell, $D_{UNIT,R}$, respectively. Figure 137(b) shows two output signals of the PG, S_{STR} and S_{COMP}, which are alternately generated on the rising edges of S_{REF}. At every unit calibration period, i.e., $2T_{REF}$, the one-hot decoder generates I<4:0> based on the value of R. Since among I<4:0>, only I<R> has a high level, thus, the switch connected by I<R> among five switches will be turned on. Then, the signal at the node of D_R is transferred to a clock signal of the dual-edge counter. When the pulse of S_{STR} from the PG reaches the gates of M_1 and M_2, the nodes of D_4 and D_0 are pulled down to the ground. The change in the level of S_{STR} from high to low makes an abrupt change in the level of D_0 from low to high. This causes the injection of ED_{TI} to the node of D_0, and ED_{TI} starts to travel through the DCO. Since the DCOs include odd-number unit delay cells, i.e., five inverters, the dual-edge counter counts at the rising and also the falling edges of its clock signal to capture the number of turns, N_C. When the counted number, N_C, by the dual-edge counter becomes Q, a switch connected by a signal of E<R> is turned on to transfer the next rising edge of D_R to the PD at the name of ED_{TO}. Therefore, the total traveling time from ED_{TI} to ED_{TO} is effectively $(5Q + R)\cdot T_{UNIT,R}$. Finally, the PD compares ED_{TO} with ED_{TI}'. As shown in the timing diagram, because ED_{TI}' is created at the drain of M_3 at the falling edge of S_{COMP}, the time difference between ED_{TI} and ED_{TI}' is exactly T_{REF}, meanwhile the time difference between ED_{TI} and ED_{TO} is $(5Q + R)\cdot T_{UNIT,R}$. In the example case illustrated in Figure 137(b), since ED_{TI}' lags ED_{TO}, S_{PD} becomes −1, and thus the output frequency of the targeted DCO is calibrated based on the updated FCW by the polarity information of S_{PD}.

8.3.3 Digitally-Controlled Oscillator and Fractional Injection Logic



(a)



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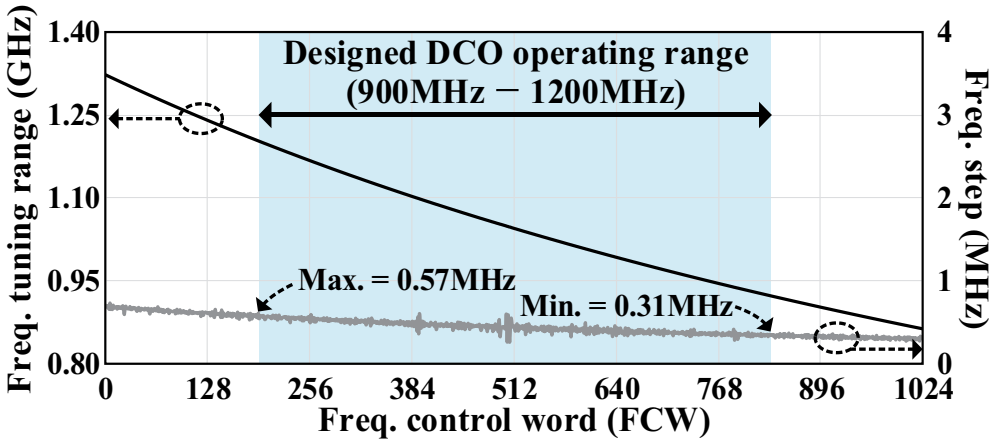


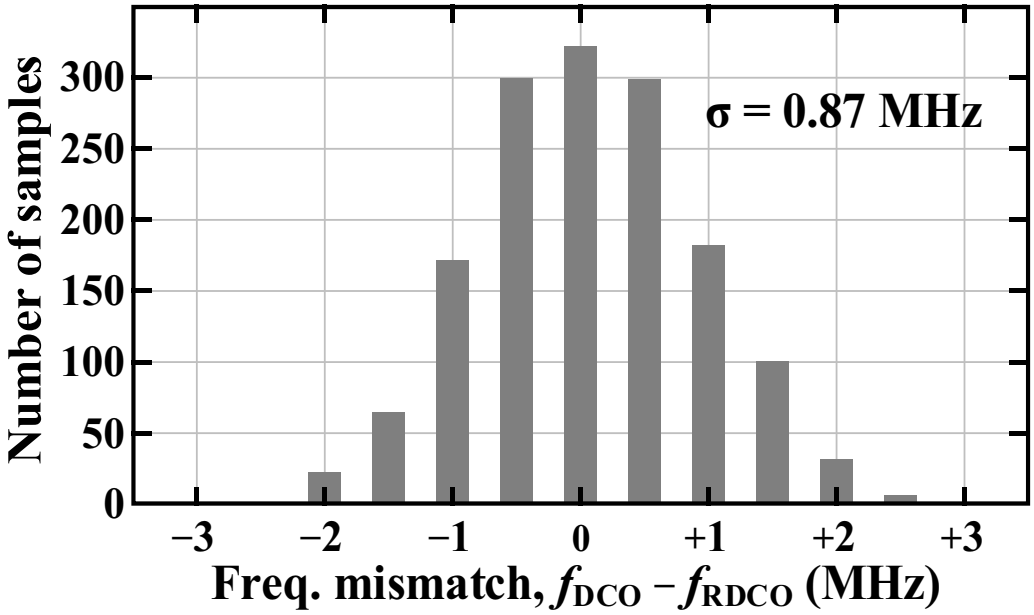
(c)

Figure 138. (a) Implementation of DCO (b) the fractional injection logic's the phase diagrams when *R* is two and three (c) Post-layout simulation results of the DCO; frequency tuning range and frequency resolutions (steps) across FCWs

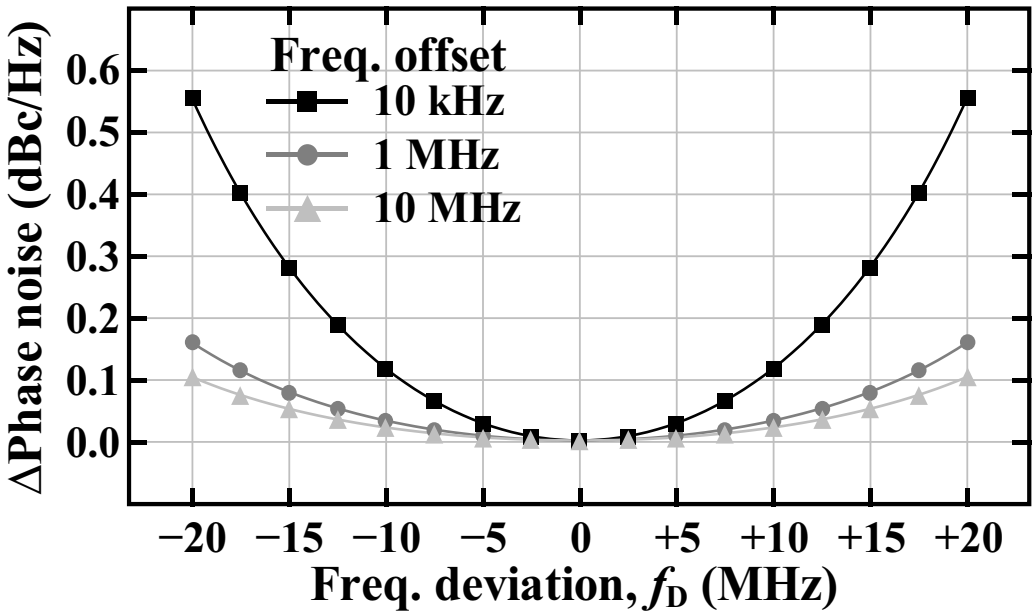
Figure 138(a) shows the design of DCO_k along with the unit delay cell including an inverter and a capacitor bank having 10-bit for the frequency control. The stream of pulses for the injection, $S_{INJ,k}$, generated by the PG are injected into DCO_k according to the injection switching circuits, which shifts the node that the pulses to be injected. To have the fractional frequency resolution, i.e., $0.1f_{REF}$, the fractional injection logic changes the injection node of the DCO among D_0, D_1, D_2, D_3, and D_4. Here, the input of the fractional injection logic is N_k [121]. To describe how the fractional injection logic controls the injection point, two phase diagrams in case of R is two (even) and three (odd) is shown in Figure 138(b). As a first case, if R is two (even), the injection point is rotated with two steps in every T_{REF}, and the injection pulse is injected into the rotated point at the same time. As a second case, if R is three (odd), the injection point is rotated with three steps in every T_{REF}, but an injection pulse is injected in every $2T_{REF}$. The reason is that the injection pulses must be aligned to the falling edges of DCOs for proper injection. In other words, the injection point will be rotated with six step in every $2T_{REF}$ and the injection pulses will be injected into that point at the same time. The DCO's post-layout simulation results about the frequency tuning range and the frequency resolution over FCWs are shown in Figure 138(c). When the FCW of the capacitor bank is swept from 0 to 1023 in decimal, the minimum and the maximum frequency resolution are 0.31 MHz and 0.57 MHz, respectively, when the output frequency of the DCO is within from 0.9 to 1.2 GHz. As shown, since the frequency change shows the monotonicity and the maximum frequency resolution is far smaller than the injection-locking range, the TIC can calibrate properly the frequency drifts of the DCO over the whole frequency tuning range, i.e., 0.9 GHz – 1.2 GHz.

8.4 Analysis of Frequency Mismatches Between DCOs and Phase Noise

8.4.1 Analysis of Frequency Mismatches Between the DCOs



(a)



(b)

Figure 139. (a) Monte Carlo simulations describing frequency mismatches between DCO_k and DCO_R (b) effect of the frequency deviations on phase noise

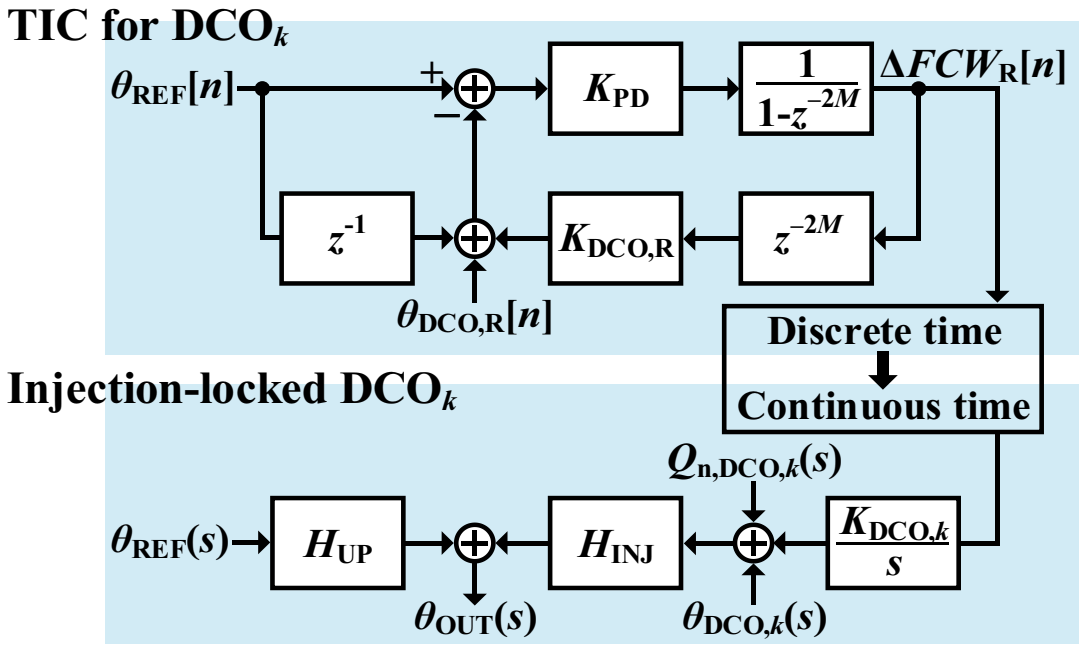
The proposed architecture assumes that each unit delay cell in the DCOs in the DCO bank and the DCO_R in the TIC can provide exactly the same output frequency if both DCO has the same FCW. Therefore, the calibrator's accuracy can only be guaranteed if the aforementioned assumption is valid.

However, even though we put many efforts in designing schematics and drawing layouts, inevitable mismatches between the delay cells of DCO_ks and DCO_R would occur since there is a local process variations. Therefore, in practice, even though DCO_R and DCO_k have same FCW_k, they cannot have the unit delay cell that can generate the same delay amount. In other words, the accuracy of the TIC inevitably degraded. Consequently, the calibrated frequency of DCO_k by the TIC will deviate from the target frequency, and thus, jitter performance of DCO_k will also be degraded greatly. Monte-Carlo simulations results are shown in Figure 139 for the frequency mismatches between the DCO_R and one DCO in the DCO bank. When the same FCW was applied to the two DCOs, each 500 samples are obtained at three different corners, i.e., TT, FF, and SS, thereby 1,500 samples in total. The used FCW is set to generate an output frequency of 900 MHz. As shown in Figure 139(a), the standard deviation of the mismatch was 0.87 MHz, which corresponds to 1.9% of the range of the injection-locking, f_{LOCK}, which was 40 MHz in this prototype. Figure 139(b) shows the phase noise degradation at the frequency offsets of 10 kHz, 1 MHz, and 10 MHz, when the frequency deviation, f_D, increases. Here, the frequency deviation is the difference between the free-running frequency of the DCO and the target frequency [134]:

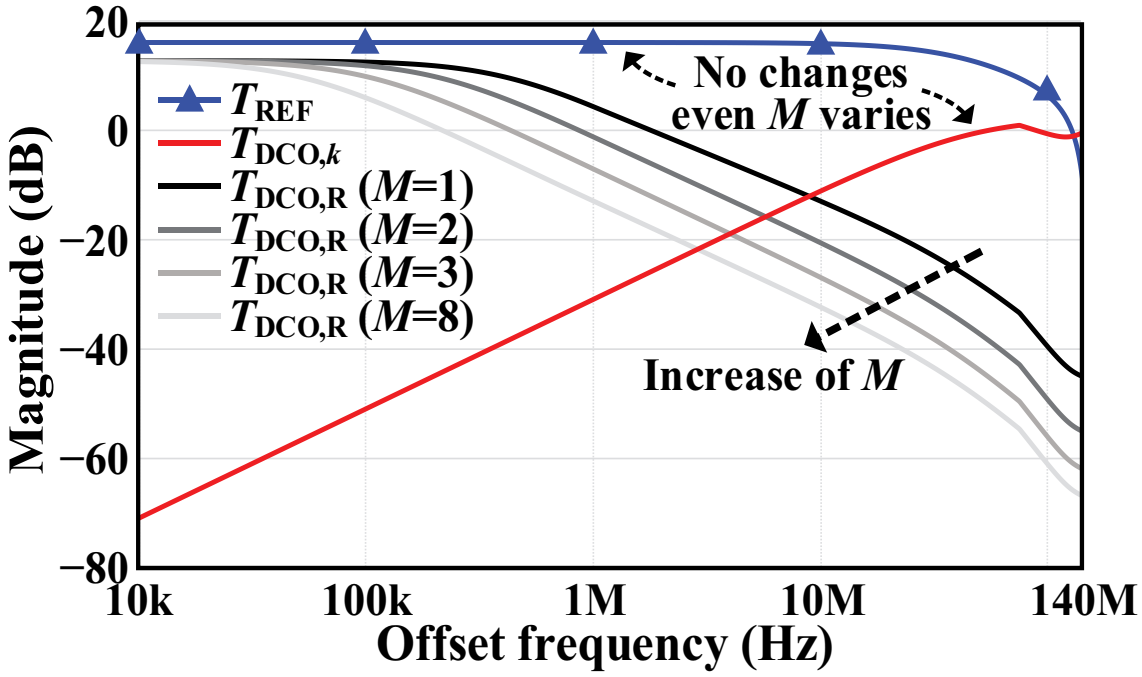
$$L_{\mathrm{LOCKED}} = \frac{(0.1N_k)^2 \cdot (f_{\mathrm{LOCK}}{}^2 - f_{\mathrm{D}}{}^2) \cdot L_{\mathrm{INJ}} + (\Delta f)^2 \cdot L_{\mathrm{FREE}}}{(f_{\mathrm{LOCK}}{}^2 - f_{\mathrm{D}}{}^2) + (\Delta f)^2} \tag{130}$$

where L_{INJ} and L_{FREE} are the phase noises of the injection signal and the free-running oscillator, respectively, and Δf is the offset frequency. The noise data of L_{INJ} and L_{FREE} were from measurements, and N_k and f_{LOCK} were set to 64 and 40 MHz, respectively. The graphs in Figure 139(b) shows that when f_D is 10 MHz, phase noise degradations at the offset frequencies of 10 kHz, 1 MHz, and 10 MHz were only 0.12 dB, 0.03 dB, and 0.02 dB, respectively, which are negligible values. In other words, there are no noticeable effect on the phase noise performance even when the frequency mismatch increases up to 10 MHz. In addition, from the Monte-Carlo simulation results showin in Figure 139(a), the level of the reference spur can be estimated based on the simple equation [46]. Based on this equation that estimates the level of the reference spur, the level of the reference spur due to 1-sigma local mismatches is estimated as –45 dBc, which is very close to the worst-case level of the reference spur measurement, as will be described in Chapter 8.5.

8.4.2 Analysis of Phase Noise of the Multi-Frequency Generator



(a)



(b)

Figure 140. (a) Noise modeling for the proposed ILFMG, which is calibrated by a time-interleaved passion; (b) noise transfer functions of each building block when M changes

The most eminent advantage of the proposed ILMFG is that each output signals can have a different output frequency with an ultra-low jitter performance by the injection-locking technique. In

this prototype, the value of M was designed as two for simply demonstrating the feasibility of the proposed time-interleaved calibration for correcting multiple DCO. However, the number of DCO, i.e., M, can be extended if required by applications. Therefore, in this subChapter, based on the theoretical analysis and MATLAB-based simulations, the capability to maintain the low-jitter performance of the proposed ILMFG will be verified even when M is large. The noise modeling of the proposed ILMFG is shown in Figure 140(a). Here, the calibrator part is modeled using the z-domain, i.e., discrete time domain. The unit of the gain for a DCO_k, $K_{DCO,k}$, DCO_R, and $K_{DCO,R}$ are [rad/s/FCW_{LSB}], [rad/s/FCW_{LSB}], [rad/FCW_{LSB}], and [rad/FCW_{LSB}], respectively. Here, for the gain of DCO_R and $K_{DCO,R}$ there is no integrator because the injection mechanism which reset the phase of DCO_R every T_{REF}. θ_{REF} is the output-referred phase noise of S_{REF} and $\theta_{DCO,R}$ is the output-referred phase noise of DCO_R. $Q_{n,DCO,k}$ is the quantization noise of the DCO_k. The transfer functions from S_{REF} to the FCWs and from the DCO_R to the FCWs, i.e., $H_{REF}(z)$ and $H_{DCO,R}(z)$, can be represented as

$$H_{\mathrm{REF}}(\mathrm{z}) = \frac{\Delta FCW_{\mathrm{R}}}{\theta_{\mathrm{REF}}} = K_{\mathrm{PD}} \frac{1-\mathrm{z}^{-1}}{1-(1-K_{\mathrm{PD}}K_{\mathrm{DCO,R}})\mathrm{z}^{-2M}} \quad \text{and} \tag{131}$$

$$H_{\mathrm{DCO,R}}(\mathrm{z}) = \frac{\Delta FCW_{\mathrm{R}}}{\theta_{\mathrm{DCO,R}}} = K_{\mathrm{PD}} \frac{1}{1-(1-K_{\mathrm{PD}}K_{\mathrm{DCO,R}})\mathrm{z}^{-2M}}, \tag{132}$$

respectively. Then, by using the bilinear approximation, the domain of $H_{REF}(z)$ and $H_{DCO,R}(z)$ can be replaced by the s domain, i.e., continuous time domain, which provides the equivalent transfer functions in the s domain [135]. The two transfer functions regarding the phase realignment by the injection-locking using the reference clock signal can be represented as follows [136]:

$$H_{\mathrm{INJ}}(j\omega) = 1 - \frac{\beta \cdot \mathrm{e}^{-j\omega T_{\mathrm{REF}}/2}}{1+(\beta-1)\mathrm{e}^{-j\omega T_{\mathrm{REF}}}} \frac{\sin(\omega T_{\mathrm{REF}}/2)}{\omega T_{\mathrm{REF}}/2} \tag{133}$$

$$H_{\mathrm{UP}}(j\omega) = \frac{(0.1N_k)\cdot\beta \cdot \mathrm{e}^{-j\omega T_{\mathrm{REF}}/2}}{1+(\beta-1)\mathrm{e}^{-j\omega T_{\mathrm{REF}}}} \frac{\sin(\omega T_{\mathrm{REF}}/2)}{\omega T_{\mathrm{REF}}/2} \tag{134}$$

where β is the phase realignment factor, whose value between 0 and 1. In other words, β represents the strength of the phase realignment when the injection pulses are injected. Based on Equation (131) − (134), the noise transfer functions (NTFs) from the reference clock to the output of the ILMFG, $T_{REF}(j\omega)$, to the DCO_R, $T_{DCO,R}(j\omega)$, and to the DCO_k, $T_{DCO,k}(j\omega)$ can be calculated as

$$T_{\mathrm{REF}}(j\omega)=\frac{\theta_{\mathrm{OUT}}}{\theta_{\mathrm{REF}}}=H_{\mathrm{UP}}(j\omega)+H_{\mathrm{REF}}(j\omega)\frac{K_{\mathrm{DCO},k}}{j\omega}H_{\mathrm{INJ}}(j\omega) \tag{135}$$

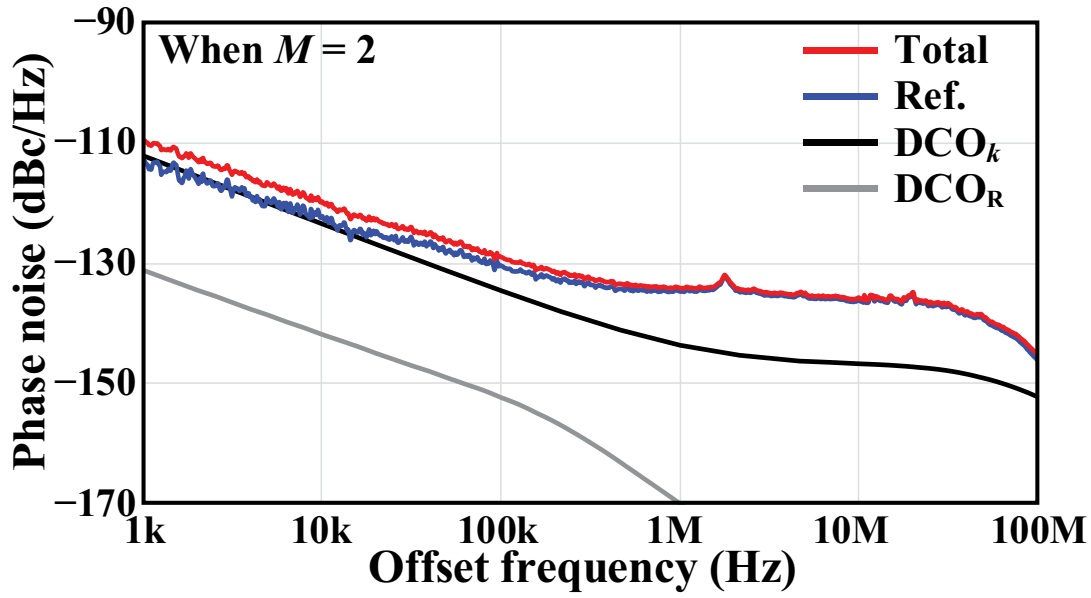
$$T_{\mathrm{DCO,R}}(j\omega)=\frac{\theta_{\mathrm{OUT}}}{\theta_{\mathrm{DCO,R}}}=H_{\mathrm{DCO,R}}(j\omega)\frac{K_{\mathrm{DCO},k}}{j\omega}H_{\mathrm{INJ}}(j\omega) \tag{136}$$

$$T_{\mathrm{DCO},k}(j\omega)=\frac{\theta_{\mathrm{OUT}}}{\theta_{\mathrm{DCO},k}}=\frac{\theta_{\mathrm{OUT}}}{Q_{\mathrm{n,DCO},k}}=H_{\mathrm{INJ}}(j\omega) \tag{137}$$

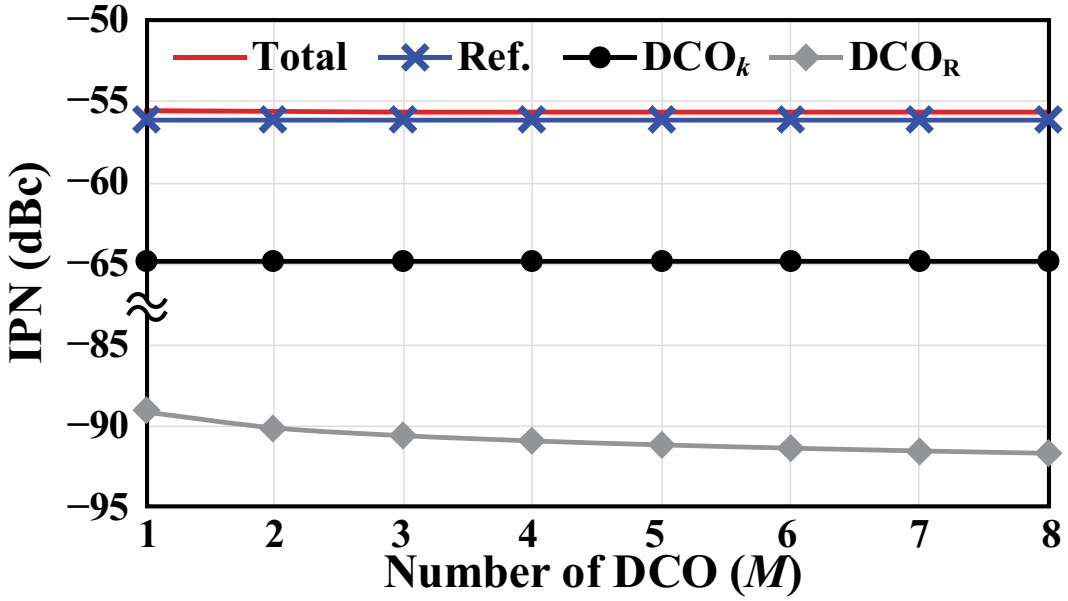
According to Equation (135) – (137), Figure 140(b) plots the NTFs of each building block, when M is swept from 1 to 8. To derive the NTFs, the output frequency of the DCO and β were assumed as 960 MHz, and 0.85, respectively. As shown in Figure 140(b), even when the value of M changes, $T_{\mathrm{REF}}(j\omega)$ and $T_{\mathrm{DCO},k}(j\omega)$ shows no changes. This is because in the NTF of $T_{\mathrm{REF}}(j\omega)$ and $T_{\mathrm{DCO},k}(j\omega)$, there is no factor related to M and they are only composed of $H_{\mathrm{UP}}(j\omega)$ and $H_{\mathrm{INJ}}(j\omega)$. This means that the jitter performance of DCO_k is independent of M. However, the bandwidth of $T_{\mathrm{DCO,R}}(j\omega)$ starts to narrow down as M increases from 1 to 8. This is because the dominant pole frequency of $H_{\mathrm{DCO,R}}(j\omega)$ is pulled toward the origin as M increases. Especially for the injection, previous analysis employed the noise modeling in paper [136], which is very useful for estimating the noise contribution of each building block. Thus, in this analysis the model was used to prove that the output jitter of the proposed ILMFG and the value of M are independent. However, the noise modeling presented in [136] shows inaccuracies when used to predict phase noise at high frequency offsets higher than the injection-locking bandwidth, because it does not take into account the noise-folding effect of oscillators. Recently, the paper [137] presented an improved method to analyze an oscillator using an injection-locking technique, by reflecting the sub-sampling effect from the injection pulses. Thus, the improved model in [137] is able to predict the exact phase noise at high frequency offsets, i.e., the phase noise is degraded approximately 3 dB compared to the noise modeling presented in [136].

When the output frequency of the DCO, M, and β was assumed as 960 MHz, two, and 0.85, respectively, by using MATLAB and the derived NTFs, the total phase noise and the noise contribution of each building block can be plotted as shown in Figure 141(a). The output-referred phase noise of S_{REF} was obtained through measurements, and that of other circuits were obtained from post-layout simulations. As shown in Figure 141(a), S_{REF} is the dominant noise source that accounts for 89.37% of the total IPN, while the contribution of DCO_k and $\mathrm{DCO}_{\mathrm{R}}$ are only 10.60% and 0.03%, respectively. There are two reasons for this. First, DCO_k was designed to intentionally consume huge power more than 2 mW to achieve low jitter. Second, the injection-locking can suppress the in-band phase noise of DCO_k up to the injection-locking bandwidth, i.e., 40 MHz. The change in the IPN to the value of M was simulated to estimate the increasing effect of M on the phase noise at each output of DCO_k. Figure

141(b) shows that the change in total IPN is less than 0.01 dBc while M varies from 1 to 8. This is because the IPN of S_{REF} shows negligible changes with the value of M, whereas S_{REF} is the dominant noise source. The analysis proves that even when the value of M increases further, the phase noise of the proposed ILMFG shows negligible changes. As shown in Figure 141(b) the contribution of DCO_R is reduced when the value of M increases. This is because as the value of M increases, the bandwidth of the calibrator decreases, thus less phase noise of the calibrator has appeared to each DCO_k.



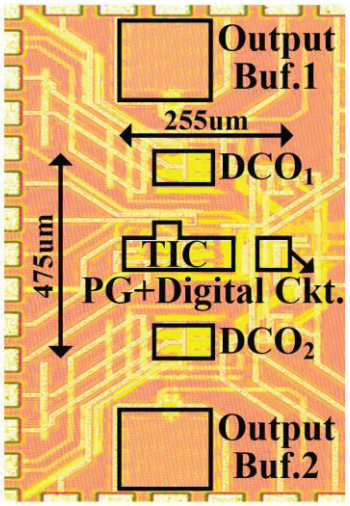
(a)



(b)

Figure 141. (a) Total phase noise and each building block's noise contribution plotted by the noise modelling through MATLAB (b) variation of the total IPN across the value of M

8.5 Experimental Results



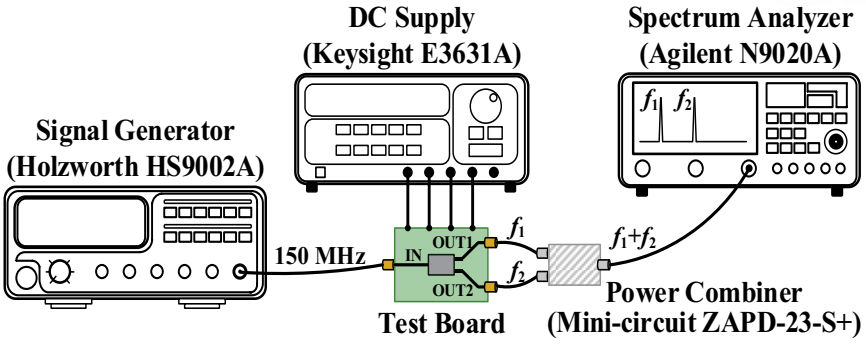
Power consumption (mW)	
TIC	2.87 (0.50*)
DCO_1	2.30
DCO_2	2.30
PG + Digital ckt.	0.27
Total power	7.74 (5.37*)

*When cal. speed of TIC slowed down by 8

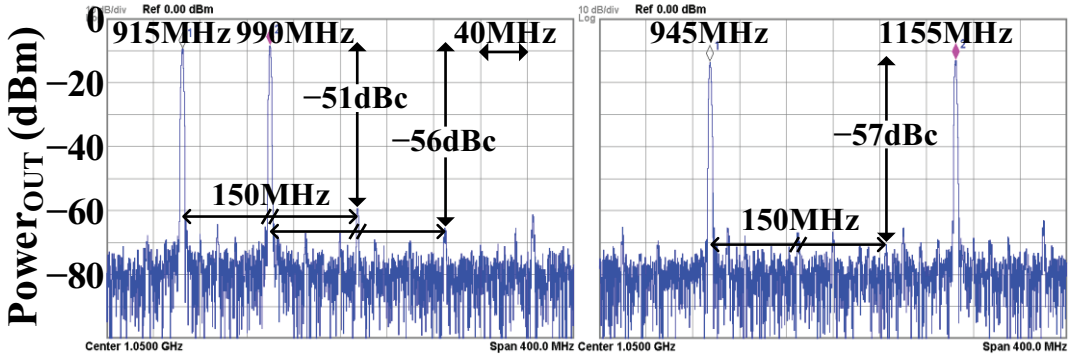
(a) (b)

Figure 142. (a) Die photograph. (b) power-breakdown table

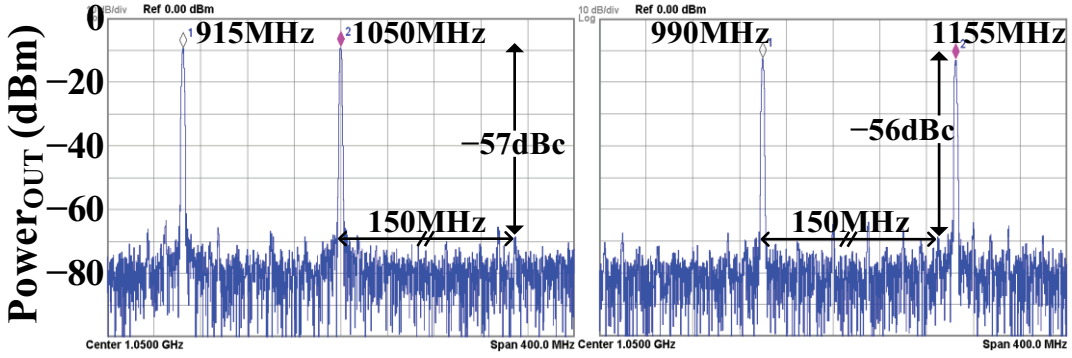
Figure 142(a) shows that the proposed ILMFG was fabricated in a 65-nm CMOS process. The total active area was 0.05 mm^2. Figure 142(b) shows the power break-down table. Here, the total power consumption was 7.74 mW for generating two different output frequencies; DCO_1 and DCO_2 consumed 2.3 mW and the TIC spent 2.9 mW. The other building blocks consumed only 0.27 mW. When the calibration speed of the TIC slowed down by eight times, the total power consumption was reduced from 7.74 to 5.37 mW, because the power consumed by the TIC is only 0.5 mW. To avoid frequency pulling between the two DCOs, they were located far from each other as shown in the die photo. However, it occurs more local mismatches between the two DCOs. Figure 143(a) shows the measurement setup how to measure the two output signals in a single spectrum. First, through an external power combiner (Mini-circuit ZAPD-23-S+), the two output signals of the DCOs with different frequencies, f_1 and f_2, are combined. Then, a spectrum analyzer, Agilent N9030A, measured the combined signal. For the reference clock, a signal source generator, Holzworth HS9002A, was used to provide f_{REF} of 150 MHz. Figure 143(b) – (g) show the spectrums of the combined two output signals with the numerous combinations of f_1 and f_2. As can be seen from the measurement results, f_1 and f_2 can be changed independently at intervals of 15-MHz between 0.9 and 1.2 GHz. In Figure 143(b) – (g), the measured level of the reference spurs at the 150-MHz offset were less than –51 dBc. The reference spur is mainly caused by the local mismatches in the operating frequency between the replica-DCO in the TIC and the DCOs in the DCO bank. In addition, there are fractional spurs, which were occurred by the operation of the fractional injection logic. According to the value of R, the offset frequency of the spur is different. When R is odd the fractional spurs appeared at multiples of 15 MHz offsets. When R is even the fractional spurs appeared at multiples of 30 MHz offsets.



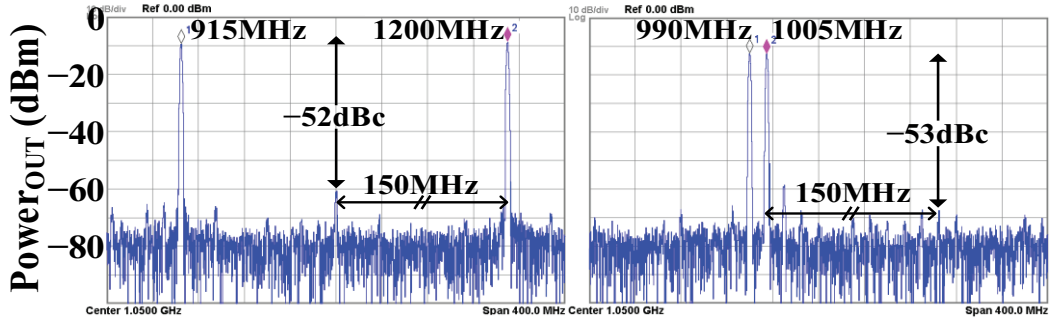
(a)



(b) (c)



(d) (e)



(f) (g)

Figure 143. (a) Measurement setup for spectrum (b) measured spectrums of the combined two output signals when f_1 and f_2 are 915 and 990 MHz; (c) 945 and 1155 MHz; (d) 915 and 1050 MHz; (e) 990 and 1155 MHz; (f) 915 and 1200 MHz; (g) 990 and 1005 MHz, respectively

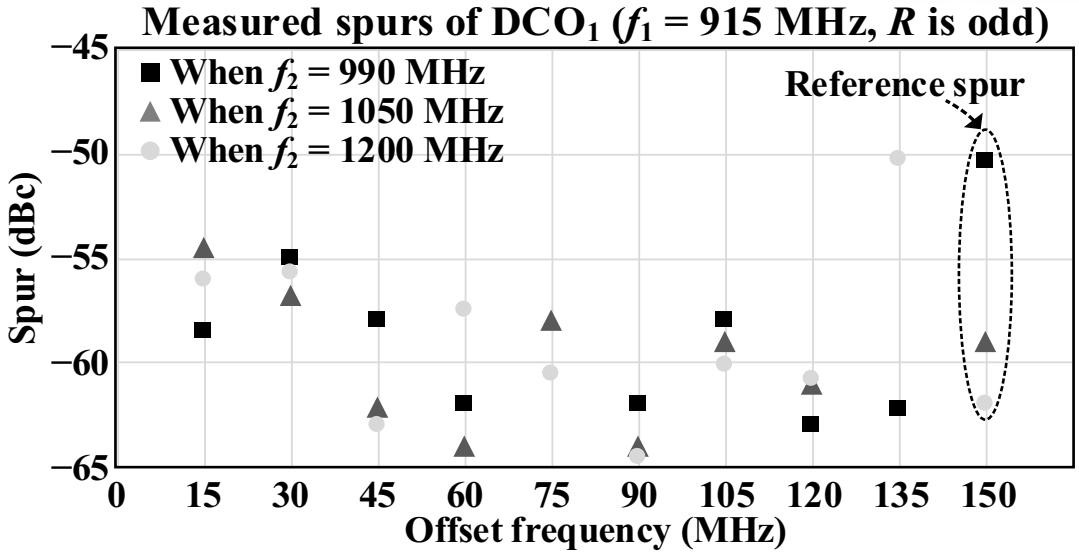
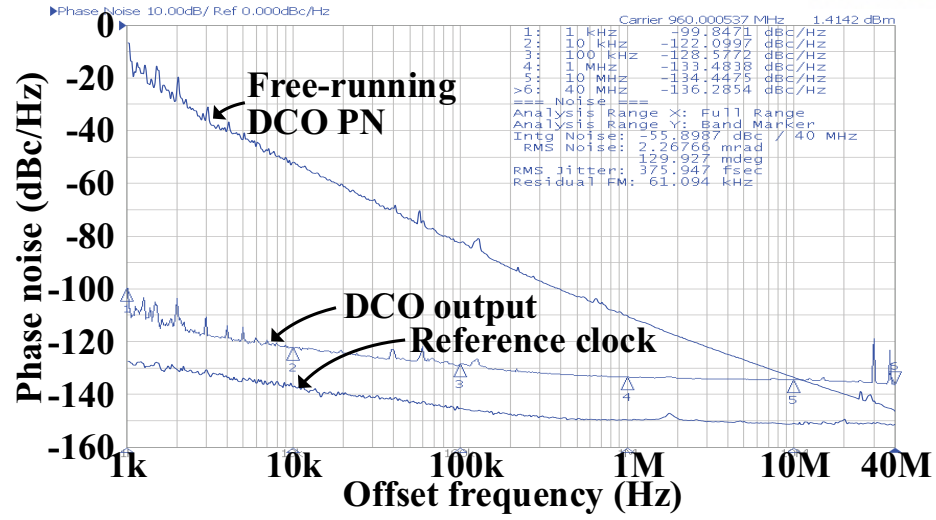
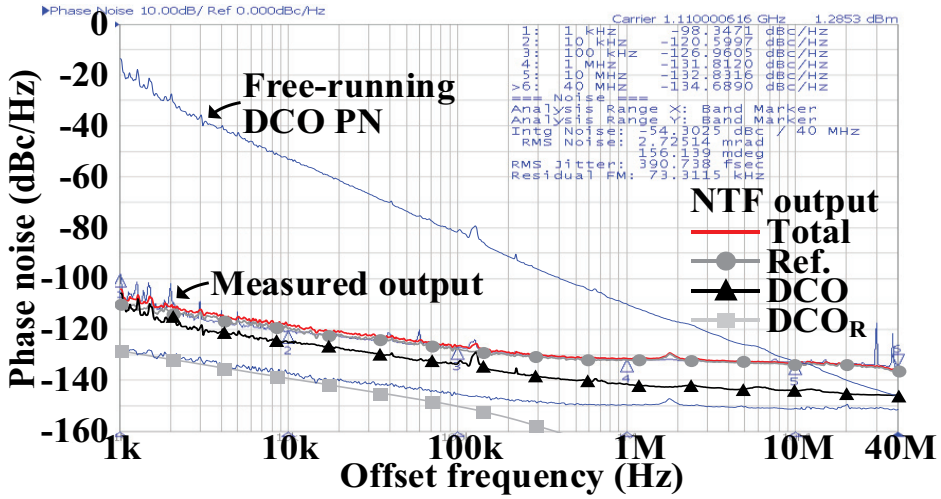


Figure 144. Measured DCO_1's levels of the spurs when f_1 was 915 MHz (R is one, odd number) and f_2 was swept; 990, 1050, or 1200 MHz

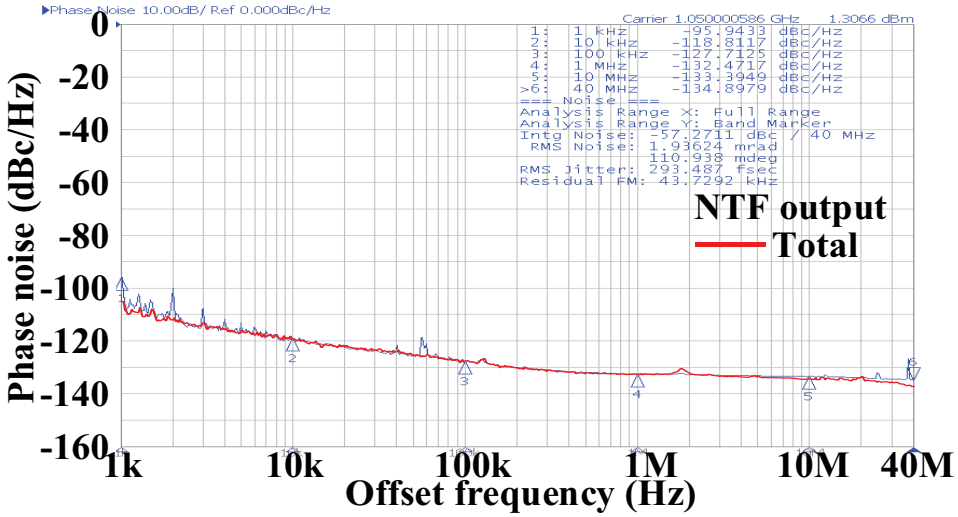
Figure 144 shows the levels of the various spurs of the signal of DCO_1 when it operates at 915 MHz and the signal of DCO_2 operates at the output frequency of 990, 1050, and 1200 MHz. As shown, the spurs existed at multiple frequencies of 15 MHz, and all less than −50 dBc. As shown in Figure 145(a), by using a signal source analyzer, Agilent E5052B, phase noise was measured when the DCO output frequency is 960 MHz, i.e., Q = 12 and R = 4. When the DCO is free-running, the spot noise of the DCO was −82.8, −110.1, and −133.9 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz, respectively. Note that the FOM [34] of each DCO was –165 dB at the offset frequency of 1-MHz) However, when the injection pulses were injected into the DCO, the phase noise of the DCO was greatly suppressed; the measured spot phase noises of the injection-locked DCO at 100 kHz, 1 MHz, and 10 MHz were −128.6, −133.5, and −134.4 dBc/Hz, respectively. The measured IPN was –55.9 dBc when the integration range was from 1 kHz to 40 MHz. The IPN of −55.9 dBc is corresponding to 375-fs RMS jitter. A spurious tone at the offset frequency of 30-MHz is a fractional spur, which is caused by the operation of the fractional injection logic, when the value of R is even. Another phase noise measurement result is shown in Figure 145(b) when the DCO operating frequency is a 1.11-GHz, which overlaid with the estimated phase noise based on (3) – (7). As shown, the estimation of the phase noise curve is almost matched with the measurement result. Figure 145(c) shows the phase noise when the DCO operating frequency is 1.05-GHz. In this integer-N mode (i.e., R = 0), since there are no fractional spurs, and much lower RMS jitter (i.e., approximately 295 fs) can be achieved. Figure 146(a) and (b) show RSM jitter variations of the DCO with 960 MHz output signal over the VT variations when the operation speed of the TIC slowed down by eight times. As shown the TIC has a capability to regulate the variations of jitter to less than 10% over VT variations. Figure 146(a) shows the worst RMS jitter happens at higher temperatures since the jitter of the free-running DCO is degraded as the temperature increases.



(a)

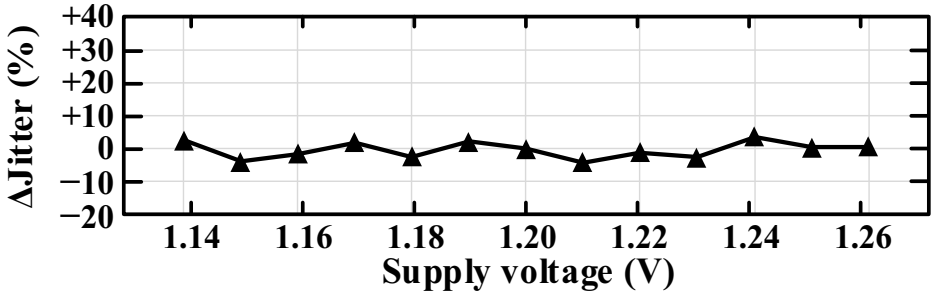


(b)

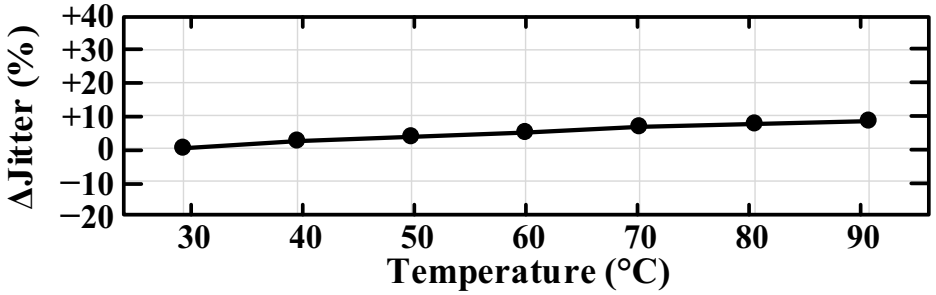


(c)

Figure 145. Measured phase noise when the DCO's output frequency is (a) 960 MHz (Q = 12, R = 4), (b) 1110 MHz (Q = 14, R = 4), and (c) 1050 MHz (Q = 14, R = 0)



(a)



(b)

Figure 146. Measured jitters in RMS across (a) the supply voltages and (b) temperatures to show the TIC's capability of regulation when the operation speed of the TIC slowed down by eight times

Table 19. Performance comparison with state-of-the-art ring-VCO-based clock generators

	This work	JSSC'18 [117]	JSSC'16 [121]	JSSC'16 [123]	JSSC'17 [125]	ISSCC'15 [127]	JSSC'15 [138]
Process (CMOS)	65nm	65nm	65nm	65nm	28nm	65nm	65nm
# of Clocks (*M*)	2	2	1	1	1	1	1
Type of VCO	Ring	Ring	Ring	Ring	Ring	Ring	Ring
Output Freq. (GHz)	0.9–1.2	0.02–1.0	1.2–2.0	0.96–1.44	2.4	0.8–1.7	1.6–1.9
f_{REF} (MHz)	150	50	400	120	75	50 – 400	50
Freq. Resol. (MHz)	$f_{REF}/10$	$f_{REF}/2^{14}$	$f_{REF}/10$	f_{REF}	f_{REF}	$f_{REF}/28/2^{16}$	$f_{REF}/2^{18}$
PN @1MHz (dBc/Hz) @f_O (GHz)	–132.4 @1.05	–132.0[****] @0.5	–122.9 @1.6	–134.4 @1.2	–115.0 @2.4	–117.0 @1.52	–119.0 @1.60
Integ. Jitter (σ_t) (Integ. Range)	375fs (1kHz–40MHz)	1.44 ps[****] (10kHz–40MHz)	440 fs (10kHz–40MHz)	185 fs (10kHz–40MHz)	700 fs (1kHz–40MHz)	3.6 ps (1kHz–100MHz)	1.4 ps (30kHz–30MHz)
Spur (dBc)	–44 (worst)	N/A	–39	–53	–58	N/A	−55
Power Cons. (P_{DC}) (mW)	7.7 (5.37[******]) (2 clocks)	6.4+P_{PLL}[*****] (2 clocks)	3.6	9.5	1.5	3.0	3.0
Active Area (mm^2)	0.05	0.12	0.032	0.06	0.024	0.048	0.09
FOM$_{JIT}$ (dB)[*]	–241.2[**] (–243.6[******])	N/A	–241.6	–244.9	–241.3	–224.2	–232.3
FOM$_{MC}$ (dB)[***]	–242.7 (–244.2[******])	N/A	–241.6	–244.9	–241.3	–224.2	–232.3

[*] $FOM_{JIT} = 10\log(\sigma_t^2 \cdot P_{DC})$ (dB) [**] Power of DCO_2 was removed from P_{DC}

[***] $FOM_{MC} = 10\log(\sigma_t^2 \cdot P_{DC}/M)$ (dB)

[****] Measured using external 5-GHz clock with 200-fs rms jitter

[*****] Power of PLL, P_{PLL}, not reported

[******] Operation speed of the TIC is slowed down by eight times

Table 19 compares the performance of the proposed injection-locked multi-frequency generator (ILMFG) with the state-of-the-art ring-VCO-based clock generators. When the ILMFG is compared to [117], this proposed work can provide two output signal with independent output frequencies with much lower RMS jitter, while less power was spent and the small area was occupied. Even when the performance of each output signal is compared to those of the state-of-the-art injection-locked clock generators (ILCGs), [121], [123], [125], [127], and [138], FOM_{JIT} and FOM_{MC} of this work are still very competitive, while it has an eminent merit of generating two different output frequencies at the same time. Since FOM_{MC} is a normalized FOM_{JIT} with respect to M, the value of FOM_{MC} of the proposed ILMFG is supposed to be improved, as M increases.

8.6 Conclusions

In this work, we presented a low jitter, all-digital injection-locked multi-frequency generator that can simultaneously generate multiple output frequencies. The proposed frequency calibrator, i.e., the TIC, can calibrate the multiple output frequencies of the DCOs in the background due to the time-interleaved operation of the calibrator. Since only a single time-interleaved calibrator corrects multiple DCOs, the power efficiency increases, as M is extended. In addition, each DCO can maintain excellent jitter or phase noise performance over the PVT variations due to the wide noise-reduction bandwidth by the injection locking. Due to the noise suppression, the measured RMS jitter were 375 fs and 295 fs in the fractional-N and integer-N modes, respectively. Through the Monte-Carlo simulations, we proved that the negligible impact of possible mismatches between the replica-DCO and the DCOs in the DCO bank to the jitter or phase noise performance. In addition, the proposed ILMFG can have a fractional resolution, which as is $0.1f_{REF}$, with the help of the fractional injection logic. Compared to state-of-the-art ring-VCO-based clock generators, the proposed ILMFG has competitive FOM_{MC} and FOM_{JIT}, while providing two output signal having independent output frequencies. Since the proposed ILMGF uses a single shared frequency calibrator, as M extends, FOM_{MC} and the efficiency in terms of the area and power are improved further, while providing clock signals with excellent jitter or phase noise performance.

9. Conclusions

In this thesis, the fundamentals of the frequency synthesizer and the VCO were introduced and the designs of low phase noise frequency synthesizer were discussed.

First, in Chapter 4, an ultra-low-IPN multi-band LO generator was presented, which concurrently can support existing cellular bands below 6 GHz and new mmW bands for 5G. First, using an RFD and an *LC* VCO with a high Q-factor, a fractional-*N* PLL generated a low-phase noise signal in the GHz range. Then, the following ILFMs increased the output frequency of the PLL to higher-frequency bands without the degradation in phase noise. The ILFMs shared one low-power FTL that continuously corrected the frequency drifts of the QVCOs, thereby preventing the degradation of the IPN of the ILFMs. The fractional-*N* mode PLL and the following ILFM_x15 generated a 29.22-GHz signal that had measured IPN and RMS jitter values of −31.4 dBc and 206 fs, respectively. When ILFM_x3 was enabled, it generated a 5.76-GHz signal that had an IPN, measured as −44.1 dBc. The IPNs were low enough to comply with the EVM requirement of 64 QAM. The value of the reference spur was less than –83 dBc at the 120-MHz offset from 29.22 GHz.

In Chapter 5, a mmW-band frequency synthesizer was presented that can generate 28 – 31-GHz output signals with less than –40-dB IPN by cascading a GHz-range digital SSPLL having an ultra-low phase noise and a mmW-band ILFM having a wide noise-rejection bandwidth. Using the sub-sampling operation and the effect of the Q-noise reduction due to the proposed OSVC, the digital GHz-range SSPLL at the first stage can achieve a very low in-band phase noise. In addition, a high-Q *LC* VCO at a GHz range help suppressing the out-band phase noise of the SSPLL. Since the OSVC uses only three 1-bit VCs, it requires small power and small silicon area, although it can achieve the significant effect to reduce the Q-noise. At the second stage, the ILFM adds little intrinsic in-band noise, and it also provides a very wide VCO-noise-reduction bandwidth. Therefore, it can multiply GHz-range input frequencies to mmW-band output frequencies with the least increase in the RMS jitter, resulting in ultra-low RMS jitter and IPN of –40 dBc and 76 fs, respectively.

In Chapter 6, a wideband and low phase noise quadrature LO-generator with a compact silicon area for multi-standard cellular transceivers was presented. Using divide-by-6, divide-by-4, and divide-by-12 dividers, the new LO-plan reduced the required FTR of a VCO to less than 39%. Thus, the entire frequency range of 699 – 2690 MHz for current cellular transceivers, supporting multiple standards from 2G to 4G, was covered by one high-Q *LC*-VCO. Because of high VCO frequencies in the new LO-plan, the tank-inductor was allowed to have a small inductance, while maintaining a very high Q-factor. The loaded Q of the VCO was further enhanced since the capacitive loading of the capacitor bank was minimized by the reduced FTR requirement. As a result, the *LC*-VCO of the proposed LO-

generator achieved low phase noise, as well as it occupied a small silicon area. To implement the quadrature divide-by-6 divider, we proposed a fully differential divide-by-3 divider with 50% duty cycle. Using the same idea, a differential divide-by-2 circuit was also proposed for divide-by-4 and divide-by-12 dividers. These LO-dividers, based on simple TSPC DFFs, generated the output signals with precise quadrature phases, and phase errors were regulated to less than 1° over all LO-frequencies.

In Chapter 7, a new wideband dual-mode *LC*-VCO with a switchable gate-biased active core is proposed. To boost up the start-up gain of the *LC*-VCO when the lower oscillation frequency is required, the switches are shorted between the primary core and secondary core, which is called as the LF mode. In the HF mode, the switches are opened to isolate the primary core from the secondary core. Therefore, the maximum oscillation frequency can be extended since there is no capacitive loading from the secondary core. In addition, the *RC* gate-bias circuits are used at the gates of the secondary core to have a high transconductance even with the DC voltage drop by on-resistance from the switches. The performance summary is shown in Table 17. Table 18 shows the performance comparison with state-of-the-art wideband *LC*-VCOs. As shown in Table 18, the proposed VCO achieved a competitive FOMT of 198.4 while provides both a wide tuning range and low phase noise.

Lastly, in Chapter 8, a low jitter, all-digital injection-locked multi-frequency generator was presented that can simultaneously generate multiple output frequencies. The proposed frequency calibrator, i.e., the TIC, can calibrate the multiple output frequencies of the DCOs in the background due to the time-interleaved operation of the calibrator. Since only a single time-interleaved calibrator corrects multiple DCOs, the power efficiency increases, as M is extended. In addition, each DCO can maintain excellent jitter or phase noise performance over the PVT variations due to the wide noise-reduction bandwidth by the injection locking. Due to the noise suppression, the measured RMS jitter were 375 fs and 295 fs in the fractional-N and integer-N modes, respectively. Through the Monte-Carlo simulations, we proved that the negligible impact of possible mismatches between the replica-DCO and the DCOs in the DCO bank to the jitter or phase noise performance. In addition, the proposed ILMFG can have a fractional resolution, which as is $0.1f_{REF}$, with the help of the fractional injection logic. Compared to state-of-the-art ring-VCO-based clock generators, the proposed ILMFG has competitive FOM_{MC} and FOM_{JIT}, while providing two output signal having independent output frequencies. Since the proposed ILMGF uses a single shared frequency calibrator, as M extends, FOM_{MC} and the efficiency in terms of the area and power are improved further, while providing clock signals with excellent jitter or phase noise performance.

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PUBLICATIONS

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