PROTECTION OF A VOLTAGE SOURCE CONVERTER (VSC) BASED HVDC SYSTEM

By

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ABSTRACT

To conserve energy and promote environmental sustainability, the power industry has invested a great deal into the generation of electricity using renewable energy (RE) sources. For such applications, high voltage direct current (HVDC) systems are considered a highly efficient alternative for bulk power transmission. Recent advances in technology favour the use of voltage source converter (VSC) based HVDC systems for the integration of RE sources. These schemes are favoured for their controllability and provide major reinforcements to the power systems. Despite its promising future, the technology is constrained by the unavailability of a reliable protection scheme, as the operating times for HVDC protection schemes are required to be ten to a hundred times faster than existing AC protection algorithms.

VSC-HVDC networks are usually more vulnerable to DC-side faults. Selective protection against these faults is therefore essential for safe and reliable operation of the network. This study provides the necessary concepts to develop VSC-HVDC protection algorithms for multi-terminal (MT) meshed HVDC systems. DC fault characteristics were initially investigated. They provided a basic understanding of the VSCs natural responses to DC fault scenarios. The study also focused on analysing factors that may adversely influence the systems protection performance. These include the DC fault distance, DC-link conductor sizes and DC fault impedance. Results obtained from these variations show that the DC-link capacitor was one of the main sources that cause the high rise of DC fault currents and that these are the highest and the most dangerous when closest to the converter station.

With a clear understanding of the DC fault characteristics, a protection scheme has been proposed. Initially, different methods are discussed with the intent of deciding on the scheme that is the most suitable. Detection techniques based on the discrete wavelet transform (DWT) for primary protection and the current derivative technique for back-up were chosen as the most promising. These techniques offer accuracy, speed and selectivity which are factors that are all important for the network. The single VSC terminal travelling wave technique was implemented to identify the exact position of a DC fault. This method reduces costs as it eliminates the need of communication links. Finally, to isolate the affected cables, the hybrid DC circuit breakers (CB) were implemented into the VSC-HVDC system. The CBs have been coupled with a reactance for fault current limiting and to isolate the system before it reaches an uninterruptable current magnitude. Back-up AC CBs were included on the AC side of the network and were stationed to separate the VSC network from the AC grid in cases where the implemented primary protection scheme fails.

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ABBREVIATIONS

DC	: Direct Current
AC	: Alternating Current
VSC	: Voltage Source Converter
LCC	: Line Commutated Converter
HVDC	: High Voltage Direct Current
HVAC	: High Voltage Alternating Current
MTDC	: Multi-Terminal Direct Current
PSCAD	: Power System Computer Aided Design
EMTDC	: Electromagnetic Transients including DC
IGBT	: Insulated Gate Bipolar Transistor
GTO	: Gate Turn-off Thyristors
GCT	: Gate Commutated Thyristors
DWT	: Discrete Wavelet Transforms
TW (P)	: Travelling Wave (Protection)
CB	: Circuit Breaker
LCS	: Load Commutation Switch
FB	: Full-Bridge
HB	: Half-Bridge
MMC	: Multi-level Modular Converter
SM	: Sub-Modules
OHL	: Overhead transmission Lines
GPS	: Global Positioning System

(S) PWM : (Sinusoidal) Pulse Width Modulation

PLL : Phase locked loop

ICC : Inner Current Loop

PI : Proportional Integrator

XLPE : Cross-Linked Polyethylene Insulation.

(S) FCL : (Super-conducting) Fault Current Limiter

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CHAPTER 1: INTRODUCTION

1.1. Background

Over the past few decades, the power industry has made major investments into contributing towards efforts that focus on energy conservation and environmental sustainability. The implementation of these efforts has been seen mostly through the massive exploitation of renewable resources such as solar, wind and hydro power as a means of generating clean electrical energy [1], [2]. The impact of integrating new resources including renewable–sources into the existing grid is important but however, will naturally result not only in growth, but also in a more complex grid. This will put increased pressure on South Africa to develop and consider different technologies to deliver electrical power efficiently and reliably to customers.

The connection of renewable generating sources and load centre has been an ongoing challenge. Due to the limited transmission right-of-way of high voltage alternate current (HVAC) systems and their resulting high transmission losses, high voltage direct current (HVDC) networks are recommended as a viable solution for this challenge and are regarded as an enabler for future expansion of the existing grid [3]. This technology will also be attractive to Southern African Development Community (SADC) countries who are attempting to increase their reserve margins and trade power using transmission systems connecting great power sources to large load systems in compliance with Southern African Power Pool (SAPP) [4], [5].

HVDC systems were first commercially used in 1954 for the interconnection of Gotland and Sweden [6], [7]. The technology has since undergone various developments and is mainly favoured for its control capabilities as well as providing efficient and stable transmission. The conventional line commutated converter (LCC) technology is currently found mostly as a point-to-point HVDC scheme. This technology makes use of thyristor valves for the AC/DC and DC/AC power conversion. LCCs are admired for their low converter switching losses and their ability to handle DC-side contingencies [8], [9]. Their main drawback however, are their low controllability which greatly impedes their possibility of being expanded into DC grids. Current trends indicate that future conventional HVDC systems could be available for longer distances, with increasing power rating and as multi-terminal systems. Research has therefore recently shifted its focus to voltage source converters (VSCs) for the transmission of power. Voltage source converter-high voltage direct current (VSC-HVDC) systems are admired for their flexibility and efficiency.

Further development of VSCs will introduce a big relief in grid connection to renewable energy, islanded power supplies and multi-terminal (MT) DC transmission [10]. VSC networks are actually regarded as the best candidate for MT systems as their power flow can be changed by only changing the direction of current [11]. In addition, unlike LCC systems, VSCs do not require reactive power support to operate efficiently. VSC technology has found application in several projects in the past two decades due to its compact design, low environmental impacts and controllability. Leading vendors in the industry such as ABB, Alstom and Siemens have played an active part in the development and application of VSCs, using this technology in several applications other than long distance bulk transmission of electrical power. Some examples of such applications include use in shipboard electrical systems and as distribution systems within congested cities [12].

Depending on the function of a converter station, VSC-HVDCs can be built as either point-to-point or MTDC transmission systems. A point-to-point connection has a single generation point supplying one consumption point [13]. These types of connections are found in almost all currently installed VSC-HVDC transmission projects. If a connection has more than two sets of converter stations, it is considered as multi-terminal. MTDC networks are considered a better suited configuration for VSC technology mainly because of their flexible controllability feature, which permits the reversal of power flow [14]. The first official VSC-MTDC system was recorded to be installed in 2013. The network is based on the modular multi-level converter (MMC) technology and was commissioned in China, with design rating of about 160 kV – 200/11/50 MW and a succession of underground, undersea and overhead lines [15]. This link is recorded as the first operating MTDC VSC-HVDC network and represents an important milestone in the potential development of future HVDC grids.

The development of this technology is also a step in the right direction for the realisation of the European "Super-grid" which is primarily aimed at integrating wind power using a meshed HVDC grid to connect multiple offshore wind farms to onshore substations [16], [17]. MTDC VSC-HVDC networks also continues to grow as the preferred solution suitable for the interconnection of existing onshore power systems [16]. In future, it is expected that VSC-HVDC transmission networks will gradually form DC grids. The simplest way of building a MTDC network is by introducing tappings from an existing two terminal system. This however is not a trivial task and will increase the complexities of control and protection with the possibility of increasing the telecommunication requirements between the stations [18]. It is required that each terminal of the VSC based MTDC system must be able to control power as well as support AC network voltage and frequency independently. The behaviour of VSC-MTDC systems also strongly depends on the control nature and on the systems topology and AC grid connection [19].

The use of insulated gate bipolar transistors (IGBTs) over thyristor switches remains the main property making VSC-HVDC technology more attractive, but also contributes to its limitations. When using IGBT valves, the DC fault current withstand-rate is much lower than with classical converters [20].As a result, when a DC fault appears in a VSC–HVDC link, the anti-parallel diodes conduct as a rectifier bridge feeding the DC fault [21]. The behaviour of VSC-HVDC networks during contingencies is vital for its successful development since they are expected to withstand interruptions both on the AC and DC parts of the network without halting the systems normal operation. Challenges in protection are one of the main restrictions to have limited VSC-HVDC systems to only point-to-point connections. The prevailing issue being that DC networks have no zero-current crossing, which then immediately eliminates the use of AC protective schemes. In addition, AC grid protection methods operate at a very low speed and would not be able to handle the DC fault current phenomena [16].

As a strategy to deal with DC contingencies in point-to-point connections, the continued operation of VSCs can be ensured by the co-ordination of AC circuit breakers (CB) strategically installed on the AC side of the network. For robust protection in point-to-point networks an AC CB is sometimes coupled with a large resistor bank of chopper resistors on the DC-link [22]. To handle low voltage fault-ride through conditions, the chopper resistors can be used. They are also capable of checking systems for over-voltage when placed parallel to the DC capacitors in a DC-link. This will therefore aid in dissipation of excess power and thus limit DC voltage rise to only within safe levels during a DC fault [22]. Most of the protection techniques under study or that have been developed have focused on improving fault detection, location and isolation. This is mainly because it is a critically important task to extinguish the DC fault current before they can affect the converter. One of the most significant characteristics of protection include accurate location techniques. Accurate location reduces maintenance times and network restoration times. Depending on various parameters including topology and configuration, DC protection systems should operate in order of 10ms from fault inception to tripping [23].

In existing VSC-HVDC systems, faults are commonly cleared with the use of AC CBs. These are usually not considered as the best option for isolation in VSC networks as they are to slow to withstand the fast-rising high fault currents. The use of the AC CBs also requires the isolation or collapse of the entire VSC network. This has thus motivated the development of HVDC circuit breakers. They are promising HVDC breaker topologies suggested by ABB and Alstom. HVDC CBs are based on semiconductor devices and are presented as promising technologies for future use. The hybrid HVDC breaker concept, although fast, reliable and with nearly zero loss, has only been verified at component and system levels. To confirm its practicality, the technology needs to be deployed in a real HVDC transmission line and must be tested under continuous full load conditions.

These solutions are also expensive and therefore not the most feasible solution. Investigations therefore continue, with the objective to find more economical isolation techniques. An alternative solution that would improve the protection of the network is the installation of hybrid converters. The concept of hybrid converters includes combining characteristics from conventional converters (i.e. LCCs) with those of MMCs. This technology results in low losses, DC fault blocking capabilities from full H-bridge converters and the low distortions presented by half-bridge MMCs.

The hybrid VSC topology can block a DC fault and offer support to the AC system during a DC fault. The technology is then believed to be a suitable candidate for MTDC grids. Implementing this approach does however seem more feasible to converter stations still under construction. Replacing the installed converters for existing stations would not be economical in the short-term and may affect the power supply. The technology does however have long-term benefits. [23]. The development of MMCs will also improve the power capability of VSC-HVDC and reduce power losses. Thus, a MTDC system based on MMC HVDC will be more attractive with respect to reliability and fault handling [24].

To maintain reliable power systems, research on DC protection remains a topic worth investment. The aim of this investigation will be to close the remaining gaps associated with detection and location protection techniques. VSC technologies will be easier to implement with the availability of a robust protection scheme. Research also includes finding methods that are faster, more accurate and selective for the VSC–MTDC network. The future of VSC-HVDC networks will ultimately strongly depend on the technologies ability to survive DC faults.

1.2. Problem identification

VSC-HVDC networks are favoured for their various interesting characteristics mentioned in the background presented in Section 1.1. This makes the future of the technology very promising especially the area of transmitting electric power to distant loads. A major drawback of VSC-HVDC systems results from the use of IGBT valves, which are characterised by their low current withstand rate. This challenge is however being addressed by the continued development of power electronic devices. The protection of VSC-HVDC networks poses as another serious obstacle. VSC-HVDC systems cannot handle DC-side faults and therefore lack of adequate protection has proven to be a significant challenge preventing the system from possible future expansion. During a DC-side fault, the DC current increases significantly. These high magnitudes can damage the converter station and the equipment close to it. In MTDC systems, the performance of the whole system is at stake as all stations connected to the common DC terminal are also at risk. DC faults occurring on a line fed by VSCs have been a re-occurring challenge and must be limited and interrupted much faster to avoid further disruption to the supply of power.

HVDC transmission lines can be affected by internal equipment failures, environmental stresses and AC or DC-side faults. Their outages could result in the interruption of power supply, operation problems such as reduced stability margins as well as loss of revenue. Therefore, to ensure reliability of such systems, current protection schemes need to be evaluated to assess their ability to provide adequate protection to HVDC systems. Fault detection and location are a major concern as they are very time-consuming in the protection of VSC-HVDC networks. Repair times can be significantly reduced if the location of permanent faults is determined accurately and fast. Examples of available protection techniques include detection and location methods such as the, current/voltage derivative methods, travelling wave methods, overcurrent and under-voltage and differential methods [16], [23]. Travelling waves and related methods are at present the most commonly used techniques for fault detection and location. These methods can respond quickly and have a high accuracy.

To protect the network completely the protection technique should include the detection, location and isolation algorithms. Isolation techniques are mainly installed to clear a DC faults. This is achieved by starving the DC fault current for a long period, ensuring that when voltage re-appears, the network will not re-strike [25]. Constraints restraining the implementation of a feasible VSC-HVDC protection technique include the lack of practical and efficient isolation devices. Although available DC switches are fast, they are incapable of interrupting high magnitude fault current within the required time [26]. Developing a DC CB with low losses, high breaking speeds and high DC voltages withstand rates would solve many challenges currently faced with DC isolation devices. After working on solving this problem for some time, ABB then developed a unique hybrid HVDC breaker. Its development to some extent ended the speculation over the feasibility of such a concept. To isolate DC faults, the hybrid HVDC breaker combines the advantages of the already existing power electronic isolation devices with fast disconnecting gas insulated switchgear technology to protect VSCs.

Testing this prototype, the company seems content with its results. The breaker has an impressive interruption time of only 5ms, it has only a few tens of kilowatts on state losses and a small footprint [25], [27].With the hybrid DC breaker, ABB is said to have solved a decade old engineering problem. The technology does however come at a high price. Hence research remains ongoing for protection schemes that might perform as efficiently without as much financial implications. Latest developments in VSC-HVDC have also emerged with not so traditional methods to protect the system. There has been remarkable investment and research in the implementation of topologies with the capability to block DC faults and isolate the contribution of AC side fault currents during a DC-side fault. Li [28] and Adam [29] suggest the half-bridge (HB) and full-bridge (FB) modular multi-level converters (MMCs) as a topology capable of at least partially meeting the mentioned requirements.

Other proposed hybrid technologies include the mixed cells MMC, H-bridge alternate arm MMC and hybrid cascaded converters [30]–[33]. The ability of a converter to have fault ride through capabilities relies on the control and topological arrangement of the system. The performance demand of DC CBs becomes more flexible when the fault level in the entire DC network is reduced. In addition, the AC grids are less affected by the DC faults. Numerous solutions to protect VSC-HVDC networks emerge regularly as this is a topic favoured by many researchers [11], [20], [23], [34], [35]. The mixing of different topologies with the systems control has also been proposed and might ultimately be the best cost-effective solution for the protection of VSC-HVDC systems as presented in various studies. This area of research could also be explored with the option of including or adding fault current limiters in conjunction with MMC as an attempt to block DC-side faults. Ultimately, the use of DC breakers is still regarded as a leading solution implemented to isolate only the faulty segment and interrupt the DC fault current.

The motivation for this study was to address the important need of protection in a VSC-HVDC system. To develop proper protection solutions, it is necessary to gain an understanding of how a DC system responds during DC-side faults and identify the critical design factors required for the protection system. This invariably involves simulation-based investigations as resources required for experimentation with physical systems are prohibitive. The studies are to include fault analysis for conventional VSC topologies. The recently enhanced capability of modelling and simulation of VSC based HVDC systems in electromagnetic transient simulation programs such as PSCAD [36],[37], was an added motivation to undertake this research. The tool was used in the investigations of existing detection, location and isolation methods appropriate for protecting the transmission cables of a VSC-HVDC system.

1.3. Scope and limitations

In principle, existing AC protection techniques are the backbone of all protection schemes including those of DC systems. DC fault characteristics however make is necessary that a DC protection scheme be refined to suit the system. To ensure reliability of a VSC-HVDC system, the basic task of a protection scheme is to detect and locate any disturbance that can occur in the system and isolate the area quickly. It is also important that they are selective, sensitive, reliable and robust, ensuring that the non-faulty sections of the system continue in secure operational state. The proposed protection scheme is set to focus on protecting a MTDC VSC-HVDC system by implementing a fast fault detection technique and isolation devices for the threatening DC faults. The interaction and coordination of different aspects of the system like topology are to be studied and discussed. The proposed scheme should be easily adaptable for use in other MTDC VSC-HVDC that are similar in nature. To ensure reliability in VSC-HVDC systems, it is important to initially study the current state of this technology in the protection domain to attempt to solve and fill the remaining gaps.

Therefore, the main objective of this study is to analyse and develop a method to assist and enhance existing VSC-HVDC protection schemes, to ensure their reliability as a developing technology in the industry. To achieve set objectives, the following are reviewed:

- Analysis of VSC-HVDC system background and current protection status
- Analysis of fault current contributions and fault response in VSC-HVDC systems
- DC fault detection and location methods
- Protection methods with DC breakers
- Proposing a best suited protection scheme for VSC-HVDC systems.

For this study, a basic 4-terminal VSC-HVDC network in a parallel meshed topology is investigated. The model is configured to be a symmetrical monopole. It is fitted with two-level VSCs and a DC cable PSCAD models. To obtain results and conclude on the effects of the above, tests on target system were performed on widely used power transient simulation software (i.e. PSCAD and/or MATLAB). The developed model only implemented DC cables and was limited to detecting, locating and isolating the DC faults in the network. Overhead lines (OHLs) have different characteristics than DC cables. This includes a relatively lower capacitance and higher inductance. The change in characteristics were expected to have an influence in the DC fault behaviour.

1.4. Research methodology

Initially a theoretical background was established on VSC-HVDC systems with emphasis on the requirements for a DC protection scheme in the DC grid, the separate components and the challenges related to them. A DC fault analysis was undertaken to understand the effects of DC faults in the VSC-HVDC network. This is evaluated for various DC fault types in different locations and for different VSC DC-link capacitors. To facilitate the selection of a feasible protection scheme, existing protection schemes were analysed. This includes a study on their reliability and their application in the industry. New possible technologies were also explored to determine if they have a future in VSC-HVDC protection.

The test model was supported by simulations in EMTDC/PSCAD. The developed model is subjected to analysis of the theoretical conclusions made on the detection, location and isolation methods suitable for the system. The results from the simulations were evaluated in order to determine the components of feasible VSC-HVDC protection scheme. Finally, relevant simulation studies were conducted to determine whether the proposed protection methods are feasible.

1.5. Contributions

One of the main contributions of this thesis includes the comparison of fault analysis or DC fault development for different grid operating topologies in VSC-HVDC systems. These include a comparison between 2-level and half-bridge MMC. As presented in the dissertation, understanding the effects of the converter arrangement/ topological arrangements is imperative when designing a DC fault protection scheme for a VSC-HVDC network. These mainly influence the type of fault detection, location and isolation techniques implemented in the network.

Another contribution, is a study presented on the theoretical analysis of mixing different topologies. Although the idea has been proposed in previous literatures it has not been extensively discussed [38]. Investigations including the fault analysis and protection requirements of the VSC network are documented. This investigation could in future assist system designers in selecting a feasible protection scheme. Every protection technique subsequently has a different interruption time and affects the system behaviour. The introduction of the isolation technique implemented will also have a subsequent influence of the overall DC protection techniques needed for the network. Therefore, in this study, the networks pre- and post-fault state are evaluated and their performance aids in the design of the protection methods.

1.6. Thesis structure

This dissertation has 6 chapters, where this introduction and background is presented as Chapter 1. Chapter 2 introduces a literature survey of VSC-HVDC protection systems, with an emphasis on the protection requirements of a VSC-MTDC system. Here, theory regarding fault currents is evaluated. The emphasis is on determining the parameters that influence the fault currents. The chapter also highlights the status of protection for such systems, the constraints limiting the technology in industry and where research seems to be heading in this field. A review of the methods for current limiting is also presented.

In the third Chapter, different DC fault detection, location and isolation techniques are presented, and analysed. Both conventional and novel DC location methods are investigated, and the most feasible techniques are later selected for implementation in the developed network. The fourth Chapter contains the description of the PSCAD model developed and results from the simulations to validate this model. It also includes fault analysis of the developed model comparing its results to theoretical findings reported in Chapter 2. Various fault detection, location and isolation techniques based around the methods discussed in Chapter 4 are implemented to protect the developed VSC-HVDC model in Chapter 5. A feasible protection scheme is then proposed. Chapter 5 concludes with an evaluation of the proposed protection scheme for the developed MTDC VSC-HVDC network. Conclusions and future recommendations are presented in Chapter 6.

CHAPTER 2: LITERATURE REVIEW

2.1. Introduction

The European concept of Super-grids is slowly gaining support around the world. This has resulted in increased high voltage direct current (HVDC) transmission projects being planned and developed. The objective of the Super-grid project is to develop a network of HVDC transmission systems that are designed and implemented to maximise efficiency and tap into available renewable resources [39]–[41]. VSC-HVDC systems, in particular the multi-terminal (MTDC) VSC systems have emerged as strong contenders for such schemes. This is mainly due to their attractive feature of being able to reverse power by only reversing the direction of current flow [7], [42]. Despite tremendous potential however, like most existing systems, VSC transmission schemes have constraints. Fault-current interruption is arguably one of the main challenges that academia and manufactures are currently engaged in [43]–[45].

The objective of protecting VSC-HVDC systems is to always certify that the power generation matches the demand while considering the reliability, security, quality and economics of the network [46]–[48]. Favouring the technology for its reduced losses, environmental considerations and controllability, the power industry continues to invest in HVDC transmission [3], [27]. These technologies will become easier to implement when an effective controlling technique and reliable protection scheme is available. Numerous investigations have been reported with innovative solutions on the protection of VSC-HVDC systems. These include works presented on DC fault-ride through or fault blocking converters [31], [49], [50] as well as the ground breaking hybrid DC CB [25], [26]. However, these solutions are novel ideas with no operational experience. Network operators are also unfamiliar with how different components of the system influence the fault response of the network.

Developing solutions for challenges in VSC-HVDC network protection is a step in the right direction. This is especially valuable when expanding the system into a MTDC network. Most existing detection and location methods that have been established and are mature for both HVAC systems and traditional HVDC systems are applicable to VSC-HVDC networks [34], [51]. Nonetheless, they are required to be applied strategically to avoid situations that might lead to potential overall instability of the system. HVDC isolation techniques are also recommended mainly because DC networks have no zero-current crossing, which immediately eliminates the use of AC protective schemes. Chapter 2 includes a brief overview of the inception, causes and type of faults that affect a VSC system. It will also highlight on parameters influencing DC faults and review the status on the protection schemes of VSC-HVDC systems.

2.2. Faults in a VSC-HVDC system

Protection of a power transmission network is of vital importance in assuring the reliability of power transmission. However, the protection of DC faults has been a significant issue that has constrained the development of VSCs especially for applications in HVDC [52]. The primary reason being the lack of mature and standardised DC protection schemes [53], [54]. A conventional VSC system shown in Figure 2-1 is typically comprised of AC side components, internal converter components and DC-side components. These have their unique protection zones for the different converter components. Different protection principles are implemented to achieve selective isolation. These could either be with the use of AC CBs, DC CBs, and DC isolators which are to be discussed more extensively in Section 2.4.3.

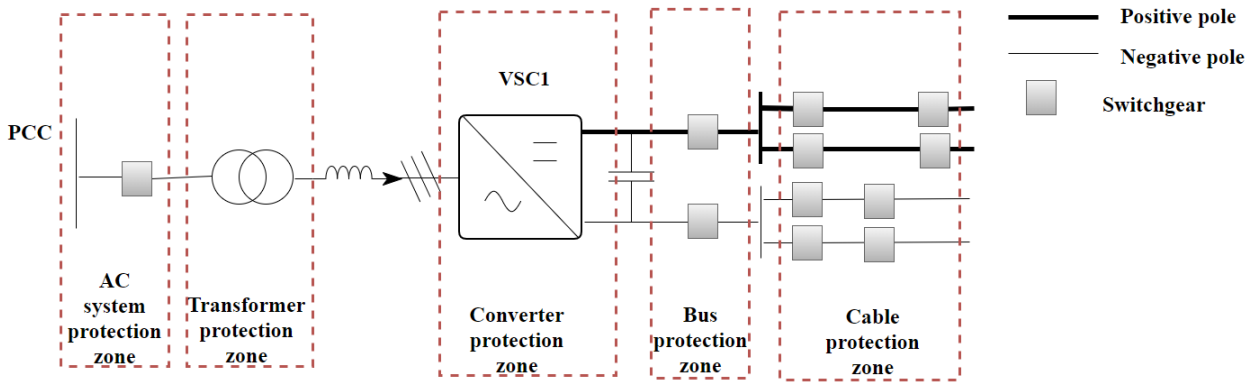

Figure 2-1: Zones of protection in a symmetric monopolar converter [55].

The main objective of a protection scheme is to retain stability of a power system by isolating only the components contributing to fault occurrence, whilst leaving the unaffected equipment in service [56], [57]. It also serves the purpose of protecting the public, minimising damage to equipment and protection against overloads. The protection of a system's equipment is realised with the help of detection, location and isolation techniques. Faults can also otherwise be minimised by [57]: -

- Improving the quality of machines, equipment and installations through the improvement of design technique.
- Regular maintenance by trained professionals.
- Effective management of electrical plant

2.2.1. Primary and back-up protection.

The protection algorithm is generally classified into either the primary or the back-up protection technique. The main protection is classified as the primary protection and therefore acts as the first line defence [58].

Its operation is expected to be fast and results in the least disruption to the power system. Sometimes faults may not be eliminated by the main protection scheme. The primary scheme may fail due to [57]: -

- Failure in emanating from the DC supply.
- Failure in CBs as a result of a mal-function in the tripping mechanism.
- Failure in the converter station controlling scheme etc.

When such failures occur in a system it is vital that the system is equipped with back-up protection. A back-up protection scheme has a small delay installed to allow for the confirmation that primary protection is really not functioning [59]. When primary protection is disconnected for testing or maintenance purposes, back-up protection is then allowed to act as the primary protection. Usually the type of back-up protection applied in the network is naturally related to the failure risks and relative economic importance of the system [58], [60]. In HVDC systems multiple primary protection schemes can also be fitted to ensure fast and reliable protection. Back-up protection is then applied as an alternative option so that the network has two separate protection schemes that are available. Back-up protection is intentionally set to operate when it meets specific performance requirements. Additionally, it may operate when multiple contingencies have occurred and result in an event whereby the back-up zone protection must be enabled [61].

Well-proven existing protection schemes are usually used for the AC side protection in VSC-HVDC networks. VSC control can also be configured to cope with AC side disturbances. Additionally, a back-up function or redundant device is usually implemented to take care of internal VSC faults [62] and so VSC-HVDC systems are left mostly vulnerable to DC cable faults. DC-side cable faults are known to occur more frequently [52]. This is mainly due to environmental stresses, cable aging and physical damage that may occur during operation. A DC fault occurs in three different stages in a conventional VSC-HVDC system. Ultimately the IGBTs are blocked and the diodes connected antiparallel to the IGBTs conduct to feed the fault current from the AC grid [52]. During such disturbances, severe overcurrents due to the discharge of the DC-link capacitances are a major issue [63]. The fault analysis of such conditions needs to be studied in detail prior to the development of a VSC-HVDC systems protection scheme.

2.3.Sources influencing DC fault current response

In designing a protection scheme for a VSC-HVDC network, there are various influences that could affect the fault response of the system. The overall reaction of the system during a fault is usually characterised by the fault type (i.e. if it is a ground fault or a short-circuit fault) [16], [62]. However, several other factors play a big role in influencing the fault response of a VSC-HVDC system. These include [23]:-

- The configuration of the systems connections (i.e. whether monopolar or bipolar)

- The topology of the converters (i.e. whether 2-level, 3-level or MMC).
- The topology of the network links (i.e. whether the system is connected as point to point or as a multi-terminal DC network).
- The converters controlling capabilities as well as those of the power electronic valves, particularly being informed about the valves blocking scheme.

A converter's topology is considered one of the main influencing factors. Due to a change in structure, the type of converter topology used in a system (i.e. 2-level topology or multi-level) is expected to have an influence on the fault response and the extent of these effects should be considered during the design of the protection scheme for the specific HVDC system [38]. Similarly, the type of system configuration (i.e. either the monopolar configuration or bipolar configuration) has an effect on the fault response and these should also be evaluated [64], [65].

2.3.1. Other influencing parameters

The factors discussed above are considered as the main contributors affecting the fault response of a VSC-HVDC system. They highly depend on the presence of a DC-link capacitor in the case of conventional VSCs and the size of the available distributed capacitors in MMCs. There are however, various other parameters that play an equally important role in the fault response of the network. In [66], Xue suggests that the fault response relies on the initial condition of arm currents and fault resistance in an MMC based VSC-HVDC system. The transmission line itself can be considered an important factor [12]. Transmission lines include line capacitance and can therefore be regarded as an energy storage element. During a DC fault, these capacitances also discharge making a noticeable contribution especially in MMC VSC-HVDC systems.

More energy is stored in lines that have longer distances. Nonetheless, these are usually considered negligible in the case of conventional converters as the size of DC-link capacitor is usually much larger [67]. The fault currents peak magnitude also highly depends on the fault location. When locating a DC fault close to the VSC station, the discharge current caused by the DC-link capacitor dominates the shape of the total short-circuit current. When distances further from the converter stations are considered, the contributions of all sources are of significance. These also include the sources from transmission lines as mentioned previously. Faults that occur towards the middle point of the VSC-HVDC network, on the other hand, take the least time to reach the fault current peak value [67]–[69]. The results obtained from these investigations are imperative and form the back-bone for the design of a protection scheme.

2.4. Current protection techniques

It has been established that one of the biggest drawbacks of VSC-HVDC systems is their vulnerability to DC-side faults. A DC fault exposes IGBTs to overcurrent, and therefore, threatening the system's normal operation [13]. Therefore, VSC-HVDC systems require equipping with a reliable and robust protection scheme. To prevent faults from threatening a systems operation, a systematic approach is recommended in most studies [20], [63], [70]–[73]. Their approach follows a somewhat traditional method in order to design a robust protection scheme.

The traditional protection process includes the following: -

- Fault detection and location

Is regarded as the process of determining whether a fault has occurred in the system. Detection methods should be accurate, fast, sensitive and selective. Early detection is always advisable as this aids in preventing the entire system from being affected by the threat.

- Proper fault identification

Identifies variables and signals most relevant to diagnose the fault. The purpose of this procedure is to allow operators to be able to focus only on repairing a certain fault in the system so that the threat can be treated or eliminated in a more efficient manner. This is discussed in Section 2.2.1.

- Fault clearance/ isolation

Is regarded as a procedure essential for reducing the effect of the fault. It can be regarded as an intervention should faults not clear up in a set time.

Depending on various factors of the system (i.e. including converter topology, system configuration etc.), the DC protection scheme implemented is expected to be fast, accurate and selective [67]. High speed fault protection techniques are mainly compulsory as DC fault currents of VSC-HVDC system rise very quickly and to very high magnitudes during the first few seconds of a DC fault [69], [74]. The fault current must then be interrupted before it reaches to the maximum interruption capacity of the isolation switch-gear. It should also ensure that that total fault clearing time includes both fault detection time and fault current breaking time within a few milliseconds [75]. Accurate fault location techniques if executed efficiently are capable of reducing maintenance and restoration times [63], [76]. However, considering the differences in structure and control, locating a DC fault within a VSC-HVDC network using conventional protection techniques used by other power systems is sometimes ineffective.

A method known as distance protection using impedance relays mostly common in AC protection, for example, is not as effective in VSC-HVDC systems. This is because unlike the transmission medium used in AC systems, the DC cables utilised in VSC-HVDC systems have very low resistance and virtually zero series reactance [77]. To ensure accuracy, sensitivity and selectivity in a minimum time, the recommended protection scheme for such networks is therefore likely to rely on signal processing techniques (e.g. wavelets) to detect and locate the DC faults [55]. Recent research is also geared towards finding innovative solutions that are both economical and feasible for VSC networks. The biggest contribution has been on the improvement of HVDC converters with a DC fault ride-through capability.

These technologies reduce the task of the detection and isolation schemes. They also decrease the overall damage to converter stations from overcurrent during a fault [50]. When a system is under threat, the primary detection, location and fault isolation procedures are employed in this sequence. The absence of anyone of the above components exposes the system to fail or shutdown entirely. Therefore, as a final measure of protection, isolation techniques currently available for VSC schemes include: -

- AC CB that are installed on the AC side of the system and virtually disconnect the entire VSC-HVDC network from the AC connected grids during a fault [8].
- DC breakers on the DC terminals are also regarded as a promising option for the scheme.

Research on protection is mostly geared towards control strategies for fast and reliable detection and isolation of faulted lines and more especially the design of DC CBs. This technology still needs optimisation of the DC opening capability, on-state losses and speed [48], [78]. The drawbacks of individual methods can be eliminated by combining various protection schemes. A few studies have addressed methods without DC breakers like the “Hand-shaking method” [20], [79]. However, when using these methods, all converters must be blocked and mechanical switches are used to isolate faults.

The feasibility of hybrid HVDC CBs with very high speed and nearly zero loss has been verified at ABB’s high-power laboratories in Sweden and Switzerland, for rated currents of 2 kA and HVDC voltages up to 320 kV [26]. The next step however is to deploy the breaker practically in real HVDC transmission lines to test their feasibility under continuous full load conditions. These solutions are also quite expensive and therefore not the most feasible solution for some. Therefore, investigations continue to find more economical isolation methods.

2.4.1. Fault identification

During steady state operations, a power system carries normal voltages and currents which results in the safe operation of the system [80], [81]. An electrical fault would therefore be the deviation of voltages and currents from the nominal values or states.

As mentioned previously, a VSC-HVDC system may experience disruptions in the form of AC-side faults, inner converter faults and DC cable or overhead line faults. Internal faults occur inside the converters and include IGBT-shoot through and short-circuits across DC rails. These types of faults are usually managed by the control systems whose task is not only to govern the basic functioning of each converter in a VSC-HVDC system but also to take care of the various disturbances that can affect the system [61]. They are less frequent as compared to external AC/DC faults or faults that occur in cables or overhead transmission lines. AC faults in a VSC system on the other hand include combinations like the single line-to-ground fault, the line-to-line fault, line-to-line-to-line (3 phase fault) and a line-to-line-to-line-to-ground fault [62].

Since they are backed by a mature protective scheme, AC faults can be prevented from influencing the grid side converters by using switch-gear like fuses, mechanical disconnectors and AC circuit breakers [13], [78]. VSC topologies are therefore mostly threatened by DC-side faults. External faults or DC-side faults can be further classified as either, short-circuit DC faults, ground DC faults, overcurrent and over-voltage [52]. Amongst these, the DC short-circuits are the most severe while the ground faults are the most frequent to look out for. During a DC short-circuit fault, the IGBTs can be blocked for self-protection leaving reverse diodes exposed to overcurrent. Analysis of the fault response is thus essential in determining the challenges involved in DC grid protection.

2.4.1.1. Line-to-line faults

Short-circuits shown in Figure 2-2 are otherwise known as line-to-line faults (where Tr_{rect} is the rectifier side transistor, L_{rect} is the rectifier-side reactor, I_{conv1} is the converter current and C_{DC1} is the converters DC-link capacitance). Short-circuits usually occur when an object falls across the positive and negative line in the case of overhead lines (OHL) or when insulation fails in cables [82]. They may also occur in the event of a failure of a switching device causing the line to short [62].

Cables are almost immune to these type of faults, in fact the mentioned facts on cables when it comes to faults almost makes them an obvious choice when designing VSC-HVDC systems [71]. OHLs are however used in some systems because of certain reasons that put them at a better advantage than cables. The fault currents caused by short-circuits may lead to the melting of transmission lines as the overhead lines, cables and windings will experience excessive heating. This may even cause a fire or an explosion [83], [84]. Stability of the power system may be adversely affected and can even lead to cascade tripping or complete shutdown of the power system.

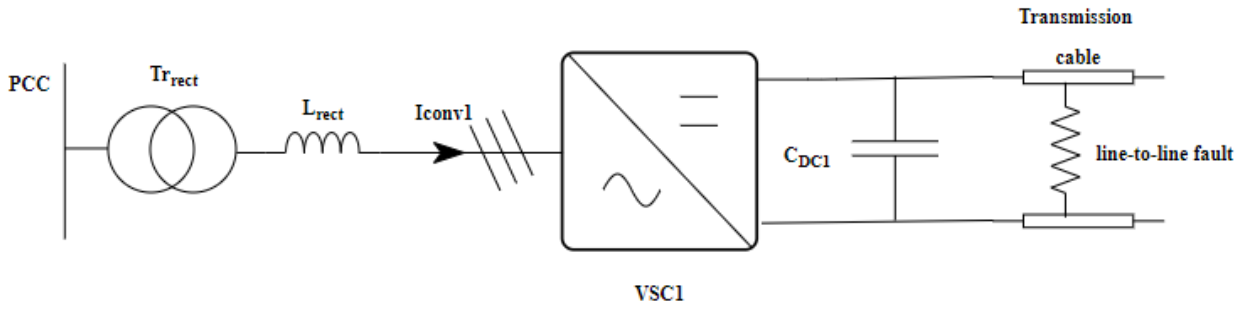

Figure 2-2: Rectifier side of VSC-HVDC illustrating line-to-line faults.

2.4.1.2. Line-to-ground faults

DC-link and DC cable ground faults as shown in Figure 2-3 are usually known as line-to-ground faults or just ground faults (the components are as described in Section 2.4.1.1). They occur when the positive or negative line is shorted to the ground. In overhead lines, this may be due to lightning strikes that may cause the line to break or fall to the ground creating a fault.

In a cable connected system, ground faults are almost always caused by insulation deterioration and breakdown due to physical damage, environmental stress and electrical stresses [11]. Although ground faults are less frequent in cable systems, they are often permanent and require removal of the affected network until the disruption is cleared. A ground fault results in the rapid discharge of the faulted poles capacitance [85]. The negative and positive pole will therefore experience an imbalance of DC-link voltage. As the voltage of the affected line begins to fall, high fault currents flow from the capacitor as well as the AC grid [86]. The high fault currents are known to possibly damage the convertor or capacitors. Ground faults behaviour are highly dependent on the systems earthing configuration. At present, there are two main grounding schemes [62]:

1. Through the neutral point of AC-side transformer.
2. In the DC-link capacitors.

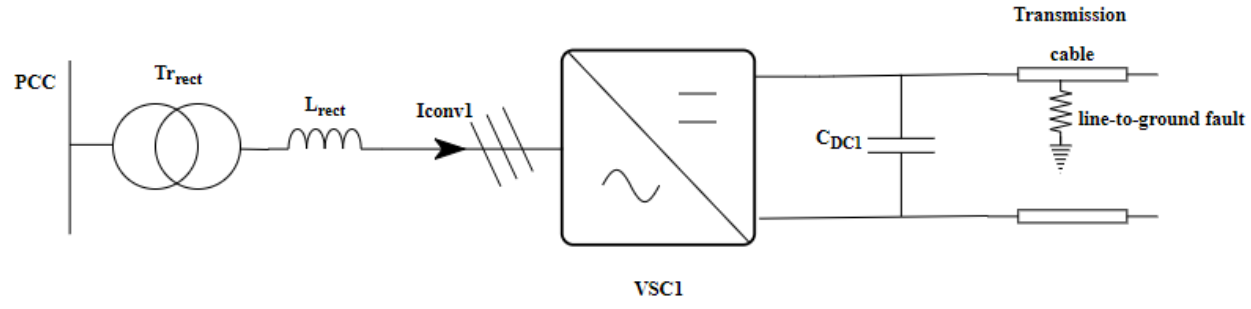

Figure 2-3: Line-to-ground faults.

A fault's current magnitude and severity depends on a variety of factors like the location of the fault and the damage caused due to the fault [52]. While analysing a given fault's severity, it is usual practice to refer to a standard fault condition for given voltage level. If DC-side faults are not taken care of accordingly, they could irreversibly damage the valves, diodes and other sensitive equipment of the system [86], [87]. This is one of the main reasons that raises the importance of VSC-HVDC protection.

Transmission line protection in particular, is based on the protection of system transients that occur during a fault condition. The DC faults mentioned previously are most likely to occur in overhead lines or transmission cables. The main characteristics of the mentioned faults is that if permanent, they cannot be extinguished until the current is brought down to zero. This will result in the collapse of the system's line voltage while the current sharply rises. Protection should dependably discriminate between these different fault cases and take appropriate action quickly. Quick reparation of permanent faults in VSC-HVDC is essential for minimising down time and outage costs [78]. Normal converter control is usually not adequate to extinguish DC fault current. It is imperative that the fault be identified quickly, accurately and selectively to continue the operation of the system.

2.4.2. Fault location and detection

Fault location and detection are very important characteristics of a protection scheme, especially in VSC systems, to ensure that the system is restored to its normal operation as soon as possible. The main roles of fault detection are to first identify the faulted section as quick as possible and to make an accurate identification of the specific fault point [18]. This means that these methods should adhere to the main philosophies of sensitivity and selectivity. The main limiting issues with fault location however are fault resistance and grounding [71]. Several methods have been investigated in the literature for locating faults in DC systems. These are classified as direct measurement based methods which include overcurrent protection method, differential current method and distance protection, as well as signal processing based methods which include travelling wave methods [88].

2.4.2.1. Direct measurement based methods

Direct measurement based methods, as the name implies, utilises the direct measurements of a systems voltage and current to locate the faulted point of a system.

a) The overcurrent and under-voltage detection technique

These methods directly use the magnitude of current and voltage to measure or detect if a fault has occurred. A DC fault is characterised by a sharp rise in current due to the capacitor discharge and this in turn causes a voltage depression. The overcurrent protection technique is therefore designed to trip if the measured current has exceeded the set threshold [12].

It is important to note that the overcurrent detection technique is only feasible when the lowest possible DC fault current is still a magnitude above the highest possible steady state operational current [12]. Overcurrent protection methods however, lack selectivity and therefore are not advised for application in multi-terminal systems or DC grids. In order to measure a lasting DC voltage drop, the protection implemented for DC levels is to measure voltage for long durations [89], [90]. Again, the system is tripped if the measured voltage is less than a certain threshold. DC voltage level protection and overcurrent protection both represent a technology that is simple and matured. However, these protection techniques are mostly considered as back-up protection due to their lack of selectivity.

b) The differential detection technique

Differential protection is also considered as a direct measurement based method. It applies Kirchhoff's current law in the VSC-HVDC system, by monitoring the current going in and out of the component being protected [79]. According to Kirchhoff's law, the systems currents are expected to remain constant during normal operation. A DC fault identified by the differential technique can therefore be characterised by the resulting difference in the currents exceeding the set threshold [91]. Differential protection offers a very high degree of selectivity, but involves some time delay as the information gathered must be transferred between the two VSC terminals. To transfer this information, the method strongly relies on telecommunication systems and their availability [79]. This makes them vulnerable to possible communication errors in the network. In cases where the system is offshore and long DC cables are required for transmission, the method is found to be less sensitive and as a result of the increased time for communication, the response time is due to also increase [67]. Due to the mentioned constraints, this technique is often recommended as back-up protection in VSC-HVDC systems.

c) The distance detection technique

The method is one of the more mature technologies in power system protection. It estimates a DC fault's location by using impedance found between the identified fault point and the protective switchgear [51]. The impedance is obtained using data on current and voltage, hence it falls under the direct measured techniques. The fact that this technique primarily uses impedance is one of the limiting constraints of this technology for implementation in VSC-HVDC networks. As mentioned previously, a VSC network mainly uses DC cables and these have very low impedance [77]. The method as it stands is therefore not feasible. In DC systems, the frequency is also known to change abruptly during a DC fault, therefore a fundamental frequency cannot be defined [70]. This factor may then influence the system to send inaccurate information about the fault distance estimations. To overcome such challenges a new approach called the "Handshaking method" is proposed in [20], [79]. Its techniques also involve the use of telecommunication links and is also based on locally sampled current and voltage measurements.

d) The derivative detection technique

The time derivative of the networks DC current and DC voltage is required for implementation of derivative protection. Like the protection techniques mentioned above, the method follows a certain process to identify a fault in the system. In this case, a pre-set threshold is compared to the sum of the measured DC current and the voltage derivatives [83]. The derivative protection technique is mainly favoured for its selectivity, as the polarity or sign of the current derivative can reveal the DC fault direction. This is helpful in identifying the precise position of the DC fault in the transmission line of a VSC-HVDC network. Detection time of this method is usually very fast as it is approximated in the order of 2-3 ms [67], [70]. The voltage derivative is however affected by impedance and therefore it becomes difficult to identifying DC faults with high impedances [92].

2.4.2.2. Signal processing based method

In this type of fault location method, a signal process translates a signal to different domain allowing for a clearer picture to be seen on the power systems behaviour.

a) Travelling wave protection

As the name suggests, this method is based on the travelling theory. This theory suggests that electrical voltage and current of a system are represented by traveling waves. In a case where there is a change of impedance, a fault or a line termination a wave is reflected and refracted through that changed junction [18], [64], [73]. Their algorithms make an estimate of the fault location based on the time it takes for the travelling wave generated by the fault to move along the line [16]. Travelling waves generated by faults travel at a velocity close to the speed of light in overhead lines. In cables, the wave velocity depends on the cable design [73]. If the travel time is accurately measured, the precise fault location could be estimated. The travelling wave technique is normally used as the main line protection technique. For accurate fault detection, the strength of the algorithm relies on both the contributions of current and voltage. They are praised for their fast response and high accuracy.

Their results are also not affected by other system factors such as bus configuration, fault type, fault resistance etc. Detection techniques including the wavelet analysis, mathematical morphology, Hilbert Huang transform and independent analysis are considered as modern travelling wave methods [93]. In addition, DC current derivative protection is also considered as a travelling wave technique. It mostly relies on the accurate measurement of the rate of rising DC fault voltage or current [61]. The diagram shown in Figure 2-4 is used to illustrate the travelling wave theory on a VSC-HVDC network. In this diagram, u represents the wave velocity and X_F the distance to where the DC fault is located in the transmission line.

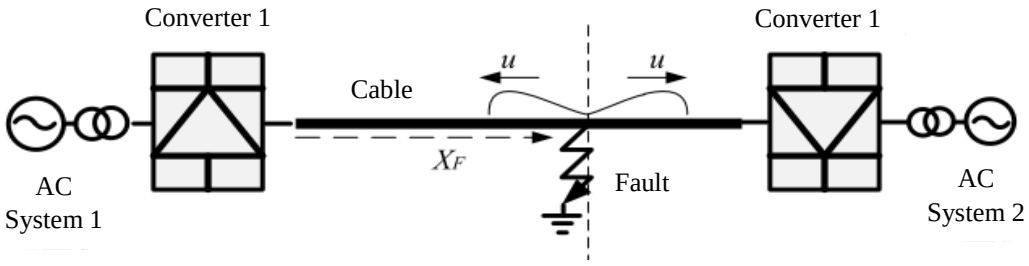

Figure 2-4: Diagram illustrating travelling wave flow along transmission [73]**.**

The technique can be based either on measurements at one end or on the measurements at both ends. The single-ended method is usually faster but less accurate than the two-ended method. The two-ended method however requires measurement of the time interval between the arrivals of initial waves at two ends [70], [73]. This method thus requires synchronisation of the measurements at the two terminals. Availability of Global Positioning System (GPS) and hardware that enables collecting time tagged data samples at very high frequencies allows for highly reliable and accurate fault location schemes [94]. This will however affect the speed and increase the costs of the protection scheme. The choice between the single ended or two-ended method therefore becomes a trade-off between speed and accuracy. Although common in all power systems, protection algorithms based on the traveling wave are more practical for the HVDC line than for the AC line. This is mainly because the DC line has a simpler structure [64].

Conventional protection techniques that are deemed unsuitable for MTDC networks should be improved. Solutions already proposed for protection include the travelling wave dispersion effect and strengthening the robustness of the scheme [16], [23]. Other proposed developments take advantage of the wavelet theory to obtain more information from the signal to increase protection accuracy [95]. All proposed solutions set to reinforce current travelling wave techniques focus mainly on accurately capturing useful information about the fault at very high speeds. This will ensure the protection the VSCs, its auxiliary components and the DC CBs.

b) Hybrid approaches

To aid in accurate and fast fault detection and location techniques, hybrid protection schemes have been also proposed. This technology combines novel protection algorithms with those already existing. Examples of such schemes include the bipolar travelling wave based differential protection method [23]. A mixed travelling wave described in detail in [96] is also developed for application in monopolar transmission line. In this scheme, information is gathered using a stationary wavelet. This information is later used to identify existing DC faults. Kong [97] utilises boundary protection to detect the fault and travelling wave to determine the direction of the fault.

The algorithm can also distinguish between lightning faults and other disturbances. Focused mainly on presenting a robust protection scheme for MTDC networks [98] suggests a combination of initial wave front detection and graph theory for wide area fault location. Accurate recognition of patterns using artificial intelligence has been highlighted an attractive trait for DC fault detection. Peng [99] explores effective ways of using artificial neutral network (ANN) to identify DC faults. The study focuses on using the wavelet transform to pre-process the DC voltage signal that will be implemented with the ANN.

Ramesh [100] shows other various detection algorithms that use the principles of artificial intelligence. Useful information applicable in DC protection can also be obtained from the frequency spectrum of voltage and current. In this algorithm, natural frequency from the travelling wave reflection process in a transmission line is used to evaluating a DC fault situation [23]. A fault can also be detected using natural frequency protection method. This technique implements the Fast Fourier transform, band pass filters and other PRONY algorithms [101] to extract useful data that aid in DC fault detection. The parameter identification is proposed in reference [61] as an alternate detection technique. For analysis of DC faults in this algorithm, measurements of capacitance are taken at both ends of the line. An internal fault is characterised by the simultaneous identification of the capacitance on both ends of the line. Any other resulting condition mean that the DC fault is external.

2.4.3. Fault isolation

The isolation of faults has thus far been implemented with AC and DC protective switchgear such as circuit breakers (CB) and fuses. They are usually placed strategically as AC CBs on the AC-side of the VSC-HVDC system. The interruption time for AC CBs is typically ranges from 50ms to100ms [67]. This makes them unsuitable for DC-side fault protection as they must be cleared only within milliseconds. To protect a VSC-HVDC system, AC CBs must disconnect the entire network. This property makes them undesirable for MTDC systems [16], [102]. The development of DC circuit breakers is regarded as the most relevant design for DC-side faults.

DC devices can interrupt constant current faster than their AC counterparts, sectionalising only the affected lines to isolate faulted lines and maintain the operation of healthy lines. This is achieved within an extremely short space of time. To maintain a power systems stability and integrity, fast fault clearing and active power recovery algorithms should be installed on the network. Since DC current has no zero-crossing, these components are also tasked with forcing the current to zero in order to interrupt the DC faults [71], [103]. DC CBs are usually characterised by their on-state losses, the withstanding rates of current and voltage as well as the overall interruption time [14], [104]. However, even though the development of DC CBs brings great relief for the designers of a protection scheme, the solution is still considered a challenge to design and manufacture.

Their application is mainly restricted by the efficiency and feasibility of the designed prototypes. Various innovative prototypes of the hybrid DC breaker have been proposed and tested either using simulation or in the laboratory environment. The technology has also been tested numerous times by reputable companies like ABB and Alstom but is not commercially and widely available today [25]. DC CBs can in general be classified into three categories. In this section, the different HVDC CB categories are highlighted, with a brief overview of the functional analysis of each class/group.

2.4.3.1. Mechanical DC breakers

The mechanical HVDC CBs are regarded as an old technology. They usually use the principles of AC CBs, but are more complex because of an additional resonant circuit [26]. This category of DC circuit breakers is known as the first generation in innovative high voltage DC CBs developed for HVDC networks. The 500 kV prototype was developed by EPRI and is discussed in [105]. Mechanical breakers are based on air-blast AC gas breakers and SF6 AC CBs [67]. The main advantages of mechanical DC CBs are that they are available for cheaper prices and have low on-state losses. However, due to a few constraints their clearance time is not favourable for a DC CB (i.e. it is typically in the order of 30-50 ms) [106], [107]. The idea of active resonance circuit discussed in [108], [109] has reduced the clearance time. The operation of the mechanical DC CB is generally slow when compared to other DC breakers. This means that it is unable to meet the DC protection requirements on its own [67]. These traits make it unattractive for application in VSC-HVDC systems. Figure 2-5 shows the basic structure of the mechanical breakers.

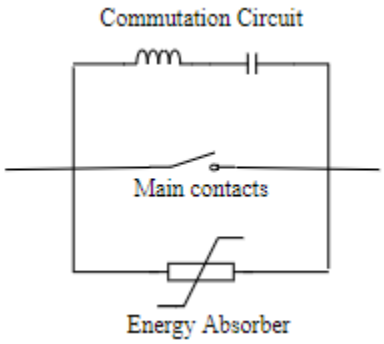

Figure 2-5: Mechanical DC circuit breakers [67]**.**

2.4.3.2. Solid-state CB

Larruskain [34], Vimalraj [63] and Jovcic [110] present the theory of solid-state CBs. This technology is generally based on semiconductor based switches (e.g. IGBTs) and gate turn-off thyristors connected in series and parallel.

An IGBT breaker has the ability to block/limit fault current and this quality makes it a good candidate in DC fault isolation. Each module of IGBT breaker is usually coupled with an anti-parallel diode. The operational principles of this technology are presented by Calenderia [11]. The basic structure of the solid-state DC circuit breakers is shown in Figure 2-6. Where V_{dc} represents DC voltage, Q the IGBT semiconductor, R_v is energy arrester and L_{dc} inductance.

These switches are tasked with supporting the voltage and current of the system during normal and faulty conditions of a VSC-HVDC system. Solid-state CBs are considered a very strong candidate for DC fault interruption. They are favoured for their high speed which is one of the main requirements for the interruption of DC fault currents. They contribute to a clearance time within 1ms, a speed considered the quickest than all other proposed topologies [111]. Their design however, has not been approved as feasible for the system since this technology has very high on-state losses. Sano [112] concludes that IGBT CB losses are much higher than those of the thyristor-based DC CBs during the networks normal operation.

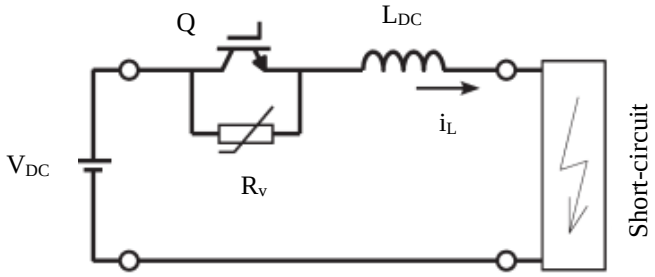

Figure 2-6: Solid-state DC circuit breakers [112]**.**

2.4.3.3. Hybrid CB

The technology of integrating the configurations of the solid-state devices and mechanical breakers is known as the hybrid breaker switching method. A basic schematic for a hybrid DC CB is shown in Figure 2-7. The mechanical switch acts as the mechanical breaker and carries the continuous current to the load. The solid-state switches are implemented as power semiconductors such as thyristors, insulated gate bipolar transistor (IGBT), gate turn-off thyristors and integrated gate-commutated thyristors and will operate only while switching on and off during the current interruption process [85], [109], [112]. These types of DC CB are considered a technology still in the developing stages. They use a relatively lower amount of IGBT power electronic devices and therefore the switching losses are less than those of a solid-state DC CB [46]. The addition of mechanical circuit breakers does however limit their action time. ABB is currently known to be developing these devices [25].

These breakers are designed with an additional path to redirect the fault current from the main path, allowing the opening of the mechanical switch to isolate the faulted zones from the system [34]. Their prototype is capable of interrupting power during a DC fault within 5ms [26], [113]. A new solution has also been proposed and tested by Alstom and its partners. This prototype can isolate the system in less than 5.5 ms, and under the real operational constraints of a HVDC scheme [114]. They have however not been implemented in real VSC systems. Recent developments in semiconductor switches and improvement in their characteristics such as conduction losses, switching time and reliability does increase their chance of being used as main DC fault interrupters. The total cost of the electronic switches is however usually increased to around 20-30% of the total cost of full VSC system [107]. This makes the solution the most expensive to implement.

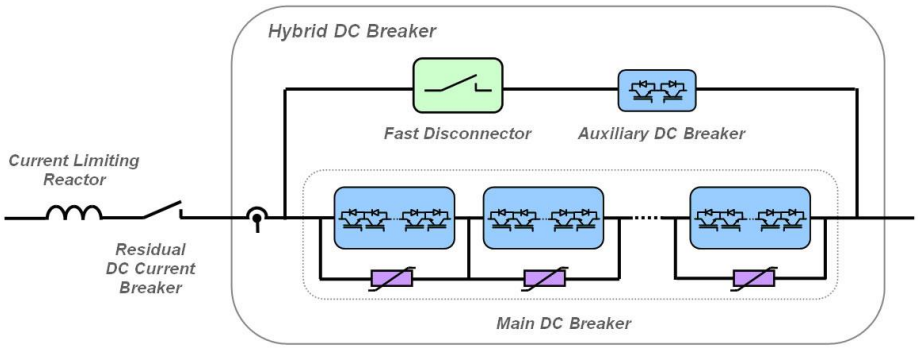

Figure 2-7: ABB Proactive hybrid HVDC breaker [26]**.**

2.4.3.4. Summary and discussions

To interrupt a DC fault, mature isolation switchgear in the form of AC CBs have been proven to lack in speed, selectivity and robustness. It is therefore necessary to design feasible technologies to deal with DC-side faults. DC CBs remain the most capable technology for this task. Due to the strict requirements for the breakers withstand currents and the response time, the design of DC isolation devices remains a big challenge. The most common types of DC CBs have been presented and briefly analysed, the main findings are summarised below: -

- The mechanical CBs operate at a slow-pace and only considered if they have assistance from current limiters.
- Solid-state CBs operate at a faster pace. Their high-on state losses remain as their biggest constraint.
- Hybrid CBs combine the strengths of the mechanical and solid-state CBs. This increases their performance as DC isolation devices.

These results also show that although solid-state breakers have the least interruption time, the hybrid DC CB are usually more favourable because of their reduced on-state losses. A longer time to break will however give rise to an increase in the peak current breaking capability of the DC breaker, thereby increasing cost for the DC breaker. Other innovative solutions of interrupting DC-side faults include the DC/DC converters as designed in [110]. These can also be used in the system as a transformer or as a current limiter but are however restricted by their high losses and cost [110]. Hajian [77] also proposes new alternate isolation techniques comparing the performances, costs, and losses of the LCL thyristor converter , hybrid DC CB, FB DC/DC chopper and HB DC/DC chopper. The main conclusion drawn from these studies there are currently no competent/viable DC CBs perfectly fit for use in VSC-HVDC networks. There is also no commercial installation of a DC circuit breaker operating on a VSC-HVDC system to date. Therefore, more extensive research should still be conducted in future.

2.4.4. Current limiters

The conventional procedure or standard used to protect a power system entails a technique that is required to accurately detect, locate and isolate a fault. HVDC isolation switch-gears are however still not effective due to the high fault current levels. Recent studies are therefore investigating the possibility of reducing the abruptly high fault current magnitude by placing a limiting component in the circuit [115]. This component is commonly referred to as a fault current limiter (FCL) [55]. The primary objective of a FCL is to limit fault current levels to a more manageable level during a fault [55]. This is to be carried out without a significant impact on the electrical system. To avoid the overshoot in the diode freewheeling stage, FCLs are mainly installed on the DC-side of the network [116]. Fault current limiting technologies can be classified as either conventional or advanced technologies. Conventional technologies usually rely on the construction of new substations, bus splitting, upgrade of the existing CBs, current limiting reactors, or high resistance grounding (e.g. the saturable core FCL) [109]. Solid-state (SS) FCL, positive temperature coefficient (PTC) resistors, liquid metals and Super-conducting FCL are proposed as the more advanced technologies[109], [117] and have higher effectiveness. Inductor-capacitor-inductor VSCs (LCL-VSCs) presented in [55] are also proposed as a promising fault tolerant topology. In this section, a brief review of fault current limiting schemes is highlighted.

2.4.4.1. Protective inductors

A simple method of limiting fault current is proposed in [118]. This method is based on theory that the addition of an inductor on the DC-side of the VSC-HVDC network can restrain the rate of rise in current during a DC fault. The protective inductor FCL method is referred by [119] as a fault current limiting reactor, as it is installed permanently on the network as a passive element that does not require external activation.

Including protective inductors results in relatively low impedance, limiting an effect to the normal operation of the system. The addition of these inductors will cause a voltage drop during normal operation of the network. This contributes to the systems losses and increases the cost of the network.

2.4.4.2. Solid-state fault current limiter

Solid-state FCLs (SS FCL) aim to limit fault current by changing the configuration of the circuit during a DC fault. This is possible due to the recent developments in power semiconductor devices. SS FCLs can be classified as impedance insertion SS FCLs, resonant SS FCLs and bridge SS FCLs. These are explained in detail in [119] and [120]. Among the mentioned categories, the impedance insertion limiters show great potential for application in HVDC systems. SS FCLs are generally favoured for their fast operation, immediate recovery and the capability of withstanding multiple operations. However, the main drawbacks are the on-state losses and commutation losses [67]. Depending on the type of SS FCL implemented, the system could also experience over-voltages, sags, voltage and current stresses on the semiconductor and high costs. However, there are proposals to improve their performance. This will reduce the footprint, voltage drop and ultimately the costs [121].

2.4.4.3. Super-conducting fault current limiters

Super-conducting (SC) FCLs are one of the strong contenders for techniques planned to be implemented in VSC-HVDC systems. They are regarded as an ideal technology for DC networks as they result in zero losses for pure DC current [122]. During normal operation, SC FCL operate in super-conducting state with zero resistance. They then change to their normal state exhibiting very high impedance during a fault in the system [119]. Though the technology is highly recommended for DC systems, currently installed SC FCL projects are mainly found in AC power networks. SC FCLs have distinct advantage over other proposed FCLs in high voltage networks. They provide an ultra-fast transition from super-conducting to normal state, are self-operating and repetitive in nature. Furthermore, the absence of resistance during normal operation results in negligibly small losses. The technology however has its own drawbacks. They are bulky due to the need for iron cores and need a complex current supply for the super-conducting winding [116].

2.4.4.4. Non-linear resistors

Fault current limiting of VSC-HVDC networks could also be realised by installation of non-linear resistors. These include the polymer PTC-resistor FCLs [123], liquid metal FCLs [124] and the super-conducting FCL described in Section 2.4.4.3. These technologies all have a different physical mechanism. They however share the similar principle of ideal and desirable characteristics, as during normal operation, they have no resistance. After a fault, the resistance increases. This is mainly due to the rise in temperature caused by DC fault current [125].

When the DC fault has been cleared their temperature once again cools down and they become low in resistivity. Their main advantage over protective inductors is that since they are merely resistive, they do not affect the dynamic response of the system.

2.4.4.5. Inductor-capacitor-inductor VSC

The inductor-capacitor-inductor (LCL-VSC) although presented in this section is not a typical FCL. It is mostly classified as a fault tolerant VSC, but without the need to re-design the system. For these reasons, LCL-VSCs are extremely economic when compared to other fault tolerant VSCs. To realise this topology, a typical VSC station is combined with a LCL circuit. The design of the LCL circuit is discussed in depth by Lin [106] and Jovcic [126]. The LCL filter is designed with the main objective of providing fault current limitation for the VSC-HVDC system. This also results in converter optimum efficiency. LCL-VSCs allow for large DC fault currents to be avoided in the event of DC faults at any point in the DC network. By limiting the fault current, the faulty section can thus be isolated using a mechanical DC CB even with a long operating delay [127]. The LCL filter can also eliminate the inclusion of AC transformers, taking the responsibility of AC voltage stepping.

2.4.5. Fault-blocking converters

An interesting alternative DC protective measure includes changing a network's converter topology. This method has an advantage of eliminating the use of additional devices like FCLs and will therefore reduce the size of converter stations and possibly the costs associated with it [11]. It does however require the redesign of the converter and is therefore not the best option for existing systems. This section aims to explore currently available fault blocking VSCs.

2.4.5.1. Full-bridge MMC

The full-bridge submodule is a variant of the half-bridge MMC [128]. It is mainly favoured for its ability to block DC faults. Apart from the DC fault-tolerant property, the FB-MMC also has the advantages of operation with low DC voltage and the ability to generate higher AC voltage for a given DC voltage limit [55]. A converter station with this configuration is shown in Figure 2-8. In the figure, I_a represents phase a current, V_{dc} represents DC voltage, V_C represents DC voltage across capacitors, V_{SM} represents submodule voltage, V_{an} represents neutral point voltage, V_{pa} and V_{na} represents the positive and negative voltage, i_{ap} and i_{an} represents the positive and negative current and L_0 are the arm inductance. In a FB MMC, the IGBTs can be blocked to stop the flow of the DC current. A negative polarity voltage then restricts the current surge [32], [129]. Using arm inductors, the voltage output of the submodules can be controlled to bring down the current to zero. In the absence of fault current, the faulty section can be easily isolated from the other parts using a mechanical DC circuit breaker [55], [108].

The full-bridge MMC converter are commercially available but are is limited by higher costs when compared to the half-bridge MMC, due to the increased number of IGBTs. The arrangement requires twice as many IGBTs and has higher power losses than the equivalent half-bridge arrangement [29], making it less attractive when compared to half-bridge topology.

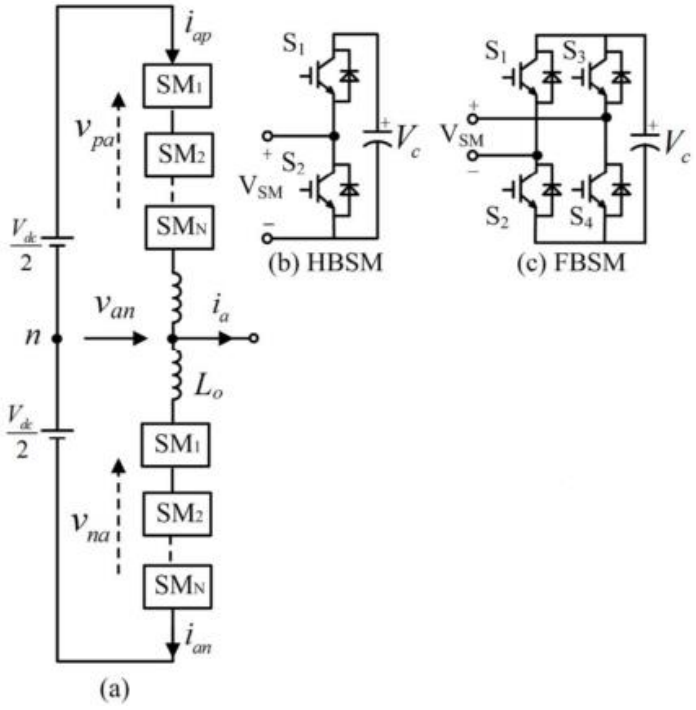

Figure 2-8: A representation of a) circuit diagram of one-phase of FB-MMC where b) is the HB submodule and c) is the FB submodule [130]**.**

2.4.5.2. Fault-blocking variants of MMC

To overcome some limitations associated with conventional MMCs (i.e. both full-bridge and half-bridge MMC), a few variants are proposed in literature. These protection techniques include new cell configuration to mitigate fault currents. A concept presented in [131] also uses the advantage of embedding protective measures in the converter. In this investigation, a new generation of converters using H-Bridge cells has been implemented to eliminate the drawbacks of VSCs and is known as hybrid multi-level converter with H bridge cells in the AC side. These converters inherently provide DC fault reverse blocking capability which can be used to improve VSC-HVDC resilience to DC-side-faults [132]. There are numerous other topologies with similar characteristics of fault blocking. An example is the addition of H-bridge valves at the AC side of the system. These are aimed to block the fault current flow between the AC and DC-sides during DC faults. This factor facilitates a fast decay to zero for the fault current allowing CBs to isolate them without getting damaged [133].

Adam [134] proposes the idea of mixed cells where 50% of the SMs are HB and rest are FB. This combines the advantages of HB and FB which is reduced semiconductor losses and fault blocking capability. The idea is also analysed by Zeng [130], who proposed that if the total voltage from the capacitors in the FB SMs is higher than the AC voltage, a DC fault can be blocked. A popular variant of the full-bridge topology is called the alternate-arm multi-level converter (A2MC) [135]–[137]. This is a hybrid topology which combines features of the two-level and multilevel converter topologies. It can block DC faults with reduced semiconductor losses compared to the FB-MMC. The clamped double-cell configuration proposed in [138], [139] is also a promising emerging topology. It can block DC faults, only withstanding a reduced amount of losses. Unfortunately, the clamped double-cell configuration does not fully solve the DC fault issue as the power losses are increased by 50% compared to using two half-bridge cells during normal operation because of the additional IGBT in the conduction path [38].

Other variants worth mentioning include the cross connected (CC) cells presented in [138], [140], [141]; the MMC based on unipolar voltage full-bridge SM and three-level cross-connected SM in [142]; the cross-connected half-bridge submodules in [143]; the hybrid cascaded multilevel converter (HCMC) in [144] and the LCC-diode-MMC (LCC-D-MMC) hybrid HVDC configuration proposed in [145], [146]. Among these DC fault-tolerant MMCs, the MMC based on FB submodules (including the mixed submodules MMC) is the only commercially available fault-tolerant technology for HVDC applications. The main attraction to converters with DC fault blocking capabilities is not only because they eliminate AC-side contributions but also to take advantage of their quick recovery time from DC-side faults. This means that DC breakers with lower current ratings can be used to isolate the faulty line and the AC breakers tripping can be avoided. This a trait very attractive especially for MTDC systems.

2.5. Protection requirements

When developing VSC-HVDC systems, the design of a feasible control and protection scheme must be a priority. The proposed design fundamental principles for these systems are drawn from conventional HVDC systems and the mature HVAC networks [16], [34], [67]. These principles serve as a guideline that can be used for both protection schemes under development and those already installed. VSC-HVDC systems are not immune to disruptions, therefore it is always advisable that an electrical system is equipped with a very strong protection scheme. System protection is defined as the art and science of detecting and disconnecting faults and other abnormal conditions on a power system [147]. A protection scheme is tasked to monitor the system continuously, removing possible threats without interfering with or limiting the normal operation of the system. Important characteristics that are usually considered in the design of a protection scheme include: -

- Inclusion of features tasked to prevent failures and;

- Features tasked with mitigating the effects of failure in cases where it does occur.

It is also just as important in a protection scheme that the following requirements are effectively met. These are considered philosophies of protection [34] and include: -

- Speed: Is essential to avoid damage to equipment, where the faults are expected to be interrupted before they can damage the equipment.
- Selectivity: The protection system must have defined protection zones which would prevent the isolation of unaffected VSC-HVDC components. The system should also be able to distinguish the difference between normal operation, possible overload and a fault condition.
- Reliability: Includes dependability which implies that the protection scheme applied to prevent the network from being affected by faults should be readily available to offer its assistance only when it is required to, especially when considering large protection zones, in which large sections are isolated in case of a DC fault.
- Sensitivity: Is important to ensure that every faulty situation is to be accurately detected and cleared without exception.
- Robustness: The protection system must be able to operate even in degraded situations. When protection systems are duplicated this also provides redundancy and can aid in robustness.
- Seamlessness/stability: Where the system is expected to reach stable operation within an acceptable period after clearing the fault thereby allowing the system to continue operating securely.

It should be taken into consideration that even though existing methods for AC grids cannot be directly applied in DC grids since they are too slow to cope with the DC fault current phenomena, the development of DC-side protection system should be guided by the same highlighted protection requirements/ philosophies as they are well established in AC systems [16].

2.5.1. Protection requirements of a VSC based MTDC system

Protection measures, securing VSC-HVDC schemes from faults and disturbances are regarded as one of the main factors to have limited the growth of VSC-MTDC systems. Although vastly admired for their controllability and flexibility, due to their nature VSC-HVDC systems are defenceless against DC-side faults [148]. Proven protection methods in AC grids are not regarded as feasible for protecting VSC-MTDC systems against DC faults as they are too slow to cope with the DC fault current phenomena and require isolation of the entire MTDC system. Protection of MTDCs is regarded as even more challenging since they require even faster communication links. Much like point-to-point systems, the basic protection requirements for a MTDC transmission scheme are speed, selectivity, sensitivity and security.

For MTDC networks the emphasis is mainly on obtaining fast and selective DC line fault detection, location and isolation techniques [67]. To satisfy the high speed operational requirements, current fast fault detection and location algorithms include travelling waves measured at the MTDC terminals. These methods use the initial transient fault signatures for detecting and locating commonly occurring faults like pole-to-pole and pole-to-ground faults [149]. A selective protection scheme ensures dependability and certainty of correct operation once a fault occurs in a protection zone. As mentioned, currently favoured fault detection and location methods for HVDC transmission include travelling waves. However, due to multiple paths in the MTDC networks, this technique becomes more complex to implement and control. Other commonly applied detection and location techniques include voltage and current differential as well as derivative methods [23]. As the technology progresses, there have been numerous other techniques presented to detect and locate DC faults in a VSC-MTDC system.

Some of these include the methods based on the electromagnetic time reversal (EMTR). This method on time reversal process is applied to travelling waves in transmission lines using measurements at one terminal only. Its details are further elaborated in [18]. Studies carried out in [150] also proposes that a DC fault is managed using what is referred to as the delayed-auto-re-configuration (DARC), for VSC MTDC networks. This protection scheme does not require additional components to be added to the existing system but instead the MTDC system is protected after the isolation of the faulted line section, where un-faulted terminals will be controlled and recovered to form a new MTDC configuration.

It is essential to note that besides focusing only on addressing the critical design requirements of selectivity and speed, the system's grounding schemes play a huge role in influencing the fault detection and protection solutions [8]. Likewise, it is important to ensure that the designed scheme is equipped with back-up protection and the auto reclosing function for quick service restoration after temporary fault trips.

2.5.2. Future of VSC- HVDC transmission protection

The development of a robust protection scheme for a VSC-HVDC system will surely play an important role in the future of these systems. The current trend that is seen implemented for the protection of these networks, focuses a lot on improving fault location and or the development of a DC CB able to withstand the fast and high rising DC fault currents. The choice to focus on these properties is understandable, as it is a vital task to detect, locate and isolate DC faults before they can affect the rest of converter of the station. It is however also important to note that there have been commendable advances in other areas of VSC-HVDC protection. In addition to fault location and isolation, research has broadened into developing ways of limiting fault currents such as including FCLs to reduce the severity of DC faults.

From the available technologies, super-conductors emerge as a promising solution. More information on the super-conducting fault current limiters is presented in references [99] and [115]. The development of new valves is also proposed by Alstom and this technology is seen as an equally promising approach in protection. The innovation of this technology aims to combine existing VSC topologies to produce a prototype that is meant to deal directly with some of the constraints posed by VSC schemes. The Alstom hybrid valve combines concepts of the conventional converters (i.e. LCCs) with those of MMCs [3]. The technology results in relatively lower losses and low distortions presented by half-bridge MMC as well as DC fault blocking capabilities from full H-bridge MMC [3]. Unfortunately, this solution is mostly beneficial for stations still under development [151].

For VSC-HVDC networks that are already in existence, it is considered more feasible to develop DC isolators or breakers to perform the task of protecting existing VSC-HVDC networks from being affected by DC faults. For complete protection, an isolation device is always necessary in the system. These work by starving the DC fault for a long period of time so that that there are no possibility of system re-striking when the voltage re-appears [152]. DC switches although fast, are incapable of interrupting fault current [152]. A feasible solution is the ABB DC breaker. Although the breaker is praised for its numerous attractive traits, the prototype has yet to be implemented in real life .The costs associated with a device of its nature are not expected to be trivial [113]. Research therefore looks to find a similar technology that can perform these functions at a reasonable amount without affecting the networks reliability.

CHAPTER 3: PROTECTION SCHEME FOR VSC-HVDC

3.1. Introduction

The aim of this Chapter is to develop and discuss in detail an algorithm for the proposed protection scheme for a MTDC VSC-HVDC system. It is important to note that an initial study and understanding of fault responses of a system is a vital task, as it sets the ground for designing a feasible protection scheme. Chapter 3 thus initially investigates the fault response of a VSC-HVDC system with different VSC topologies. The information obtained from this analysis was used to formulate a reliable protection method for the system. Later in the Chapter, the proposed methods of detecting, locating and isolating a DC fault in a VSC-HVDC scheme are discussed in detail. The Chapter concludes with a flow diagram detailing the working principles of the proposed protection scheme for the system.

3.2. DC fault response

The fault response of a VSC-HVDC system is typically expected to vary with the type of fault experienced. As highlighted in Chapter 2, VSC-HVDC systems are potentially exposed to either ground faults or short-circuit faults. Ground faults are considered the most frequent but less harmful to the system than its variants. However, due to the change in structure, a converter's topological arrangement (i.e. 2-level topology or multi-level) or type of system configuration (i.e. either the monopolar configuration or bipolar configuration) can influence the fault response of a VSC-HVDC system [64], [65].

Similarly, fault distance or location, the type of transmission medium used (i.e. cable or overhead line) and the fault resistance in the case of ground faults are also expected to affect the fault response of the system [52], [101], [153]. These factors should therefore be taken into consideration when designing a protection scheme for a VSC-HVDC system. Section 3.2 aims to investigate a VSC-HVDC system's DC fault response.

This is achieved by examining some of the factors previously mentioned that influence the system's transient fault phenomena. The analysis will focus mainly on evaluating influences for the more severe but less frequent short-circuit fault. A similar analysis approach to that used for short-circuits can however still be followed for the ground fault as discussed in [52] and [74]. Focusing solely on line-to-line faults, important factors to consider during this analysis include the influence of HVDC network topology and system configuration on the magnitude and rate of rise of fault current and other aspects such as network reliability and post fault contingency.

3.2.1. Converter topology - fault analysis for conventional VSCs

The correct design of a protection scheme is only possible after a proper fault analysis study has been carried out. The critical parameter limits identified during these studies were later used as settings in the implemented DC protective switchgear (e.g. the critical time limits of a DC fault current were useful in the configuration of a DC CB's speed requirements). In a conventional VSC-HVDC system a DC fault is usually known to occur in three different stages (although some literatures can expand the number of stages as in [154]). In these stages, ultimately, IGBTs are blocked and the AC grid will feed fault currents through the antiparallel diodes [13], [23]. A line-to-line fault as already mentioned poses the most serious threat for VSC systems.

During a DC fault, the blocking of IGBTs exposes diodes to overcurrent. Active power is reduced to zero while reactive power is left to flow from the AC side to the converter increasing the fault current due to the AC contribution [55]. This is possible through the freewheeling diodes and causes a severe voltage dip. It is expected that after the fault clearance the AC side converter switches will experience high inrush current while the DC-side works on rebuilding itself. The equivalent circuit is as shown in Figure 3-1, where R_c and L_c are the equivalent resistance and inductance respectively.

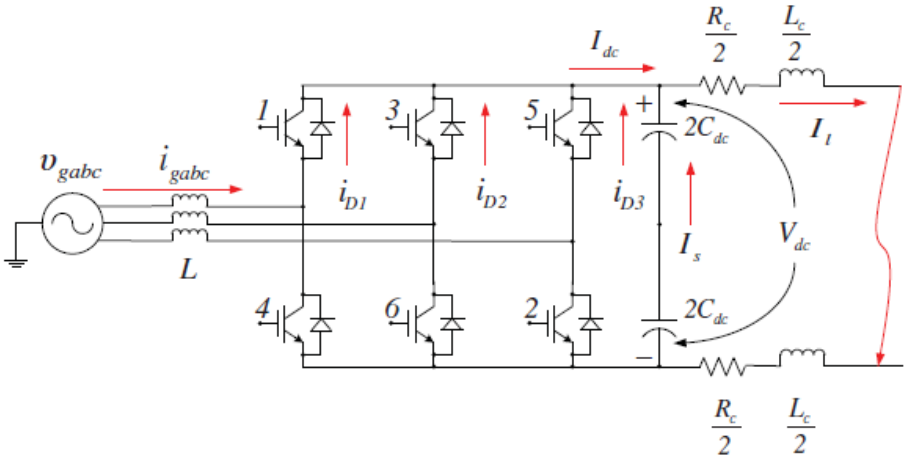

Figure 3-1: A two-level VSC-HVDC converter station following a cable-to-cable DC fault [55]**.**

To analyse and understand the response of a DC for a VSC-HVDC network, the results obtained can be divided into three stages. In this section, the different stages of the DC fault are analysed individually, as it progresses.

3.2.1.1. Stage 1: Capacitor discharging stage

This is considered the natural response of the circuit and occurs immediately after the fault. As the name suggests, during this stage the DC-link capacitor is discharged.

Under the conditions $R_c \leq 2\sqrt{\frac{L_c}{C}}$ an equivalent circuit resulting from the fault is shown in Figure 3-2. The solution of the second order circuit natural response results in equations (3-1) and (3-2) for DC-link voltage and cable current respectively.

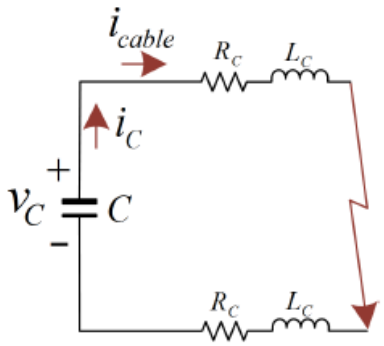

Figure 3-2: Equivalent circuit for capacitor discharge stage during short-circuit fault [71]**.**

Assuming that the fault occurs at time $t = t_0$ and also that $V_c = (t_0) = V_0$ and $I_{cable}(t_0) = I_0$, the DC bus voltage can be represented as [55]: -

$$V_{DC} = \frac{V_0 \omega_0}{\omega_n} e^{-\gamma t} \sin(\omega_n t + \delta) - \frac{I_0}{\omega_n C} e^{-\gamma t} \sin(\omega_n t) \qquad (3\text{-}1)$$

While the cable current is expressed as [55]: -

$$I_{cable} = I_{DC} = C\frac{dV_{DC}}{dt} = -\frac{I_0 \omega_0}{\omega_n} e^{-\gamma t} \sin(\omega_n t - \delta) + \frac{V_0}{\omega_n L_c} e^{-\gamma t} \sin(\omega_n t) \qquad (3\text{-}2)$$

Where $V_{DC} = V_C =$ DC voltage

V_0 and I_0 = Initial values of DC voltage and current respectively

C = DC-link capacitance

R_c, L_c = cable resistance and inductance respectively

I_{cable} = cable current

$\delta = \tan^{-1}(\frac{\omega_n}{\gamma})$ and is defined as the systems phase angle

$$\omega_n = \sqrt{\frac{1}{L_c C} - (\frac{R_c}{2L_c})^2}$$

$$\omega_0 = \sqrt{\gamma^2 + \omega_n^2}$$

In a conventional VSC system, the DC-link capacitor qualifies as one of the highest contributors to the DC fault current magnitude in the initial stages of the DC fault [52], [62]. It is therefore important during the design of protection that the size of the capacitance used and their discharging rates are considered.

3.2.1.2. Stage 2: Freewheeling diode stage

The diode freewheel phase is also a natural response. It is initiated when the DC-link voltage has dropped to zero. In this phase, the cable current is transferred to the antiparallel diodes of the VSC. It can be solved using the equivalent circuit shown in Figure 3-3, where the cable has an initial current $I_{cable}(t_0) = I_0^{'}$

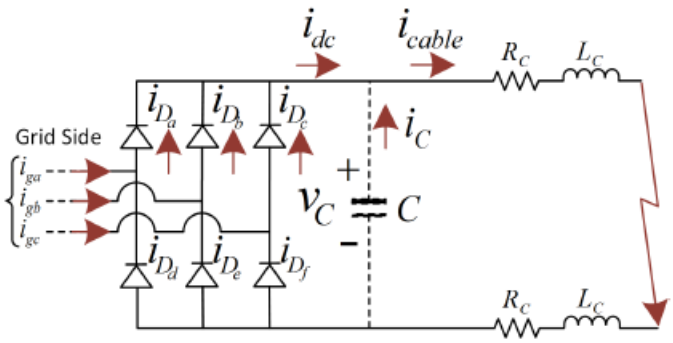

Figure 3-3: Equivalent circuit freewheeling diode stage during short-circuit fault [71]**.**

As mentioned previously, as an initial condition, the DC bus voltage at this stage is expressed as [55]: -

$$V_{DC} = V_C = 0 \qquad (3\text{-}3)$$

While cable current becomes [55]: -

$$I_{cable} = I_0^{'} e^{-(\frac{R_C}{L_C})t} \qquad (3\text{-}4)$$

Where the parameters used are as defined above.

3.2.1.3. Stage 3: AC grid current feeding stage

This part of the stage is known as the forced response stage. It can be solved using the equivalent circuit shown in Figure 3-4.

The IGBTs are blocked when the current through them rises above a threshold, however the DC voltage does not drop exactly to zero. Initially a three-phase short-circuit analysis is done. The following expressions can be deduced for both fault current and DC bus voltage.

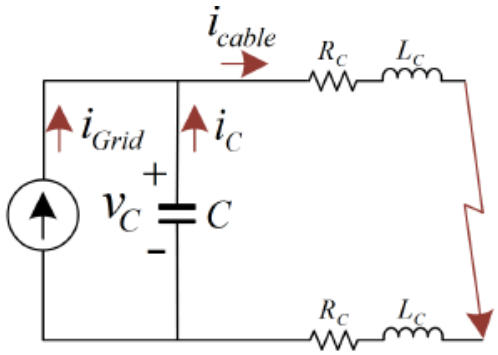

Figure 3-4: Equivalent circuit AC grid current feeding stage during short-circuit fault [71].

The DC bus voltage can be represented as [55]: -

$$V_{DC} = V_C = 2R_C I_{cable} + 2L_C \frac{dI_{cable}}{dt} \tag{3-5}$$

Cable current is given by [55]: -

$$I_{cable} = C_1 \sin(\omega_g t + \lambda) + C_2 e^{-t/\tau} + \frac{C_3 \omega_0 e^{-\gamma t}}{\omega_n} \sin(\omega_n t + \theta_{g0}) + \frac{C_4 e^{-\gamma t}}{\omega_n} \sin(\omega_n t) \tag{3-6}$$

Where $C_1 = I_m \sqrt{(1-\omega_g^2 L_c C)^2 + \omega_g (R_c C)^2}$

(Phase-a grid current) $i_{ga} = I_g[\sin(\omega_g t + \theta_{g0} - \delta) - \sin(\theta_{g0} - \delta)e^{-t/\tau}] + I_{a1} e^{-t/\tau}, t_1 \le t$

$I_{a1} = i_{ga}(t_1)$

$\lambda = \theta_{g0} - \delta - \sigma$

$\sigma = \tan^{-1}(\frac{\omega_g R_c C_{DC}}{1-\omega_g^2 L_c C_{DC}})$

$C_2 = I_m(\frac{\tau^2}{\tau^2 - R_c C_{DC}\tau + L_c C_{DC}})$

$I_m = I_{a1} - I_g \sin(\theta_{g0} - \delta)$

$$C_3 = -C_1 \sin \lambda - C_2$$

$$C_4 = \frac{C_2}{\tau} + \omega_g C_1 \cos \lambda$$

To calculate the fault current, contributions from both the converter and the AC side were considered. The common reaction of a VSC system when disrupted by DC-side faults is a sharp current rise and voltage dip. Results adapted from [154] for a 2 level VSC-HVDC system with a rated DC voltage of 10 kV are presented in Figure 3-5 and reveal the outputs characterising the cable current and the DC voltage during a short-circuit fault. The figure shows 4 stages instead of 3 as described above. Stage 1 shows results when the capacitor discharges whilst the diodes are turn off whilst stage 2 shows results of the capacitor discharge when diodes have been turned on (these two stages are normally grouped as the first stage and have been represented as such in the discussion). Stage 3 shows results when the inductors discharge through the diodes (this stage is represented as stage 2 in the explanation). Finally, stage 4 represents the AC grid feeding stage (i.e. represented as stage 3 in the explanation).

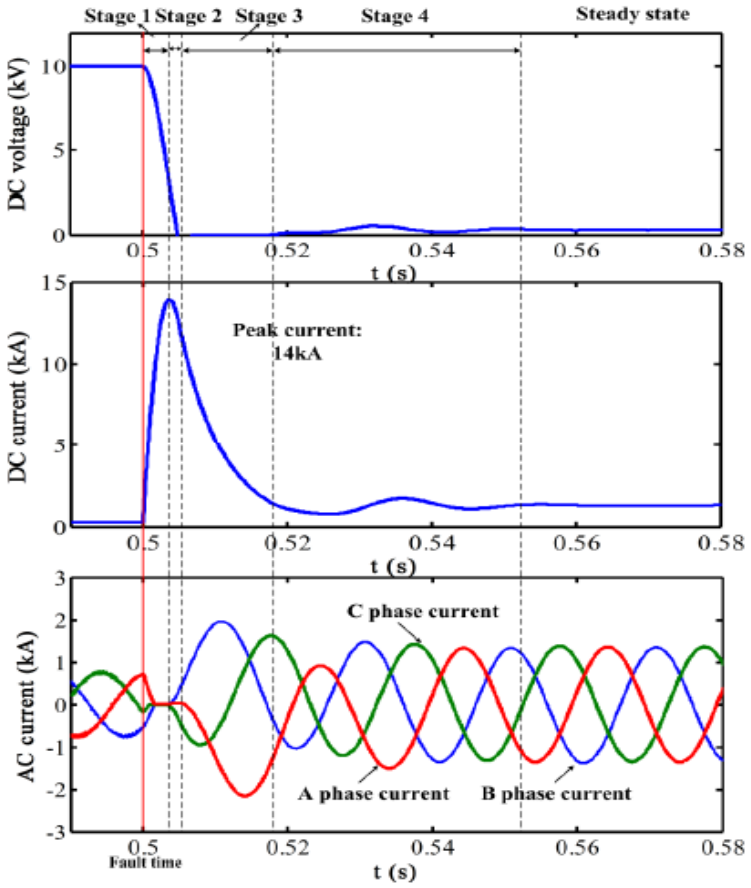

Figure 3-5: The fault characteristic of the VSC during a DC short-circuit fault [154]**.**

Although the discussion of stages resulting from a DC fault can be represented a bit differently (i.e. as either 3 or 4 stages), a characteristic evident in all is the sharp rise in DC current. This is a value much higher than the DC CBs short-circuit capability of 9 kA [155]. It is important to note that even though the cable current rises very sharply during the capacitor discharge phase, the most critical phase for the system is the free-wheeling phase [156]. The IGBTs are blocked as soon as current through them rises above a specified threshold. Therefore, appropriate device protection measures should be considered.

3.2.2. Protection of conventional VSC systems

When a DC fault occurs in a VSC system, the two-level converter station goes through the phases of response mentioned above [17], [157]. The biggest disadvantage of conventional VSC systems is their inability to block or control the current during DC faults. Since the fault current in the cable rises extremely fast, it is also very challenging to meet the requirements for the protection system of such networks [70]. It is thus expected that if a two-level VSC topology system is affected by DC faults, quick detection, location and isolation of the fault should be the main characteristics of the implemented protection scheme. Travelling waves and related methods are at present the most commonly used for fault detection and location [158]. These methods can respond quickly and have high accuracy.

The isolation of faults on the other hand has thus far been implemented with AC and DC protective switchgear such as CBs [85], [152]. DC devices are a better option than AC protective switchgear. This is because DC devices can interrupt constant current faster than their AC counterparts to isolate faulted lines [159]. DC circuit breakers are probably the most relevant DC protective switchgears. They are tasked with forcing the current to zero in order to interrupt the faults since DC current does not naturally have a zero crossing [71], [103]. For multi-terminal VSC-HVDC applications, DC breakers are more applicable, however, these devices have low short-circuit capability. The protection for VSC-HVDC systems must therefore be fast enough to clear the fault before the current exceeds the equipment limits.

Mourinho [155] and Xue [154] propose that in order to mitigate the effects of fault currents in VSC-HVDC systems, super-conducting fault current limiters (SFCL) can be identified as a potential solution to significantly minimise the impact of high fault currents and improve system stability during fault conditions. It is suitable for a system with a high fault current and a high current rising speed. However, the integration of the SFCL has a serious influence on the coordination of the protection. Available literatures and future proposals make little mention of improving conventional VSC technologies as they are geared towards developing and improving converters with fault blocking capabilities to reduce and ultimately eliminate the use of DC CBs to reduce costs [142]. Therefore, it is only the main principles developed in such systems that are likely to be improved for better application in new converter technologies.

3.2.3. Converter topology - fault response of the MMC

In recent years, an alternate option known as the modular multilevel converter (MMC) has been developed for the conversion of power. The objective for the development of MMCs was to address limitations and constrains experienced by conventional converters. One of the main contributors of fault current in a conventional VSC is the discharge of the DC-link capacitor. To reduce contributions on fault current, MMCs are designed not to have a large DC-link capacitor [160]. MMCs are traditionally classified as either the half-b ridge (HB) or full-bridge (FB) MMCs. The half-bridge MMC topology has gained more popularity amongst major HVDC manufacturers. This is mainly due to the reduced semiconductor losses when compared to the full-bridge MMC. The analysis and comparisons discussed in this sub-section will therefore mainly apply to the HB MMC. Additionally, the influence of the topology on the design of a protection scheme will be detailed, highlighting the main challenges and possible solutions.

A line-to-line fault as shown in Figure 3-6 creates a direct path inside the MMC for the fault current, as the antiparallel diodes conduct to feed the fault current from the AC side. A current overshoot is then initiated by the discharging of the SM capacitor voltages. This causes a risk on the converter switches due to the DC fault. Like conventional VSCs, HB MMCs are unable to block AC grid current contribution therefore DC fault survival may strongly rely upon the protection scheme implemented.

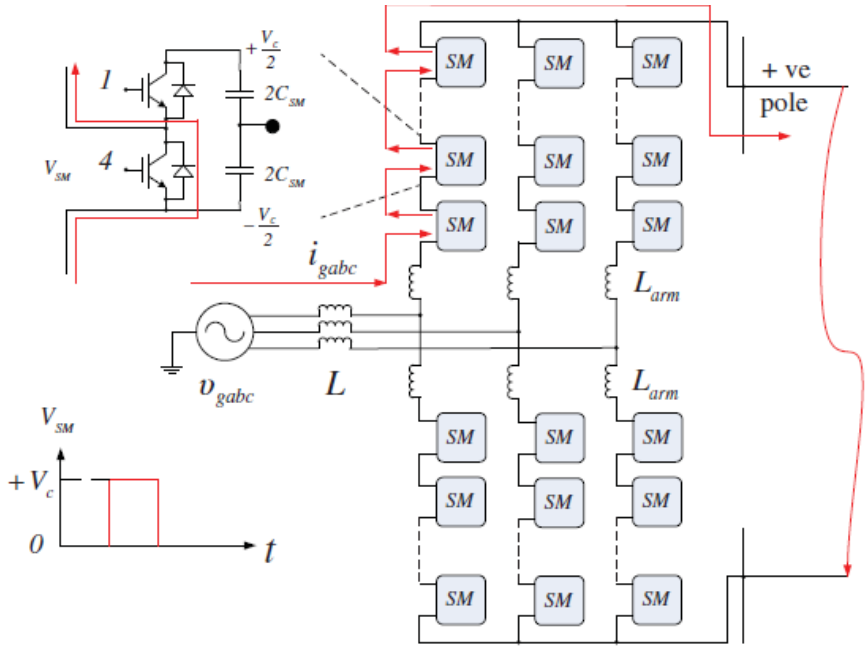

Figure 3-6: A converter station with half-bridge MMC configuration during a short-circuit fault [55]**.**

To analyse and study the fault response of the MMC topology, the fault response is categorised into three stages. Only the positive phase-a equations are shown as results obtained for other phases and for the negative pole are similar. Once again, this study will focus on analysing only the more severe short-circuit faults for this topology, however similar analysis can be followed for the ground fault as in [65], [161].

3.2.3.1. Stage 1: Before IGBT are blocked

Initially the IGBTs are not turned off. The main contributor of fault current are the DC cable and SM capacitance discharge. During this stage, DC current rises very fast and increases the arm currents. Figure 3-7 shows the equivalent circuit during short-circuit fault in stage 1.

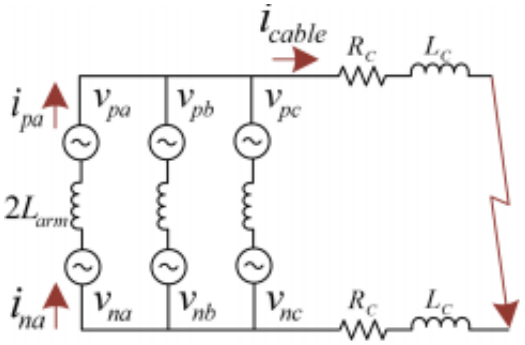

Figure 3-7: Equivalent circuit during short-circuit fault Before IGBT are blocked [71]**.**

For an MMC based system, the DC voltage can be deduced from the positive phase-a voltage [55]: -

$$V_{pa} = \frac{V_{DC}}{2} - L_{arm}\frac{dI_{ap}}{dt} - V_a - R_c I_{cable} - L_c \frac{dI_{cable}}{dt} \qquad (3\text{-}7)$$

The current can be expressed as [55]: -

$$I_{ap}(t_1) = \frac{i_{ga}(t_0)}{2} + \frac{I_{DC}(t_0)}{3} + \frac{V_{DC}(t_0)}{2L_{arm}}(t_1 - t_0) \qquad (3\text{-}8)$$

Where V_{pa} = positive phase-a arm voltage

L_{arm} = arm inductance

I_{ap} = positive phase-a arm current

V_a = equivalent phase voltage in phase-a

I_{cable} = DC cable current

L_c = cable inductance

i_{ga} = phase-a diode current

I_{DC} = DC-side current

R_c = cable resistance

V_{DC} = DC voltage

3.2.3.2. Stage 2: Diode freewheel phase

When the IGBTs have been blocked, the current starts freewheeling through the antiparallel diodes. One arm current will increase while the other reduces to zero. On the AC side, the entire AC voltage gets applied across the inductor L which results in increase in the AC current.

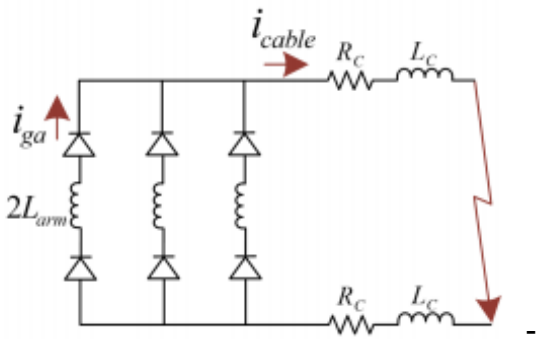

Figure 3-8: Equivalent circuit Diode freewheel phase during short-circuit fault [71]**.**

In this stage, the resulting DC voltage calculated using the equivalent circuit shown in Figure 3-8 can be deduced from equation (3-9) [55]: -

$$L_{arm}\frac{di_{ga}}{dt} = \frac{V_{DC}}{2} + R_c I_{cable} + L_c \frac{dI_{cable}}{dt} \qquad (3\text{-}9)$$

The current can be expressed as [55]: -

$$i_{ga} = 2\left(\frac{V_{DC}}{2(L_{arm})}(t_1 - t_0) + \frac{I_{cable}}{3}\right. \qquad (3\text{-}10)$$

3.2.3.3. Stage 3: Grid current feeding

In the current feeding stage shown in Figure 3-9, the arm inductor has a direct impact on the diode current. The arm fault current includes AC fault current and SMs capacitors discharging current

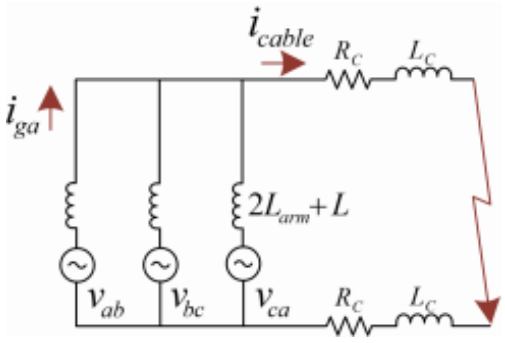

Figure 3-9: Equivalent circuit AC grid current feeding stage during short-circuit [71]**.**

The capacitor current eventually damps to zero leaving AC current to continue feeding into the converter through the anti-parallel diodes. The DC voltage can be deduced from equation (3-11) [55]: -

$$V_{ab} = \frac{V_{DC}}{2} - (L_{arm} + \frac{L}{2})\frac{di_{ga}}{dt} - V_a - R_c I_{cable} - L_c \frac{dI_{cable}}{dt} \quad (3\text{-}11)$$

The current can be expressed as [55]: -

$$i_{ga} = 2(\frac{V_{DC}}{2(L_{arm} + \frac{L}{2})}(t_2 - t_1) + \frac{I_{cable}}{3}) \quad (3\text{-}12)$$

Where V_{ab} = line-to-line arm voltage across phase-a and –b and L = phase reactance.

3.2.4. Protection of modular multi-level converters (MMCs)

Reviews [130], [162], [163] have analysed the transient behaviour of HB MMCs, with [28] also analysing a HB MMC pole-pole fault. Figure 3-10 shows a typical response of the HB MMC VSC-HVDC system with a rated DC voltage of 12 kV during a DC fault. It is considered that shortening the duration of stage 1 could reduce the overcurrent level significantly and benefit the recovery of the system. This means that if the fault detection is fast enough to provide a blocking signal for the SMs (before the IGBT self-protection), the overcurrent level of the system could be reduced significantly.

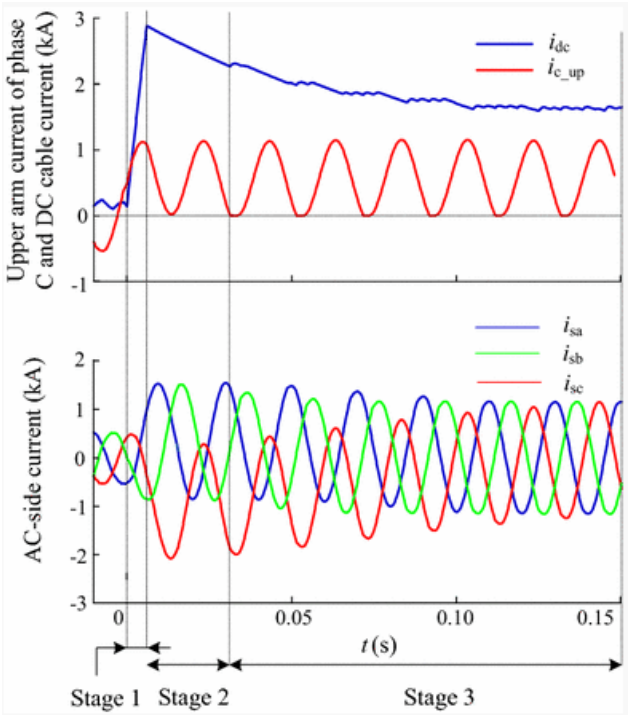

Figure 3-10: Process of DC short-circuit fault in an MMC based VSC system [28]**.**

Fast and selective DC line fault detection makes use of initial transient fault signatures [164]. During a DC fault, the duration of a transient signal mainly depends on the size of the inductors, as they determine the rate of change of current. The system's signature is characterised by the magnitude and duration of the fault current and can also be influenced by the type of fault and DC cable link as these are the main fault contributors in a MMC VSC system. Traditionally the detection and location techniques mentioned for 2-level conventional systems with appropriate adjustments, work just as well in MMC topologies [55]. AC or DC CBs are implemented to physically disconnect the converter from the AC grid to starve the fault. A solid-state DC circuit breaker (CB) may be used to overcome the DC-side problems in HVDC converters. Its main drawbacks, however, are cost and the relatively high conduction losses [165].

AC CBs may be used to achieve protection in point-to-point configurations. There is however a risk in depending only on AC CB protection since the semiconductor devices may be damaged due to high fault currents [81]. In most cases, literature suggests the implementation of fault limiters to assist HB MMCs at limiting or eliminating the contributions from the AC side [81], [120], [121]. These limiters allow HB MMCs to have characteristics that mimic the topologies with fault-ride through capabilities while maintaining its efficiency. Some of the widely popular fault current limiters proposed include a thyristor and a bypass switch at the AC side of the submodule [81]. The application is also extended to eliminate the use of a bypass switch and include two thyristor valves to reduce the transient of a fault [166].

Considering the total number of SMs in each arm is N, to successfully block a DC fault, the total number of SMs must be greater than 0.43N [130]. The voltage formed by half of the FB SMs is 0.5N in each arm. This means therefore that half of a FB MMC is sufficient to block a DC fault. Thus, to reduce the total number of power devices and losses, the remaining 0.5 submodules in a converter can be replaced by HB SMs [130]. A hybrid MMC VSC system has full blocking capability and therefore the protection scheme is designed differently to that of a system without fault blocking capabilities. A fault blocking converter eliminates the use of additional fault current limiters. The main attraction to converters with DC fault blocking capabilities is not only because they eliminate AC side contributions but also to take advantage of their quick recovery time from DC-side faults [30]. This means that DC breakers with lower current ratings can be used to isolate the faulty line and the AC CBs tripping can be avoided, a trait attractive especially for MTDC systems.

3.2.5. System configuration fault response.

Although considered as an influencing factor, the effect of a systems configuration on the fault response of VSC-HVDC system is a topic that has not been covered extensively in literature. When discussing fault response current literature usually makes the assumption that the configuration is monopolar [65], [69], [75], [87].

It is however worth noting that some present and mostly future HVDC grids are expected to develop into systems with a bi-pole configuration. This is mainly because bi-pole configuration offers increased flexibility and higher extensibility in developing HVDC grids [75]. In this sub-section, the impacts of a system configuration and the main contributing factors to the fault current during DC-side faults are evaluated. Similarly, the important factors to consider during this analysis include the magnitude and rate of rise of fault current.

3.2.5.1. Symmetric monopole

Monopolar configuration can be classified into two main categories; the symmetric monopole and asymmetric monopole. Amongst these the symmetric monopole is the configuration most used in VSC-HVDC systems and will thus be considered for this evaluation. A symmetric monopole is a single converter with mid-point ground between positive and negative voltage polarities as shown in Figure 3-11. The analysis of this configuration is the same as that described in Section 3.2.1 for 2 level converters.

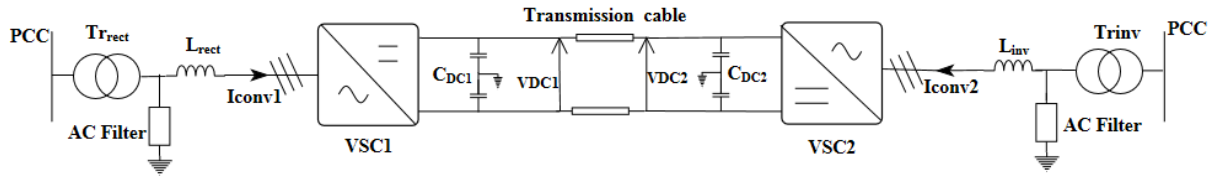

Figure 3-11: Symmetrical monopole configuration.

If a DC short-circuit fault has disrupted the normal operation of the network, IGBTs can be blocked for self-protection, leaving reverse diodes exposed to overcurrent [74]. During a short-circuit fault in a DC transmission line, the capacitor will be discharged rapidly. When fault occurs in DC-side, the IGBTs can be blocked for self-protection during faults, leaving reverse diodes exposed to overcurrent [82].

The fault demands that both converters should be blocked. It is evident in Figure 3-5 that the DC fault causes a very sharp rise in the DC current, putting the converters and other components of the system at the risk of failure. Figure 3-5 presented in the Section 3.2.1. for 2-level converters shows the graphical results of the fault current response of a monopole VSC system in case of line-to-line fault, resulting from previously developed dynamic models. Similarly, the main contributions are from the DC capacitors and energy storage elements in the transmission cable. Their size directly affecting both the magnitude and peak time of the fault current. In the case of a ground fault, the faulty pole is temporarily grounded. The contributions from the AC side are restrained through the freewheeling diodes therefore there is zero steady state fault current.

There are over-voltages at the healthy pole because of contributions from the DC capacitors that lead to a steeply increasing circuit breaker current [87]. If both cables and transformers are rated to operate under DC-link voltage stress, the link can be operated as asymmetrical monopolar. All monopolar configurations however lack redundancy as, in the case of a DC fault, all terminals are affected by the high fault currents. The main requirement for this type of configuration is therefore that the fault clearing techniques clear the fault before the end of discharging of DC capacitors to ensure that VSCs can continue their operation and resume power transmission.

3.2.5.2. Bi-pole

In this configuration, two asymmetric monopole systems may form a bi-pole system via series connections. Its structure is shown in Figure 3-12. It can achieve double power rating of monopolar topologies but unfortunately, it exposes the transformer to DC stresses. In a point-to-point bi-pole HVDC link a fault that is more likely to occur is between one converter pole and the ground. The healthy pole conductor can be used as the return path in case of the single pole outage. However, a low voltage dedicated conductor (metallic return) is required to operate as the return path in meshed HVDC grids [38].

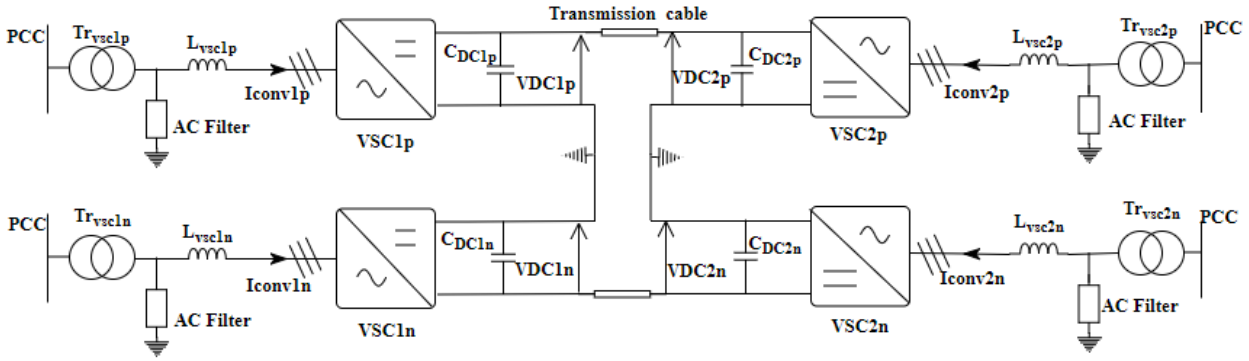

Figure 3-12: Bi-pole configuration.

In theory, the bi-pole configuration, is considered a more reliable and redundant technique favourable for implementation for future developments. Again, assuming that the bipolar system is mostly affected by single pole-to-ground faults, the healthy pole is still capable of transmitting at least 50% of the total active power, provided the power command to healthy VSC terminals is not reduced to zero. Furthermore, provided that the AC networks are sufficiently strong to tolerate the impact of DC faults while accepting additional power [38], [66]. This means that before, during, and after the fault, the positive pole converters operate independently from the negative pole converters. The redundancy of this configuration is however only valid if the system is only affected on one converter pole.

Should there be a rare case where both the converter poles are affected at the same time the entire system will be affected by the system threatening overcurrents as in the case of symmetrical monopoles [12]. Bi-poles are expected to give rise to much higher fault current levels due to the additional infeed from the AC side. The transients are also associated with the discharge of stray capacitors of the affected DC cables. As mentioned previously, not much has been covered in literature on the fault response of the bi-pole configuration as most evaluations assume that the system is monopole. Studies that have taken the initiative to address this issue are mostly limited only to ground faults [68], [86], [167], [168].

Wang [165] takes a different approach analysing DC fault in bi-pole HVDC grids, in particular taking unbalances and grounding relocation into consideration. The analysis is still however carried for ground faults. A representation of short-circuit faults is seen in the study of over-voltages by Jardini in [87]. This study proves by means of simulation that although the configuration is redundant, it also has limitations like in the case of a short-circuit fault. Protection scheme techniques for these systems remain primarily to detect, locate and isolate any potential threats to the system. In theory, for both configurations, during DC-side faults, the protection methods presented in Chapter 2 will apply for both configurations. The travelling wave method is still highly recommended for its speed and accuracy. To isolate the faulted sections during a DC fault, isolation techniques include the use of a DC CB. Additionally, AC CB are included to aid in protection, isolating the DC system in its entirety.

3.2.6. Summary

In view of the above discussion, depending on the type converter topology, the fault currents in VSC networks can be decomposed into contributions from various sources. In a network built from 2-level VSC converters, the first few milliseconds are dominated by the discharge of DC-side filter capacitors. This is followed by the discharge of adjacent transmission cables in the system. After the discharge period of the capacitive elements is over, the AC side infeed starts. In the case of MMC VSC converters, there are no inherent DC-side filter capacitors. Hence, the fault current is mainly contributed by the neighbouring cable connections and the converter submodule capacitor discharges. For these reasons, the resulting peak fault current magnitudes of an MMC are much lower than that of a 2-level VSC (i.e. when considering that the MMC operates under the same conditions as a 2-level system.

The converter submodule capacitor discharges can also be prevented by blocking each of the submodules in a converter. By using the freewheeling diodes as a path, after a converter blocks, the fault current is fed from the AC side of the nearby converters and from the other converters at remote terminals. These factors play a big role in influencing the magnitude of the fault currents rise time, peak magnitude and duration to steady state. Analysing these factors allows for unique identification of the signature of the fault and this is used to detect and locate the DC fault in the system.

Therefore, it may not be feasible to apply the exact protection scheme designed for a conventional system on the MMC as the signature of the fault (i.e. the shape and magnitudes of resulting transients) would differ and hence the protection scheme may fail to accurately confirm that the system has been affected by a fault. HB MMC are taking the lead and seem to be considered as the preferred topology for planned systems. Although these systems have their limitations they have characteristics which make them superior to conventional 2-level VSC.

This may result in the use of most technologies employed in the protection of 2-level VSCs ultimately being reduced or eliminated altogether. Essentially the principles applied in both topologies are similar. MMC technology can be improved by enhancing and developing the fault management capability by mixing it with other topologies. The mixing of different topologies with the systems control has not been explored extensively but might ultimately bring the best cost-effective solution for the protection of VSC-HVDC systems as presented in various studies [151]. This area of research could also be explored with the option of including or adding fault current limiters in conjunction with MMC as an attempt to block DC-side faults. Ultimately, the use of DC breakers is still regarded as a leading solution implemented to isolate only the faulty cable and interrupt the DC fault current. With this protective gear, although the principle is similar in both technologies, for systems based on the MMC topology the DC CBs with lower current ratings can be used to isolate the faulty line a solution that is both feasible and cost effective [169].

In theory, for a monopole or bi-pole topology, the marginal influence of a DC fault can be observed during the first few seconds, when the capacitive discharge dominates. Afterwards, the fault current increases gradually in a bi-pole due to the increasing AC infeed and it decreases to zero in the AC infeed blocking symmetric monopole configuration [68]. Moreover, the healthy pole in a symmetric monopole suffers less over-voltages than the bi-pole. The symmetrical monopole therefore seems to have less effect on fault current magnitude. Bi-pole configurations do however remain more favourable because of their redundancy a trait very attractive for power delivery in the industry.

3.3.The proposed protection method

3.3.1. The primary protection scheme

To devise a feasible protection scheme for VSC-HVDC systems, principles and protection requirements obtained during a systems fault analysis are utilised. These requirements dictate the need for a fast, selective, accurate and robust protection scheme. As briefly highlighted in Chapter 2, a protection scheme should be designed to have both primary and back-up protection for the system. The primary or main protection scheme is the main defender, whilst the back-up scheme aids in cases where the main defender is unable to operate for certain reasons [58], [170].

Detection and location methods are therefore designed and selected for either main or back-up protection depending on their ability to satisfy necessary requirements for the system. From the evaluation carried out in Chapter 2, some of these strategies include the implementation of the derivative protection method [67], [70] and the differential protection method [51], [171]. Others include the use fault blocking converters with mechanical isolators [44], [166], [172]. These protection strategies however need improvements in speed, selectivity or accuracy. To improve the accuracy of fault location in VSC-HVDC systems, it is vital to implement a scheme that will produce precise detection of wave front arrival times.

It is apparent from the literature review that the traveling wave (TW) protection method coupled with DC CBs is one of the most promising protection technique available [73], [173], [174]. The travelling wave fault location and detection technique has been used in many practical HVDC systems as the main protection scheme. It has numerous advantages that make it attractive for implementation in VSC-HVDC systems, including both speed and accuracy. These benefits have thus motivated for its use in this study. Section 3.3 will therefore further explore the theory of travelling waves, investigate its suitability for the protection of a MTDC VSC-HVDC system and analyse an appropriate back-up protection strategy for the system. The hybrid DC CB is then evaluated for effective isolation in the system. An overall protection algorithm is finally presented as a block diagram at the end of the section.

3.3.1.1. Travelling wave theory

The concept of travelling wave protection (TWP) was briefly introduced in Section 2.4.2.2.1. According to the theory, the characteristics of a wave front, resulting from a transient in the system can be used to detect a fault [153]. This theory stems from the principle that states that the development of a DC fault triggers waves to propagate in the DC cable in an opposite direction (i.e. away from the DC fault) [175] as shown in Figure 3-13. In this diagram, the waves are initiated due to a fault f1 located at distance X_F away from terminal A and the resulting waves travel at a constant velocity denoted by v.

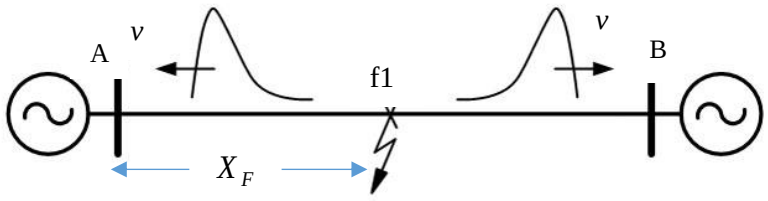

Figure 3-13: Travelling waves caused by fault.

Travelling waves are caused by changes in stored energy [144]. When the waves reach the VSC station, they are refracted and reflected according to the refraction and reflection coefficients [153], [176].

The characteristic impedance of the DC cable can be used to determine these coefficients. Alternatively, the equivalent impedance of the VSC station can be utilised. To detect a fault using this method, a sample of instantaneous voltage and current are continuously taken. These are given by equation (3-13) and (3-14) [67], [70]: -

$$V_0 = \frac{2Z_t}{Z_t + Z_c} V_i = K_{rv} V_i \qquad (3\text{-}13)$$

$$I_0 = \frac{2}{Z_t + Z_c} V_i = \frac{2Z_c}{Z_t + Z_c} I_i = K_{ri} I_i \qquad (3\text{-}14)$$

Where Z_c = characteristic impedance of cable = $\sqrt{L/C}$

Z_t = equivalent impedance of converter station (where fault is terminated)

V_i / I_i = incidence or forward for voltage and current respectively for the travelling wave

K_{rv} = refraction coefficient for voltage travelling wave

K_{ri} = refraction coefficient for current travelling wave

A lattice structure shown in Figure 3-14, is used to locate a fault when using the TWP method. Assuming that the transmission line between converter A and B is lossless, f1 represents a DC fault in the system, Vb1 represents the backward voltage and Vf1 represents the forward voltage. The calculation procedure for fault location differs with the type of travelling wave protection method implemented (i.e. whether single ended (Type A) of double ended (Typed D)).

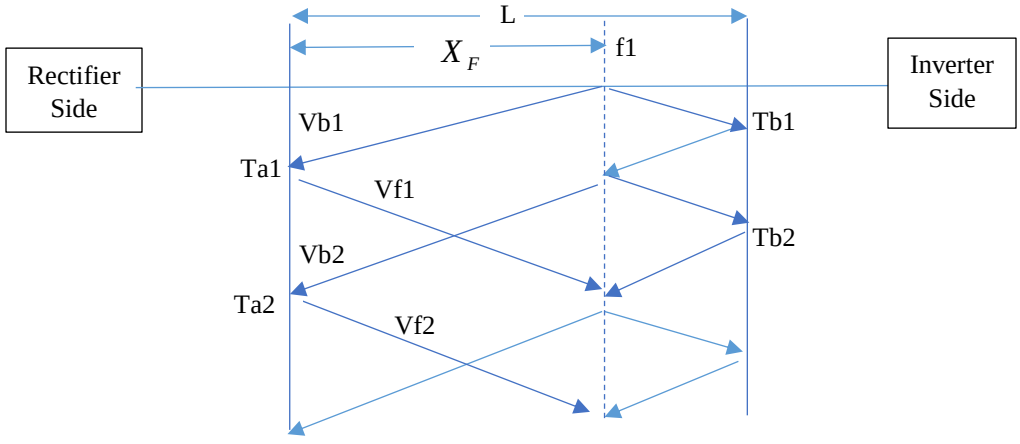

Figure 3-14: Lattice structure resulting from fault [70], [177]**.**

The location of a fault is typically calculated using the time difference between the arrival times of the fault induced initial wave surges [98]. In the diagram Ta1 represents the first-time arrival at terminal A and Tb1 represents the first-time arrival at terminal B. For a single-ended method, DC line fault location can be calculated as shown in equation (3-15) [67]. X_F represents the fault distance from the converter station and v represents the wave velocity.

$$X_F = \frac{(T_{a2} - T_{a1}) \times v}{2} \tag{3-15}$$

As already mentioned, the location of a fault can also be approximated using the double-ended method. Its general expression is shown in equation (3-16) [67]. In this case, L represents the full length of the transmission line between converter A and B.

$$X_F = \frac{(L - (T_{b1} - T_{a1}) \times v)}{2} \tag{3-16}$$

Contrary to the double-ended method, analysis of the single-ended method is regarded as more sophisticated [95]. As shown in equation (3-16), the double-ended method is based only on timings from the initial wave surges and hence the characteristics of the reflected waves are not included in calculations as with the single-ended method. The double-ended method does however require an accurate and easier way of bringing the measurements from the two terminals to a common point [67]. This increases the detection and location time, an undesirable property for VSC-HVDC systems. Because of the delay in time, the single-terminal method is chosen for applications where short operation times are listed as a requirement.

One of the shortcomings of conventional TWP techniques is that they are highly affected by fault resistance. At a fault point, high resistance attenuates the magnitude of the traveling wave, making the signal too weak for detection [61]. This affects and reduces the methods accuracy. These methods are also not sensitive to faults over long fault distances (i.e. distances greater than 200 km) [83]. This is mainly due to their inability to calculate the wave propagation of a traveling wave, due to the lack of suitable mathematical tools. To improve conventional methods, literature proposes the use of the wavelet transform for accurate identification of the wave front [175]. The single-ended or double ended techniques are still however entrusted to locate the faults inception point. Wavelet analysis is a mathematical tool used typically for signal processing. The method has the ability to detect abrupt changes in a system, and can therefore be applied to effectively overcome difficulties of the traveling wave protection techniques [16], [94], [178].

The following section will review the brief theory and operating principles of the wavelet TW protection method, focusing on the discrete wavelet transform (DWT) technique for fault detection and the single ended method to fault location. The aim is to discuss how this protection technique can be developed in order satisfy the requirements of effectively protecting a VSC-HVDC system.

3.3.1.2. The wavelet analysis

Wavelet analysis is a signal processing method that is suited to detect abrupt, local changes in a signal (e.g. transients in a power system) [179]. This technique is executed using a transform. A wavelet transform is used to extract fault features of a travelling wave that would aid in the detection and the elimination of a fault on a system. Unlike conventional signal processing tools (i.e. Fourier transforms), the wavelet transform has the capability of time location and frequency location simultaneously during the signal analysis [95], [179]; thus, it is widely employed to detect travelling waves. The analysed signal is decomposed into different scales using a wavelet analysing function called 'mother wavelet'. This wavelet is scaled and translated to match an input signal locally. The subsequent calculated wavelet coefficients represent the correlation between the (scaled) wavelet and the signal [158].

The accuracy of the wavelet traveling wave based fault detection and location methods are proven to be more accurate than conventional TW techniques [177]. However, the feasibility of these methods highly depends on the accurate detection of the wave heads at the terminals of the transmission line. In cases where the measurements at the terminals of the transmission line fail to identify the wave heads, the method is ineffective. To identify the wave head successfully, a high sampling frequency of data is required [101]. This technique has made a great contribution to traveling wave based fault identification.

a) Wavelet transforms

A wavelet transform is a linear transformation mathematical analysis tool. It analyses a signal by means of scaling and translating (shifting) the original wavelet. The method is expressed by equation (3-17) [95], [177], where the translation parameter is represented by u and the scaling factor is represented by s. For each 'mother wavelet' φ, a family of wavelets can be obtained by scaling φ by s and translating it by u.

$$\varphi_{u,s}(t) = \frac{1}{\sqrt{s}} \varphi\left(\frac{t-u}{s}\right) \qquad (3\text{-}17)$$

A wavelet transform can be categorised into either a continuous wavelet transforms (CWT) or the discrete wavelet transform (DWT). The different techniques have their own strengths and limitations and are desirable depending on a specific scenario.

The CWT technique is regarded as more reliable, accurate and effective. It is however consumes memory and time, and is thus not considered as the best technique for fault detection [180]. The DWT technique has a digitalised wavelet transform, making it more viable in fault detection [181]. A few references also acknowledge a third class of wavelet transforms, referred to as the stationary wavelet transform (SWT) [95], [96], [182]. It is widely applicable in systems that require denoising. In addition, the SWT has constant translational parameter so that the transform obtained from different lines are compared without shift in time [27].

The application of a wavelet transform that will detect DC faults in a VSC-HVDC system is of interest for this study. The DWT wavelet-based fault detection method is therefore used in the analysis and detection of DC faults. The main focus is fault detection, DWT can however also be used for exact fault location estimation by looking at the time interval between subsequent events, i.e. the properly selected reflections [181]. However, this estimation fails for long cables due to the high attenuation produced by the cable itself to differentiate faults within or outside the protection zone.

b) Discrete wavelet transform

The discrete wavelet transform (DWT) is an implementation of the wavelet transform using a discrete set of the wavelet scales and translations obeying some defined standards [93]. This transform decomposes the signal into mutually orthogonal set of wavelets. DWT can be decomposed into the same or lower number of the wavelet coefficient spectrum as is the number of signal data points. These wavelet spectrums are good for signal processing and compression. The discrete wavelet transform can be expressed as in equation (3-18) [36], [181]:

$$DWT(m,k) = \frac{1}{\sqrt{a}} \sum x[n] g[\frac{k-b}{a}] \qquad (3\text{-}18)$$

Where x[n] represents the mother wavelet, a and b are functions of an integer parameter m, $a = a_0^m$ and $b = na_0^m$. The result is a geometric scaling that is $1, \frac{1}{a}, \frac{1}{a^2}$ and translational by 0, n, 2n…. etc. The mother wavelet is a function which decays fast at the edge and has zero average in a short time [36]. There are various families of mother wavelet available. They include: -

- Haar wavelet, shown in Figure 3-15a is often recognised as the first known wavelet basis. The Haar wavelet is the simplest type of wavelet and resembles a step function.
- The Daubenchies (db) wavelet is a modified version of the Haar. It is a more viable option, as suggested in reference [183]. The 4th order Daubenchies (db4) wavelet is shown in Figure 3-15b.

- The Symlets is a modified version of the db wavelets. Figure 3-15c shows an 8th order Symlet.
- Coiflets are another variation of db wavelets. It is shown if Figure 3-15d.

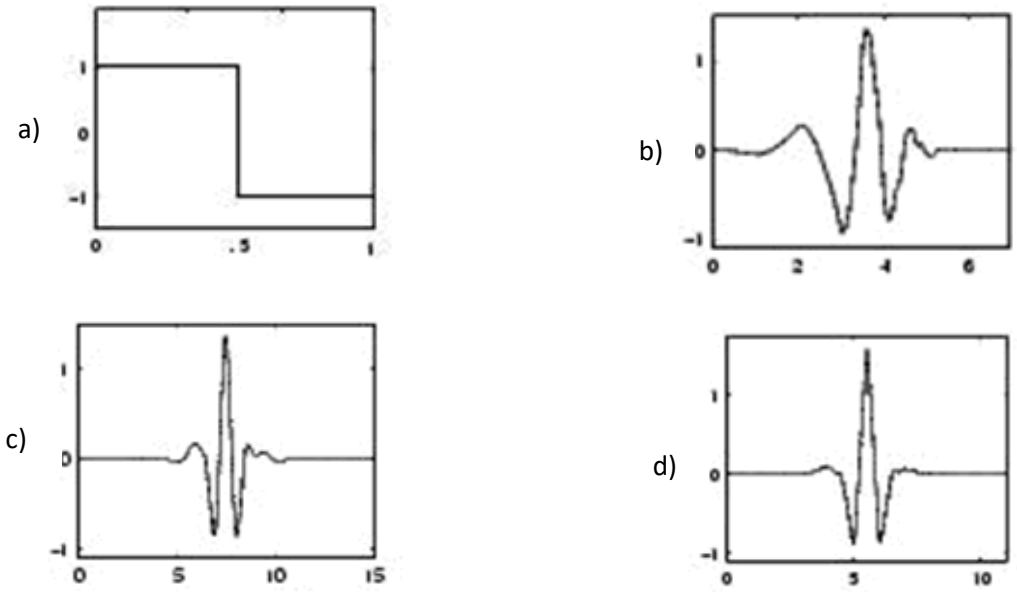

Figure 3-15: Mother wavelets where a) Haar wavelet, b) is the Daubenchies (db) wavelet, c) is the Symlets wavelet and d) is the Coiflets wavelet [36]

The filter bank configuration shown in Figure 3-16 was used to implement the wavelet transform based on the DWT technique [36]. The DWT signal (x) is calculated as an output that has passed through several low-pass filters (L) and high-pass filters (H). The outputs (Y) produce results of the approximation coefficients and detailed coefficients. This is denoted in equation (3-19) and (3-20) [36].

$$Y_{low}[n] = \sum_{-\infty}^{\infty} x[k]L[2n-k] \qquad (3\text{-}19)$$

$$Y_{high}[n] = \sum_{-\infty}^{\infty} x[k]H[2n-k] \qquad (3\text{-}20)$$

The resulting sampling frequency is usually halved since half the signals have been removed. This results in resolution time being doubled, and therefore each output should have a doubled frequency resolution [67]. A second layer of approximation and detailed coefficients can be obtained if the low pass filter is further passed. The decomposition process for the high frequency spectrum can be repeated numerous times to further increase the frequency resolution [36], [67]. A 'filter bank' otherwise known as a binary tree is as presented in Figure 3-17.

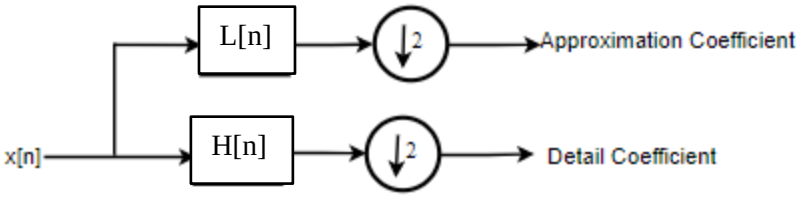

Figure 3-16: Block diagram if filter analysis [67]**.**

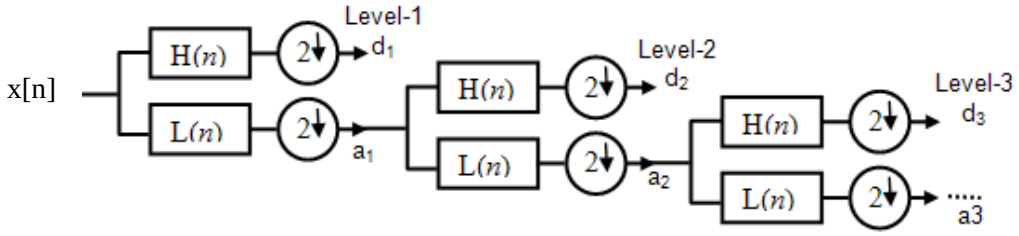

Figure 3-17: Block diagram of filter bank [36]**.**

Figure 3-18 shows a flow diagram of the implementation of the DWT. The travelling wave fault detection scheme depends only on local measurements, and it is based on measured DC currents. The fault generated travelling waves consist of a wide range of frequencies, and the propagation speed of each frequency component is different. Typically, the highest frequency components will reach the relay first. The DWT method needs a few decomposition levels since only the highest frequencies are needed to detect the fault.

Once all coefficients are obtained, the wavelet energy coefficient can be calculated as in equation (3-21) [178]:

$$WTC^{2} = \sum_{k=1}^{n} d_k^2 \qquad (3\text{-}21)$$

Where WTC^2 is the sum of the squares of the wavelet transform coefficients, d_k is the k-detail wavelet coefficient and n is the decomposition of level in the wavelet transform. The travelling wave method monitors if the wavelet energy is in excesses or within the predefined threshold. A DC fault is identified if WTC^2 is exceeded. A trigger signal should be sent to the isolators of the system to isolate the faulty section from the rest of the system.

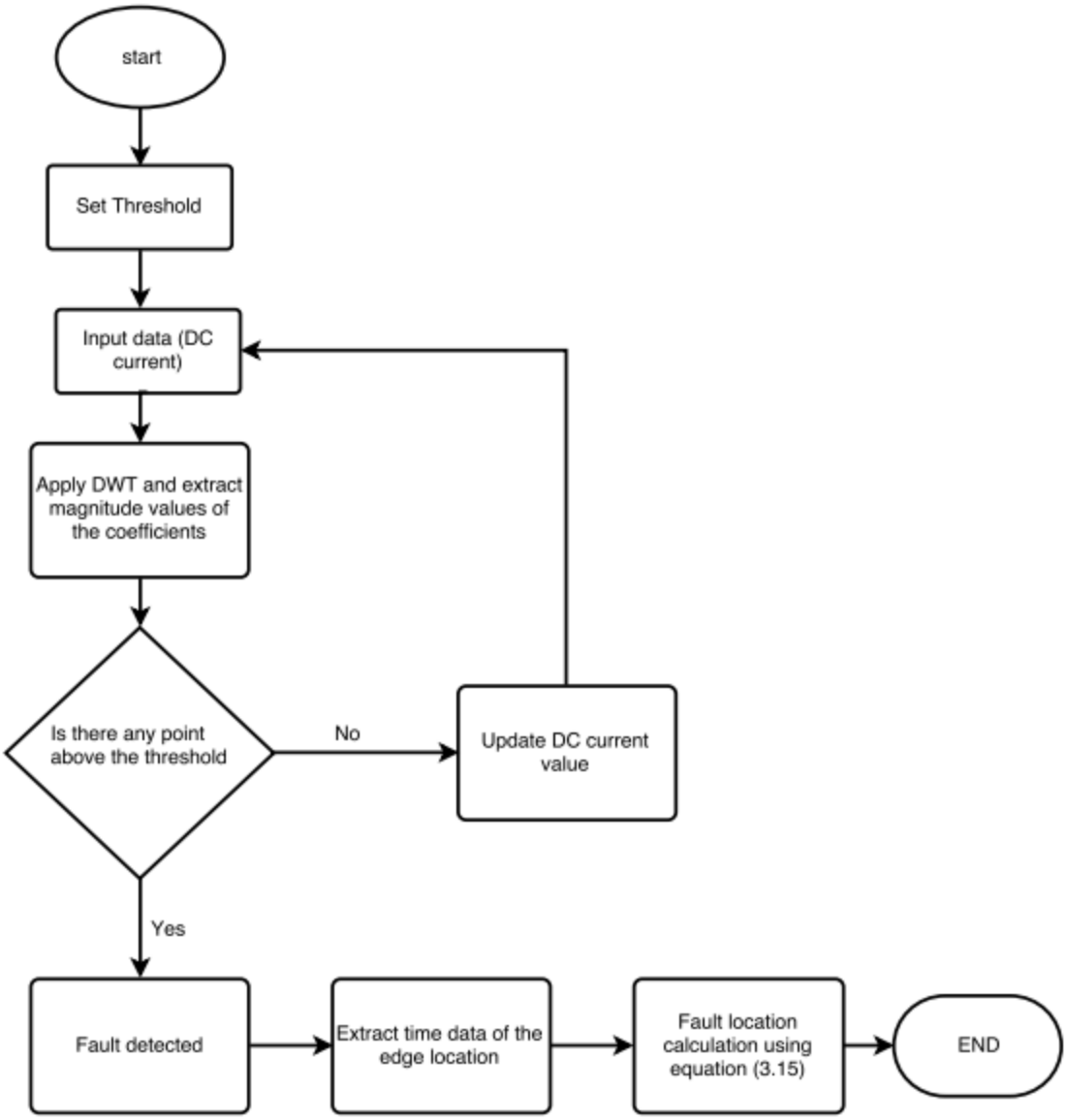

Figure 3-18: Implementation of the DWT on a VSC-HVDC system.

The occurrence of a DC fault on a VSC-HVDC cables results in steep DC current wave. The DC current can be further used to determine the arrival time of the travelling wave. When assuming that information of the faulty DC line is gathered correctly, the DC fault location can be estimated by using velocity of the wave velocity and arrival times.

a) Wave velocity

Wave velocity (v) is mainly relies on the transmission cable property. It is calculated by equation (3-22) [67]: -

$$v = \frac{c}{\sqrt{LC}} \qquad (3\text{-}22)$$

b) Arrival time(s)

Arrival times are found using the current derivative calculated from the measured DC currents. The arrival of the wave front considered during location are only those above the derivative threshold. This value can be read from the corresponding plots. A MATLAB code is however developed for precise location.

3.3.2. Back-up protection

Back-up protection is usually included to strengthen the protection scheme of the network. The algorithm should be just as fast and selective to ensure the reliability of the network. Possible back-up methods are detailed in this sub-section and include:-

- The overcurrent protection method.
- The differential protection method.
- The derivative protection method.

3.3.2.1. Basic principles of overcurrent protection.

The overcurrent detection technique is very reliable and represents a mature and simple technology. Figure 3-19 shows a flow diagram of the general operating principle of overcurrent protection. The overcurrent protection method uses the magnitude of current or voltage to measure or detect if a DC fault has occurred. The system trips if the measured current has exceeded the set threshold [12]. Overcurrent protection is however limited by its lack of selectivity.

It is therefore used mainly in cases where the primary detection scheme fails to perform its function, which is regarded as back-up protection. The technique's very low degree of selectivity also constraints its application in multi-terminal systems or DC grids. This then immediately eliminates its possible use in this project, as the developed model is a MTDC VSC-HVDC system.

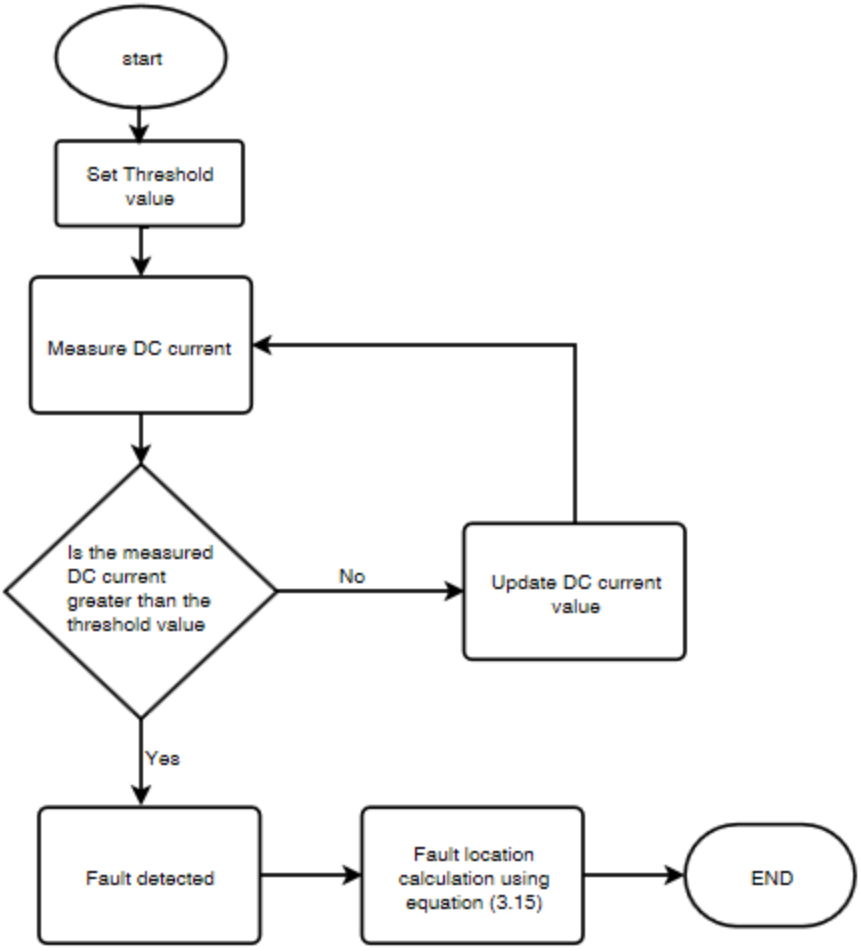

Figure 3-19: Overcurrent protection method.

3.3.2.2. Differential protection

One of the most reliable techniques in power system protection is differential protection. The operating principle of this technique is to calculate the difference between the current entering and leaving the protected zone. This information is relayed to the converter stations via a telecommunications structure. Differential protection is admired for its ability to protect a system selectively. This kind of selectivity exploits the principles of Kirchhoff first law at the node, where the sum of the currents in a node must be equal to zero, if the summation of the currents is different from zero it means there is a fault [91].

In a VSC-HVDC system, although Kirchhoff's principle is still applicable, it should be noted that when a fault occurs on the DC cable, the DC current flowing through one end of the cable differs from the current flowing at the other end. This is a consequence of the resulting wave attenuation found in long distance DC cables and the communication delay [67]. VSC terminal arrangements or topology could also be a possible cause of unequal fault currents at faulty cable ends.

The algebraic sum (or difference calculated) will sometimes have an offset value not equal to zero. The value is used to detect DC faults. For this technique, the resulting difference is compared to a threshold for selective DC fault identification. If a part of the system exceeds the set threshold for a predefined time the protection is set to be enabled to isolate the faulty equipment from the rest of the system.

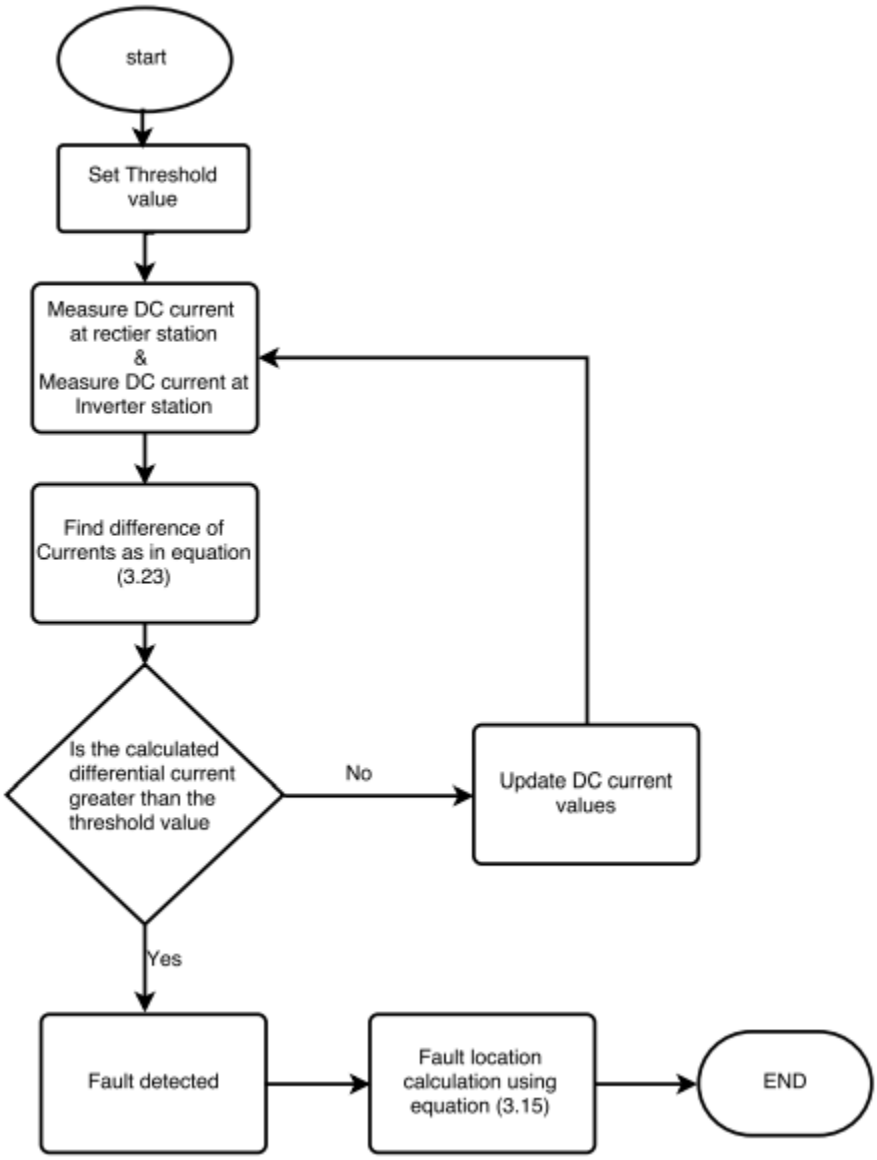

Figure 3-20: Differential protection method.

A flow diagram applying the principle of this method is shown in Figure 3-20. During a DC fault, the cable differential current value increases quickly and reaches a large positive value. This can also be used as an indication of the faulty cable since all healthy cable will measure a negative differential current after the fault.

Differential currents measured at all cable breakers are then compared with a positive threshold to detect the fault location. The differential current equation is represented by equation (3-23) where $i_{\_diff}$ is equal to the-real-time local measurement $I_{DC\,rect}$ and $I_{DC\,inv}$ represent the DC current from the rectifier and inverter VSC terminals respectively and t_0 represents the initial time of the system [70].

$$i_{\_diff} = I_{DC\,rect}(t_0) + I_{DC\,inv}(t_0 - 1ms) \qquad (3\text{-}23)$$

Unlike most mentioned detection techniques, the differential protection is highly selective. However, information from each converter must usually be transferred between two ends of the DC cable. For very long cables, the sensitivity of the technique is lowered. The response time increases due to the increased communication time. Errors in the communication system also contribute to the schemes vulnerability. The lack of selectivity and prolonged time delay are also undesirable characteristics for a MTDC systems and so the protection strategy has not been selected for implementation in the developed MTDC VSC-HVDC system.

3.3.2.3. Derivative protection.

Current or voltage derivatives have proven to be very useful in HVDC protection, particularly for the location of faults in a system. To detect a fault through derivative protection, a calculated threshold magnitude is compared to the sum of the measured current and voltage derivative. The process is shown in the flow diagram in Figure 3-21 [184]. A trip signal is triggered if the resulting derivative magnitude exceeds the set threshold. The current derivative is usually the only input used for determining faulted DC cable. Since voltage is usually measured at each DC bus for each VSC station, its results are no good indication of locating the DC cable that is faulty. DC-link capacitors closer to the fault are the station components that first get discharged during a DC fault. They contribute the most to the fault current. Because of the large change in the current of the faulty line, the current derivative is higher for the faulty line than for the rest of the network [70].

A DC fault very close to the converter yields higher derivative magnitudes. The detection of faults using the technology is also quite fast. This complies with the requirements of the protection system that state that VSC stations closest to DC faults are the most vulnerable and have a short reaction time. The biggest advantage of the derivative protection technique over the mentioned possible back-up protection strategies is its ability to be selective. In this method, the sign of the current derivative points to the fault location. A derivative magnitude with positive polarity means the fault is in the designated protection area. A negative derivative magnitude on the other hand indicates a fault is located outside its assigned zone of protection [83].

The main advantage of derivative protection is its detection speed and selectivity. The location method is however very sensitive to noise [11]. To determine the relevant threshold settings, detailed network studies are to be carried out to ensure that the protection scheme implemented is stable for all other disturbances except those that affect the DC line. For the implementation of derivative protection, the line currents and their derivatives during a fault are simulated beforehand. The current derivative thresholds must be evaluated based on the system parameters and are different for different topologies. These threshold values depend greatly on the cables and the DC-link capacitor size.

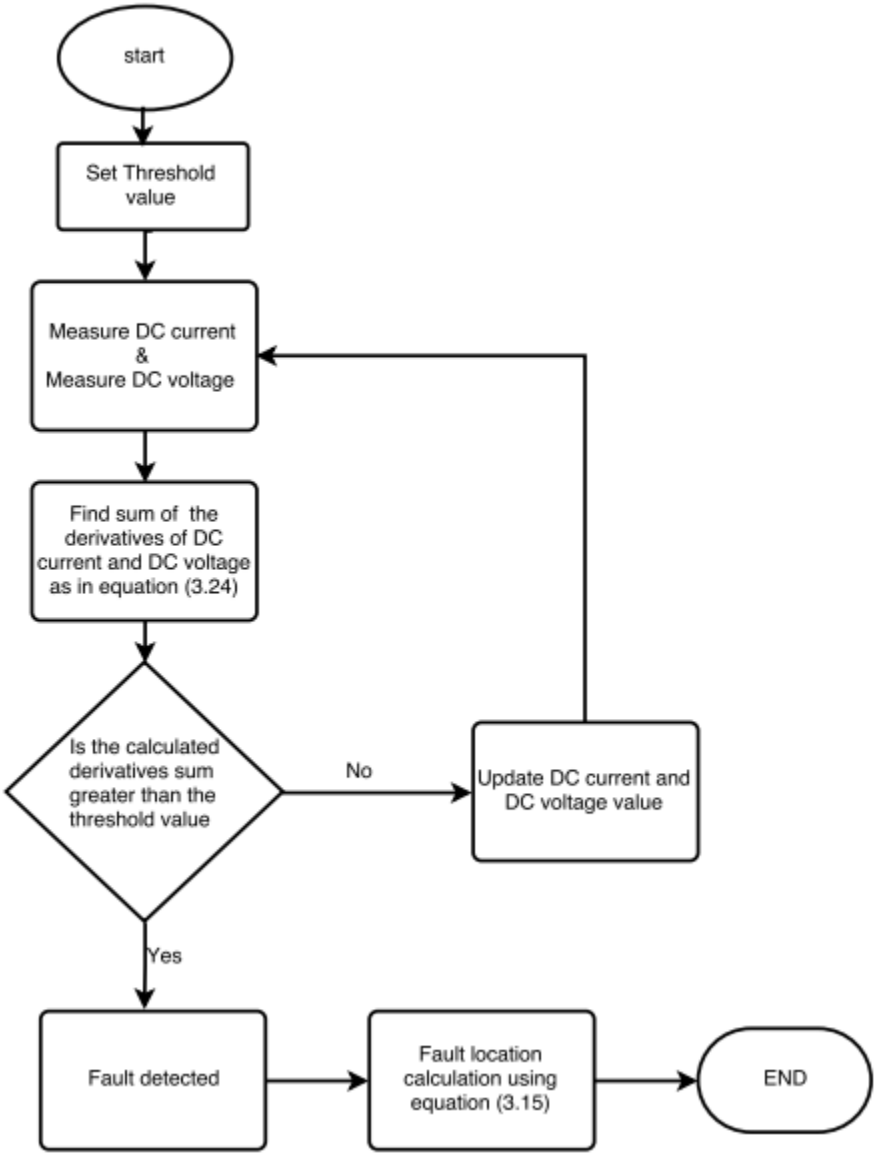

Figure 3-21: Operational process of voltage derivative protection.

A weighted sum of the derivatives is calculated using equation (3-24). The weight of current derivative is represented by K_1 and voltage derivatives by K_2. K_1 is typically rated at 1 and K_2 at 0 [83]. This implies that only the current derivative contributes to the weighted sum when determining a faulted cable.

$$\in = (K_1)\frac{dI}{dt} + (K_2)\frac{dV}{dt} \qquad (3\text{-}24)$$

3.3.3. Isolation methods

The isolation of faults has thus far been implemented with AC and DC protective switchgear such as circuit breakers (CB). An arc is usually formed when interrupting current by separating two conductors [26], [46]. This is usually naturally extinguished at the current zero crossing for AC networks. These devices have an advantage of being the more mature technology with lower costs and shorter lead time. Therefore, even with the development of HVDC systems AC CBs have remained the most active isolation method used. Their biggest disadvantage is that the method involves slower fault clearing time and momentarily disconnecting the entire system and then clearing the fault before reconnection.

The MMC topology if implemented would perform current interruption, thus decrease the time required to clear the DC fault. The entire VSC-HVDC system would still need to be taken offline momentarily to isolate the DC fault. This is an undesirable trait especially for use in MTDC systems. In such networks, DC switchgears are considered as a better solution. This is mainly because they can interrupt the constant DC current faster than available AC devices. The most relevant DC isolation devices available are DC CBs. They are installed to isolate the non-zero crossing DC current. This is usually achieved by forcing the current to zero in order to interrupt the faults [71], [103]. A DC CB should also be responsible for dissipating the systems store energy and must be able to withstand the voltage response of the network after current interruption [34].

3.3.3.1. Hybrid CB

As presented in Figure 2-7 of Section 2.4.3.3., the hybrid DC CB consists of a combination of mechanical switches and semiconductor devices. The branch labelled (a) is a bypass branch formed by a semiconductor based load commutation switch (LCS) in series with a fast-mechanical disconnector. The LCS is a solid-state breaker with sufficient breaker cell to commutate the current into the main breaker branch. During normal operation, the current will only flow through the bypass, and the current in the main breaker is zero. [132]. When a DC fault occurs, the load commutation switches immediately commutate the current to the main DC breaker and the fast disconnector opens. The hybrid CB can overcome conduction losses by allowing nominal current under normal operation to flow through the path of branch (a) [25].

The main CB component contains arrester banks that are dimensioned for full voltage and current breaking capability. The load commutation switch on the other hand matches lower voltage and energy capability[72]. The main CB also controls the voltage drop across the HVDC reactor to zero to prevent a further rise in the line current. The response signals of the hybrid HVDC breaker as shown in Figure 3-22. The maximum duration of the current limiting mode depends on the energy dissipation capability of the arrester banks. In the case of a breaker failure, the back-up breakers should be activated almost instantaneously, typically within less than 0.2 ms [26].

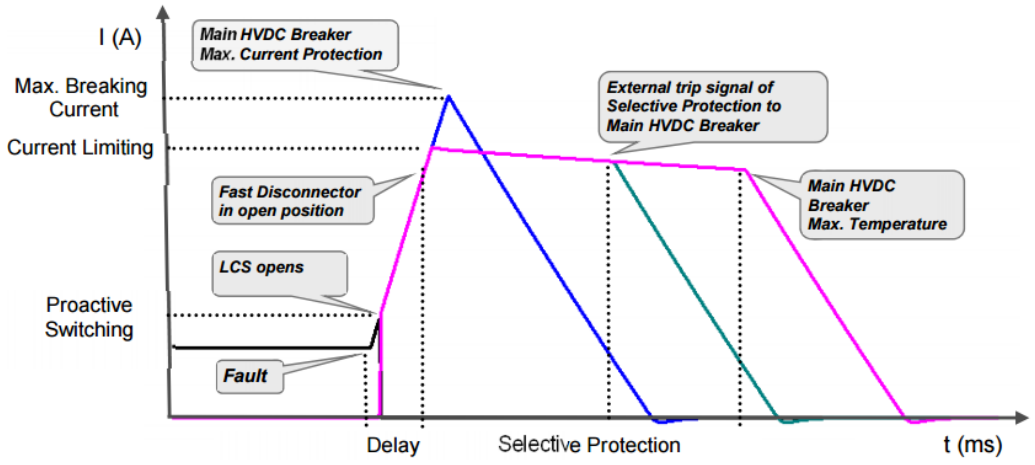

Figure 3-22: Proactive response of hybrid HVDC breaker [26].

Due to the proactive mode in hybrid DC CBs, initially, overcurrents in the line are expected to activate the current transfer from the bypass into the main HVDC breaker. This is activated prior to the trip signal of the back-up protection [46]. This is to avoid major disturbances in the HVDC grid, and keep the required current-breaking capability of the back-up breaker at reasonable values. Back-up CBs used can also include the implementation of AC CBs or mechanical isolators. The implementation of mechanical Isolators would however require an increase in the size of the converter station as each of these would need to be positioned on each side of the DC cable as with the hybrid DC CBs [127]. The AC CBs in this case offer a better solution for back-up protection. The implementation of AC CBs would however mean that the failure of DC CBs would result in the entire isolation of the AC grid and system converters.

3.4. Implementation of proposed protection algorithm

The proposed algorithm scheme is composed of two units responsible for fault detection and two units implemented for isolation purposes. To locate the position of the fault, equation (3-15) represented in Section 3.3.1.1 is used. The travelling wave-based unit was used as the main protection strategy, whilst the derivative method was used as its back-up method in fault detection.

To isolate the faulted cables the main isolating switchgear implemented in the system are DC CBS. For extra pre-caution, these are also coupled with a back-up strategy to be used in cases where the DC CBs are faulty or are going through maintenance. The back-up isolation gear implemented is the AC CBs. Although the method has been discussed as undesirable for the main protection of MTDC VSC-HVDC systems, its use for back-up protection is only in emergency situations and when all other implemented protection strategies have failed to work. It is therefore assumed that the system is in danger and that the best solution would be to isolate it entirely from the AC grid. During the design of the implanted protection algorithm, the following assumptions were made:

- Both DC voltages and DC currents are measured at relatively high sampling frequency
- Only single-ended measurements are available, i.e. the communications at cable level are considered unavailable.
- The threshold values are different for the DWT travelling wave and the derivative method.

A flow diagram representing the protection algorithm is shown in Figure 3-23. In the figure, the following are assumed: -

- In the main protection DWT represents the discrete wavelet transform coefficients.
- In back-up protection X represents standard multiplication and $\frac{d}{dt}$ represents taking the derivative of the input signal.
- The output resulting from the comparison between DWT / summation and the system threshold is represented as Ans.
- Ans is expected to either be the value 0 or 1.
- If there is a fault in the system Ans is expected to be equal to 1.
- Due to possible failures in the main protection scheme, Ans can be 0 even when there is a fault in the system.
- During this case, a switch enables the operation of the back-up derivative protection strategy.
- The switch is also designed to produce either an output of 1 or 0. It ensures that only one detection protection strategy operates at a time.

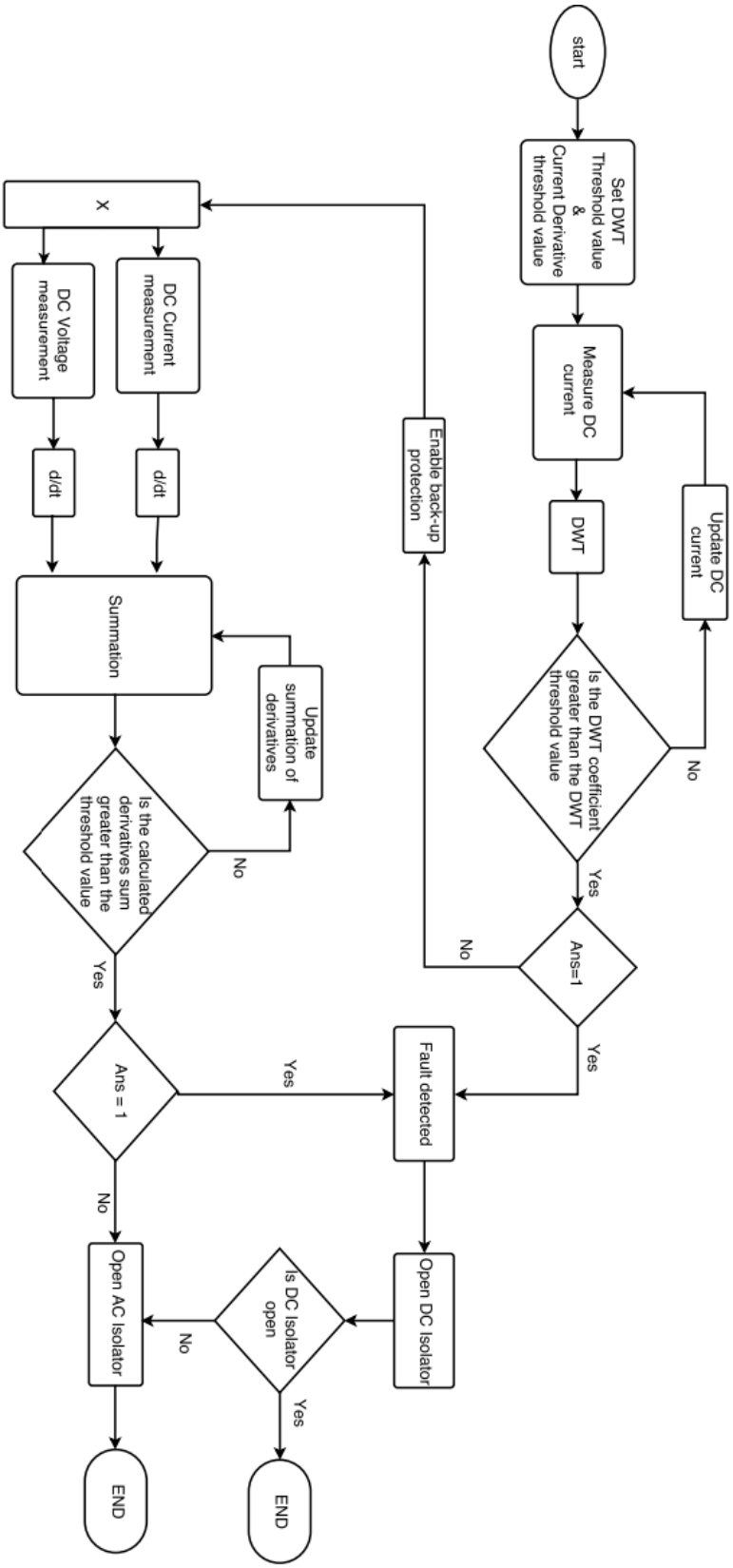

Figure 3-23: Flow diagram of proposed scheme.

CHAPTER 4: VSC-HVDC PROTECTION SCHEME ON PSCAD

4.1. Introduction

In the first part of Chapter 4, a description of the MTDC VSC-HVDC model, its parameters and control techniques are detailed. The latter part of the Chapter then deals with the proposed VSC-HVDC protection schemes that were implemented in the developed network. This includes the simulation models of the main detection and isolation protection unit as well as the back-up protection unit. The models provided a base platform and could be utilised for further studies in various other projects relating to the protection of VSC-HVDC systems.

4.2. PSCAD/EMTDC and simulation

The basis of this thesis is the evaluation of a protection scheme for VSC-HVDC transmission systems. This inherently requires an extensive study of DC transients. The simulation studies and results obtained for different types of DC-side faults are thus investigated using PSCAD. The Power System Computer Aided Design abbreviated as PSCAD, is considered as an effective tool for power transient simulations. PSCAD also has a good reputation in advanced HVDC cable modelling and DC fault transient simulation. This has thus been a motivation for selecting the tool for this study.

4.3. VSC-HVDC system model

With reference to available VSC models like the one developed by CIGRE [185], a 4-terminal, VSC-HVDC test model that can interchangeably send or receive power was developed. The test model could be categorised as a radially meshed MTDC system with a symmetrical monopole configuration and adopts the 2-level converter topology. To transmit power from one converter to the other, the system made use of underground DC cables. Due to the symmetrical nature of the system, the DC cables with positive and negative voltage were designed to be identical.

The DC cables were installed in conjunction with DC breakers whose function was to protect the system by interrupting potential high peak DC fault currents that might threaten the healthy operations of the network. In addition, AC CBs have been installed on the AC side of the converters as a back-up isolation technique in cases where the DC breaker is unable to perform its duties to ensure reliability of the network. The system was designed to transmit a DC voltage of about ±400 kV. The DC currents were measured in each CB while the line-to-line voltage was measured between two poles at each VSC station.

During steady state, station VSC1 and VSC4 were set to control voltage while VSC2 and VSC3 control the power flow. Figure 4-1 shows the system's VSC single line diagram model with a zoomed view of VSC1 and its direct connections shown in Figure 4-2. In Figure 4-3 a schematic diagram with a detailed view of the inside of the converter unit is shown. In this case the rectifier converter unit is shown. However, all converter units were made identical. The specifications for the VSC-HVDC system under study are given in Table 4-1.

Table 4-1: Specifications of MTDC VSC-HVDC model under study.

VSC-HVDC SYSTEM SPECIFICATIONS	
Configuration	2-level Symmetrical monopole
Grid Voltage VSC1 and VSC3	±420 kV
Grid Voltage VSC2 and VSC4	±500 kV
AC frequency VSC1 and VSC 4	60 Hz
AC frequency VSC2 and VSC 3	50 Hz
DC voltage	400 kV
Active power (P)	200 MW
Transformer ratings	Star/star connection Vprim VSC1 and VSC3 = 420 kV Vprim VSC2 and VSC4 = 500 kV Vsec = 230 kV S= 1500 MVA
System AC filters	q = 25 $Freq_{base}$ = 60 Hz (VSC1 and VSC4) $Freq_{base}$ = 50 Hz (VSC2 and VSC3) Q = 5 MVar
System phase reactors	R = 0.015 Ω = 0.005 pu L = 0.002 H = 0.26 pu
DC capacitance	C= 300μF

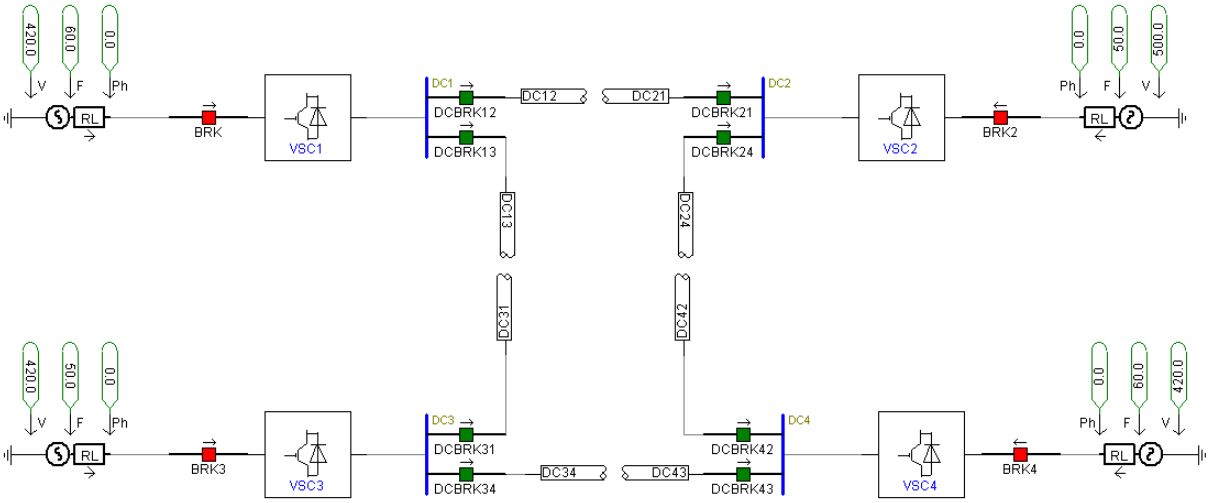

Figure 4-1: Single line diagram of the 4-terminal VSC system developed.

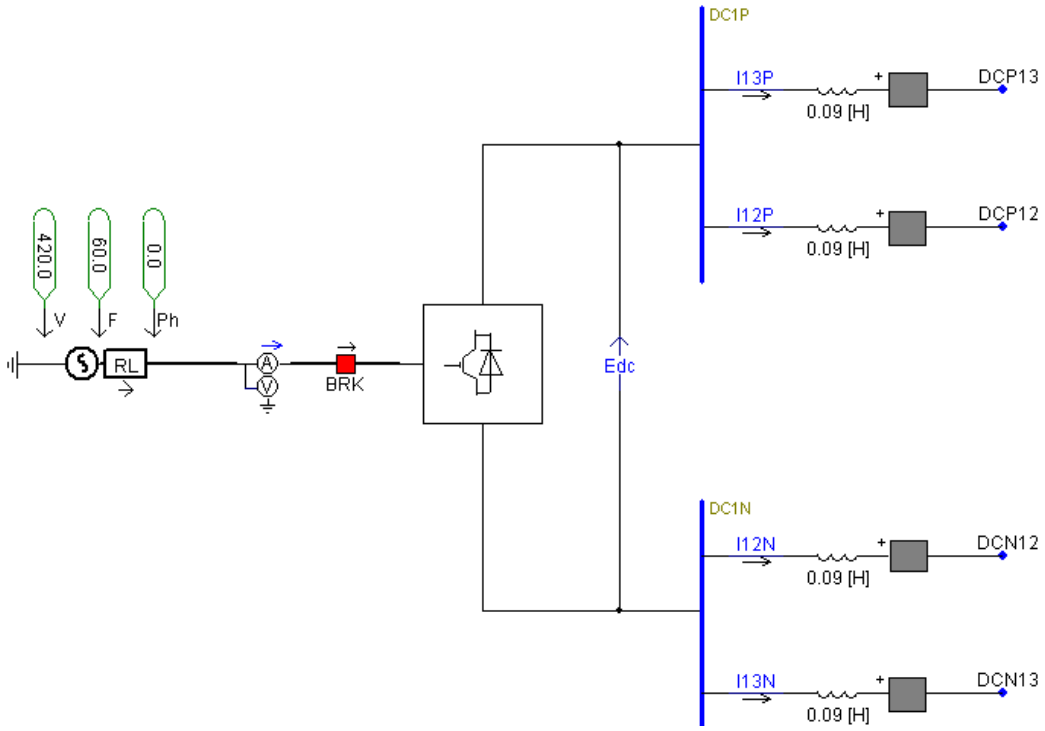

Figure 4-2: VSC1 of the 4-terminal VSC system developed.

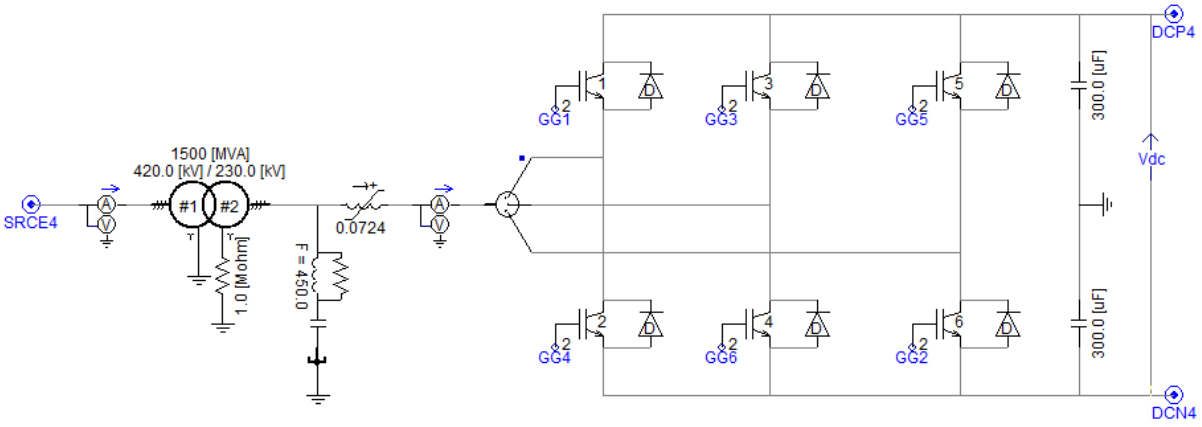

Figure 4-3: Rectifier side of VSC-HVDC scheme on PSCAD.

4.3.1. Voltage source converter unit

The developed system used series-connected IGBTs as switching devices to share the high blocking voltage [185]. A two-level converter was adopted for this test model. The PSCAD converter model is illustrated in Figure 4-3. For this converter topology, six switch valves were used. These contain several IGBT switches, and anti-parallel diodes to facilitate the bi-directional power flow of the converter [186]. The switches were controlled with PWM techniques to reproduce a sinusoidal waveform on the AC side. For their own protection, during faults, the IGBTs were designed to self-block; the fault current is then forced to flow through the freewheeling diodes [102]. The converter unit was controlled using a technique known as a decoupled vector control, which includes the inner loop current controllers and outer loop controllers. This will be explained a bit further in this Chapter.

4.3.2. Transformer

The MTDC VSC-HVDC test model has been connected to the AC system through 50/60 Hz AC transformers. The main function of a transformer in the system was to adjust the voltage level of the grid to an appropriate level of the VSC station. In addition, the power transformer was used to provide a reactance between converter AC terminals and AC system [186], [70]. Its ratings are presented in Table 4-1.

4.3.3. Filters

Filters have been included on the AC side of the converter to limit the harmonic content of the converter current and voltage. The filters were located between the converter and the converter transformer. Their components were calculated using equation (4-1) to (4-3) [70].

$$C = \frac{Q_{shunt}}{2\pi f V_n^2} \qquad (4\text{-}1)$$

$$R = \frac{q}{\omega_0 C} \qquad (4\text{-}2)$$

$$L = \frac{1}{C\omega_0^2} \qquad (4\text{-}3)$$

Where C = capacitance, Q_{shunt} = shunt reactive power, f = switching frequency (i.e. the rate at which the DC voltage is switched ON and OFF during the PWM process), ω_0 = the tuned resonant frequency, V_n = the rated voltage, R = the resistance, q = quality factor and L = the inductance as given in reference [67], [187]. In the model, switching frequency is set as 1350 Hz, the shunt reactive factor Q_{shunt} = 0.06 pu and the resonant frequency is $2\pi f$ [67].

4.3.4. Phase reactor

The phase reactor acts as a filter for the harmonic currents generated by the converter's switching. This aids in preventing rapid changes in polarity that can be caused from the valves switching, while it limits short-circuit currents. An additional purpose of the reactor was to permit independent and continuous control of active and reactive power, by controlling the voltage drop and the direction of the current flow through it. A common size for the phase reactor is 0.15 pu and was also chosen for this model [67].

4.3.5. DC-link capacitor

DC-link capacitors were installed to maintain the DC voltage for VSC operation. They were also tasked to filter the ripples that results on the DC-side of the system. The DC-link capacitance was calculated using the equation (4-4) [70]: -

$$C_{DC} = \frac{2 \times \tau \times P_{\_ref}}{V_{DC}^2} \qquad (4\text{-}4)$$

Where τ = time constant (is time needed to fully charge the DC-link capacitor to its base/rated power and rated voltage level), $P_{\_ref}$ = reference power and V_{DC} = DC voltage. In this test model, the DC-link capacitor was divided into two DC-link capacitor components which are connected to the neutral ground point of the VSC, therefore making the network one with the symmetrical monopole topology.

4.3.6. Transmission medium

Amongst its numerous advantages, VSC-HVDC technology is favoured for its ability to transmit power underground and underwater over longer distances.

Although both AC and DC cables can be motivated and are technically feasible, DC cables gives no technical limit to the transmission distance. The cables add no short-circuit power and enable improved reactive power balance due to the properties of the converters [188]. Most VSC cables are manufactured are either cross-linked polyethylene (XLPE) or mass impregnated insulation [67]. These consist of a copper or aluminium conductor surrounded by metallic sheath and plastic outer coating to protect the cable. For subsea cables an additional steel armouring is required to increase the cables strength and to protect it from harsh sea conditions. The cables shown in Figure 4-4 and Figure 4-5 were designed to be buried underground. These were set to be a 100 km long and designed to carry ± 400 kV and 200 MW.

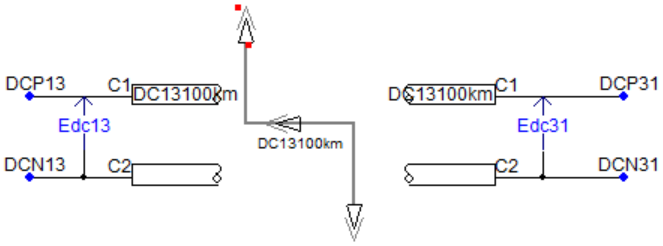

Figure 4-4: Cable connections in PSCAD.

During design, the frequency dependent (phase) model option was selected. Figure 4-5 shows the cable configuration used. The two cables were set at a depth 1.5 m below ground and 0.5m apart from each other as shown. The frequency dependent (phase) model implemented in the system is recognised as the most advanced time domain model available in PSCAD [189], [190] when investigating transients.

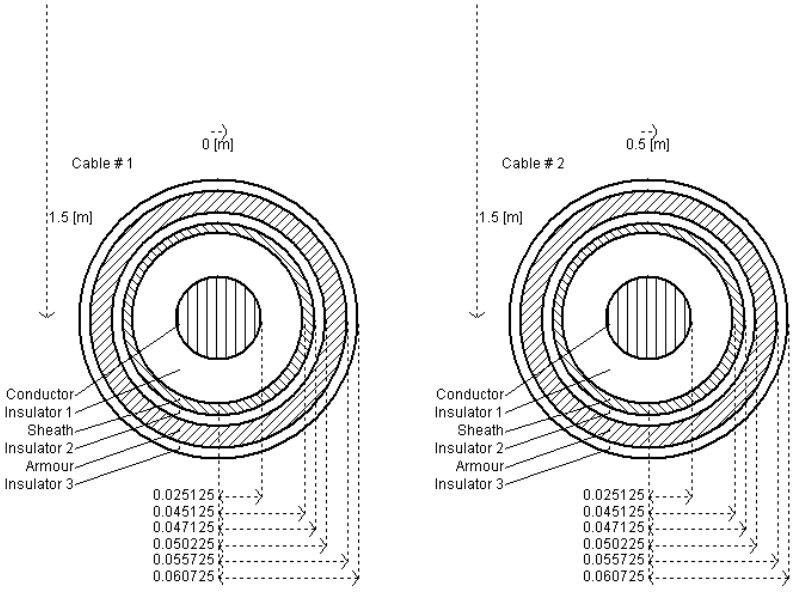

Figure 4-5: Cable configuration.

4.4. VSC-HVDC control

4.4.1. VSC-HVDC operating principle

The developed VSC-HVDC transmission system consisted of VSC units interconnected on the DC-side. Each converter unit used an IGBT based voltage source converter and advanced control strategies to achieve efficient power transmission. The VSC network operated in all 4 quadrants of the P-Q diagram, providing independent control of active and reactive power with less equipment [191]. This was achieved by controlling the switching of the IGBTs. The valves depended on pulse width modulation (PWM) which allows for simultaneous adjustment of the voltage amplitude and phase angle of the converter AC output voltage while keeping DC voltage constant [10].

VSC units of the developed system could be operated either as an inverter, injecting real power into the AC system or as a rectifier absorbing power from the AC grid. A passive or active AC system could be usually connected on the AC side of the VSC. The system presented in this study was connected only to stiff active AC sources. A connection to an active AC system allows for the bi-directional power flow by controlling the AC voltage output of the VSC. The exchange of active and reactive power between a VSC and the AC system was controlled by the phase angle and amplitude of the VSC output voltage in relation to the voltage of the AC system [13], [192]. Active power control was accomplished by changing the converter voltage phase angle δ, while keeping all other parameters constant. Reactive power control was accomplished by changing the converter voltage magnitude, while keeping all other parameters constant [7], [193]. At fundamental frequency, by neglecting the resistance and representing the voltages by line-to-line voltages, active (P) and reactive (Q) power can be expressed as in equation (4-5) and (4-6) [13]: -

$$P = \frac{V_s \sin \delta}{X_l} V_r \qquad (4\text{-}5)$$

$$Q = \frac{V_s \cos \delta - V_r}{X_l} V_r \qquad (4\text{-}6)$$

Where V_s = sending end voltage

δ = phase angle between the voltage

X_l = ideal reactor connecting the two AC voltage sources

V_r = receiving end voltage

In the VSC transmission system, DC voltage polarity is always the same and therefore, the direction of the power flow on the DC line is determined by the direction of the DC current.

The direction of a DC current is always from a higher DC voltage level to a lower DC voltage level [10]. As mentioned previously, VSC1 and VSC4 were tasked to control voltage while VSC2 and VSC3 control the power flow in the MTDC VSC-HVDC system.

4.4.2. Implemented control strategy

There are numerous control strategies available for VSC-HVDC systems. These all exhibit a common operating concept, the control of the voltage magnitude and the control of the phase angle. The only input to the converter is the firing pulses to the converter valves. This means that by controlling the phase shift and duration of PWM pulses, the active and reactive powers can be controlled [9]. VSCs can be controlled either by the direct control or vector control technique. Direct control is a strategy for absolute control and is mainly favoured for its simplicity. However, due to coupling between voltage and current, change in one quantity affects the other and so it is not possible to obtain independent control of active and reactive power [88], [194]. Vector control is a current control strategy that permits the independent control of real and reactive power by the adjusting action of the modulation index M from the phase angle δ. In this technique, the coupling is removed using feed-forward control loops to achieve independent control [195]. For these reasons, vector control was therefore selected for implementation in this study. Its disadvantage however, was that the current control loop was additional and may slow down the speed of response.

In vector control, three-phase currents are transformed to d- and q-axis quantities based on the conventional abc to dq transformation, synchronised to the AC side three-phase voltage through a phase locked loop (PLL) [10]. The d- and q-axis voltages generated by the vector controls are transformed to three-phase quantities and converted into line voltages by the VSC. A VSC transmission scheme which implements vector control deals with 2 layers of control, the outer control system and the inner control system (ICC) [91], [194]. In a network that consists of more than two VSC-HVDC terminals, like the test model designed, assigning one converter for DC voltage control puts the burden of DC voltage regulation on just one converter terminal. A droop controller is then recommended for such systems. DC voltage control by droop characteristics enables two or more terminals in the MTDC to share the duty of DC voltage regulation according to their predetermined DC voltage droop characteristics [196]. The inner current controller and the various outer controllers will be described in detail in the remaining part of this section.

4.4.2.1. The inner current controller (ICC)

The ICC technique is adapted from Kirchhoff's Voltage Law (KVL). This indicates that a voltage drop across the phase reactor should then be equal the potential difference between the AC grid source and the VSC terminal. The ICC is governed by equations (4-7) – (4-9) [191], [194].

$$V_{abc} = Ri_{abc} + L\frac{di_{abc}}{dt} + V_{conv,abc} \quad (4\text{-}7)$$

$$L\frac{di_d}{dt} + Ri_d = V_d + \omega Li_q - V_{conv,d} \quad (4\text{-}8)$$

$$L\frac{di_q}{dt} + Ri_q = V_q + \omega Li_d - V_{conv,q} \quad (4\text{-}9)$$

Where V_{abc} represents the 3-phase AC voltage and V_{conv} represents the converter voltage. Rearranging and deriving the above equations accordingly, an inner controller is modelled as seen in Figure 4-6 and Figure 4-7. (N.B. The above equations are changed to the Laplace transform to deduce the following model). The signal 'DBlk' is included to assist in blocking the IGBT for protection during start-up. Overall, the operating of the PMW is managed by the control signals.

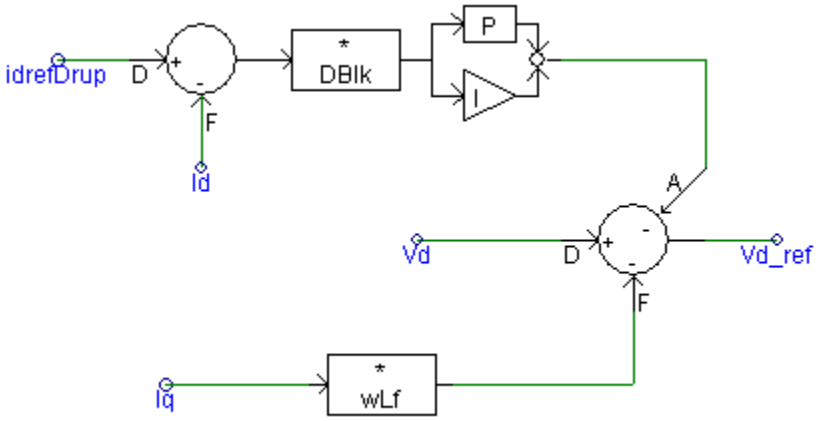

Figure 4-6: Vd Inner current controller.

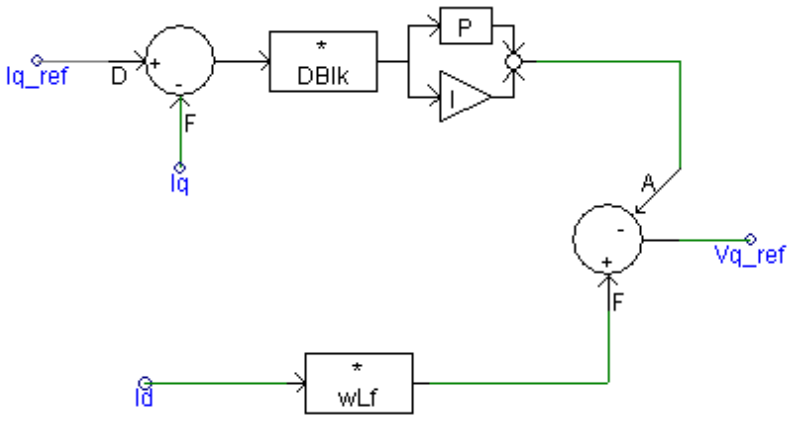

Figure 4-7: Vq Inner current controller.

Where $Idrefdrup$ = droop reference q frame current

I_d = measured d frame current

I_{q_ref} = reference q frame current

I_q = measured q frame current

V_d = measured d frame voltage

ωLf = angular frequency × phase reactance

V_{d_ref} = d frame voltage output

V_{q_ref} = q frame voltage output

The modulus optimum method in [67] was used for PI tuning. It has an inner loop control that offers a fast response. Equations (4-10) and (4-11) were used to calculate the time integral and proportional gain [10].

$$T_i = \tau_{pu} = \frac{L_{pu} / \omega_b}{R'_{pu}} \qquad (4\text{-}10)$$

$$K_p = \frac{\tau_{pu} \times R'_{pu}}{2T_a} \qquad (4\text{-}11)$$

Where ω_b (base angular frequency) = $2\pi f_{base}$

$T_a = \frac{T_{switch}}{2}$ where is T_{switch} the switching time

T_i = time integral constant

L_{pu} = inductance (pu)

R_{pu} = resistance (pu)

K_p = proportional gain

There are various strategies to pulse width modulate converter switches to shape the output AC voltages to be as close to a sine wave as possible. An example is the sinusoidal pulse width modulation (SPWM) technique. In SPWM, to obtain balanced three-phase outputs, a triangular wave form is compared with three sinusoidal control voltages that are 120º out of phase. In the linear region of modulation (amplitude modulation index, M ≤1), the fundamental frequency component of the output voltage of the converter varies linearly with M. The AC voltage fundamental component can be expressed as in equation (4-12) [38]: -

$$V(t) = \frac{M \times V_{DC}}{2} \sin(\omega t + \delta) \qquad (4\text{-}12)$$

Where $M = \frac{\sqrt[2]{V_d^2 + V_q^2}}{V_{DC}}$ and $\delta = \tan^{-1}(\frac{V_q^2}{V_d^2})$. The line-to-line voltage at the fundamental frequency can be written as in equation (4-13) [38]: -

$$V_{abc} = \frac{M \times V_{DC}}{2} \approx 0.5M \times V_{DC} \qquad (4\text{-}13)$$

Where V_{DC} = DC voltage M = modulation index

ω = angular frequency δ = systems phase

V_d = measured d frame voltage V_q = measured q frame voltage

By using SPWM with high switching frequency, the wave shape of the converter AC voltage output can be controlled to be almost sinusoidal with the aid of phase reactors and tuned filters.

Changes in waveform, phase angle and magnitude could be made by changing the PWM pattern. The choice of the modulation index is a trade-off between output power and dynamic response. The higher the modulation index, the higher the output power rating. The outputs of the ICC are transformed from the dq0 frame back into (abc) phase, using the Parkes transformation block. A sinusoidal pulse width modulation (SPWM) switching technique with triangle carrier (tri) provides the gate signal for VSC-HVDC network. The resulting voltage, Va, Vb and Vc are then compared with a triangular wave which has a defined switching frequency. The results are then fed as pulses into the gate of the IGBTs.

4.4.2.2. The outer controller

The outer controller technique can be classified into two categories. In each category: $I_{d\ ref}$ can be controlled by either DC voltage (V_{DC}) or active power (P), while $I_{q\ ref}$ can be controlled by either AC voltage magnitude or reactive power (Q). The outer controller system provides reference signals of d and q-component for the ICC. DC droop control is a modification of the fixed power, fixed DC control [10]. In this control strategy, the horizontal line sections of the characteristic curves (i.e. constant V_{DC}) will be replaced by a small slope (i.e. droop).

The power-DC voltage droop control could be implemented with the use of proportional or a PI controller in the DC voltage regulator [3] as is shown in Figure 4-8. Several of the research works in HVDC networks have focused on control of VSC terminals. These control strategies characterise how the converters respond to changes in power flow in the DC grid. The DC voltage droop control has been favoured and preferable due to its better performance with DC voltage regulation of MTDC and due to its ability to facilitate provision of security. Similarly, $I_{d\ ref}$ can be controlled by either DC voltage or active power, while $I_{q\ ref}$ is controlled either by AC voltage or reactive power.

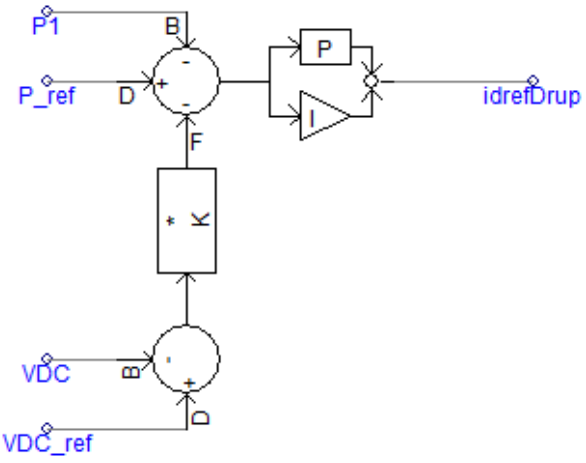

Figure 4-8: Outer controller representation of DC voltage droop control in VSC-HVDC scheme.

Where P_1 = measured active power of VSC

$P_{\_ref}$ = reference active power

V_{DC} = measured DC voltage

V_{DC_ref} = reference DC voltage

K = DC voltage droop

The "symmetrical optimum" method was used to tune the PI controllers [67]. For this non–linear system, linearisation is around the operating point. The controller be represented mathematically in equation (4-14) and (4-15) as [191]: -

$$(V_{DCref} - V_{DC})G - \frac{2P_{ref}}{3V_d} + \frac{2P}{3V_d} = 0 \qquad (4\text{-}14)$$

$$\Delta V_{DC} = \frac{2\Delta P_{ref}}{3GV_d} \qquad (4\text{-}15)$$

Hence the DC voltage droop, K is given by equation (4-16) [191]:-

$$\frac{\Delta V_{DC} / V_{DC\_rated}}{\Delta P_{ref} / P_{\_rated}} = \frac{2}{3GV_d}\frac{P_{rated}}{V_{DC\_rated}} = K \qquad (4\text{-}16)$$

The proportional gain G can be selected according to the required amount of the DC droop, K

4.4.3. Summary

The controls can be designed to work closely with the VSC transmission protection system, allowing the VSC system to ride through temporary faults in the transmission system. This feature usually requires, adequate filtering of key signals. An excessive filter poses negative effects as it decreases the speed of the control system. A protection scheme is required to act very fast but accurately in a VSC transmission system (within 5 or 10 milliseconds) [58], [197]. Strategies implemented in designing and rating the controls and protection should therefore be accurate and precise as converters are sized to meet the expectations of designer. When the system is recovering from a disturbance, the controls must be fully functional, running free of limits, and not suffering from prolonged blocking of firing pulses.

4.5. Proposed protection method models

A feasible protection scheme should be equipped with a reliable and effective fault detection, location and isolation technique. These methods are expected to be fast, sensitive and selective. The objective of the protection strategy is to detect as to whether a fault exists, discriminate the faulty part and send out a signal on which breakers to trip. Receiving instruction from the detection and location scheme, the isolation technique is tasked only with separating the faulty section from healthy state as soon as possible. This section aims to present the simulation models of the main and back-up detection, location and isolation protection strategies of the designed system on PSCAD in detail.

To implement the detection, location and isolation protection techniques, the DC current signals were mainly utilised over DC voltage signals. Although DC voltage signals could be just as useful, they were limited by their inability to distinguish a line affected by a fault from an unaffected DC line when a DC fault occurs too close to the converters that control DC voltage. In this case, this means that they were not efficient for detecting faults that occur close to VSC1 and VSC4. Currents listed below will be measured and used as signals: -

- Current flowing out of the positive and negative cable sides of VSC1 denoted as IDC12P, IDC12N, IDC13P and IDC13N.
- Current flowing out of the positive and negative cable sides of VSC2 denoted as IDC21P, IDC21N, IDC24P and IDC24N.
- Current flowing out of the positive and negative cable sides of VSC3 denoted as IDC31P, IDC31N, IDC34P and IDC34N.
- Current flowing out of the positive and negative cable sides of VSC4 denoted as IDC42P, IDC42N, IDC43P and IDC43N.

In this study, the feasibility of various fault detection strategies was initially be investigated. These include the main DWT protection scheme as well as overcurrent protection, differential protection and derivative protection presented as different possible back-up strategies for the model. The implemented main and back-up strategy are then to be chosen considering operational speed, reliability and selectivity. To locate the exact position of the fault, this study focused only on the implementation of the fast travelling wave technique. To avoid the inclusion of communication structures, the single-ended travelling wave protection method was explored. Finally, to isolate the faulted area, as presented in Chapter 3 the project explored hybrid DC CBs as the main isolating technology and AC CBs as an emergency back-up method.

4.5.1. The primary protection schemes

The travelling wave protection method is currently one of most promising protection technique for a MTDC VSC-HVDC system. The method operates at high speed and is more accurate than its variants [73]. It was thus chosen as the main detection and location technique for the developed model. To maximise on the technologies accuracy, the wavelet based travelling wave fault detection was implemented.

The discrete wavelet transforms (DWT) was selected in this case. To implement the protection scheme in the developed model, a "DWT" component block provided by the PSCAD master library was added in the system. The signal of current measured at the DC cable links was used as the input to the DWT block. The DWT component has different mother wavelets that can be chosen. It is also equipped with coefficient levels and appropriate sampling frequency. For this study, the DWT block was configured as follows: -

i. Sampling frequency was used for digitalisation. It is consistent to the solution time step of the developed model.
ii. The Haar wavelet was chosen as the mother wavelet based on recommendations in [67]. It is described as the simplest and the most practical when compared to its variants.
iii. The value of the level selected depended on the desired detail. The highest level that could be selected is 6. The 5^{th} level was selected in this study mainly because that is when the wavelet coefficient was clearly selective.

The implementation of the DWT travelling wave detection and location algorithm is shown in Figure 4-9. For operation, the protection system received current signals from the converters. Since they are very sensitive to noise, these signals were filtered using a built in PSCAD filter block. The DWT block produces two outputs, A represents the low frequency output and D the detailed high frequency output. Since the level chosen was 5, a total of 5 high frequency outputs were produced. The highest (i.e. Level 5) was then used as an input signal in the comparator.

The magnitude of the 5^{th} level DWT signal and the set threshold were compared in the comparator. The set threshold value was calculated by estimating a DWT coefficient slightly higher than the one recorded on the healthy cables during a DC fault scenario [70]. In wavelet protection, the general operating principle is simple. Typically, a DC fault would be identified when the detailed 5^{th} wavelet coefficients level exceeds the pre-set threshold value.

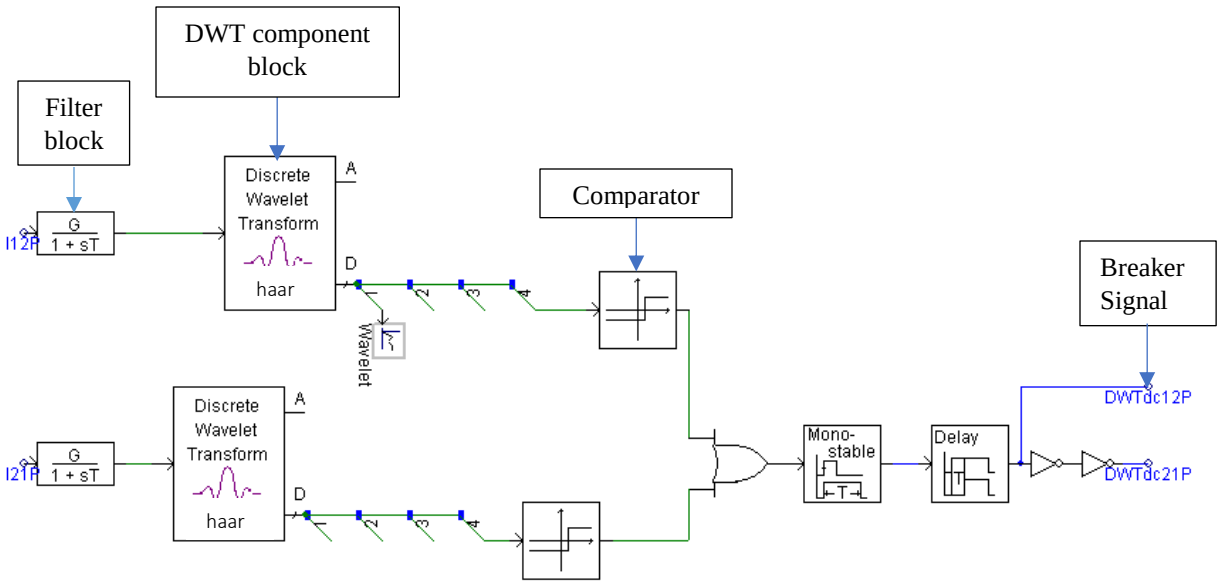

Figure 4-9: Implementation of travelling wave detection method.

4.5.2. The back-up protection scheme

A back-up fault detecting method is usually added into the system to improve the performance and reliability of the protection system. Possible techniques include: -

- Overcurrent protection method
- Differential protection method
- Derivative protection method

4.5.2.1. Implementation of overcurrent protection on MTDC model

As previously mentioned the implementation and working principle of overcurrent protection is straightforward. Current on the DC-side of the converter is measured and used for this scheme. An overcurrent detection element, shown in Figure 4-10 is found in the PSCAD master library and was used to implement this protection scheme.

To identify a fault in the network, the overcurrent component compares the measured DC current with a set current threshold for the system [4]. If at any point, the DC current magnitude exceeds the set threshold, a fault signal is generated. The peak current of both the healthy and faulty poles is needed to set the threshold for this technique. Figure 4-10 shows the control strategy implemented in the system for overcurrent protection. In this configuration, an absolute value of currents was measured on the positive and negative DC-side of VSC1, VSC2, VSC3 and VSC4. These current signals were being monitored for possible overcurrent. If any of these currents rose above the set threshold value, the system was designed to send trip signals to the corresponding DC breakers.

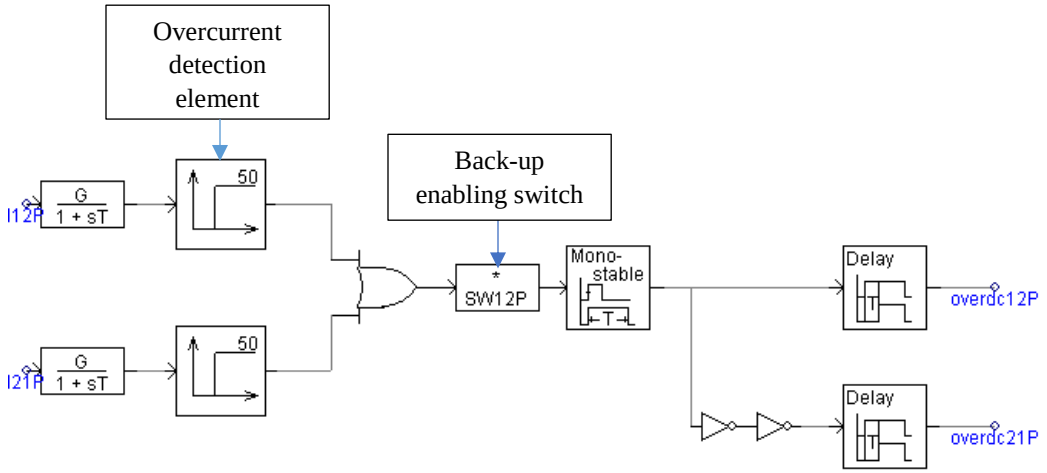

Figure 4-10: An overcurrent control scheme.

4.5.2.2. Implementation of differential protection on MTDC model

To detect a fault using the differential protection technique, a difference was taken between the current entering the protected cable and the one at the opposite inverter end (as shown in Figure 4-11). After a specified delay time, the result of summation was compared to pre-defined threshold value. Setting an appropriate threshold aided in discerning the faulty line from the rest. Similarly, the peak differential current of both the healthy and faulty poles was needed to set the threshold for this technique [67]. The differential current equation could be represented as equation (3-23) presented in section 3.3.2. When the differential protection method has identified a fault in the system, the DC CBs were enabled to isolate the faulted section.

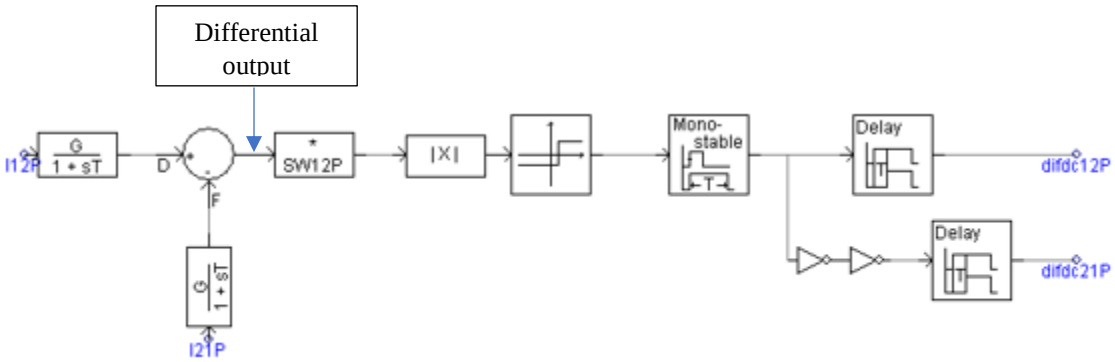

Figure 4-11: Differential method on PSCAD.

4.5.2.3. Derivative protection.

To apply derivative protection, a derivative with time constant component found in PSCAD was used. This is shown in Figure 4-11. A time constant of 0.001s was set for this study. Applying the derivative function determines the rate at which a signal would be changing. This block however has the tendency to amplify noise. To minimise noise interference, particularly when the derivative time constant is large, and the calculation step is small, it may be necessary to add a noise filter. A weighted sum of the derivatives was calculated using equation (3-24) presented in Section 3.3.2. To determine the existence of a DC fault, the results obtained from the current derivative were compared to a set threshold.

To set the threshold of derivative technique, two values were considered. This includes the lowest value measured during a DC fault in the designated protection zone and the largest value found for a fault outside the protected zone. To successfully determine a threshold, the first value was to be larger than the second value. The control developed in Figure 4-12 was developed and implemented for derivative fault protection in the MTDC system. In this system currents drawn from the rectifier (I12P and I12N) and inverter side (I21P and I21N) of VSC1 and VSC2 were used to describe the working principle. The current signal derivatives were compared to the determined threshold of the system. A signal was sent to open the DC breaker if the signal had risen higher that the specified threshold.

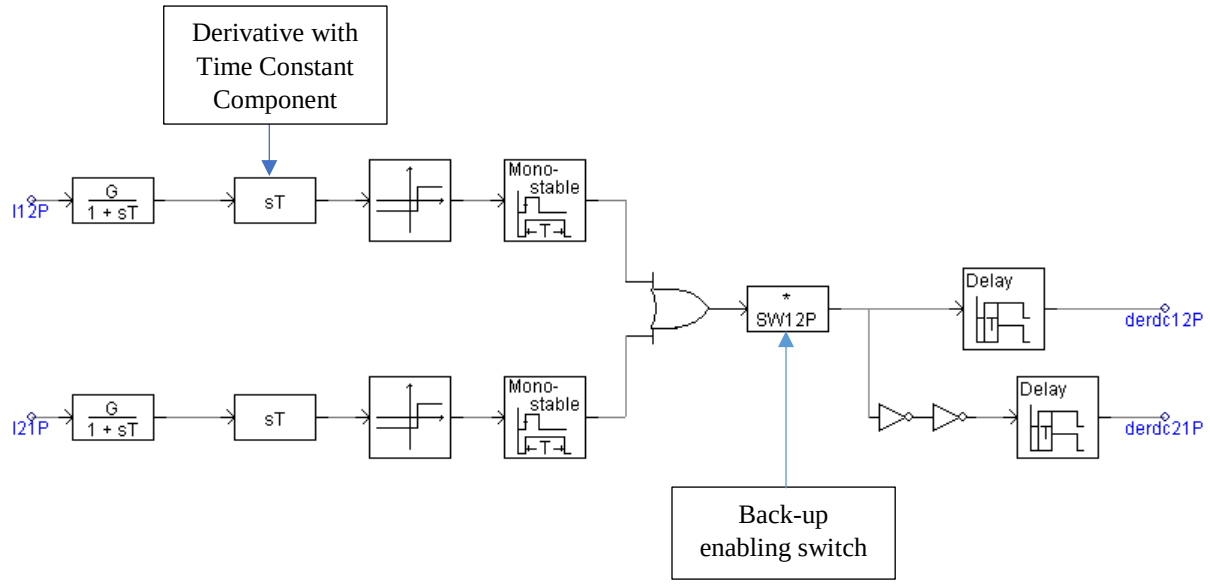

Figure 4-12: Derivative method on PSCAD.

4.5.3. Implementation of the location method

Once the faulty line had been identified, the exact location of the DC fault could be determined. Fault location is required mainly in permanent faults. During fault location, the data used to locate the fault could be obtained from the outputs of fault detection. The algorithm was expected to be within the fault clearance period of approximately 5ms. In this study the single ended travelling wave fault location techniques was adopted. For this method, fault location could be determined using equation (3-15). The travelling wave location method was implemented using the MATLAB software tool. A transient arriving at a terminal/ measuring point is known to cause a sudden increase in current. Taking this information, the current derivative was used for determining when a transient reached the CB. The precise location of the DC fault could only be determined if the arrival times of the first and second transients were recorded correctly.

4.5.4. Implementation of the isolation method

The DC circuit breakers were implemented into the network to isolate the faulty cables from the rest of the system. They were installed on both positive and negative poles and on both ends of the transmission cable. This ensured selective isolation of the faulty line and avoids the disruption of power transmission on the healthy part of the network. The hybrid DC CBs were modelled as ideal switches. This means that their time delay was equal to the total duration taken to detect and interrupt the DC fault. In this study, the main focus was only on clearance time. DC fault clearance time is however demanding for VSC-HVDC networks, as currents rise to high DC current magnitudes at a very fast rate.

The breakers receive their instructions straight from the implemented detection and location methods. It is required that their operation is as fast as the rest of the implemented protection scheme as they play a key role in starving the DC fault disrupting the network.

During design, it was anticipated that the components could also have errors, not performing their function even when receiving the correct signal. A back-up strategy was therefore employed to ensure a robust protection scheme. AC CBs were installed as the back-up protection system. They were used only when the main hybrid DC CBs fail to interrupt the fault. AC CBs were found as a component on PSCAD and do not have to be developed as in the case of the hybrid DC CB. AC CBs were used in this case only when all other protection schemes have failed to stop the fault disrupting the normal operation of the system.

4.5.4.1. The hybrid CB in PSCAD.

To implement DC isolation in the MTDC network, the hybrid DC CB was developed and incorporated into the system. Its properties imitate that developed by ABB as shown in Figure 4-13.

In the figure, the ResCtrl breaker represents the residual current breaker; FastCtrl represents the fast-mechanical isolator, the Aux Brk represents the auxiliary path of the CB and Main BRK is the main breaker tasked with the function of isolating the connected DC-link. The parameters for the IGBT and the diode are obtained from the model provided by Knowledge Manitoba in reference [198].

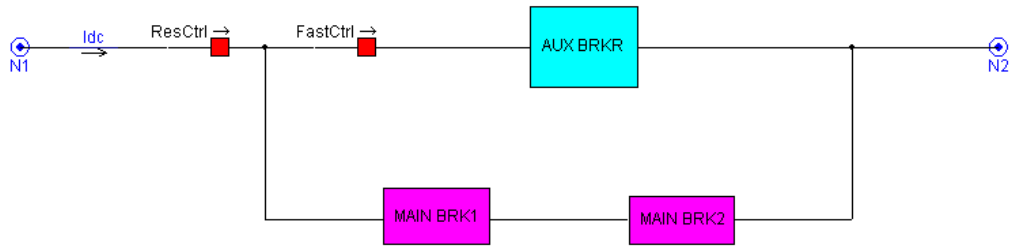

Figure 4-13: Implementation of hybrid DC breaker on PSCAD.

To operate the breaker systematically, a control method was developed to communicate with the hybrid DC CB. Figure 4-14 shows the control strategy set to control the opening and closing of the auxiliary and main circuit breaker. BRKCtrl represents the DC breaker control that was activated by the instructions received from the detection techniques. It is only when this control was enabled that the breaker would able to operate. During steady state, the current flows through the Aux Brk. When a fault occurs, the load commutation switches commutate current to the main HVDC breaker and the FastCtrl opens.

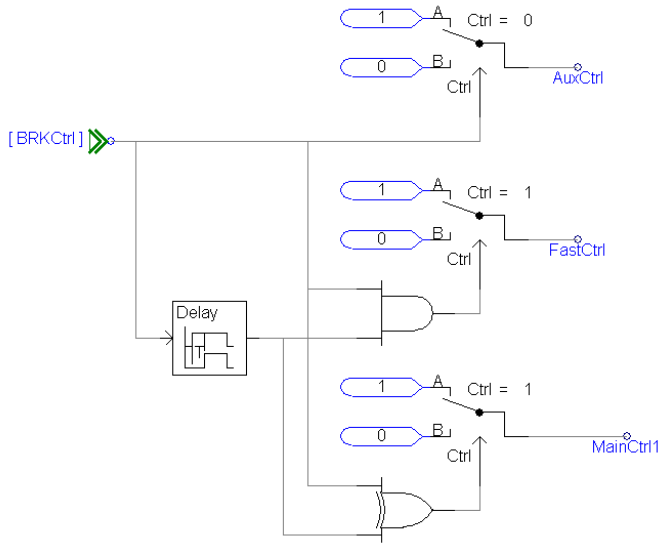

Figure 4-14: Control strategy of the auxiliary breaker, fast mechanical isolator and main breaker 1.

4.6. Simulation procedure

To test the validity of the protection scheme strategies presented, the developed MTDC VSC-HVDC model was run for 10 seconds without any disturbances. The network was then exposed to DC-side faults. Initially, the system was not equipped with any protection strategies. This data was used to analyse the fault response of the system. The information was later used to optimise the design settings of the protection scheme. To test the feasibility of the proposed protection strategy, DC faults were applied at different cable locations. The faults were set to be triggered after 5s and were regarded as permanent as they lasted till the end of the simulation duration. The only type of DC faults applied to test the feasibility of the protection strategies was the short-circuit fault. The fault impedance was set to 5Ω in the simulation. The single-phase fault component in PSCAD was used to implement this type of fault. It is placed in between the positive and negative transmission cable. To apply DC cable faults in the developed model on PSCAD, the DC cables were divided into several cable connections sections. This was done so that all lengths could be easily accessible during the DC fault distance test

4.7. Chapter summary

The methodology used to develop the test model and the design of a protection scheme is presented. The operation of the MTDC VSC-HVDC system was made possible with the use of the droop control technique. This is an indirect protection measure allowing the network to operate even in instances where the VSC controlling the DC voltage has been damaged. Underground cables were used as a transmission medium. As mentioned, cables and OHL have dissimilar characteristics. Although these differences may affect the fault response of the network the protection principles remain the same.

Protection designed for cables has to however react a bit faster than in OHLs as the fault is closest to the ground and so the voltage drop is greater. The developed model was initially used to analyse the DC fault characteristics of the network. Thereafter, a protection scheme was tested on the model. Protection schemes evaluated include the highly selective DWT detection method, the simple yet unselective DC overcurrent detection method, the highly selective but distance restricted differential detection method and the fast detecting but noise sensitive derivative method. Results from this evaluation were used to propose a reliable detection method for the scheme. In addition, a precise fault detection technique was implemented (i.e. the single converter current derivative travelling wave location method). The method used MATLAB code to point to the location of the fault. This was useful for permanent faults. Finally, a hybrid DC CB was installed on both sides of the DC cable. Their selective nature allowed that the rest of the system operate while the faulty cable is being repaired. As an extra precautionary measure AC side DC CBs were installed to isolate the entire system to protect the grid from the occurring faults or the converters from faults that occur in the grid.

CHAPTER 5: RESULTS AND DISCUSSIONS

The developed test model is illustrated in Figure 5-1 and indicates implemented fault points and measuring points. Initially, results validating the operation of the developed model are presented. This includes an analysis of the output results of current (represented by I), line voltage between two poles (represented by Edc), pole-to-ground voltage (represented by V) and powers measured on the AC side (represented by P) in the VSC-HVDC network during steady state (i.e. when there are no faults or disruptions injected into the system). A fault analysis of the developed network was then carried out. During this study, a DC fault was injected on the system with no protection scheme put in place to disrupt the threats. A single-phase PSCAD fault component was then applied as a DC fault on the cable representation model. In the figures presented in this Chapter, active/reactive power that moves initially from the AC grid, towards the VSC stations and then to the DC cables has been considered to be positive.

The DC fault analysis has been carried for the different fault types and fault locations. The main objective of DC fault analysis was to investigate the effects of a DC fault on a MTDC VSC-HVDC system. A fault analysis study is vital for investigations carried out on protection schemes, as the information obtained from the results can be later used for determining the design ratings of the proposed protection scheme. In addition, an analysis of the effect of the change in the DC-link capacitance and impedance was carried out. The main objective of this investigation was to further evaluate the effect that these factors may have on a MTDC VSC-HVDC network during a DC fault. This information can also be used later in the design of the protection scheme.

Finally, the Chapter presents and discusses the results obtained when implementing different protection strategies in the developed system. The key objective was to evaluate the available strategies and propose one that would be the most suitable for the developed MTDC VSC-HVDC network. To validate the model and implement potential protection strategies, the duration run of the simulation was set to run for a duration of 10 seconds.

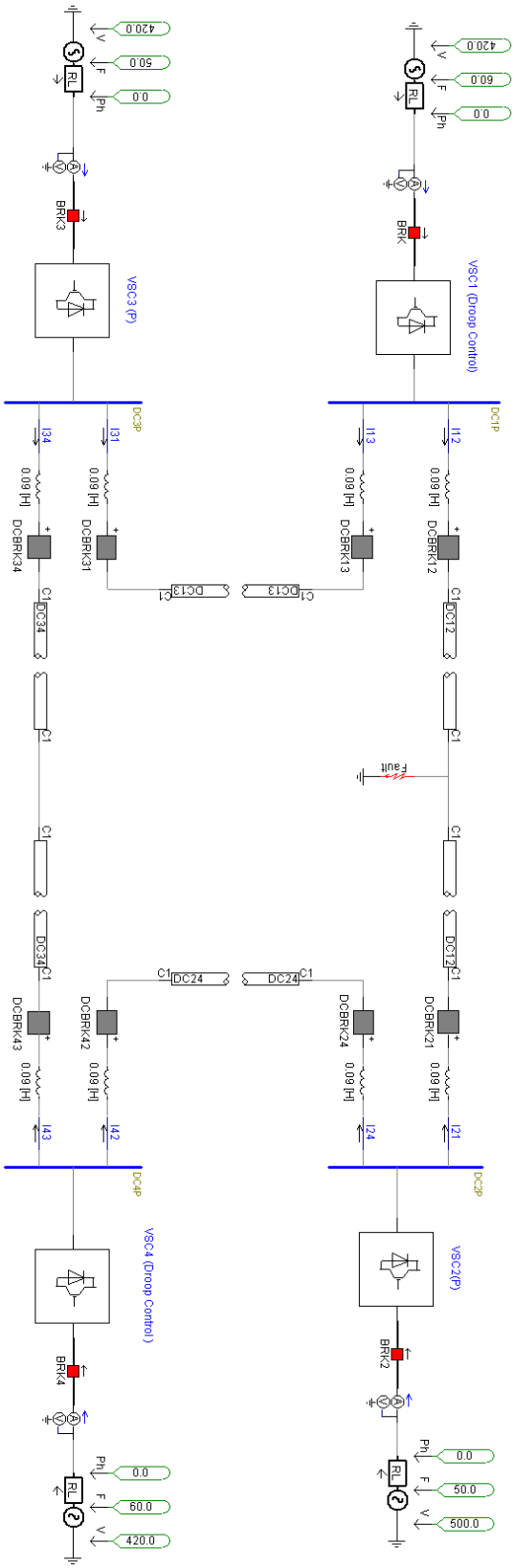

Figure 5-1: Single line diagram of the developed MTDC VSC-HVDC network.

5.1. Model validation

To illustrate the basic behaviour and functionalities of the MTDC VSC-HVDC network, a 400 kV DC-link test model was simulated as presented in Chapter 4. For system validation, the simulation scenario has been set as follows:

- The simulation was initially run from an un-initialised state of time t = 0.0 seconds
- After the system enters steady state operation (i.e. around 0.3s for this system), the reference values in the VSC stations remain constant.
- At time t=4.0s, the directions of power in the system were gradually interchanged. This was done to illustrate the effects that the change of power flow direction may have on the MTDC network.
- Although not shown in the results, each converter operates at a unity power factor and therefore approximately zero reactive power will be injected into the network.

The network was designed to either control DC voltage and the magnitude of AC voltage or active power and the magnitude of AC voltage. Therefore, during the test, only the networks DC voltage, DC current as well as the active powers were of interest and were observed. As discussed in Chapter 3 and Chapter 4, both VSC1 and VSC4 were tasked to control DC voltage. This was also a protection strategy as it means that a sudden malfunction in one of the DC voltage regulators will not necessarily lead to a system collapse as the other station would still be available for voltage regulation.

The two VSC stations (i.e. VSC1 and VSC4) were responsible for ensuring that the voltage remains constant at a rated value of 400 kV for the duration of the simulation test. This is a basic requirement for any MTDC network and proved to be true during the simulation test. Due to unforeseen circumstances, sometimes a VSC station might need to change its role to start generating the power or to absorb power from the system. To test the effects of this phenomenon, at time t=4.0s the roles of VSC2 and VSC3 were gradually interchanged. During these changes, the voltage was expected to remain constant, only reacting at times where there are changes. As seen in Figure 5-2, although there are initial transients indicating the change in operation for the network, for most of the time, the voltage remains fairly constant.

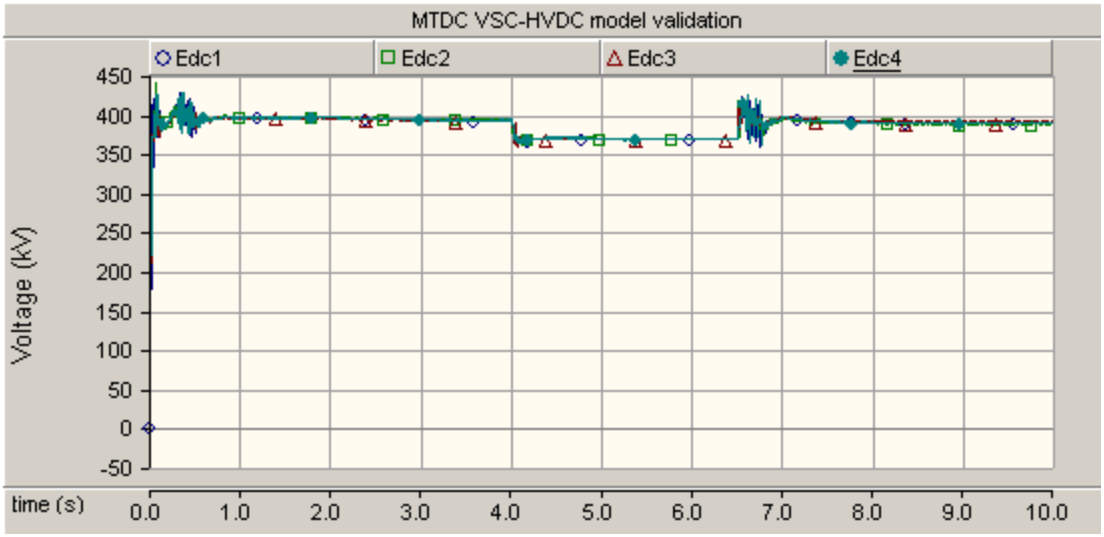

Figure 5-2: DC Voltage measured at terminals of VSC1, VSC2, VSC3 and VSC4.

DC currents were initially measured directly at the DC poles of each VSC terminal. As mentioned previously, since VSC2 was pre-set to 200 MW and VSC3 to -200 MW, power was transferred from VSC2 to VSC3 through the DC cables. No direct connection exists between the two stations and so power was transmitted via the DC cables also connected to VSC1 and VSC4. The DC cables were connected to the VSC stations through DC buses, as shown in Figure 5-1. Although station VSC1 and VSC 4 were designed with a reference power of 0 MW, during the power transmission, a small fraction of the energy was absorbed by the stations. As the main supplier of power, VSC2 had risen to approximately ±0.5 kA. However when counting the powers absorbed by VSC1 and VSC4 as well as transmission line losses the current measured at VSC3 has reduced to ±0.35 kA. This is shown in Figure 5-3.

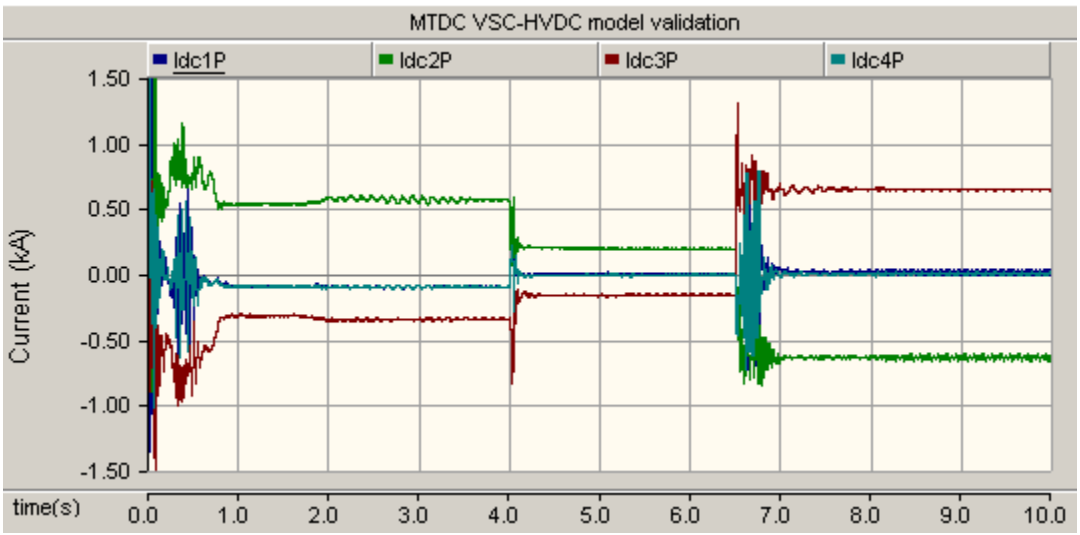

Figure 5-3: DC Current measured in terminals of VSC1, VSC2, VSC3 and VSC4.

The DC currents measured at DC cables DC12P (connecting VSC1 and VSC2), DC13P (connecting VSC1 and VSC3), DC24P (connecting VSC2 and VSC4) and DC34P (connecting VSC3 and VSC4) are shown in Figure 5-4. Since the DC bus is virtually a node/junction, according to KCL, the total sum of currents I21P and I24P measured at DC bus 2 of VSC2 were to be equal to the current measured in Idc2P. The current measured at I12P connected to bus 1 of VSC1 was measured at -0.25 kA, confirming that direction of power was away from VSC2. A current magnitude of approximately +0.20 kA was then measured at I13P re-affirming that the power will flow from VSC1 to VSC3 and has decreased due to transmission line losses. A similar process was also recorded for the current path moving from the buses connected to VSC2, VSC4 and VC3. With I24P measured at DC bus 2 recorded to be +0.25 kA and I34P measured at bus 3 of VSC3 recorded to be approximately -0.20 kA. During the change in operation at t=4s, unlike voltage, the current magnitude was seen changing according to the new specifications. When the new steady state was reached, the current was seen settling back at their rated values.

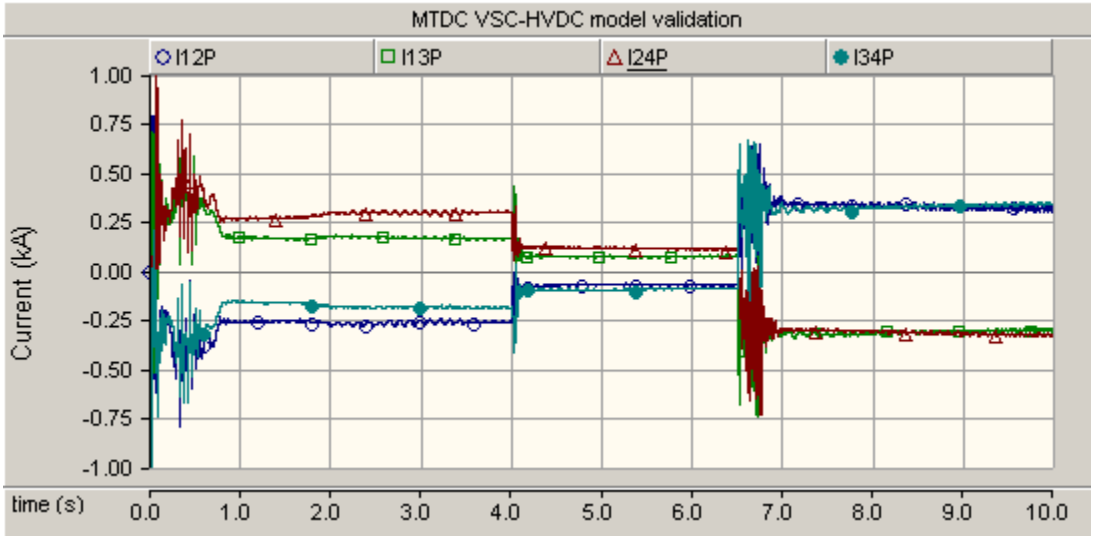

Figure 5-4: DC Current measured in cables connecting VSC1, VSC2, VSC3 and VSC4.

The system was kept at +200 MW for the stations feeding power and at a total of approximately -200 MW for the stations absorbing power from the system as presented in the results in Figure 5-5. What was also evident in this test was that P1 measured on the AC side of station VSC1 and P4 measured on the AC side of VSC4 absorb some power even though they have been set to only regulate DC voltage for this test. This means that the network ultimately had a single rectifier and three inverters. These conditions could of course be changed; however, this requires a few adjustments in the control of the network. This was not investigated in this study.

When the roles of the stations were now changed, the active power measured at VSC2 gradually changed to -200 MW, while VSC3 changed to +200 MW. During this test, the changes in current magnitude were followed by the changes in power. This is also shown in Figure 5-5. An additional function of droop control was present to also assist in maintaining the power dispatched from converters VSC1 and VSC4 independent of changes implemented on other terminals. This was confirmed in the results when the powers dispatched by VSC1 and VSC4 reduce to 0 MW and then remain at 0 MW despite the change in converter functions at time t=4s.

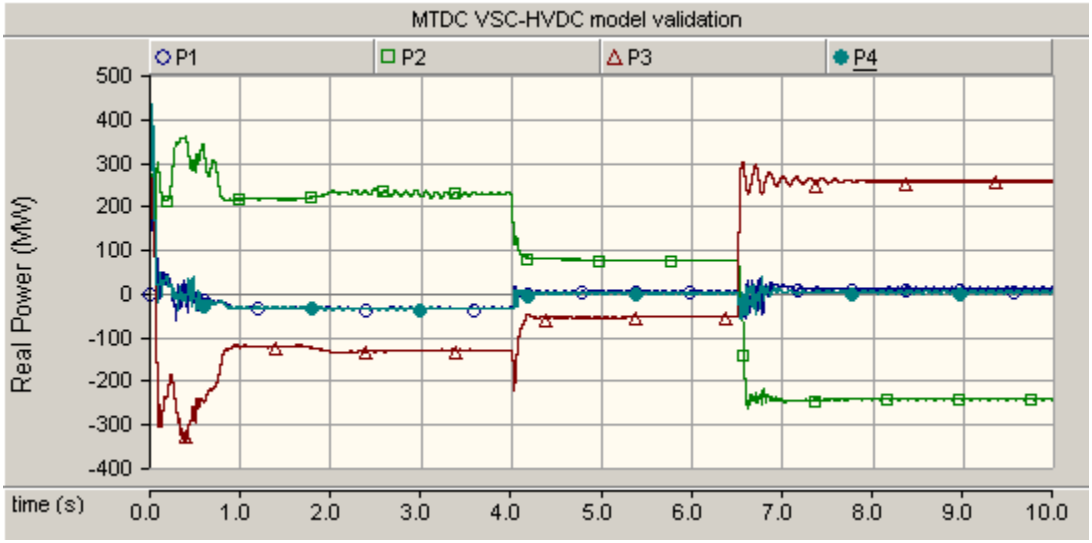

Figure 5-5: Active power (P) between all terminals during a gradual change of roles.

It was important to change the functions of the VSCs in steps as an abrupt change would cause the whole system to fail. An abrupt change of roles for each VSC station changes its function without being switched off to allow for a gradual change of duties. These changes may have a negative effect on the system. Since voltage was kept fairly constant, a rise in current results in a rise in power. If the power rises to magnitudes too high for the system to handle, the system faces a potential threat. Figure 5-6 illustrates the results depicting the effect of power when abruptly changing the roles of the converters. In these results, after the abrupt change of roles, P1 and P4 drop to approximately-40 MW, while P2 and P3 rise to much higher magnitudes for the rest of the simulation duration. The new steady state power magnitudes (i.e. of P2 and P3) rise to more than 50% of the rated value. If kept for a long duration, the high rise in power could ultimately pose a threat for the system causing it to fail.

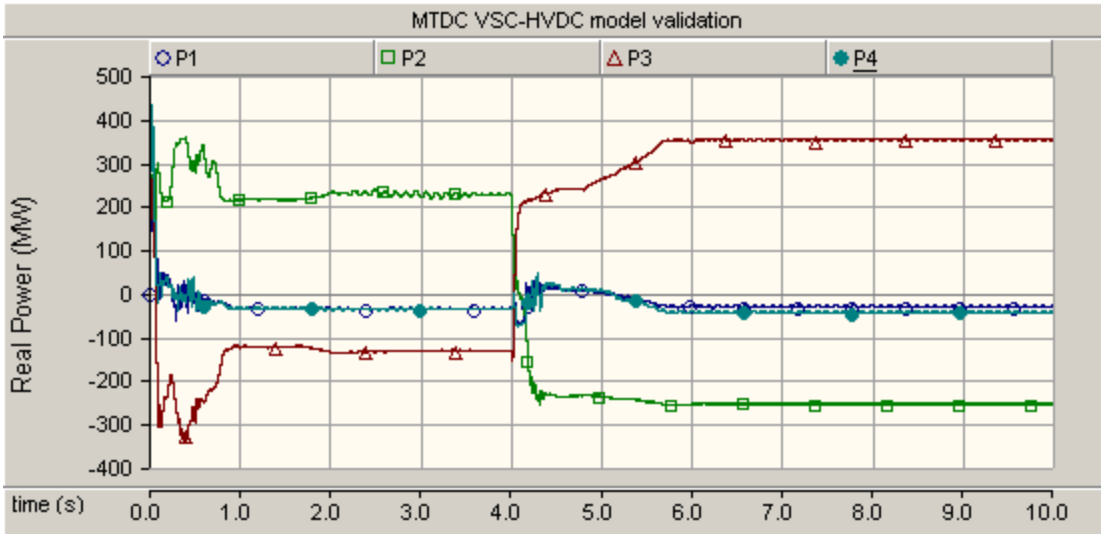

Figure 5-6: Active power (P) between all terminals during an abrupt change of roles.

In summary, to verify the model, a base case simulation test was conducted. The results obtained from these tests successfully validated that the developed test model works as expected, reacting accordingly to the imposed load/production varying scenarios. This developed test model was set to be used for works in the remainder of this study in which the proposed protection scheme will be implemented.

5.2. Fault analysis

For DC fault analysis, a DC fault was applied along the 100 km DC cable model representation of the MTDC VSC-HVDC network developed. Important factors to monitor during this analysis included the peak magnitude of DC fault currents and the time to peak value of the DC fault also known as critical time. The DC fault was implemented after the system enters a steady state. As mentioned previously, this MTDC network reaches its steady operational state at time t=0.3s. When the DC fault was applied to the system, the cable current was expected to rise above the magnitudes obtained in Section 5.1. The fault currents were expected to develop in three stages, as mentioned in Chapter 2. Although theory states that a DC fault currents has 3 stages, none are clearly recognised from the results obtained. The DC faults could occur on either the converters or on any of the DC cables. During this test however, the DC faults were only simulated on the cable connecting VSC1 and VSC2.

5.2.1. Fault type

As discussed in Chapter 2, a DC fault can be between transmission lines or between a transmission line and ground.

The type of fault a system experiences usually affects the fault current shape and peak magnitude. To study and analyse the DC fault response of VSC-HVDC networks, the developed test model was subjected to a DC ground fault and a short-circuit fault, 0 km away from VSC1. During this investigation, a 5Ω fault impedance was applied. In addition, the currents flowing through the diodes were also analysed to illustrate their behaviour during the disruption.

5.2.1.1. Ground fault applied 0 km away from VSC1

When a positive pole or a negative pole is short-circuited to the ground, a ground fault is known to have occurred. During this test, the positive pole connecting stations VSC1 and VSC2 experienced a ground fault. The permanent fault was applied to the system at t=5s, exposing the healthy pole to full DC-link voltage and transformer voltage stress. Results depicting the response of current are as shown in Figure 5-7. As was expected, after start-up the currents rose to the steady operational magnitude mentioned in Section 5.1. However, when the VSC-HVDC network experiences a DC fault, current measured from the affected/faulty cable rises sharply and to a higher magnitude than current measured in other parts of the system. The sharp rise lasts only for brief period, but its high magnitude can be detrimental to the system. I13P flowing through the cable connecting VSC1 and VSC3 rose to the second largest current at -4 kA. Although no faults were directly injected to it, the rise was mainly as a result of the DC fault occurring very close to the converter and the connecting bus of VSC1 in which I13P was also connected. To illustrate the effect of a DC ground fault on a VSC-HVDC system more accurately, Figure 5-8 presents the results of the current response that clearly depicts the fault current shape and peak magnitude for the cable connecting VSC1 and VSC2.

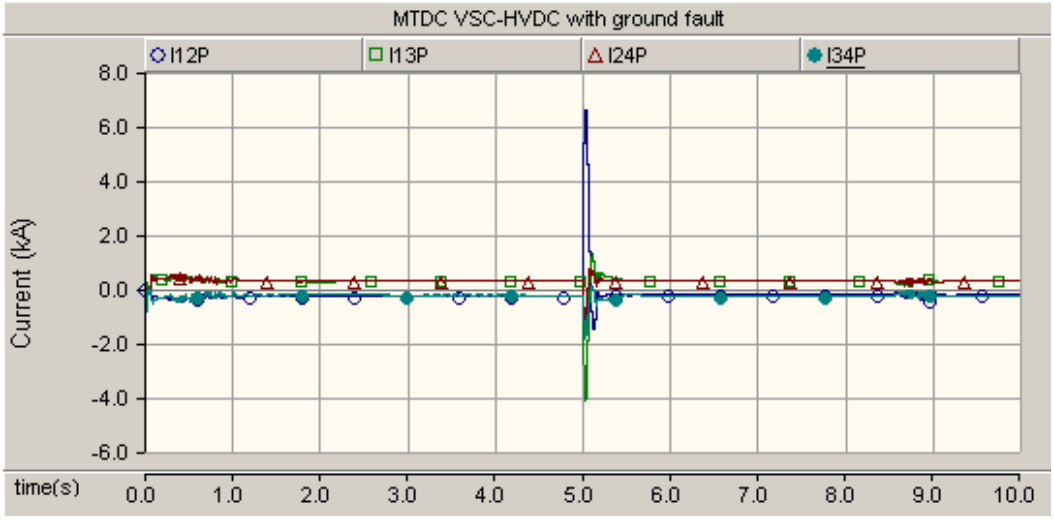

Figure 5-7: DC Current measured in cables connecting VSC1, VSC2, VSC3 and VSC4.

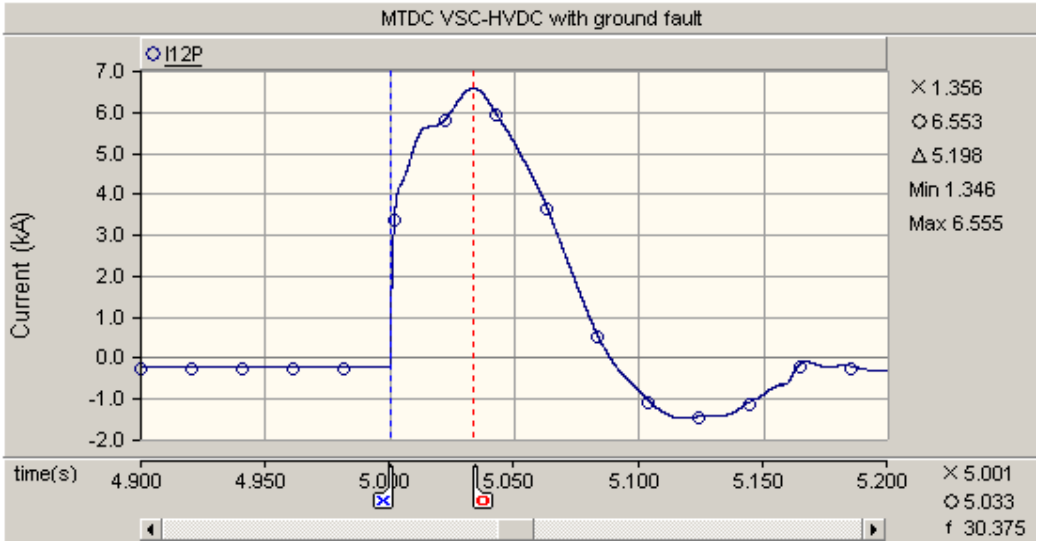

Figure 5-8: DC Current measured between cables connecting VSC1 and VSC2 during ground fault.

As mentioned in Chapter 2, the primary contributor to the initial rise of DC fault current results from the discharge of the DC-link capacitor. The discharging of the DC cable capacitance although also present has an almost insignificant contribution since the DC-link capacitor is much larger. The critical time limit recorded for this test was 0.033s and the peak fault overcurrent magnitude for the cable with a ground DC fault was measured to be 6.553 kA at time 5.033s. This magnitude is clearly much higher than that measured during normal operating conditions. This therefore justifies the necessity for a DC protection scheme and one that can manage high fault currents which operate at very high speeds.

After a few transients, a new post-fault steady state was reached at approximately 5.2s. This means that the system has fully discharged to the ground and so there are no threatening currents left in the system. An intuitive response would be to then restart or continue with the operation of the converter. Figure 5-7 also shows that even though the healthy cables were affected by this disruption, they rose to lower magnitudes. This made it easier to discern the affected cable from the rest. At the instant that the DC fault was injected into the system, an abrupt overcurrent was also experienced by the diodes, putting them at a very high risk. The diode currents (represented as iD) are illustrated in Figure 5-9. A similar response was seen when current magnitudes rose to approximately ±4.0 kA, a value much higher than their maximum magnitude of ±0.5 kA during normal operating conditions. These irregularities continued till the post-fault steady state was reached again

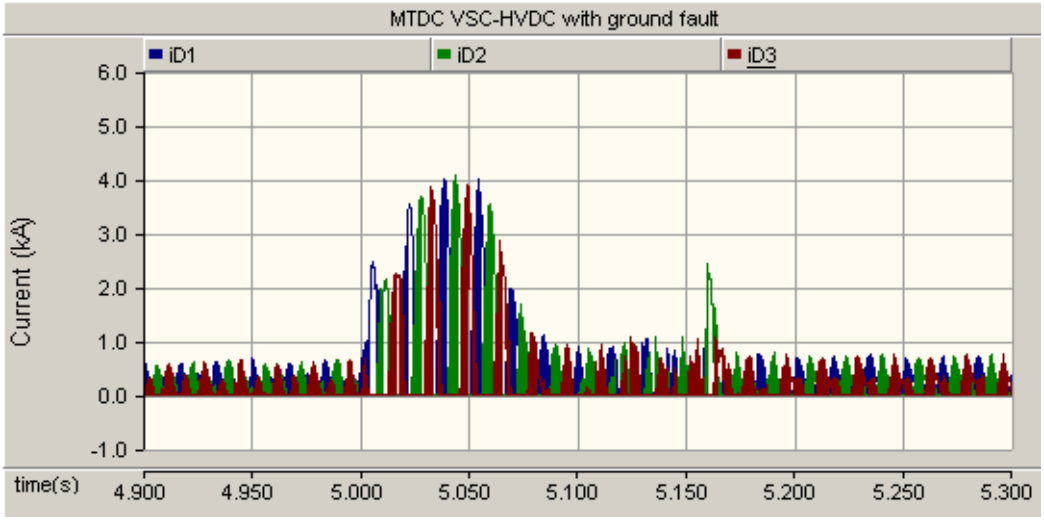

Figure 5-9: Diode current measured in terminals of VSC1.

Chapter 2 highlights that the high current rise caused by a DC fault was expected to cause a voltage dip in the VSC-HVDC system. Proof of this theory has been shown in Figure 5-10, where the DC voltage was seen dropping to a value of ±350 kV. The changes in the line voltage seem to last only for a few seconds, as voltage settles back at 400 kV even though the fault was permanent. During a ground fault however, the faulty pole was temporarily grounded. As this pole discharges to 0 kV, it exposes the healthy pole to full DC-link voltage of the system. The transients shown in Figure 5-11 illustrates the results for this case (where V12P and V12N represents the pole-to-ground voltage for the positive pole and negative pole of the DC cable respectively). In the figure, the unaffected negative pole was seen rising to full line voltage of 400 kV due to the injected DC fault in the system.

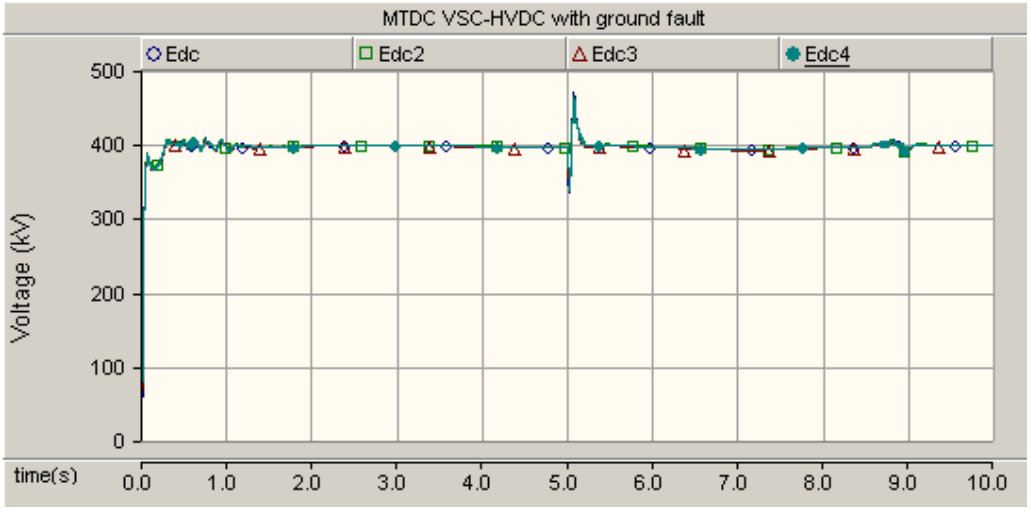

Figure 5-10: DC voltage measured between all terminals during DC ground fault.

If both cables are rated to operate under the voltage stress, the link can be operated as asymmetrical monopolar under permanent pole-to-ground fault and continue to exchange active power between the AC networks. This solution may not be feasible in the real-world applications of the VSC-HVDC link.

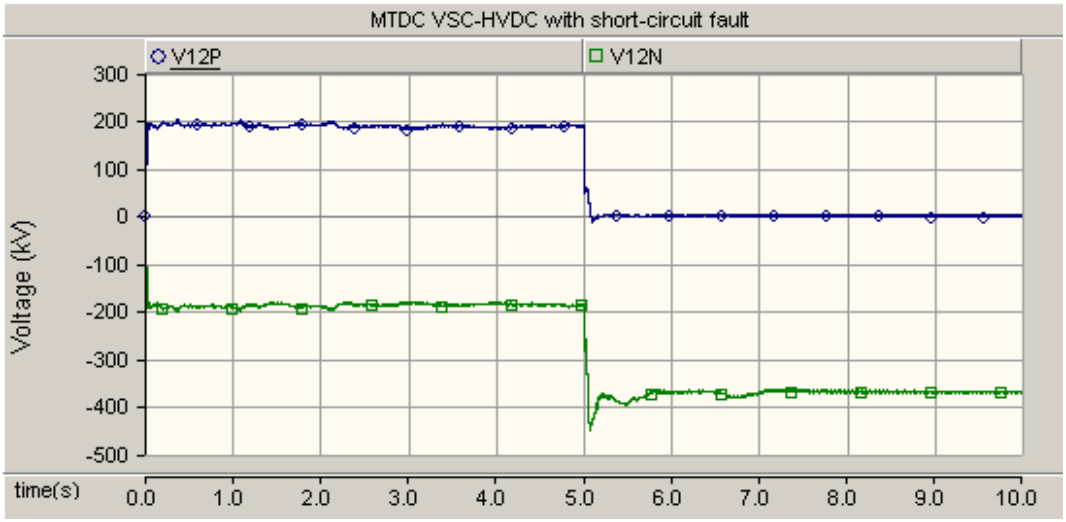

Figure 5-11: DC voltage measured between all terminals during DC ground fault.

5.2.1.2. Short-circuit fault applied 0 km away from VSC1

When the positive pole and negative pole were short-circuited, the system was threatened by a short-circuit fault. To analyse its effects, a fault was applied 0 km away from cable connecting VSC1 and VSC2. Figure 5-12 shows a very sharp rise in the DC current that threatens the converters operation. During a short-circuit fault, both poles were in direct contact with the DC fault, exposing the system to full DC-link overcurrent.

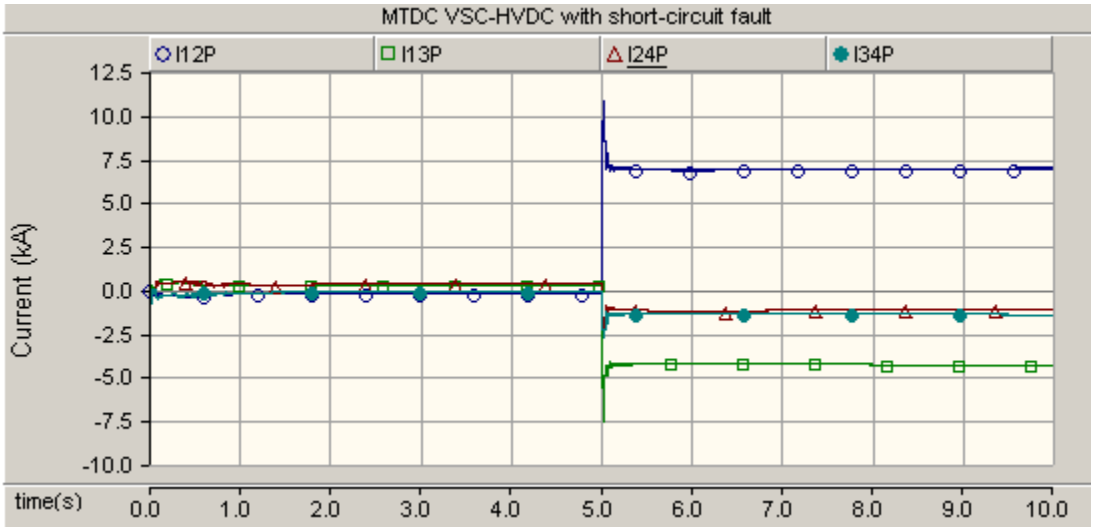

Figure 5-12: DC Current measured in cables connecting VSC1, VSC2, VSC3 and VSC4.

In Figure 5-13, the overcurrent magnitude for the faulty cable was 10.725 kA, with a critical time limit of 0.025s. This magnitude was larger than one measured during a ground-fault. These results validate that DC short-circuit faults pose a bigger threat than ground faults. The healthy cables although also affected by this disruption rose to lower magnitudes, with I13P at 7.59 kA, I24P at 2.25 kA and I34 P at 2.72 kA.

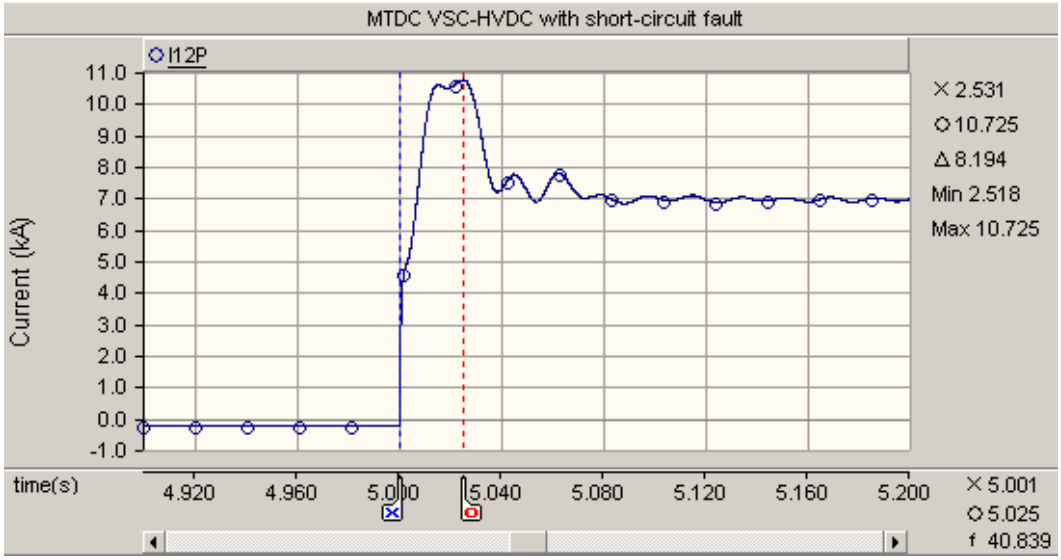

Figure 5-13: DC Current measured between cables connecting VSC1 and VSC2 during short-circuit fault.

Once the capacitor fully discharges, the diode current increases. These currents reach a magnitude as high as ±7.2 kA as shown in Figure 5-14. The diode currents decrease for a larger fault distance, as the most severe fault was expected to take place 0 km away from the converter. The measured currents vary with each individual diode. This indicates that the AC grid was now feeding the DC fault.

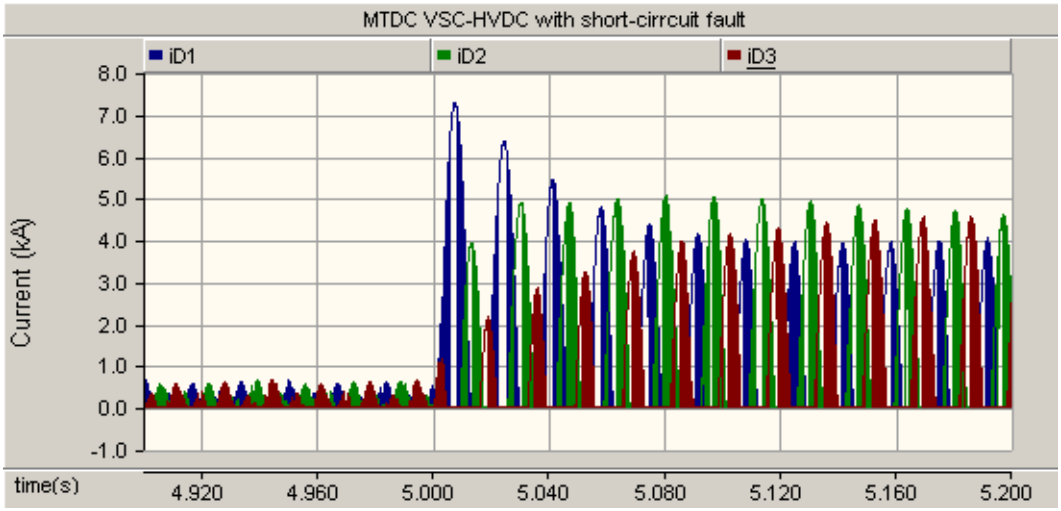

Figure 5-14: Diode current measured in terminals of VSC1.

Figure 5-15 shows the results of DC voltage during a short-circuit fault. The voltage dips to ±50 kV. This was an expected result as DC currents were still flowing through the diodes. Unlike ground faults, high currents and low voltage remain for the duration of the test. This was mainly because both poles were affected and so both were exposed to the same stresses during the DC fault. Since short-circuit faults are mostly permanent they should be disrupted by isolating the affected cables from the rest of the network.

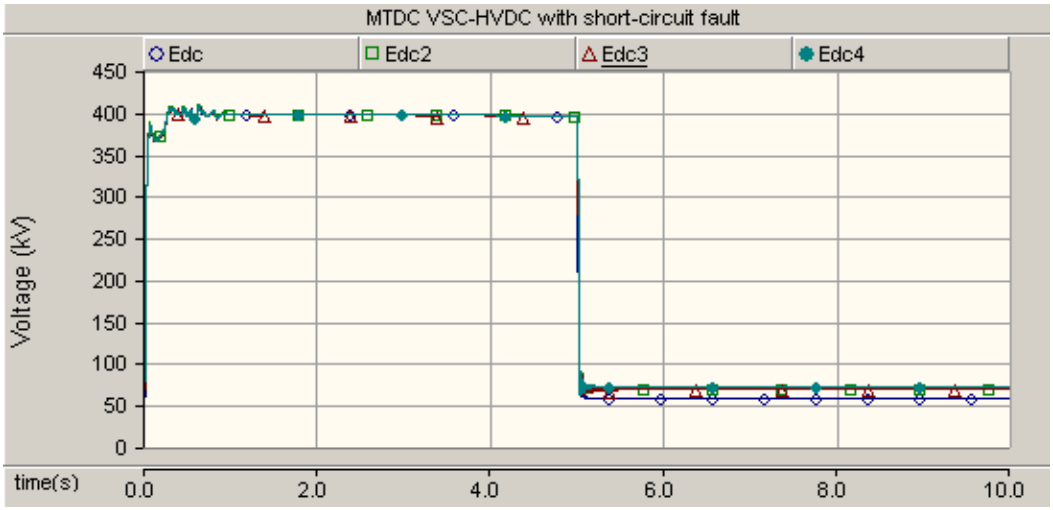

Figure 5-15: DC voltage measured in cables connecting VSC1, VSC2, VSC3 and VSC4.

Current signals ultimately carry very important information, since from them, the affected cables can be identified. For ground faults, the currents in the faulted pole rises to magnitudes higher than those of the unaffected cable. An additional threat during such faults was also the overcurrent experienced by the healthy pole. For short-circuit faults, although there were less chances of over-voltage, both poles experienced the disturbance therefore, a more severe overcurrent disruption was experienced. A distinction was seen between the different fault types injected into the network and was only evident in the small variations of the DC current magnitude, the fault signature and the duration of the DC fault. The rest of Chapter 5 will therefore focus on the more severe short-circuit faults.

5.2.2. Effect of fault location

Short-circuit DC cable faults with different distances to VSC1 were simulated in cable DC12 to investigate the effect of fault location. To implement the faults with various locations effectively, cable DC12 was modelled into various segments of 10 km, 30 km, 50 km and a 100 km in length. The results presented were measured and recorded at VSC1 during the different scenarios. Factors of interest during this test mainly include the magnitude of peak current and the critical time. To investigate the effect of distance, a fault was initially injected 10 km away from station VSC1. At 5s, the current gradually rose linearly as seen in Figure 5-16.

During this test, the fault current rose to a magnitude of 9.061 kA in 0.042s. Although the rise in magnitude was still sharp, a slight decrease in magnitude was seen during this test when compared to the scenario where a fault was injected 0 km away from VSC1 shown in Figure 5-13. This was largely due to the introduction of distance. The time to peak increased from 0.025 kA at 0 km to 0.042 kA at 10 km validating that the DC faults were a bigger threat when close to converter as they rose to peak values at a very high speed

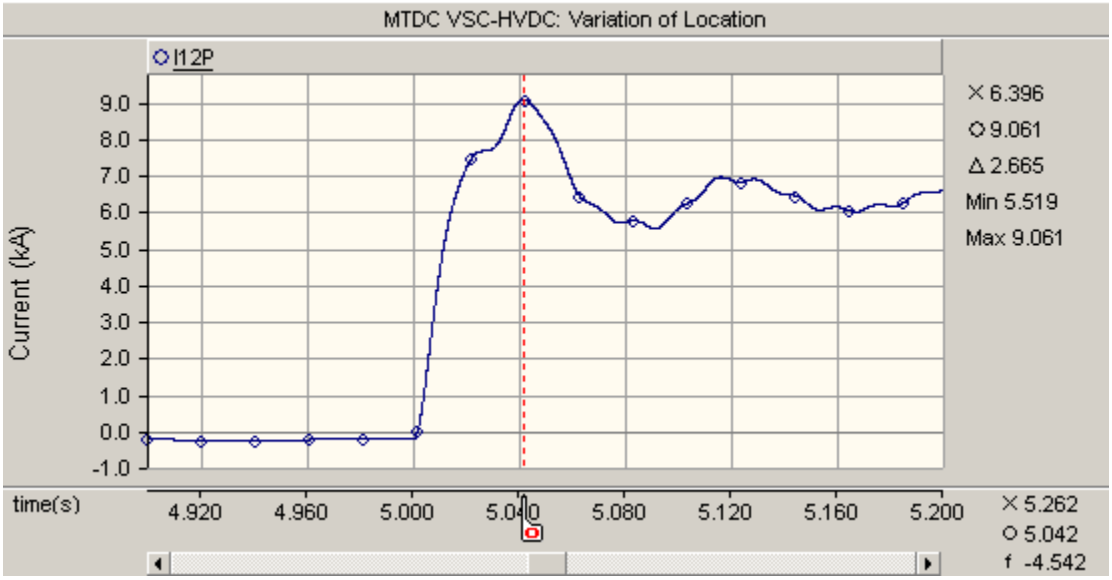

Figure 5-16: DC Current measured 10 km away from terminal VSC1.

Results obtained during the test of different fault distances have been depicted in Table 5-1. They confirm that distance between a VSC station and a DC fault have a significant impact on the characteristics of current. DC faults occurring close to the converter result in an almost immediate change. In this case, the rise of current was not only faster but the DC current magnitude was also high. This means that the converter was exposed to a greater threat. For longer distances, the DC critical time limit was not only reached later but the severity of the fault decreases because of the larger impedance between the VSC terminal and the DC fault point.

Table 5-1: The effect of varying fault distance during a short-circuit fault.

Fault distance	**10 km**	**30 km**	**50 km**	**100 km**
Fault current (kA)	9.059	8.733	8.282	7.405
Critical time (s)	0.0420	0.0448	0.0452	0.0471

Thus, it can be deduced that DC faults closest to VSC1 result in larger DC current magnitude and a shorter critical time. An additional observation was made when zooming in on Figure 5-16. In this plot, the travelling wave effect in the DC current flowing out of VSC1 was observed as the current was rising in a stepwise manner. This characteristic was useful in the design of the protection scheme.

5.2.3. Effect of fault impedance

To investigate the effects of fault impedance, DC cable short-circuit faults with fault impedances of 0.01Ω, 1Ω, 10Ω, 50Ω were simulated in cable DC12 at time t=5s. These faults were implemented one at a time at a distance 50 km away from VSC1. To investigate the effect of varying the injected fault impedance, a short-circuit fault of 0.01Ω, was injected into the system. A rise in current was seen exactly at 5s as in Figure 5-17. The fault current rose to a magnitude of 11.56 kA in 0.037s. The results obtained during the test of fault impedances are depicted in Table 5-2. Results show that fault resistance had a limiting effect on the fault current. Unlike in these tests however, fault impedance cannot be naturally controlled and so this analysis was carried out only to find cases that would pose the most threat, analyse the response of the system during these worst-case scenarios and design a protection scheme that would be effective even in such cases.

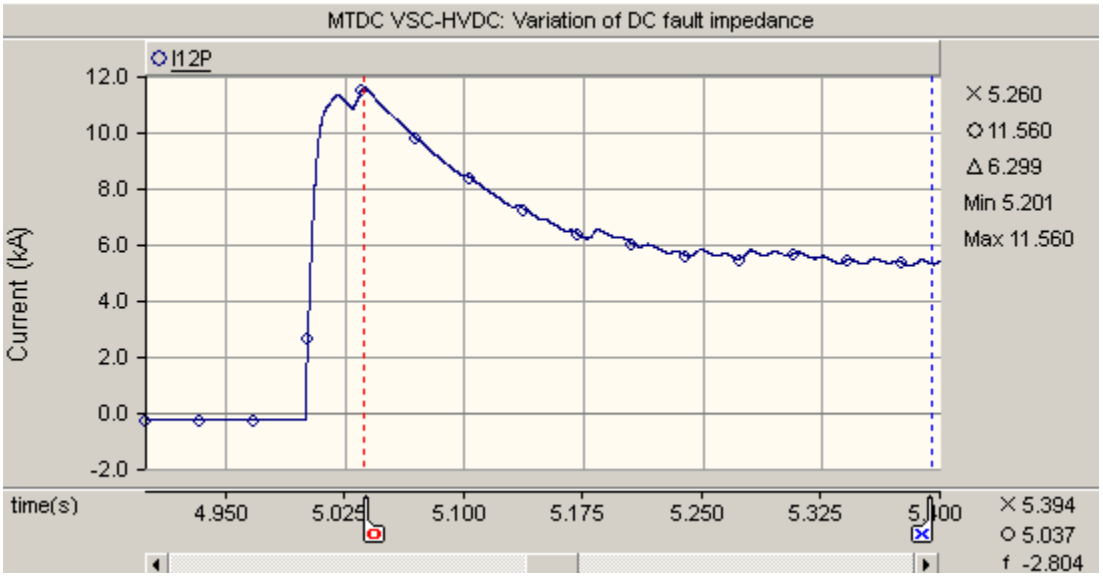

Figure 5-17: DC Current measured for 0.01Ω in terminals of VSC1.

Table 5-2: Varying fault impedance of the short-circuit fault.

Fault impedance	**0.01 Ω**	**1 Ω**	**10 Ω**	**50 Ω**
Fault current (kA)	11.560	10.477	7.914	4.001
Critical time (s)	0.037	0.0373	0.039	0.055

The rise of the current magnitude experienced during the discharge of the converters DC-link capacitor were mostly affected by the implemented AC filter, the DC-link and line capacitance, the injected fault impedance as well as the cable impedance. Using the equation (5-1) [70] given as: -

$$\tau = RC_{DC} \qquad (5\text{-}1)$$

The time constant is directly proportional to R (representing the total impedance) and C_{DC} (representing the system DC capacitance). This would mean that an increased fault impedance would result in an increased critical time

A clear conclusion from these tests was that an increased DC fault impedance resulted in reduced peak fault current and an increased critical time due to the increased time constant. The most severe case was seen during the lowest impedance. This means that for effective protection, the designed protection scheme should be able to handle currents as high as 11.560 kA.

5.2.4. Effect of fault capacitance

Using equation (4-4) presented in Chapter 4, the DC-link capacitance was calculated to be 300μF. This value has been kept constant for all investigations done thus far in this study. The DC-link capacitance is famously known to keep DC voltage constant and additionally acts as a DC-side filter. It is however also regarded as one of the biggest contributors to the rise in fault current. Equation 4-4 presented in Chapter 4 can also be used to set the upper and lower limits of the size of the DC-link capacitor. In this case, the equation uses the minimum and maximum rated power and DC voltage that can be withstand by the system without posing a threat to it. The maximum values are set at 105%, while the minimum values are set at 95 % of the rated values. For this investigation the lower and upper limits for the DC-link capacitance are therefore selected to be 250μF and 350μF respectively.

To investigate the effect of varying DC-link voltage, magnitudes ranging in the above limits were implemented on the system. Due to the switching action of the IGBTs, the DC-link contains harmonics. These produce a DC voltage ripple. The DC voltage ripple should however be small enough for the voltage to be virtually constant during the switching period. This characteristic was used to set the lower limit of the capacitor size. The distance was kept constant at 50 km from VSC1 and the fault impedance was kept as 5Ω. Initially, capacitors valued at 200.0μF were implemented to the system. During this test, a rise in current was seen exactly at 5s in Figure 5-18. The fault current rose to a magnitude of 9.002 kA in 0.0360s.

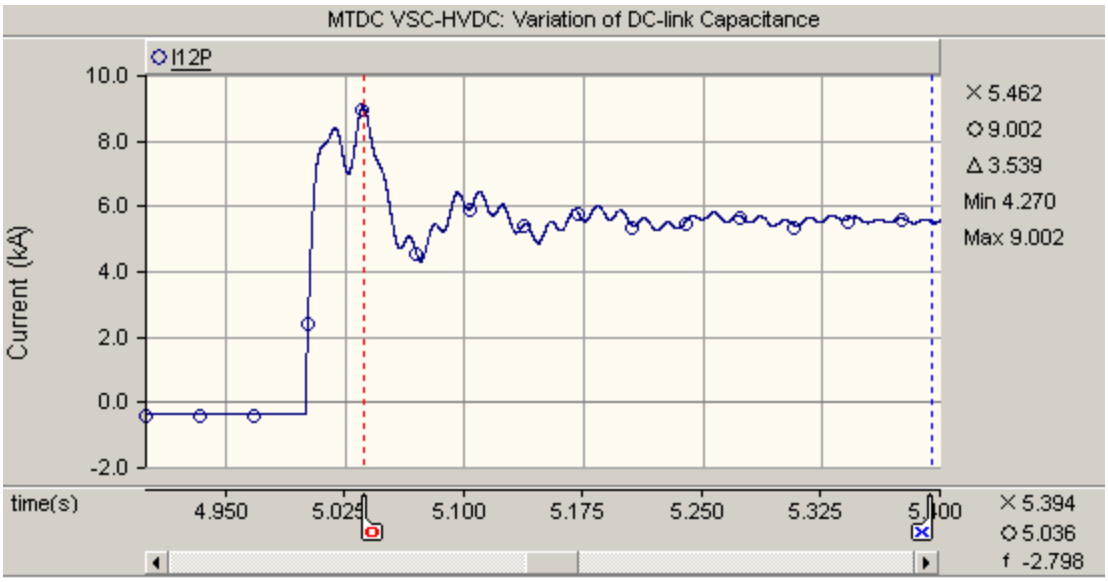

Figure 5-18: DC Current measured for 250.0µF.

Results obtained when varying the DC-link capacitance are presented in Table 5-3. From these results, it can be concluded that reducing the magnitude of capacitance results in lower fault peak current. The smaller DC-link capacitors take longer to reach the critical time limit; however, they are also quick to get discharged. The opposite was seen to be true for DC-link capacitors with higher magnitudes. Considering the use DC-link capacitors with smaller magnitudes seems almost like the best choice. This choice however holds its own disadvantages, as at low capacitor magnitudes the signals have more noise.

Table 5-3: The effect of varying DC-link capacitance during the short-circuit fault.

DC-link capacitance	**250µF**	**275µF**	**325µF**	**350µF**
Fault current (kA)	9.002	8.968	9.020	9.111
Critical time (s)	0.0364	0.3670	0.0390	0.0391

5.2.5. Summary

The objective of carrying out a fault analysis for the network was to determine the networks strengths, weaknesses and its limits. This has been tested by varying different parameters including the fault type, distance, fault impedance and finally the magnitude or size of the DC-link capacitor. Conclusions that can be drawn from this analysis, indicate the importance of selecting the right size of your components for the designed network.

The dangers were posed mostly by the fault overcurrent fuelled by the discharge of the DC-link capacitors. Taking from these results, a good protection strategy would be to clear the faults before the critical time limit can be reached. This should protect the system from overcurrent. The key to effectively protecting a MTDC VSC-HVDC network during a DC short-circuit fault lies in the fast disconnection of the affected DC cable before its current magnitude exceeds an uninterruptable current state. Results obtained during tests dictate that when a DC fault occurs, the system should proceed to correctly detect, precisely locate and isolate the faulty cable within 5ms.

5.3. VSC-HVDC protection strategies

In this section, the output results of the proposed protection strategies are presented and discussed. This analysis includes both the main and back-up protection strategies introduced in Chapter 3. From this analysis, it should be easier to propose strategies that would be most suitable for the developed MTDC VSC-HVDC network and similar systems. For all tests, the faults were implemented at 5s with a constant fault impedance of 5Ω used.

5.3.1. Detection techniques

As mentioned, there are numerous DC fault detection techniques available for VSC-HVDC systems. Most of them are adopted from methods used in HVAC and in the conventional HVDC networks. However, a faster DC fault localisation technique is required since the time frame available to distinguish and isolate DC faults in a VSC network is limited. The results and discussions of the proposed detection strategies are detailed below.

5.3.1.1. Wavelet transform

The travelling wave, discrete wavelet transforms (DWT) detection technique is currently suggested as one of the most promising detection strategies. The DWT technique detects the wave front affected by a DC fault in a short space of time, and in addition aiding in the process of distinguishing the faulty line from other healthy lines. Each wavelet transforms results in a total of 6 wavelet coefficients, and only one of these were used for fault detection. Figure 5-19 shows the output results detailing the coefficients of all 6 levels detected at DC12P, DC13P, DC24P and DC34P for the implemented mother wavelet. Lu [67] recommends using only one level for the detection of a fault, which is usually the highest coefficient level. Results presented in Figure 5-19 show that the 6^{th} level coefficient (in the lime/ avocado green colour) mostly reaches the highest coefficient level.

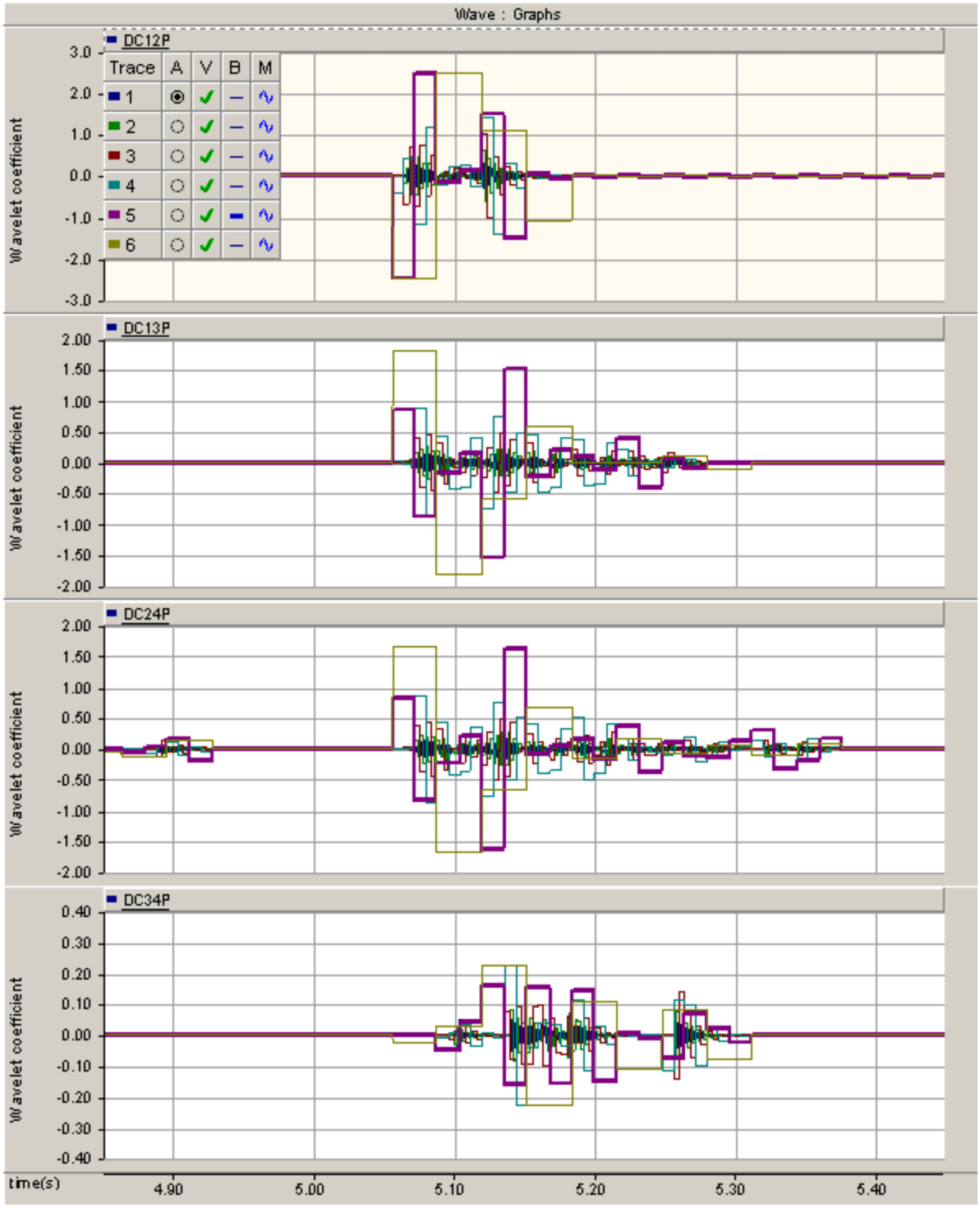

Figure 5-19: DWT signals for cables connecting VSC1, VSC2, VSC3 and VSC4.

A high coefficient level indicated that the signal was less sensitive to noise. It was however also evident that with the highest coefficient level, all the measured coefficients were relatively close to each other.

This makes it rather difficult to discern the DC cable affected by the fault, thus jeopardising the methods selectivity. Using this level for fault detection would not recommendable. The next step would be to find the next highest coefficient level which will also easily integrate the principle of selectivity. Considering the above, the 5th level coefficient highlighted in the purple colour was chosen for implementation. This means that the scope will only consider the detailed coefficients of the 5th level detected at DC12P, DC13P, DC24P and DC34P to distinguish DC faults, as shown in Figure 5-20. To detect a DC fault, the chosen output level of the wavelets was compared to a threshold value. From this investigation, a cable affected by a DC fault can be easily distinguished when its voltage levels exceed those pre-set as the threshold. The coefficient levels of the affected cable rose to higher levels discriminating the faulty cable from the rest of the system

In this study, the Haar mother wavelet was used for testing DC faults located at various distances away from VSC1. Figure 5-20 highlights the DC breaker signal generated when a fault has been detected using the DWT technique. In this diagram, it was quite evident that the signal can only pick-up the presence of a DC fault in the system only 0.038s after the DC fault was implemented on the system. This is regarded as the signal delay time and could ultimately affect the duration of a protection scheme. Since it has been determined in the previous section that distance influences the DC response of the VSC-HVDC system, the DWT analysis was carried out at various locations. Table 5-4 summarised the obtained results.

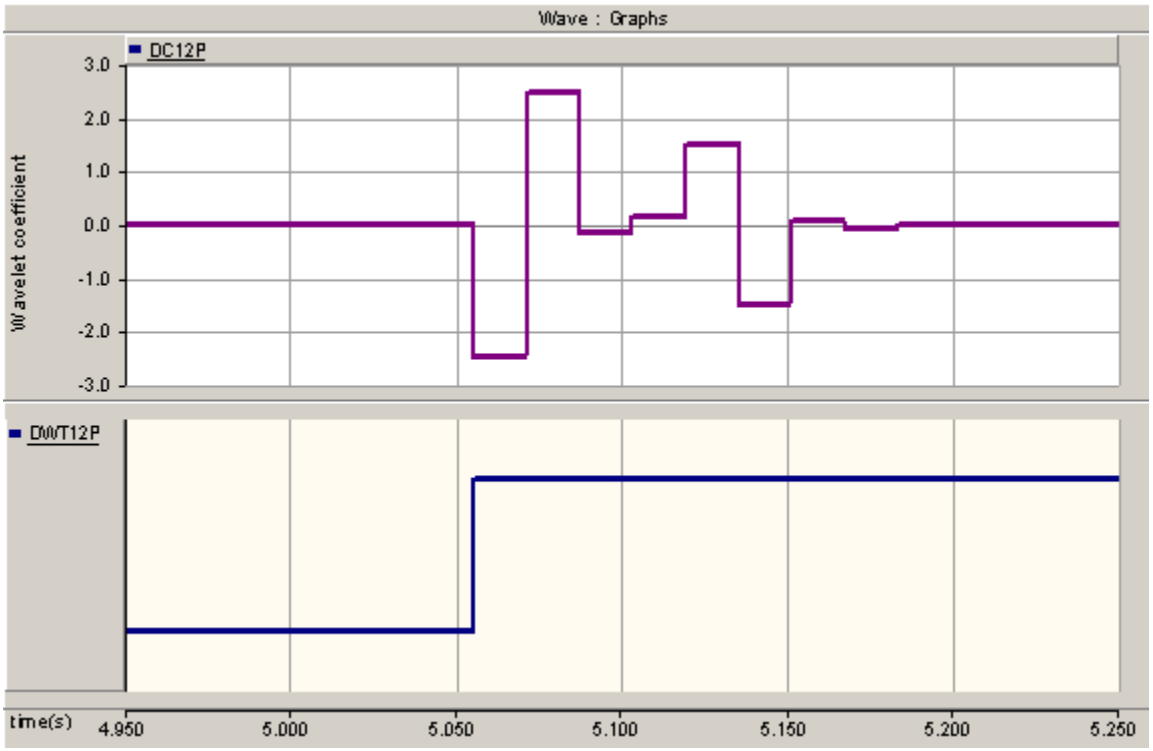

Figure 5-20: 5th-level coefficient with detection signal.

Table 5-4: The 5th level detail wavelet coefficients magnitude.

Magnitude		Haar (5th level)			
Distance from VSC1		**10 km**	**30 km**	**50 km**	**100 km**
DC12P (faulty)	**Wavelet coefficient**	4.206	3.890	3.533	2.900
	Breaker signal delay time	0.038s	0.040s	0.041s	0.042s
DC13P (healthy)		2.6	1.8	1.600	1.4700
DC24P (healthy)		1.7	1.6	1.576	1.4500
DC34P (healthy)		0.3	0.1	0.060	0.490

From the results shown in Table 5-4, the magnitude of wavelet coefficients decreases with increasing distances. Again, this then confirms theory that states that a DC fault was most severe when it was closest to the converter [52]. On the contrary, the breaker signal delay time seemed to increase with increasing distance. This was mainly due to the increased cable impedance that keeps increasing as the distance kept being increased. The calculation required for the DWT protection technique are quite complex. Applying this technique in real-life could be therefore a bit more challenging.

The time window given to calculate the wavelet coefficients affects the delay between the detection of the trip signal and an increase in the DWT level. The size of the time window depends mainly on the type of mother wavelet chosen, the number of levels chosen for the DWT technique, and the sampling frequency. Higher coefficient levels usually require extra computation times. This would further increase the delay between the wavelets and the produced detection signal. This means that lower levels of the DWT could potentially reduce the delay time. In this study, since the 5th level Haar wavelet transform works were desirable and effective, lower level wavelet transform were not tested. To enhance the performance of the DWT technique, Wavelets can be coupled with a back-up protection scheme as an auxiliary unit. The best back-up protection technique would be one that can introduce the factor of finding the precise location of the fault.

5.3.1.2. Overcurrent protection

As reported throughout this study, the results of overcurrent were the general way of detecting the presence of a DC fault in a VSC-HVDC system.

The technique explored during the DC fault analysis was carried out in Section 5.2. An advantage of this method was simplicity that resulted in less calculations and its breaker signal was detected almost immediately after the fault was detected as shown in Figure 5-21. Protection using overcurrent was further explored in this section. From the plot shown in Figure 5-22, the peak DC current magnitudes measured at DC12P, DC13P, DC24P and DC34P rose during the DC fault period. As expected, the current magnitude recorded in DC12P were much higher than the rest of the signals. This means that cable DC12P was distinguished as the faulty cable. The magnitudes were however not that far apart from each other which raised questions on the methods selectivity.

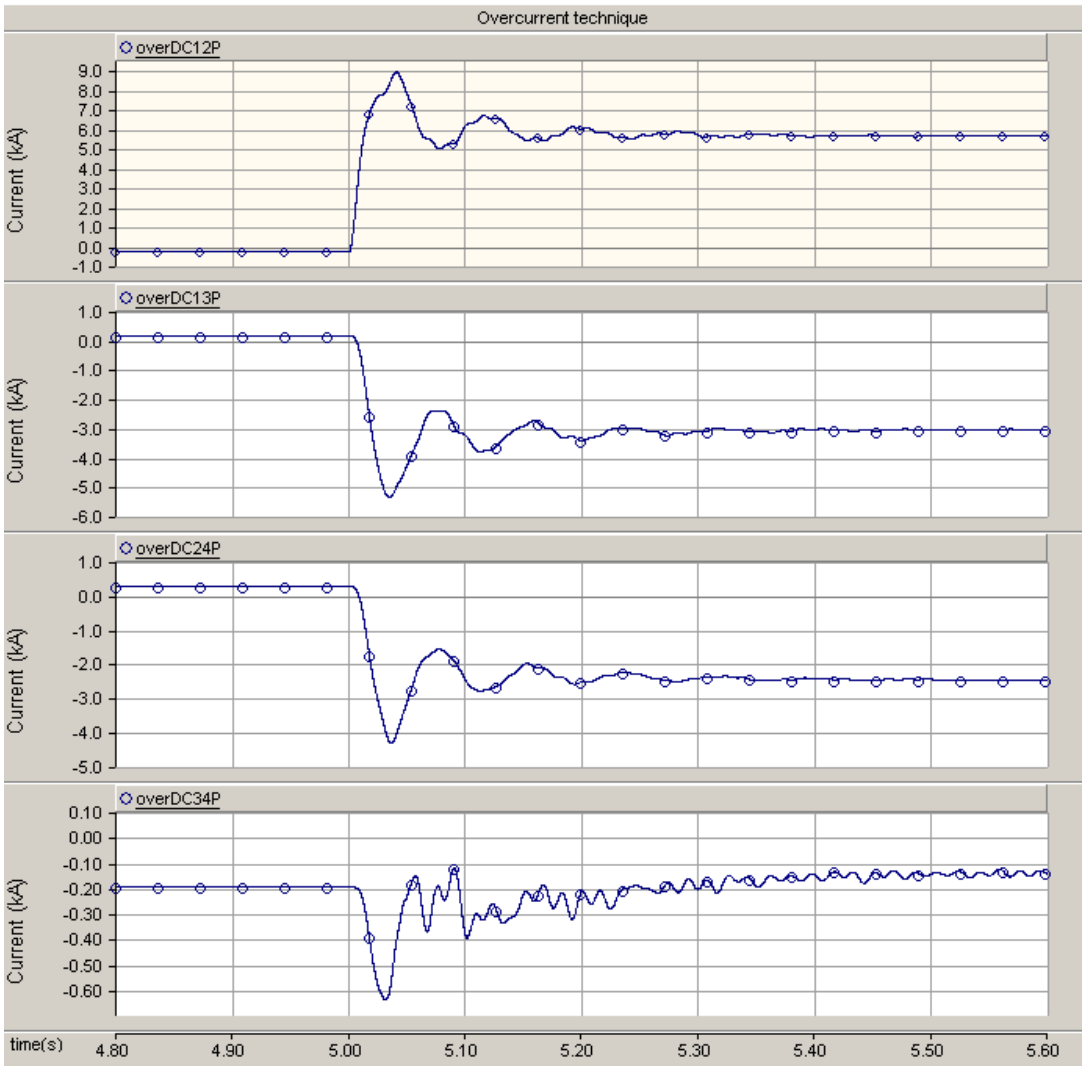

Figure 5-21: Overcurrent measured 10 km away from terminal VSC1.

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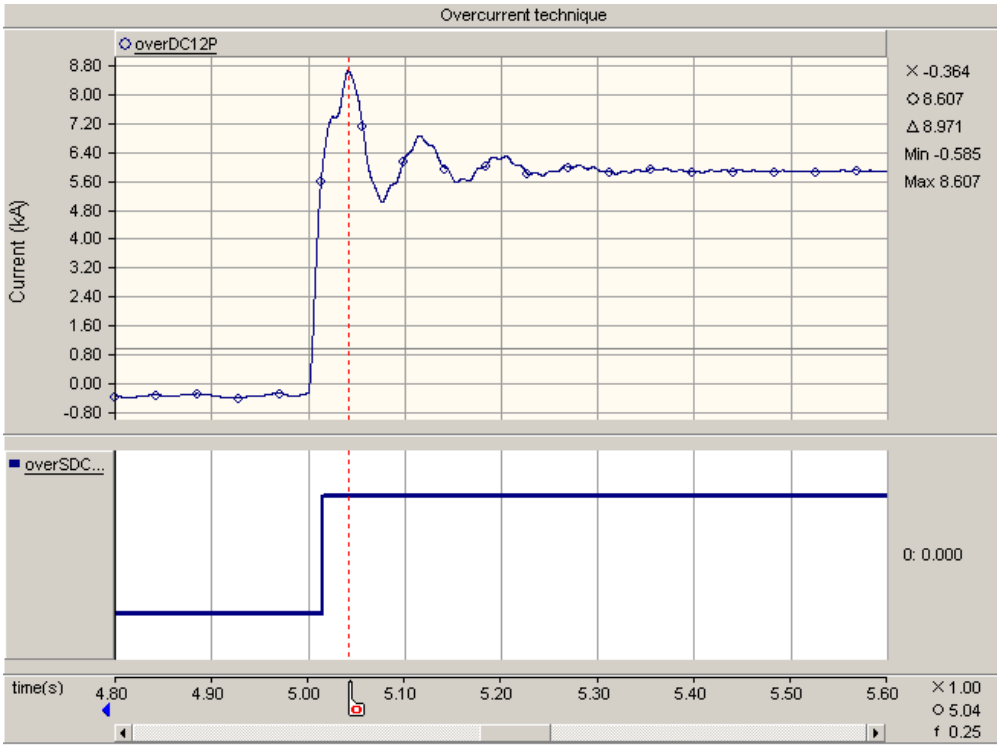

Figure 5-22: DC Current measured 10 km away from terminal VSC1.

Table 5-5 summarises the maximum DC fault current magnitudes measured at different DC fault distances. Again, the highest magnitudes were recorded at the distances that were closest to the converter station. In practice, at very high DC fault current magnitudes, fuses or instantaneous overcurrent relays can be used to clear the fault current before they have the chance to damage the entire network

Table 5-5: Analysis of overcurrent protection

Magnitude	**Overcurrent magnitude (kA)**			
Distance from VSC1	**10 km**	**30 km**	**50 km**	**100 km**
DC12P (faulty)	8.607	8.202	7.871	7.141
DC13P (healthy)	-5.174	-5.006	-4.809	-4.376
DC24P (healthy)	-4.185	-4.457	-4.634	-5.141
DC34P (healthy)	-0.645	-0.419	0.250	0.966

In terms of protection, the overcurrent protection method lacks selectivity and was therefore not recommended as a main protection scheme for the MTDC VSC-HVDC system. However, it was regarded as a good candidate for back-up protection due to its simplicity.

5.3.1.3. Differential protection technique

A different option available for back-up protection includes the use of the differential detection technique. As mentioned in Chapter 2, due to different factors, the current magnitudes measured from the opposite ends of a cable were slightly different. This information can be gathered to detect the presence of a DC fault on the developed system. The technique was investigated in this section to decide whether it would be suitable for the developed VSC-HVDC system.

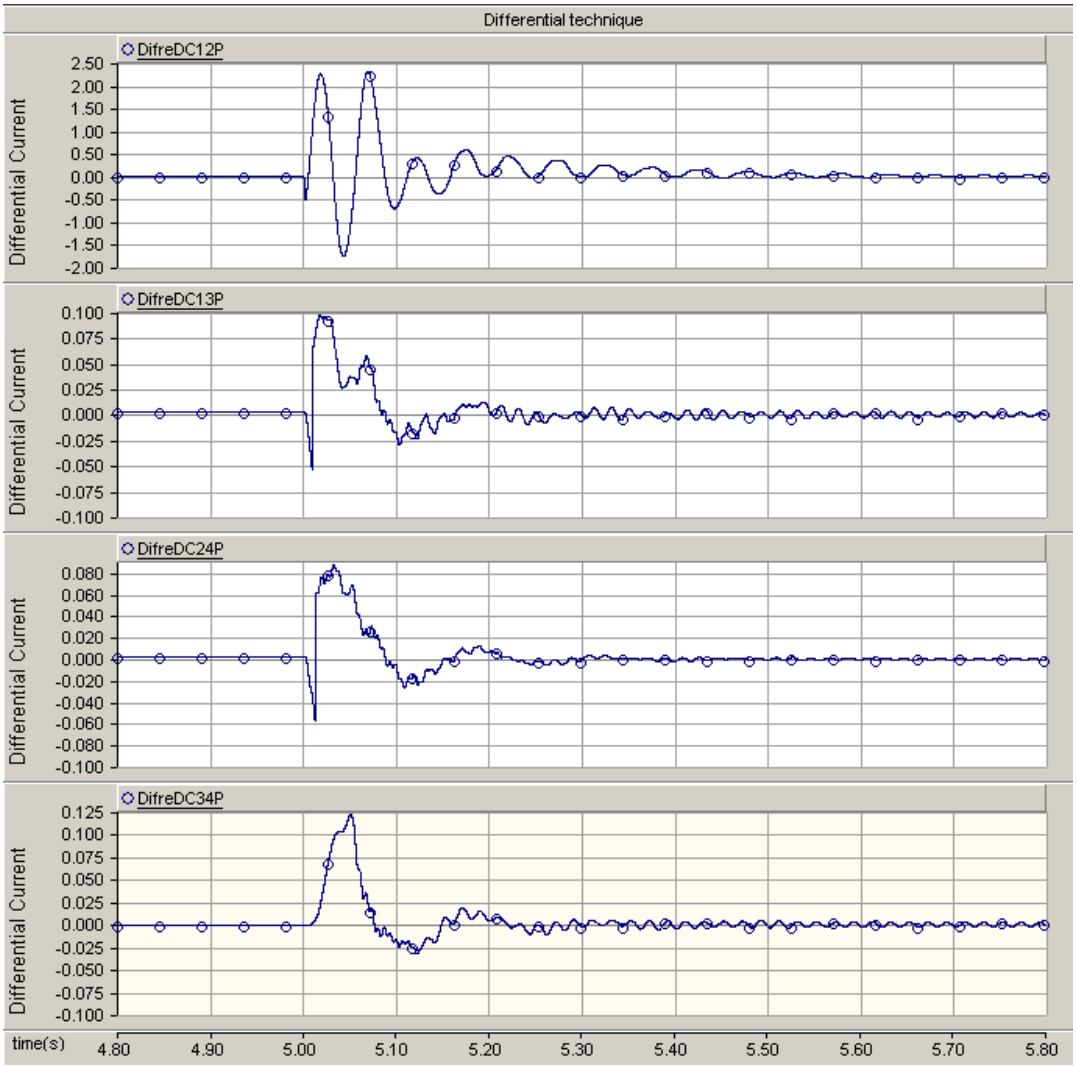

Figure 5-23: Differential current 10 km away from terminal VSC1.

From Figure 5-23 the differential protection method proves to be highly selective when detecting DC faults. This was shown by the magnitudes recorded, as they were much higher in the faulty cables than in the healthy cables. The difference was also much further apart than with previously discussed techniques.

From the plots shown in Figure 5-24, the faulted pole (DC12P) resulted in the highest DC current magnitude which was measured to be 2.307 kA at 0.069s. The results shown in Figure 5-24 also depict the time delay associated with the detection of the fault. This was mainly due to wave attenuation and the delay that comes with the gathering of information from each station on both ends of the cable, otherwise known as communication delay. The reliability of the differential DC fault detection technique could be ultimately reduced by its dependence on communication.

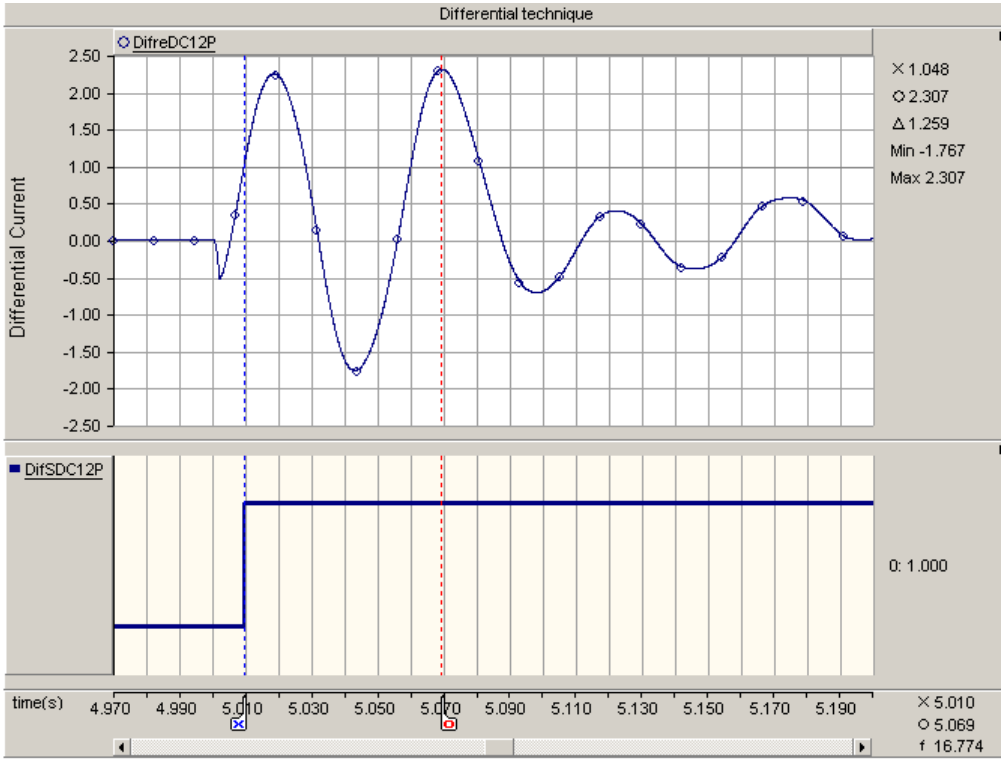

Figure 5-24: Differential current 10 km away from terminal VSC1.

Table 5-6 is a summary of the obtained results during the differential detection tests at different DC fault distances. It can thus be concluded from this test that: -

- During a DC fault, the resulting differential current magnitude was reduced to some extent as one advances along the transmission cable.
- Differential protection provides an intrinsic selectivity. This was independent of the of the fault location distance as it was true for all measured fault positions.
- For faults located further from the VSC station, the maximum differential magnitude detected at the healthy poles were similar as the transients at increased distances were less significant.
- Although not clearly shown, the most threatening stage can be avoided at DC fault distances located further from the VSC station as voltages never completely drop to 0 kV.

Table 5-6: Analysis of differential protection.

Magnitude	Maximum I_diff detected at converter with time delay			
Distance from VSC1	**10 km**	**30 km**	**50 km**	**100 km**
DC12P (faulty)	2.307	0.930	-1.33	-5.1
DC13P (healthy)	0.096	0.093	0.088	0.084
DC24P (healthy)	0.087	0.086	0.087	0.108
DC34P (healthy)	0.121	0.122	0.119	-0.115

Results obtained during tests carried out on differential protection proved its outstanding selectivity. Accuracy of this technique depends highly on the information transferred between communication links. This means that an error in communication could result in a false decision imposed on the network. To improve its reliability, the method should be coupled with other available detection techniques. Although not shown in this study, the methods reliability also depends greatly of the length of the transmission cable such that longer DC cables could result in a significant time delay due to communication. This could have negative effects on the entire protection scheme of the network. Overall the technique was a good candidate for fault detection. Its drawbacks however, were too big to ignore especially if considering expansion of the network. The method was therefore not selected for implementation.

5.3.1.4. Derivative protection technique

Derivative protection is mostly favoured for its unique capability of indicating DC fault direction. This information mostly aids in improving the selectivity of the entire protection scheme. Due to its high sensitivity to noise that impedes on reliability, derivative protection is only limited to play its role as back-up protection for the system. High current derivative results in the affected cable during a DC fault. This magnitude differs greatly to that measured at the unaffected DC cables.

With previously discussed detection techniques, the general principle in this technique was that when the magnitude of the derivative value exceeds the set threshold, a fault was identified. The pre-defined threshold value could be set to lower magnitudes if the technique was co-ordinated with another back-up protection. This was however not explored in this study. In the simulation, the derivative detection technique was tested out for faults located at various distances away from VSC1. Figure 5-25 shows the output results of the derivative magnitudes measured at DC12P, DC13P, DC24P and DC34P 10 km away from VSC1. Firstly, these results confirm the theory that the resulting current derivatives have more noise. This was depicted by the continued ripples seen even after the initial peak. It was more evident in the graph showing DerDC34P as its highest magnitude was closer to the rest of the resulting oscillations.

Coupling the method with a different technique is recommended, just to confirm the presence of a fault in the network. The polarity of the initial spike of the derivative magnitude determines the DC fault direction. A negative current magnitude denotes that the DC fault has occurred behind the protected zone, while a positive polarity denotes the opposite. Using this information, Figure 5-25 then also re-confirms that the system detects a fault only on the cables connecting VSC1 and VSC2. The maximum current derivatives measured also correspond with arrival of the current waves. This was information was used to find the exact location of the injected DC fault.

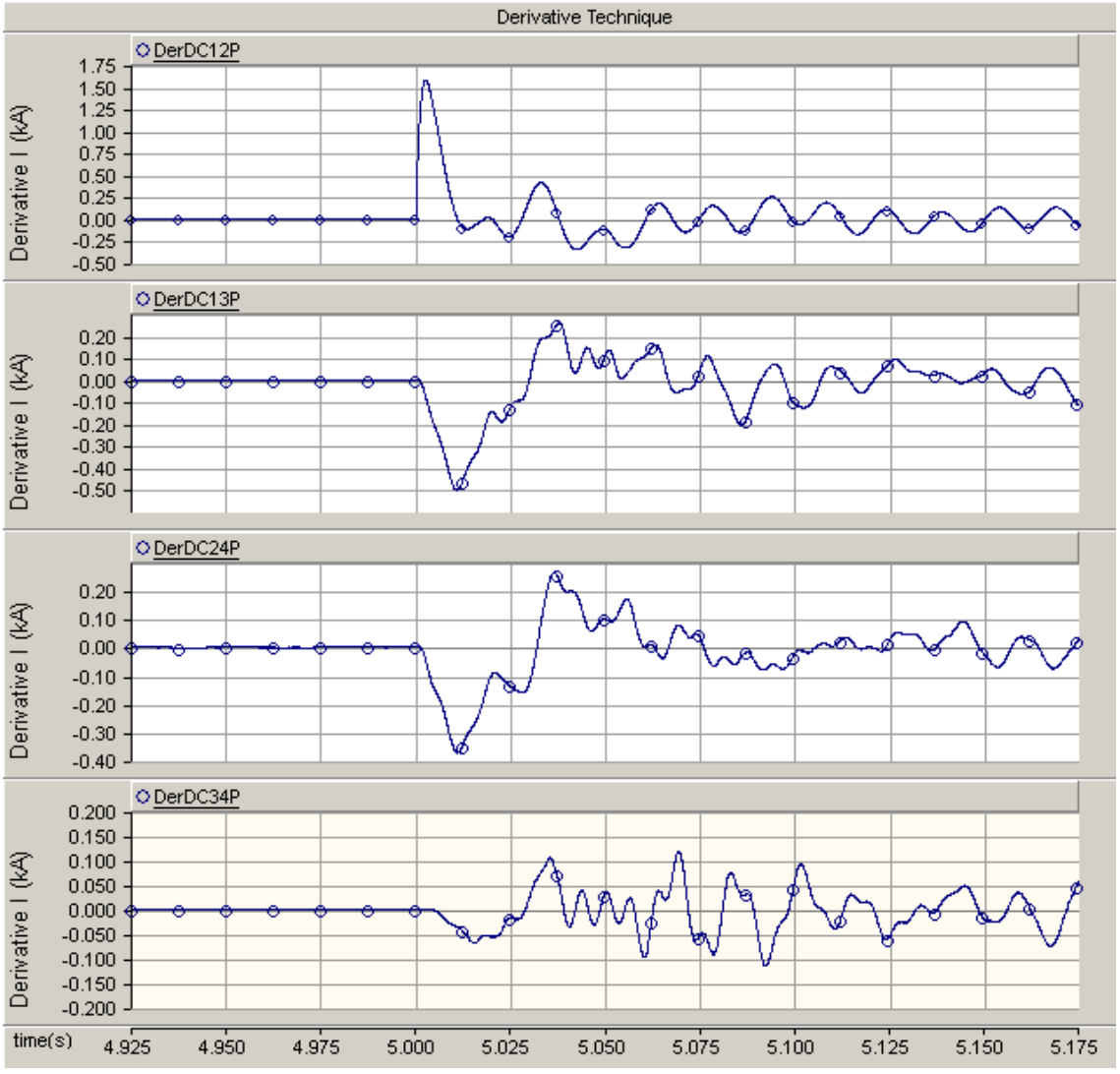

Figure 5-25: Derivative current 10 km away from terminal VSC1.

A summary of the peak derivative currents is presented in Table 5-7. It can thus be concluded that at DC fault distances further from the VSC, current derivatives were smaller. The main reason being the increased fault path impedance associated with the increase in distance.

Additionally, Figure 5-26 highlights the DC breaker signal generated when a fault has been detected using the derivative technique. In the diagram, it was evident that the signal can only pick-up the presence of a DC fault in the system exactly at 5s when the fault was triggered. This means that it has reduced delay time and should perform faster that the previously presented techniques.

Table 5-7: Analysis of derivative protection.

Magnitude		**dI_DC/dt Maximum magnitude**			
Distance from VSC1		**10 km**	**30 km**	**50 km**	**100 km**
DC12P (faulty)	**Derivative magnitude**	1.578	1.488	1.382	1.233
	Breaker signal delay time	0.0030	0.0022	0.0015	0.0010
DC13P (healthy)		-0.498	-0.479	-0.454	-0.385
DC24P (healthy)		-0.373	-0.424	-0.455	-0.558
DC34P (healthy)		-0.102	-0.089	-0.074	-0.052

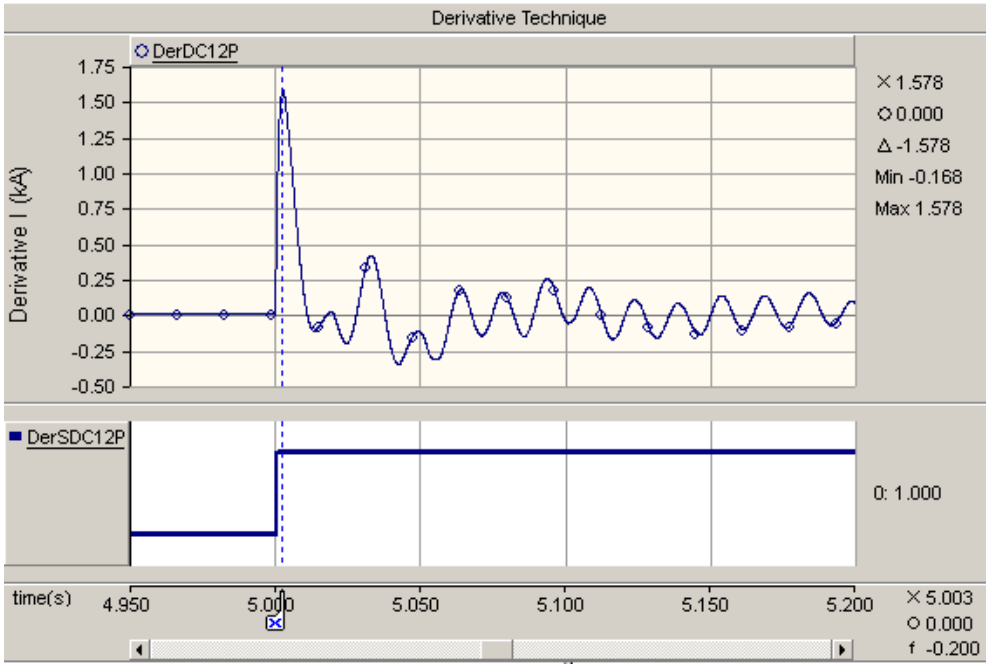

Figure 5-26: Derivative current 10 km away from terminal VSC1.

It can thus be concluded that the recorded current derivatives increased rapidly to very large magnitudes for short distance faults. At increased DC fault distances, the magnitude was decreased.

Due to its sensitivity to noise the method should be used in conjunction with others. The initial derivative peak polarity recorded for all DC fault locations did however prove reliable for determining fault direction. Its capability in indicating fault direction helps in improving the performance of other techniques and it was therefore very strategic to include as back-up protection.

5.3.2. Fault location

As briefly mentioned in Section 5.3.1.4, during a DC fault, the effect of an arriving derivative transient wave can be used to estimate the location of a DC fault. The derivative at the faulty cable is usually characterised by a higher derivative magnitude than those at the healthy cables; making it easy to detect only the affected cable. The arrival times of the derivatives could then used to find the precise location of a DC fault in a VSC-HVDC network. For the single terminal travelling wave fault locator (also known as Type A), the sample rate should be high enough to detect and identify the wave front. The distance was calculated using the equation presented in equation (3-15) found in Section 3.3.1.1.

The wave velocity in the fault distance equation, can either be measured from tests done prior to the systems operation or can be calculated from the properties of the DC cable. For this study, wave velocity was calculated using equation (3-22) of Chapter 3. Using current derivative data that was stored during DC fault detection, the arrival times of the derivative transient waves can be obtained. Given that the test models simulation time was set at 10 μs and the wave velocity was calculated to be 198 km/ms, the range allowed for error of the located distance was ±1.98 km. The exact distance of a DC fault was then estimated using the wave velocity, recorded arrival times.

Unlike the rest of the tests carried out, determining the correct DC fault distances proved to be easier when using a MATLAB code. The details of this code are found in Appendix A. Figure 5-27 depicts the arrival times taken to locate a fault injected at a distance 10 km away from VSC1. The results obtained during other test scenarios are summarised in Table 5-8. From these results, one can clearly pick out the peaks above the threshold values. Using the MATLAB code, the distance between VSC1 and the fault was then estimated by the Type A travelling wave location method. In this case the information recorded for DC faults located 10 km away from the VSC terminal were omitted. The main reasons being that the resulting information was incorrect. This could be due to noise. This proves that for this technique it can be difficult sometimes to identify the DC fault in the system.

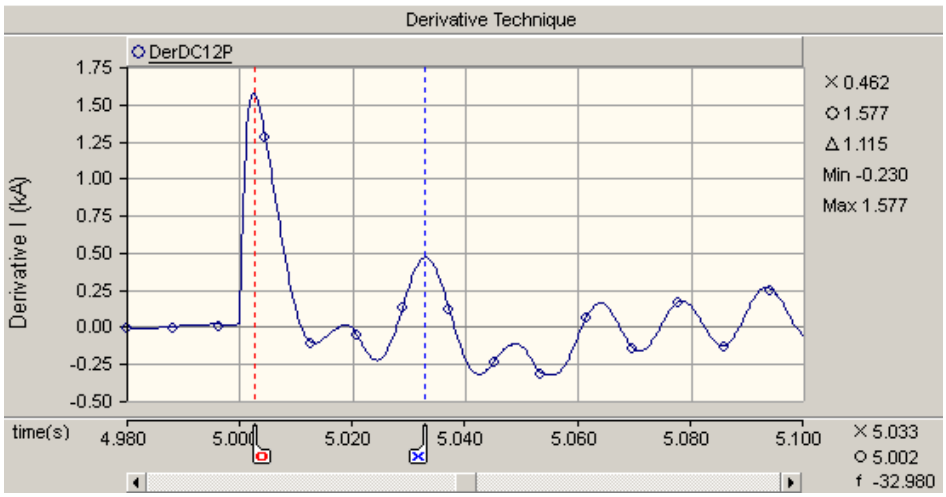

Figure 5-27: Current derivative for cable DC12P.

Table 5-8: Arrival times based on current derivatives.

Distance to fault	10 km	30 km	50 km	100 km
T1 (s)	0.002	0.152	0.253	0.505
T2 (s)	x	0.455	0.758	1.515
ΔT (s)	x	0.303	0.505	1.010
Estimated distance	x	29.952	49.995	99.9
Absolute error	x	0.048	0.005	0.10

Based on the results it can thus be summarised that:

- To locate DC faults, the method of using derivative polarities was reliable. As mentioned however, the techniques sensitivity to noise could much likely result in incorrect estimations. This can be avoided if a highly selective threshold has been chosen.
- A second error could be where there was no second peak above the threshold. This was seen in the case of d=10 km. A solution to this would be to explore other techniques like the DWT.
- More data was required for DC faults located further from the measuring point. This results in long in post-fault steady states. To avoid this problem, data can be collected from terminals that are the closest to a DC fault.
- Ultimately the derivative technique was able to carry out precise location of DC faults with only a small error margin.

5.3.3. Isolation technique

To avoid any damage to the VSC-HVDC network, in this section, the hybrid DC circuit breaker was inserted into the developed model for isolation. The breakers were to be mainly triggered in cases where excessive currents that threaten the networks reliability were detected. The requirements of the DC breaker depend highly on the systems configuration and on the current limiters that might be included. It was also very important to ensure that the stations voltage ratings were not exceeded when switching high DC currents caused by DC faults. The literature of the hybrid DC breaker was thoroughly highlighted in Chapter 2, therefore in this section, only simulation results and discussion of the hybrid breaker are presented.

It is important to note that in this study, DC CBs were modelled as ideal switches with the corresponding overall interruption time which includes both the detection and isolation time. This indicates that other breaker factors including on-state losses, maximum withstanding current, etc. were not considered. The design of a more practical type of DC CB is however still worth more attention and research in the future. For optimal results, the isolation method must work within a set interruption time to avoid reaching the high peak currents that will damage the system's components. It should also work synchronously with the detection techniques implemented. To clarify DC line fault clearing characteristics, the main parameters that are considered for discussion include: -

- Circuit breakers co-ordination with the detection technique.
- Fault current interruption of hybrid breaker

For these tests, the DC fault was applied in cable DC12P, 50 km away from VSC1. For reasons stated in previous sections, only results of positive pole are shown. In addition, since the fault was injected between the VSC stations, results of the breaker located in VSC1 (i.e. DCbreaker12P) are presented.

5.3.3.1. Confirmation of hybrid DC breakers co-ordination with detection techniques

To validate the operation of the CB in the network, various fault cases were investigated. In this study only three of cases have been discussed. This includes a scenario considered as normal operation of a DC CB during a DC fault (Case A), a scenario where the detection technique failed to respond accordingly (Case B) and a scenario where the DC breaker had an error and was unable to isolate the threat in the network. Zero in the results represents the OFF state, while a one represents the ON state. In addition, 'Fault' indicates the DC short-circuit fault signal while W12P and W12N were the output signals for each pole in the station. SW12 is the activation switch for the back-up detection algorithm, DWTdc12P is the signal from the DWT primary detection scheme, derdc12P is the derivative back-up signal, breakerCtrl is the DC breaker controlling signal and ACBRK1 represents the AC breakers control signal.

a) Case A- During a short-circuit DC fault

When a fault was injected into the VSC-HVDC system, the DC current rose towards very high peak magnitudes. The systems protection scheme should detect and isolate the fault within the set interruption time. Figure 5-28 shows the results obtained during a DC short-circuit fault. The results depict the signals sent to switches in an event of a DC fault. When a fault was injected at t=5s, the 'Fault' signal rose to one to indicate that a fault was present in the system. Since the fault was line-to-line, signal W12P and W12N were triggered, indicating that they have both been affected. When all the systems components perform their function as designed, switch SW12 should remain at zero, indicating that the back-up protection has been currently disabled to send signals to the breaker. As expected, the signal from the DWT detection technique and the DC breaker control were both triggered to one, sending an instruction that the breaker must immediately isolate the affected cables from the rest of the system. This means that the main IGBT switches found within the DC CB were opened and so current was then commutated to the arrester path (i.e. path designed to absorb energy from the system). The back-up switchgear control signals were both not triggered confirming that the main protection techniques were fully operational.

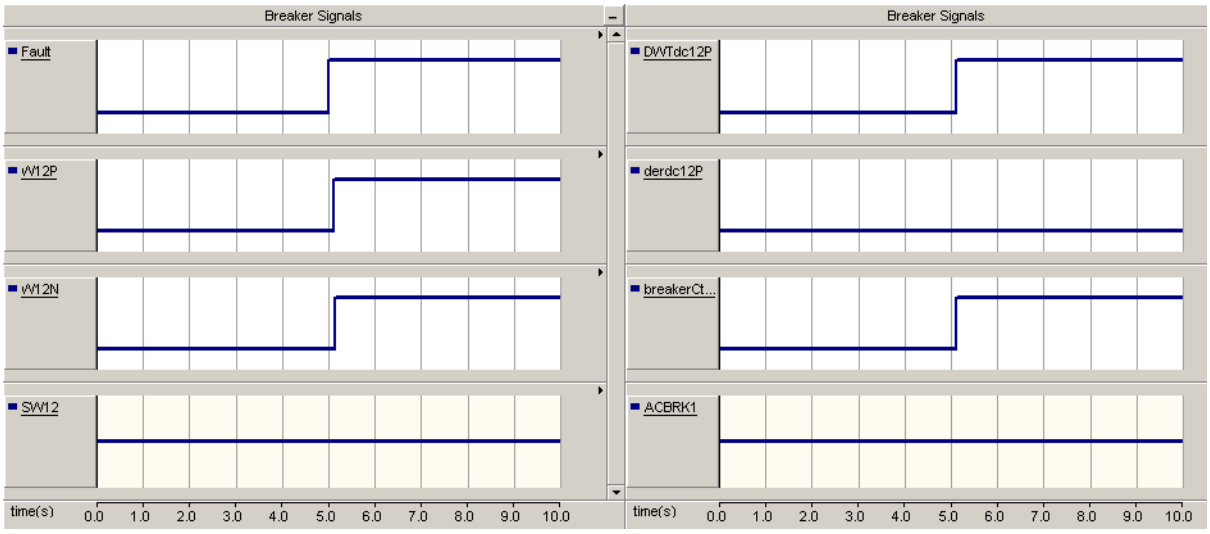

Figure 5-28: Breaker signals for breaker located terminal VSC1 for case A.

b) Case B- Error in the main detection technique

Although a system may be equipped with a strong and reliable protection scheme, errors constraining its normal operation are never ruled out. Failure to configure the networks components correctly for example, may cause the main protection algorithm to fail. When this occurs, back-up protection must be readily available to perform the function of isolating the fault to ensure the robustness of the protection scheme. To investigate the networks response for such scenarios a fault was forced on the DWT control algorithm causing it to crash. Results of this test are presented in Figure 5-29.

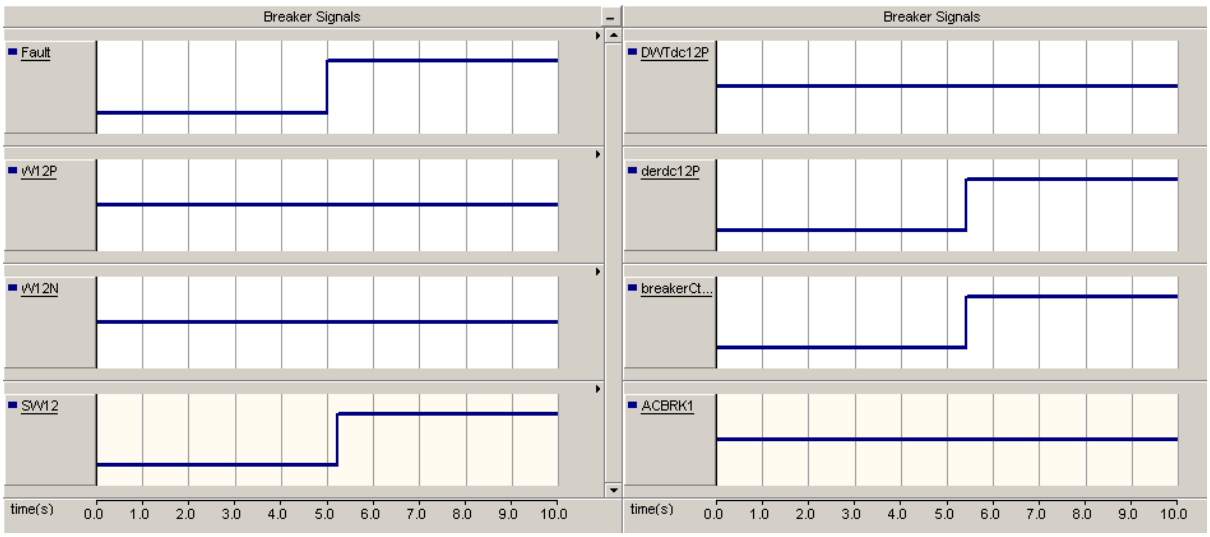

Figure 5-29: Breaker signals for breaker located terminal VSC1 for case B.

In the event of a fault in this case, the 'Fault' signal rose to one to once again indicate that a DC fault was present in the system. Signals W12P and W12N show that there was error in the detection technique as the both remain at zero giving off the idea that there was no fault in the system even though a fault signal has been triggered. After a short time, delay, signal DWTdc12P confirms that there was indeed an error with the main protection and so the back-up protection switch SW12 was immediately enabled allowing the current derivative detection technique to further assess the system for any possible faults. When the derivative protection detects the disruption in the system, the DC breaker signal breakerCtrl12P was again triggered to isolate the faulty cable. Even though by the help of the back-up scheme the network was still protected, after isolation it was recommended that the main detection be fixed and put back into operation as soon as possible to avoid further disruptions.

c) Case C- Error with the DC CBs

Due to natural variations such as switching transients and over-loading, the DC breaker can also face numerous problems that might prevent it from performing its functions properly. In this case a scenario was tested when the DC breaker was unable to isolate the affected cable despite instructions to do so. At this point the AC breaker control has to pick up the detection signal to identify the presence of a DC fault in the system. In complex power systems, this is usually done using sophisticated algorithms. In this study, however, a logic control algorithm will trigger the AC breaker to isolate the affected VSC terminals. Since this method has been designed to isolate VSC terminals and not DC cables only as with the case of DC CBs, the technique was only used as a last resort after all other protection strategies implemented have been exhausted.

In fact, the technique should only be enabled for very severe cases in order to maintain the reliability of the system. The technique will also ensure that the AC grids in which the VSC terminals are connected stay protected even in rare cases where the whole protection technique implemented fails.

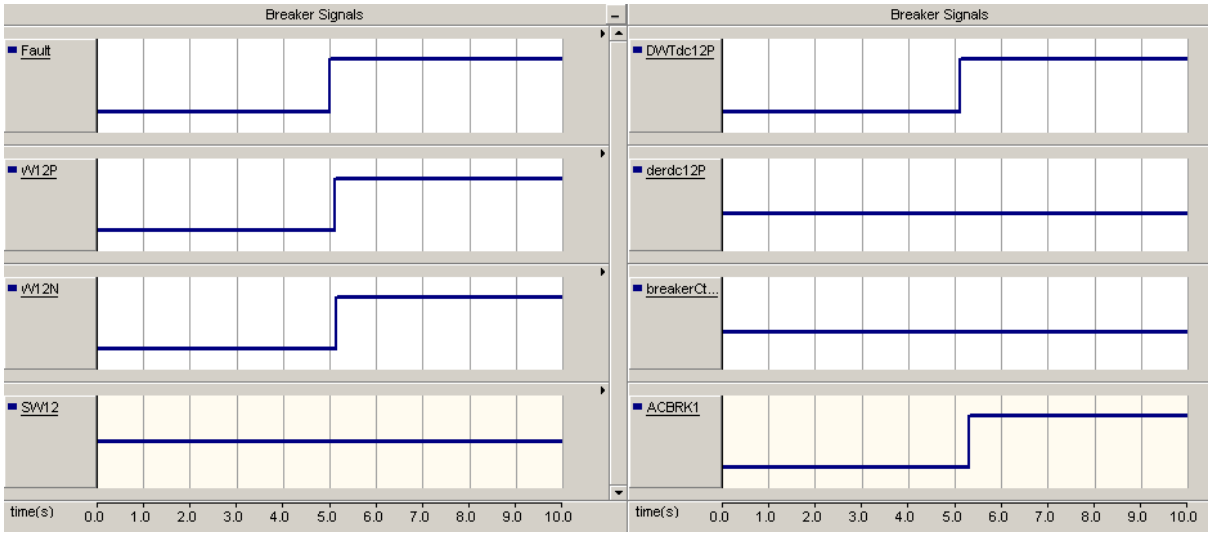

Figure 5-30: Breaker signals for breaker located terminal VSC1 for case C.

In the event of a fault in this case, the 'Fault' signal rose to one to indicate that a DC fault was present in the system. Signals W12P and W12N also respond accordingly, showing that there was a fault present in the system. After a small time, delay, signal DWTdc12P resulting from the DWT detection technique confirms the presence of a DC fault and so the back-up detection protection switch SW12 was not enabled. Unlike the previous cases, during this test, the DC breaker signal breakerCtrl12P was unable to detect or read instructions from the detection signals. Fortunately, by the help of the back-up isolation strategy the network threat could still be isolated by the AC CB and so the network was still protected. As mentioned, the protection technique should be quickly fixed and put back into operation as soon as possible to resume the transmission of power to customers.

In summary, A DC CB was included in the MTDC VSC-HVDC system to isolate possible threats posed to the system. DC CBs installed in the network receive their trip order from the detection algorithms chosen for the MTDC network. This was verified in the cases discussed in this sub-section. AC CBs were included as part of the networks isolation criterion. They act as back-up protection for the DC CB.

5.3.3.2. Fault current interruption of hybrid DC breakers

The time that the DC breaker takes to react to the fault determines the interruption time of the breaker. DC systems have no natural current zero crossing and so the interrupting device must be equipped with a mechanism to create current zero crossing.

This can be achieved in the general interruption processes that includes the creation of a counter-voltage that exceeds the systems voltage. Ideally, the fault should be isolated before the peak magnitude can be reached. Knowing the interruption, time plays a big role in determining the overall design of the protection scheme set-up. In this case current limiting reactors of 90mH were used at ends of each cable. A current limiting reactor as the name suggests was included to limit the amount of current flowing into the DC breaker.

The correct sizing of these reactors is important as its size affects current flowing through the breaker, voltage across the breaker and the magnitude of energy absorbed by the DC breaker. Although the proposed protection scheme incudes detection and location using the wavelet and derivative techniques, in this section, overcurrent was used to analyse the fault current interruption time of the breaker. The simulation results for a fault occurring 50 km away from VSC1 on cable DC12p are presented. For this test, during a DC fault the line-to ground voltage (Vbreaker) measured right after the DC breaker drops to zero (as seen in Figure 5-31). The fault current (Ibreaker) reaches a peak of 5.56 kA at 5.0019s. At this point, the circuit breaker starts to build a counter- voltage to force the current to zero to allow for isolation. A maximum of 400 kV (Vbrkout) was reached by the circuit breaker during this process (shown in Figure 5-32). At 5.005s the current drops to zero meaning that the breaker has opened or isolated the cable from the rest of the system. During a fault current interruption by an HVDC CB, the system voltage restores before the fault current was completely cleared. The voltage recovery process starts the moment the CB begins to generate the counter voltage.

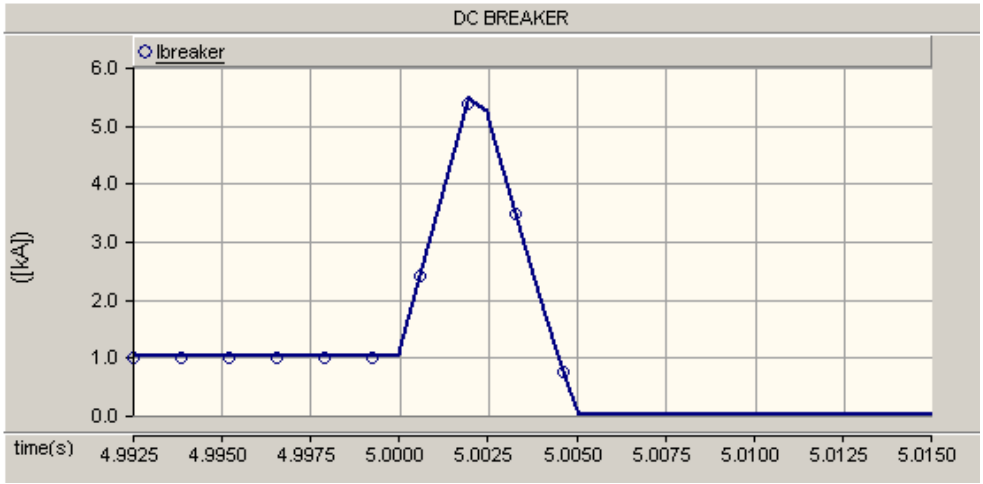

Figure 5-31: Current measured at breaker located at terminal VSC1.

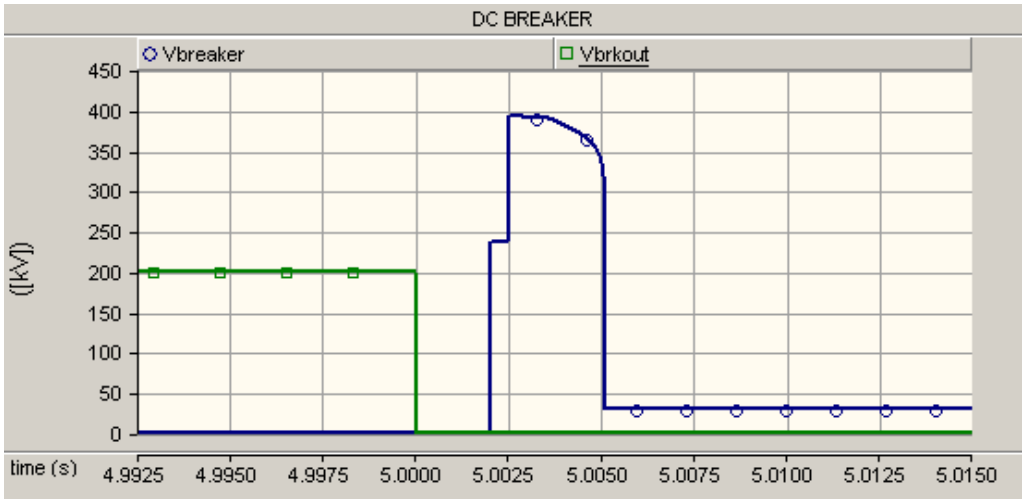

Figure 5-32: Voltage measured at breaker located at terminal VSC1.

When given the breaking time and the maximum breaking current capability, the only adjustable parameter is the inductance of the HVDC reactor, which decides the rate of current rise. The HVDC reactor therefore needs to be selected in such a way, that within the breaking time, current does not reach a level higher than the maximum breaking current capability of the HVDC breaker. From these PSCAD simulation results, it can be concluded that the model shows good responses for opening and closing on the detection trip order. Breaking time has been governed by the response time of the protection, and the action time of the HVDC switch. A longer breaking time would require the HVDC switch to have an increased maximum current breaking capability. This increases the energy handled by the arrester and correspondingly leads to a higher cost for the HVDC breaker.

5.3.4. Summary

To find an effective protection scheme for the developed VSC-HVDC scheme, in this Chapter, various protection strategies were tested and discussed. Important factors drawn from these tests include:

- The DWT fault detection technique was both highly selective and reacts within required speeds. Its need for massive and complicated calculation did however make its implementation a bit more complex and affected its operational speed. To enhance the methods performance, pairing the technique with back-up protection units is recommendable.
- Overcurrent protection was a simple straightforward protection technique. It can only be considered for back-up protection since it lacks selectivity.
- Differential protection was most attractive for its intrinsic selectivity. The method however only worked best for shorter distance transmission cables due to the time delay in communication.

- This constraint remains a threat even if the technique was selected as back-up protection. It was also not considered since it means it in case of expansion, it cannot work effectively.
- Current derivative detection was fast and effective. Its sensitivity to noise did sometimes result in incorrect data samples. Nevertheless, its capability in indicating fault direction helped with diagnoses in other detection methods. It was therefore recommendable to include as back-up protection.
- Type A current derivative travelling wave based fault location was relatively accurate in estimating the exact fault distance. However, due to the current derivatives sensitivity to noise, the method might not work with noisy signals.
- Due to the nature of the network and its response to DC-side faults, isolation switchgear needs to react at very high speeds. This was mostly possible by using the hybrid DC CB.
- In the hybrid CB, the fault current in the arrester bank establishes a counter-voltage, which reduces the fault current to zero by dissipating the fault energy stored in the HVDC reactor. Total fault clearing time consists of the breaking time corresponding to a period of rising current, and fault clearing corresponds to a period of decreasing current. Both time intervals are important considerations in the design and cost of the HVDC breaker.
- As an extra measure of security, AC CBs were included on each side of each VSC terminal. These ensured that the grid was not affected in cases where the system had not isolated the fault.

A feasible protection scheme can be proposed based on the results discussed in Chapter 5. The scheme includes: -

- A main protection scheme that uses the DWT fault detection technique. For optimal performance, sampling rate was set as 10μs and the threshold at 2.0
- The derivative protection was selected as a back-up plan, with a threshold set at 1 kA.
- The exact location of the fault was estimated based on the current derivative travelling wave method. This information relays the arrival time of the wave front.
- The isolation switch-gears were chosen as the hybrid DC CB. They have a total clearance time of 5ms. This includes both the detection and isolation of the DC fault on the affected cable. The AC CB were included as a back-up protection scheme and will isolate an entire VSC terminal rather than the affected cable.

5.4. Evaluation

The aim of this section was to evaluate the proposed protection scheme based on the protection requirements and principles introduced in Chapter 2.

5.4.1. Speed

Due to its response to DC-side faults, one of the strictest requirements of a VSC-HVDC protection scheme is speed. As shown by the results obtained and discussed in this Chapter, the selected protection scheme can effectively isolate the fault within the critical time. Its overall interruption time was recorded as ±0.005s, and isolates the fault before the peak fault current can damage the systems components.

5.4.2. Selectivity

The degree of selectivity required is mostly dictated by the type of VSC-HVDC configuration adopted. Selectivity during these tests was guaranteed by the threshold setting. For a system with main and back-up protection like the one developed, an appropriate time lag needs to be implemented to ensure consistency in selectivity. Results of breaker signals shown in Section 5.3 confirm that the system was able to isolate only the faulty cable from the system. Therefore, the requirement of selectivity was met.

5.4.3. Reliability

Results shown on the protections trip signals show that the scheme was able to correctly identify and isolate the affected cables. This ensures its reliability.

5.4.4. Sensitivity

The sensitivity of the network was proven by injecting different DC fault types. This study concentrates on the severe short-circuit faults which means it can handle the biggest threats imposed on the system.

5.4.5. Robustness

Having a main (DWT method) and a back-up (derivative method) detection method as well as main (DC CB) and back-up (AC CBs) isolation techniques guaranteed the robustness of this protection scheme.

5.4.6. Seamlessness

The fault recovery factor was not explored in this study and so the seamlessness of the protection technique was not confirmed. This will be considered in future.

5.5. Chapter summary

In this chapter, the general principle and a more detailed illustration of the protection scheme has been proposed for a 4-terminal VSC-HVDC system. The Chapter starts with a fault analysis investigating factors that might affect the fault response of the system and if they are severe enough to be considered. From this information various protection strategies were proposed and the most effective has been chosen for implementation for the developed system. It also defines the main constraints in the design of the protection. To investigate its feasibility lastly the system was evaluated to check if it satisfies the general requirements speed, selectivity, reliability, sensitivity, robustness and seamlessness.

CHAPTER 6: CONCLUSIONS AND RECOMMENDATION

To improve its reliability, the protection of a VSC-HVDC system was studied. The following can thus be concluded: -

- The literature review confirms that DC-side fault currents pose a serious threat to VSC-HVDC networks. Unlike in HVAC systems or traditional HVDC systems however, these faults result in a high rise in current magnitude at a very high speed. The resulting DC characteristics therefore constrain most of the traditional techniques from being implemented for protection of the VSC-HVDC networks.
- A DC fault response study was initially undertaken. The most noticeable results were seen in the changes of the systems current during a DC fault. Large fault currents were recorded during the first few seconds of the DC fault. This was mainly due to the discharge of the DC-link capacitors.
- During fault analysis it can be concluded initially that the short-circuit DC fault (which rose
- to maximum of 10.725 kA) affects the VSC-HVDC system more severely than the ground DC fault (which rises to maximum of 6.553 kA).
- Variations in the converters distance between the DC fault and converter resulted in the change in magnitude and shape of the response of DC current. The highest current magnitudes were recorded at distances that were closest to the converters. This means that that in these cases, the converters faced a bigger threat.

The analysis results obtained require the proposed protection scheme to operate at a speed that is even faster to isolate the faulted section. The challenge and main focus of this study was to therefore propose protection methods that would be most suitable for MTDC VSC-HVDC systems. This should improve the reliability and therefore increase the potential development of these networks for electricity transmission.

- The protection methods implemented in the MTDC VSC-HVDC network included the DWT wavelet technique for main detection and the derivative protection as a back-up detection technique.
- The wavelet protection technique was implemented with the fifth level Haar chosen as the mother wavelet. During a DC fault, the magnitude of the DWT wavelet rose to higher magnitudes. There was a significant magnitude difference seen for wavelets resulting from the affected DC cables and those in the healthy cables. This ensured the methods selectivity factor, a characteristic very vital for a MTDC VSC-HVDC system.

- Derivative protection was also reliable at detecting DC fault transients and finding the fault direction. Its biggest drawback however, was in selectivity, as it was not always easy to distinguish high impedance faults within the protection zone from low impedance faults there were located outside the designated protection zone. The derivative method was however mostly attractive for its ability to locate DC faults in the cable. It was then used with the travelling wave method to determine the exact location of the DC fault.
- Travelling wave DC fault localisation was based on the first two transients of the derivative current arriving at one converter station. The localisation time depended on the fault distance, and is equal to the time that the fault wave travels to the DC breaker, then to the fault and then back to the DC CB again.
- To isolate the faulty cable, the IGBT based hybrid DC CB was implemented as the primary system disconnector. The AC breakers are then included only for cases where every other protection techniques implemented in the system has failed to function. The hybrid DC CB was able to isolate the affected cable before the current magnitude rose to uninterruptable fault currents.
- To avoid large overcurrent magnitudes that might damage the system, the currents were to be interrupted within 5 ms for a permanent short-circuit DC fault. DC CBs have a delay between the fault detection and the fault interruption. This is mainly due to the size of the overall system. The CB can however be able to quickly find faults that were closer to converters and with lower fault impedances.

6.1. Recommendations for further studies.

1. The complexity of the grid is considered as one of the other major challenges with fault protection. The radial meshed grid was used in this study. It is expected that as the complexity of the grid increases, fault detection and localisation would be more complex. It would be a vital contribution to therefore do a further study on other system configurations and how they may affect the protection of a VSC-HVDC system.
2. The investigations for protection in this system were also based solely on the 2-level VSC system. There are however more advanced and more effective converters topologies available for such systems. The MMC in particular, is of special interest, as this configuration also includes an added advantage of fault limiting or the fault blocking characteristics for the MTDC VSC-HVDC system.

3. While the combination of wavelet protection and current derivative protection proved successful for this system, effective protection solutions should be investigated a bit further. These methods do however show a promising future in this subject.
4. It was determined that the idea of including fault current limiters could play a big role in the protection of VSC-HVDC systems, as these components will reduce the threat that the converters are exposed to during a DC fault. This idea should be explored in detail in future.
5. In this study, the DC CBs were simplified into an ideal time-delayed switch. The designing of a more practical type of DC CB is therefore still worth more attention and research in the future.
6. The results presented in this study and in many evaluations on this subject were mainly from computer simulations. These results would differ from those obtained in the real world due to different factors coming into play. It is important therefore that there be more investments in the laboratory testing of the proposed solutions to see if real life implementation is possible.

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APPENDIX A

MATLAB M FILE

```
% Code to find fault location
% Vartime represent the time in seconds and Varderv represents the current derivative in kA.
% Since there is a large amount of information the code analyses only in sections of d=10000
k = 0;
s = 9999;
d = 10000;
r =(length(Vartime)/2)+d:d:(length(Varderv)-1);
%n1 = zeros(2,1);

Thr = 0.6; %Current Derivative Threshold
for g = 1:10
   x = g*d;
   Le = Varderv(g*d:r);

   for n=1:length(Le)
    s = s+1;
    if abs(Le(n))>=Thr&&abs(Le(n))>abs(Le(n-1))&&abs(Le(n))>abs(Le(n+1))
       k=k+1;
       n1(k)=s; %n1 is an array whose elements are positions of peaks
    end
   end


   if numel(n1) == 2
      break
   end
end

p1=Varderv(n1(1));
str1=['The first fault peak value is ',num2str(p1),' kA'];
```

```
disp(str1)



t1=Vartime(n1(1));
str2=['The first fault arrival time is ',num2str(t1),' seconds'];
disp(str2)

p2=Varderv(n1(2));
str1=['The first fault peak value is ',num2str(p2),' kA'];
disp(str1)

t2=Vartime(n1(2));
str2=['The first fault arrival time is ',num2str(t2),' seconds'];
disp(str2)

plot(Vartime,Varderv);
M = ones(11,1).*0.6;
h = 0:1:10;
hold on
grid on
plot(h,M);
Z = ones(11,1).*-0.6;
plot(h,Z);
xlim([4.9 5.25]);
```