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Digital Object Identifier (DOI): 10.1109/EPE.2015.7309381

Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on; September 2015

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Suggested Citation

M. Andresen, K. Ma, M. Liserre and F. Blaabjerg, "Thermal stress comparison in modular power converter topologies for smart transformers in the electrical distribution system," *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, Geneva, 2015, pp. 1-10.

Thermal Stress Comparison in Modular Power Converter Topologies for Smart Transformers in the Electrical Distribution System

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Acknowledgement

The research leading to these results has received funding from the European Research Council under the European Union's Seventh Framework Programme (FP/2007-2013) / ERC Grant Agreement n. 616344 – Heart.

Keywords

«Reliability», «AC/AC converter», « Thermal stress», «Smart microgrids»

Abstract

A Smart Transformer (ST) can cover an important managing role in the electrical distribution grid. For the moment, the reliability and cost are not competitive with traditional transformers and create a barrier for its application. This work analyses one promising modular ST topology, and the focus is put on the loading and thermal stress of power devices in order to discover critical parts of the system during different loading conditions in realistic distribution system scenarios.

I. Introduction

A global trend goes to increased distributed power generation, which typically is fed into the electrical distribution grid. This changes the concept of large centralized power plants for which the actual electrical distribution system is designed [1],[2]. Especially the renewable energy sources challenge the actual grid configuration, because of their variable power penetration and the resulting bidirectional power flow in parts of the grid, which challenges the controllability. The managing capability of the grid with the present transformer is limited and a Smart Transformer (ST), which based on power electronic converters and can provide additional services for the electrical distribution grid [3],[4],[5].

The actual ST cannot compete in terms of reliability with the traditional transformer. Nevertheless, the advantage of additional services might outweigh the disadvantages in some cases, if the ST is optimized. However, the system architecture needs to be chosen carefully, because it is crucial for maximizing the reliability and the efficiency. In the existing literature, there is an analysis of the efficiency of different modular ST topologies, which is dependent on the number of power semiconductors [6],[7], but for the reliability and fault tolerance, there is a lack of knowledge. In contrast to other applications of power converters, the ST operates under partial load for most time and the bidirectional power flow is challenging the power semiconductors [8]. The existing research for reliability is often limited to studies of redundant systems or neglects the operating conditions like thermal stress or the environmental conditions [9],[10]. For the reliability analysis, the physics-of-failure analysis is of great importance, and it is possible to use mission profiles of one transformer in the grid to simulate how the semiconductors are stressed and to calculate the expected lifetime [11]. However, the thermal cycling for the power electronics in ST applications has not been investigated with its characteristics of partial load operation and reverse power flow.

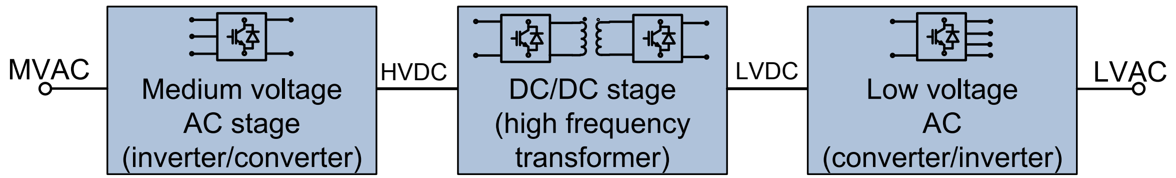

Fig. 1. Three stages of the Smart Transformer

This work analyses a promising modular three stage ST topology for the electrical distribution system based on the thermal stress of the power semiconductor devices. Three different mission profiles with different loading conditions are used to evaluate the thermal stress for all three stages of the chosen topology. First, the chosen ST topology is introduced in section II, while section III describes the considered mission profile. The thermal stress of the components is evaluated in section IV and in section V the effect of the thermal profiles on the lifetime is shown. Finally, the last section concludes the work.

II. Smart transformer power electronics architecture under study

The power electronics based smart transformer can be built with a different number of conversion stages and by different topologies. The single stage ST is realized with a matrix converter and requires the least number of components, but can provide least additional services with respect to the traditional transformer. Two stages provide additional services, such as DC connectivity either in the low voltage or the medium voltage side. However, it has been shown in [6] that all large smart transformer activities are based on three stages, namely a rectifier, an isolated DC/DC converter and an inverter as in Fig.1. In the low voltage side the grid is a three phase four wire system, which can be loaded asymmetrically, which is not considered in this study. As a candidate for the medium voltage stage, the cascaded H-bridge (CHB) [12] and the Modular Multilevel Converter (MMC) [13] are of interest because of their modularity. In this study, an MMC built by half bridges (as shown in Fig. 2 (a)) is chosen, because the CHB would not enable an MV DC link [6]. In the isolation stage most projects use the single phase Dual Active Bridge (DAB) [14]. Another solution is the Quadruple Active Bridge (QAB), which has three ports connected to the transformer in the medium voltage side and only one in the low voltage side, bringing the advantage of full soft switching in certain operation conditions [5]. In Fig 2 (b), the QAB is shown.

In the low voltage stage the three phase 2-level voltage source inverter (VSI) is a widely used solution, which is taken in this study (see Fig. 2 (c)). Possible alternatives are single phase full bridges built by MOSFETS or three level converters, such as the NPC topology. The two level converter is chosen because of the wide knowledge and the existing potential to improve the operation with wide bandgap

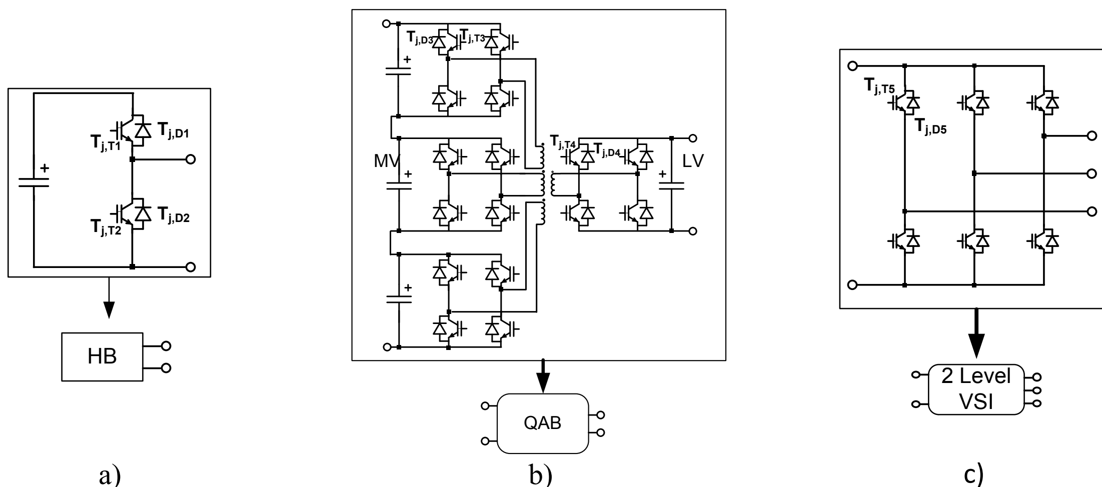

Fig. 2. Considered topologies for the low voltage stage in the smart transformer: a) Half bridge, b) Quadruple Active Bridge, c) 2 Level VSI.

power semiconductors. Nevertheless, it is not the perfect solution to connect the four wire low voltage side.

The selected topology is designed for an ST with a power rating of 1 MW with the parameters in Table 1. It is worth to mention that the optimal topology is difficult to define because different topologies require different voltage and current ratings, different filter sizes, different number of power semiconductors and different control methods. Furthermore, the number of modular components has strong impacts on the device loading and needs to be defined carefully [15]. However, the thermal stress for the chosen modular system is analyzed and can be transferred easily to other systems with different topologies.

Table 1: Parameter of the studied smart transformer architecture.

Rated Power	MV side converter	MV line-to-line voltage	MV dc-link voltage	Isolation stage	LV dc-link voltage	LV side converter	LV line-to-line voltage
1 MVA	MMC15 HB cells	11 kVrms	19 kV	9 series QABs	700	3 paralleled 2-Level VSI	380 Vrms

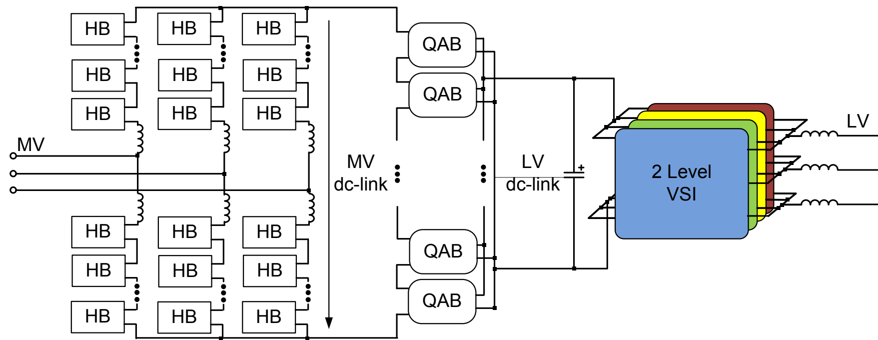

Fig. 3. Full ST architecture for the study case.

The full ST structure consisting of the several modules is shown in Fig. 3. The medium voltage DC link and the low voltage DC link are shown and can be individually connected with additional DC grids. Since today transformers only connect AC grids, DC grids are not considered in this study.

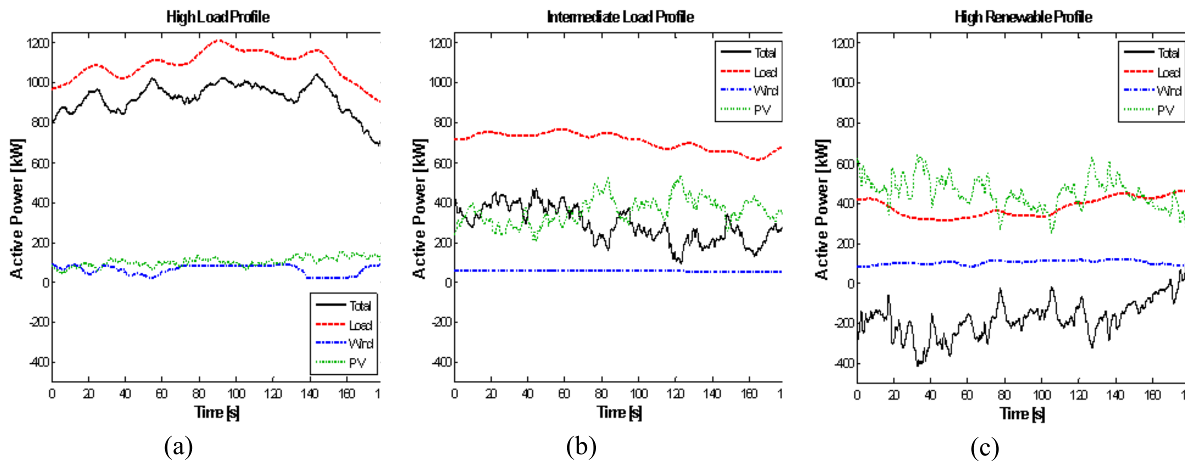

Fig. 3. Load Profile for the study with active power in a grid: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

III. Considered mission profiles

For the mission profile of the ST a low voltage grid with connected photovoltaic (PV) and wind generation and loads is considered. It is assumed that the medium voltage side converter does not generate reactive power for the grid and operates with $cos(\varphi)=1$, while the low voltage side converter is transferring reactive power into the grid. The loads operate with a constant $cos(\varphi)=0.95$, whereby the renewable do neither consume nor produce reactive power. Thus the whole reactive power in the low voltage grid is provided by the ST.

Since thermal analysis is difficult to perform in long term studies, three different profiles are studied. The first profile in Fig 3 (a) is characterized by high power consumption of the loads and low production by the renewable power plants, which results in high power flow from the medium voltage grid into the low voltage grid. The second profile in Fig 3 (b) shows medium power consumption by the loads and medium generation in the grid. This is expected to be the loading condition of the ST for the most time and results in a power transfer into the low voltage grid. The third profile is characterized by high production of the renewable sources and low consumption by the connected loads, which results in bidirectional power flow and a higher fluctuation of the power.

IV. Thermal stress analysis

Description of the thermal model (TBD by Ke Ma)

Ambient temperature $T_a=40°C$

The profiles of Fig. 3 are in the following tested for each ST stage with power semiconductors designed for a junction temperature of 80 °C. Since the power profile exceeds the rated power for short time periods, the maximum temperature is also expected to exceed this temperature.

A. Medium voltage stage

The medium voltage side MMC is composed by 15 half bridge modules and the parameters of Table 2 with a rated current of $I_{load,HV}=74.2A$. For the thermal stress analysis, the three mission profiles are simulated. In Fig. 4 the junction temperature of all power semiconductors in one half bridge are shown as shown in Fig. 2 (a).

The first profile leads to junction temperatures between 60 °C and 85 °C. The IGBT T1 and the diode D1 are the most stressed devices in this condition and the maximum junction temperature is in accordance with the design. T1 shows a thermal swing of $\Delta T \approx 4\ K$ in the fundamental period, while T2 is stressed less with $\Delta T \approx 3\ K$. The diodes obtain approximately the same temperature swing of

Table 2: Parameters of the medium voltage side MMC.

Rated power of converter P_0	Output fower factor	Rated load current $I_{load,HV}$	Fundamental frequency f_0	Switching frequency f_c	Filter inductance L_f
15 x 66.7 kW	1.0	74.2 A	50 Hz	2 kHz	57.8 mH (0.15 pu)

$\Delta T < 1\,K$. In the second profile (Fig. 4 (b)), the average temperature is remarkably reduced for all power semiconductors and the temperature swing is much lower than in the first profile. Especially the stress for the diodes D1, D2 and T1 is significantly reduced. The third profile (Fig. 4 (c)) with reduced load and bidirectional power flow shows further reduction of the mean temperatures of T1, D1 and D2. The IGBT T2 is now higher loaded than T1 and the diodes undergo higher thermal cycles that in the case before. This is mainly caused by the high power generation of the renewable sources, which affect high power fluctuations.

B. DC/DC converter

The isolation stage of the ST is built by 9 QABs with a power rating of $P_0=111\ kW$ with the parameters of Table 3. The thermal simulations are shown in Fig. 5 for the three load profiles with the power semiconductors named as in Fig. 2 (b).

Table 3: Parameters of the medium voltage side QAB.

Rated power of converter P_0	Medium dc bus voltage	Rated load current $I_{load,HV}$	Switching frequency f_0	Low dc bus voltage	Switching frequency f_c	Leakage inductance L_f
9 x 111 kW	19 kV	55,6 A	50 Hz	700 V	5 kHz	48 µH

The temperature fluctuation under the high load mission profile is approximately proportional to the mission profile for the most stressed components T3 and D4. Remarkably, T3 is installed in the high voltage side and D4 in the low voltage side. The diode D3 is almost not stressed for the conditions of the high and the medium load profile, while the maximum temperature is 86°C, which in accordance with the system design. For the medium load profile, the thermal swing is very low and the average temperatures are low as well. The third profile with reverse power flow has also relatively low average temperatures, but the anti parallel power semiconductor is stressed higher. Thus T3 and D4 are less stressed than T4 and D3.

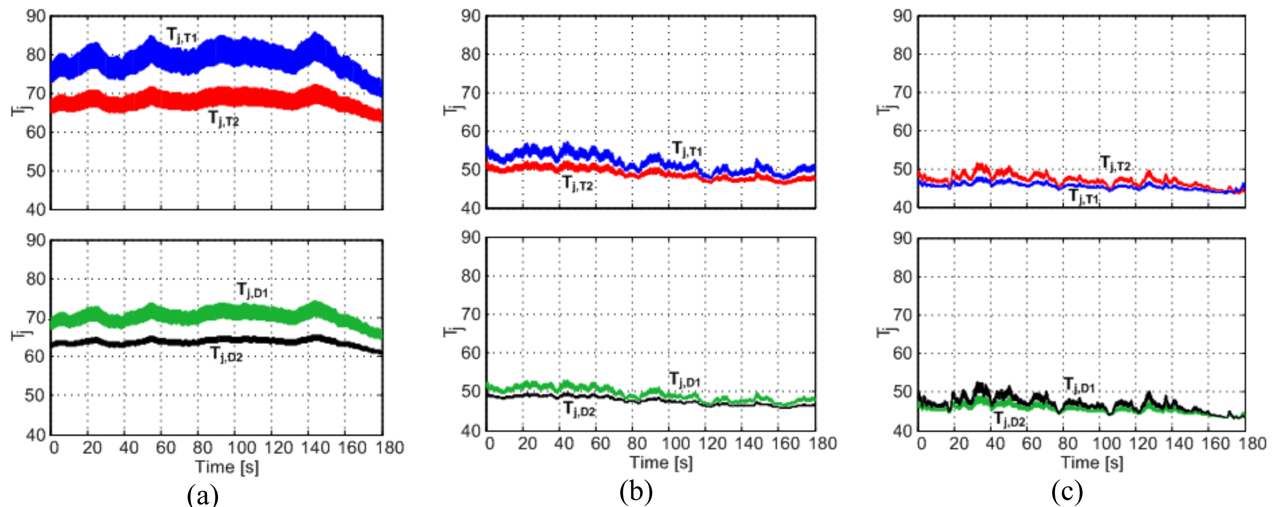

Fig. 4. Thermal stress for the MMC during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

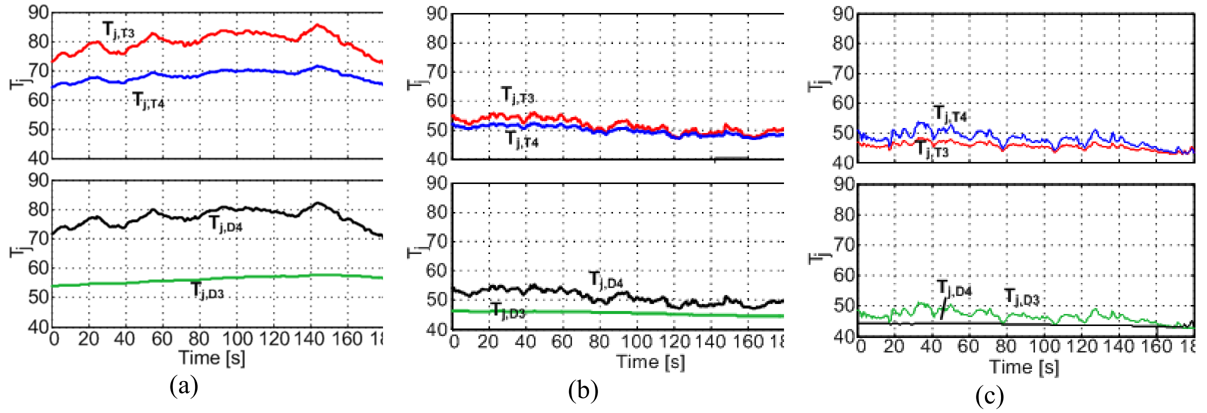

Fig. 5. Thermal stress for the QAB during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

C. Low voltage stage

In the low voltage stage four parallel 2 level inverters with the parameters of Table 4 are used. Because of the reactive power consumption in the grid, the converter is designed for *cos(φ)=0.9* and the rated load current is $I_{load,LV}=397A$. The temperature profiles for the mission profile of section III are shown in Fig. 6 for the IGBT T5 and the diode D5 as shown in Fig. 2 (c).

Table 4: Parameters of the low voltage side 2 level VSI.

Rated power of converter P_0	Output power factor	Rated load current $I_{load,LV}$	Fundamental frequency f_0	Switching frequency f_c	Filter inductance L_f
4 x 250 kW	0.9	397 A	50 Hz	4 kHz	0.37 mH

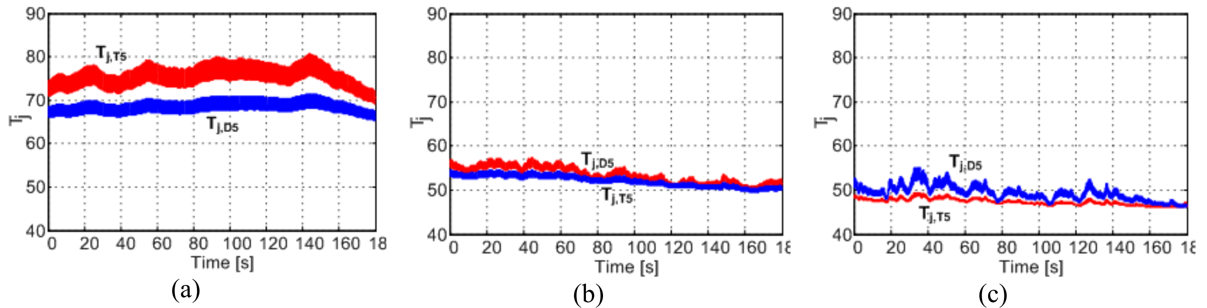

Fig. 6. Thermal stress for the 2 level VSI during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

For the high load mission profile, the junction temperatures of T5 is highest and between 70°C and 81°C, while the temperature of D5 is between 65°C and 71°C, which is in accordance with the power semiconductor choice as in the two cased before. The cycles in the fundamental period are approximately $\Delta T \approx 5\ K$ for T5 and $\Delta T \approx 4\ K$ for D5. The junction temperature profile for medium load profile in Fig. 6 (b) shows reduced stress for the diode with lower average temperatures and lower thermal swing for both semiconductors. Similar to the MMC topology, the high renewable energy production in Fig. 6 (c) shows high temperature fluctuation for the diode. Remarkably, the IGBT T5 has a much smaller thermal swing compared to the diode D5.

V. Reliability Comparison

The thermal profiles from section IV can be used to compute the consumed lifetime of the power semiconductors, which is also defining the lifetime of the power semiconductors. The common failures in power electronic modules are found at the bond wires and the interconnections within the modules, namely chip solder, base plate solder and bond wire liftoff. The mechanisms, which cause the wear out are based on the temperature swing, which needs to be separated from the temperature profile. A common way to do is to apply thermal cycle counting, such as Rainflow counting [16]. From the counted cycles, there are models to derive the thermal stress and the accelerated damage. One of the models available is the LESIT lifetime model based on the accelerated tests of IGBT modules leading to solder fatigue [17]. The data is only available for limited thermal swings between $\Delta T = 30K$ and $\Delta T = 80K$, but in this work the range is extrapolated to smaller magnitudes. Furthermore, the technology has proceeded and there are new IGBT generations, which are having a higher thermal cycling capability. Nevertheless, the failure mechanisms and the dependence on the temperature swing remains [18]. Based on the LESIT models, the accumulated damage is derived from the Rainflow counted cycles. In this work thermal swings with amplitude smaller than 1 K are neglected. In Fig. 7 the analysis is

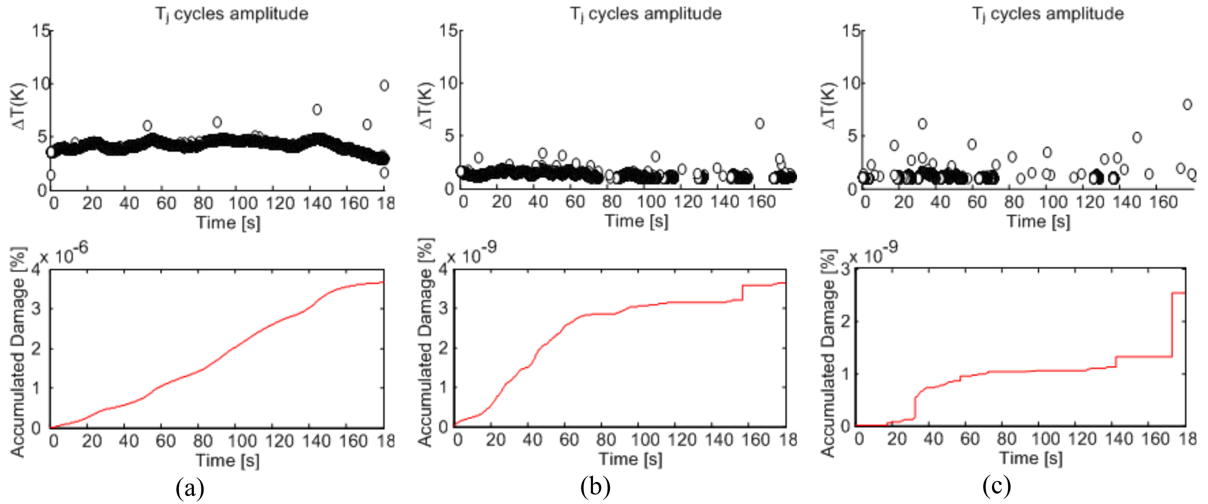

Fig. 7. Rainflow cycle counted for junction temperature of T1 in the MMC during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

demonstrated for the IGBT T1 in the MMC, which is the most stressed power semiconductor in this topology.

Most thermal cycles in all load conditions are generated by the fundamental frequency, which can be identified by the density of cycles with similar amplitudes. The other thermal cycles are generated by the load profile and under the medium load and the low load conditions some are visible as steps in the accumulated damage. The accumulated damage is added, when the thermal cycle is completed. The total consumed lifetime is highest for the high load profile, while the others obtain almost similar consumed lifetime. Nevertheless, their consumed lifetime is much lower than the consumed lifetime of the high load profile.

In Fig. 8 the thermal cycling is shown for IGBT T4 of the QAB undergoing the three load profiles. T4 is chosen, because it is stressed most in this topology for high power flow into the low voltage grid. The DCDC converter has much less thermal cycles than the MMC under the same profile, because cycles are only generated by the load profile.

In Fig. 9 the thermal cycles are counted for the IGBT T5 in the VSI. The identified thermal cycles of

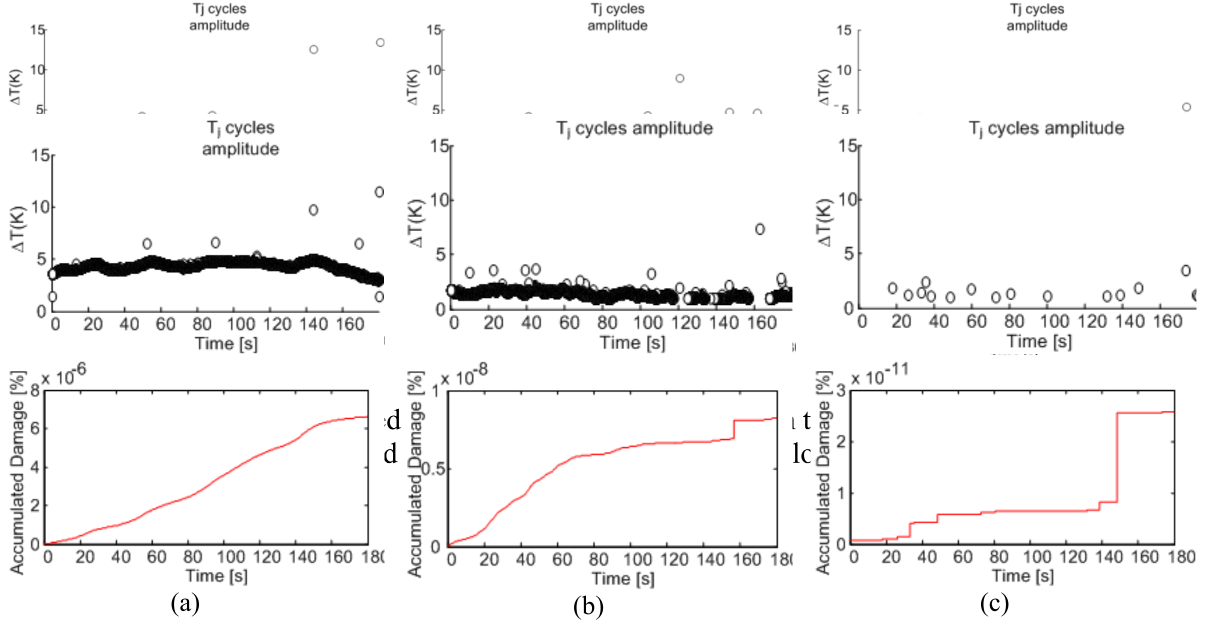

Fig. 9. Rainflow cycle counted for junction temperature of T5 in one two level inverter during the different loading conditions: (a) High load and low generation, (b) Medium load and medium generation, (c) Low load and high generation.

the Rainflow counting are quite similar to those ones of the semiconductors in the MMC. During reverse power flow of mission profile 3, the accumulated damage is very low in T5, while for the other power semiconductors it is almost comparable to the profiles of the power semiconductors in the other topologies.

Finally, a comparison of the total accumulated damage is done and presented in Table 5. Because of the low damage in the medium load and the inverse power profile, only the damage in the high load profile is shown and normed on the most stress power semiconductor, T5. It can be seen that the lowest accumulated damage is derived for the QAB, while the MMC has still al lower consumed lifetime than the VSI. The result comes despite the design for a similar maximum junction temperature of the power semiconductors. Furthermore, the accumulated damage of the IGBTs is higher than the accumulated damage of the diodes. The MMC has the most equal stress distribution for the diode and the IGBTs, while the QAB and the VSI obtain very unequal lifetime consumption.

Table 5: Accumulated damage of the high load mission profile normalized on T5.

	High load profile
Damage of T1 in the MMC [normalized on T5]	0.56
Damage of D1 in the MMC [normalized on T5]	0.24
Damage of T3 in the QAB [normalized on T5]	0.03
Damage of D3 in the QAB [normalized on T5]	0
Damage of T5 in the2 level VSI [normalized on T5]	1
Damage of D5 in the2 level VSI [normalized on T5]	0.10

Beside the normal operation addressed in this work, failures in the grid, voltage sags or current and voltage imbalances are expected to have high influence on the stress for the power semiconductors. The ST will have the capability to balance voltages or currents of an unbalanced low voltage grid, for example. This can be performed by different stages of the ST with a different impact on the lifetime of the three stages. Since the accumulated damage is lowest for the QAB, it will be the preferred stage to carry out the balancing with the cost of higher consumed lifetime, while the impact on the other stages should be kept low.

The results for the lifetime derivation need to be considered carefully, because several influences are not covered in this study. First, the lifetime model only covers the mechanism of solder fatigue, while

vibration, humidity or cosmic rays is not included. Furthermore, the transition between the mission profiles and their impact on the total lifetime has to be considered. In long term studies also the ambient temperature needs to be taken into account to estimate the lifetime.

VI. Conclusion and future work

The thermal stress for a modular ST topology built of a modular multilevel converter, quadruple active bridges and two level voltage source inverters has been analyzed. For each stage three different mission profiles have been simulated and the accumulated damage has been derived. Under the analyzed normal operation conditions, the lifetime of all stages is expected to be high, while high power transfer has the highest lifetime consumption. The isolation stage of the ST has the lowest accumulated damage in all conditions. Consequently, balancing of the grid currents should be done in the isolation stage. Future work includes the impact of faults and grid imbalances on the lifetime of the system.

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