Frequency-domain thermal modelling of power semiconductor devices

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Abstract - The thermal behavior of power electronics devices has being a crucial design consideration because it is closely related to the reliability and also the cost of the converter system. Unfortunately, the widely used thermal models based on lumps of thermal resistance and capacitance have their limits to correctly predict the device temperatures, especially when considering the thermal grease and heat sink attached to the power semiconductor devices. In this paper, the frequency-domain approach is applied to the modelling of thermal dynamics for power devices. The limits of the existing RC lump-based thermal networks are explained from a point of view of frequency domain. Based on the discovery, a more advanced thermal model developed in the frequency domain is proposed, which can be easily established by characterizing the slope variation from the bode diagram of the typically used Foster thermal network. The proposed model can be used to predict not only the internal temperature behaviours of devices but also the behaviours of heat flowing out of the devices. As a result, more correct estimation of device temperature can be achieved when considering the attached cooling conditions.

I. INTRODUCTION

Power electronics are being widely used in many important applications of energy conversion system like renewable energy production, motor drives, transportations and power transmission, where the cost of maintenances and failures is very high. Consequently the reliability requirements for power electronics in these systems are getting more critical [1]-[4]. As one of the most expensive and most critical components, thermal loading of power semiconductors are especially important. It has been demonstrated in [5], that the thermal dynamics under various time scales either inside or outside the power semiconductors could contribute to quantified damage of the component. As state in [6]-[12], the fast thermal cycling inside the power devices will cause many important fatigues like bond-wire lift-off and cracks/voids in the chip soldering layer, while the slower thermal variations outside the device (i.e. on the case/baseplate of the device or the heat sink) will cause

fatigues like cracks on the soldering layer and the thermal grease. As a result the accurate temperatures estimation including the thermal dynamics either inside or outside the power device is critical information not only for the reliability enhancement, but also for cost-efficient thermal management of the power converter.

Unfortunately, the thermal stress of the power device is challenging to model, because it is not only related to the characteristic of the device itself, but also depends a lot on the performance of the attached thermal grease and heat sink. Generally, the thermal behavior for the power devices can be modeled by a series of lumps of thermal resistance R and capacitance C [13]-[17], which together are referred as the thermal impedance Z. According to the connection of RC lumps, they can be grouped into Foster or Cauer type thermal networks, as shown in Fig. 1. The Cauer RC network, which is based on the physical structure of the device, is considered to be a relatively correct model to describe the thermal behaviors of power devices. However, an accurate Cauer model is normally hard to be acquired because the internal geometry, materials and effective heat path of device have to be all determined with the help of Finite Element Method (FEM) simulation. The other RC network named Foster type is more popularly used because it is based on the measurement of temperature dynamics of power devices [15], [17], and it is independent of the internal structure or material.

One problem of the Foster type thermal network is that its parameters are based on mathematical fitting of the measured/simulated temperature curves, and the single RC lump in the Foster network represents no physical meaning. Therefore by using this model, only the overall temperature behaviors between the measured points can be guaranteed, provided with a known temperature at the node, where heat is flowing out [15]. It has been found that when extending the Foster type thermal network with the thermal models for the thermal grease and heat sink, unrealistic temperature behaviors either inside or outside the power devices will be experienced [13]-[17]. These drawbacks make the Foster type thermal model hard to be utilized for thermal design or lifetime prediction, where the external temperature and cooling conditions of power devices need to be carefully characterized.
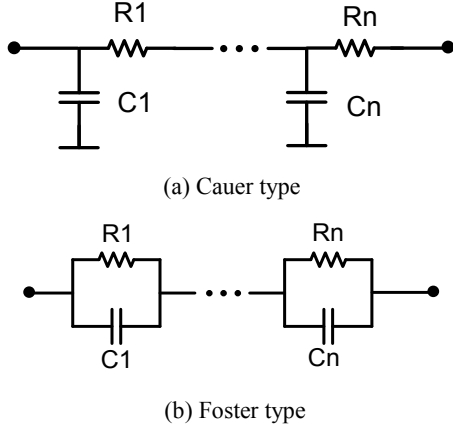
(a) Cauer type

(b) Foster type

Fig. 1. Commonly used thermal networks for power devices based on RC lumps.

In order to improve the thermal modeling based on Foster thermal networks, a mathematical transformation is developed which can convert the Foster network to an equivalent Cauer type with the same number of RC lumps [18], [19]. Although the obvious error of the device temperature when including the cooling conditions seems to be avoided, this mathematical transformation does not regain any physical means of the internal structure of the power device, and the accuracy of the estimated device temperature still needs to be evaluated.

In the last decade, some more advanced modelling techniques have been introduced to improve the prediction of thermal dynamics for power device [19]-[22], however they mainly focus on the internal temperature behaviours of the device, and the problems of the existing thermal models when considering the external cooling conditions are not considered or solved.

In this paper, the power loss/heat and temperatures of power semiconductor devices are considered as signals under frequency domain, and the corresponding frequency-domain models are first established for several typically used thermal networks. Afterwards the performance and limits of the Foster type and its equivalent Cauer type thermal model are explained from a new point of view. Based on the discovery, a new thermal model is proposal which put more efforts to establish correct transfer function for the filtering of power loss, and thereby it can overcome some of the limits in the exiting RC thermal networks for the power devices. Finally some simulation results are given to validate the accuracy and advantage of the proposal thermal model under both time and frequency domains.

II. FREQUENCY DOMAIN THERMAL MODELLING AND LIMITS OF THE EXISTING THERMAL MODELS BASED ON RC LUMPS

A multi-layer Cauer type thermal network for a IGBT module is first defined as a study reference in this paper, as shown in Fig. 2. This Cauer thermal model is extracted from the internal structure and material specifications for a 1700V/100A IGBT module used for wind power application, as shown in Fig. 3 and Table I, where a heat spreading angle of 45º is assumed. It can be seen that 7 Cauer type RC lumps are introduced to represent 7 layers of the internal materials of device as indicated in Fig. 2. To model the cooling conditions outside the device, a large thermal resistance is used to represent the thermal behaviour of thermal grease, and a series of small thermal resistances with large thermal capacitances are used to represent the thermal behaviour of heat sink. It is assumed that the network in Fig. 2 and the parameters in Table I can correctly reflect the temperature behaviours of the given IGBT module under the given specifications and cooling conditions. Although more detail and complicated modelling techniques such as [21], [22] can be introduced to refine the parameters in Table I, they can be updated depending on the needs of accuracy, but are not considered in this paper.
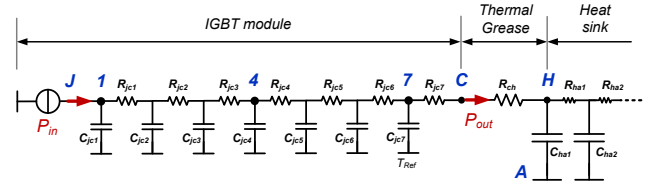

Fig. 2. Cauer type thermal network based on Fig. 3 as reference for this study.
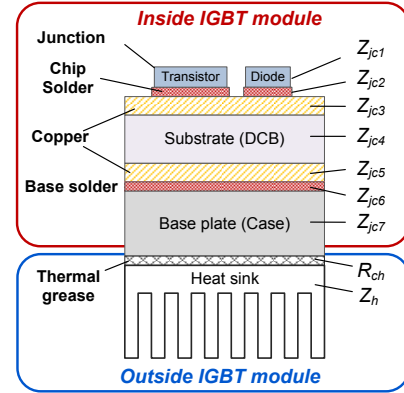

Fig. 3. System consisting of an IGBT module mounted on a heat sink as reference for the study.

Table I. Parameters for the material, layer and thermal impedance of Fig. 3.

Layers	Thickness (mm)	Density (g/cm3)	Specific heat (J/kg·°C)	Thermal conductivity (W/m·°C)	Thermal resistance (K/W)	Thermal capacitance (J/K)
Chip (Silicon)	0.3	2.3	790	83.6	0.0194	0.1021
Chip solder	0.05	9.7	260	78	0.0034	0.0179
Copper	0.3	8.9	397	386	0.0040	0.2092
DCB (Al₂O₃)	0.7	3.7	880	18	0.1732	0.5118
Copper	0.3	8.9	397	386	0.0030	0.2732
Base solder	0.1	9.7	260	78	0.0048	0.0517
Base (Copper)	3	8.9	397	386	0.0209	4.0898
Thermal grease	0.021	2.25	NA	0.8	0.0518	NA

Inspired by the typical approach used for the analysis of electrical RC circuits, it is also possible to model the frequency-domain characteristics of thermal RC networks in order to further understand the thermal behaviors and thermal dynamics of power device, which will be detailed a follows:

A. Thermal modelling under frequency domain – reference Cauer network

Normally the power loss P_{in} is injected into the node J or node 1 of the Cauer type thermal network in Fig. 2, and a series of temperatures and heat flows can be identified in this network. It is noted that the power loss or heat source P_{in}, which is generated in the chips of IGBT the module, can be seen as a input signal; while the corresponding temperatures on each node of the thermal network or different layers of the material can be seen as response signals, as well as for the heat flow after each node/layer. As a result the gain from disturbance P_{in} to each of the thermal response under Laplace domain can be analytically solved with the information of R and C parameters.

One group of important relationships between the thermal disturbance and responses, are the gains from input heat P_{in} to the temperature responses on each node of Fig. 2, these gains can be solved as the following functions:

$$Z_{P_{in}T_{X\_H}}^{\mathrm{Ref}}(s) = \frac{T_{(\cdot)}}{P_{in}}$$

$$= \frac{\cdots}{(s)+\cdots} = $$

where s is the Laplace operator, $Z_{P_{in}T_{X\_H}}^{\mathrm{Ref}}(s)$ represents the impedance from input loss (P_{in}) to the temperature difference between node X and the heat sink node H (T_{X_H}), when the reference Cauer network (Ref) is analyzed. R_{ch} is the thermal resistance of thermal grease, R_{jcX} represents the thermal resistance of each of the 7 layers inside the device, and C_{jcX} is the thermal capacitance for each layer. The parameters of R_{ch}, C_{jcX} and R_{jcX} can be found from Table I. It is noted that, for simplicity of analysis the heat sink temperature T_H is considered as a reference temperature in the modelling process of this paper, because normally the thermal capacitance of a suitable heat sink is a factor of 100-1000 compared to the internal thermal capacitances of the power device, and the temperature on node H is much more stable than the temperatures on nodes 1 to C. However, other reference node such as ambient A can be chosen as the reference temperature, coming with some small deviations in function (1).

Another group of important relationships between the thermal disturbance and responses are the gains from input heat P_{in} to the heat flowing out of each node in Fig. 2. This group of relationships is typically not considered in most of the existing thermal networks, and can be solved as the following functions for the reference Cauer model:

$$G_{P_{in}P_X}^{\mathrm{Ref}}(s) = \frac{1}{\cdots(s)\cdots + \cdots} = $$

where $G_{P_{in}P_X}^{\mathrm{Ref}}(s)$ represents the gain from input heat/loss (P_{in}) to the heat flowing out of node X (P_X), when the reference Cauer network (Ref) is chosen.

Based on (1) and (2), the gain from P_{in} to the temperature difference between junction node J and case node C, as well as the gains from P_{in} to the heat flowing out of the device P_{out}, can be solved as:

$$Z_{P_{in}T_{jc}}^{\mathrm{Ref}}(s) = \frac{T_{(\cdot)}}{P_{in}} = $$

$$G_{P_{in}P_{out}}^{\mathrm{Ref}}(s) = \tag{4}$$

It is noted that G_{PinTjc} and $G_{PinPout}$ are selected as two of the indicators to benchmark the accuracy of thermal models focused in this paper. As a result the frequency-domain model for the reference 7 layers Cauer type thermal network is established.

B. Thermal modelling under frequency domain – Foster network

When applying a step power loss P_{in} to the reference Cauer network shown in Fig. 2, the temperature response in node J and node C can be measured and recorded, afterwards the Foster type thermal network and its RC parameters can be extracted by curve-fitting the time-domain temperature responses with the following functions [10]:

$$Z_{jc}^{\mathrm{Foster}}(t) = \frac{T_{(\cdot)}}{P_{in}} = \sum \tag{5}$$

where R_{fn} and C_{fn} represent the mathematically-solved thermal resistance and thermal capacitance for the Foster thermal network, and are connected in the form as indicated in Fig. 4. In (5) X means the number of pairs for the used R_{fn} and C_{fn}, normally 4 pairs of Foster RC parameters can achieve an accurate fitting to most of the temperature responses between node J and C for IGBT module, in the case of this paper they are summarized in Table II.

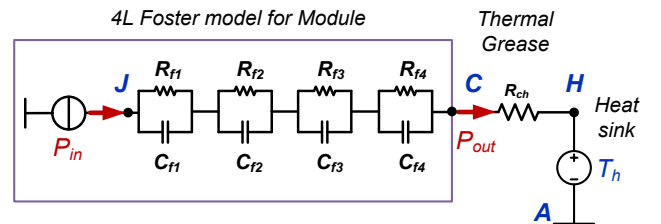4L Foster model for Module — Thermal Grease

Fig. 4. Foster type thermal network fitted from the referenced Cauer network shown in Fig.2.

Table II. Parameters of the Foster and equivalent Cauer network in Fig. 4 and Fig. 5 for the reference device.

Foster network		Equivalent Cauer network	
Thermal resistance R_{f1-4} (W/K)	Thermal capacitance C_{f1-4} (J/K)	Thermal resistance R_{ec1-4} (W/K)	Thermal capacitance C_{ec1-4} (J/K)
0.0014	15.646	0.0249	0.1062
0.0188	0.0023	0.1602	0.7285
0.0892	0.4059	0.0422	8.39
0.1191	0.1167	0.0013	11950

The gain from input loss P_{in} to the temperature difference between node X and heat sink, as well as the gain from input loss P_{in} to the heat flow/power loss after each node X can be solved in (6) and (7) respectively for the Foster thermal network.

$$Z_{P_{in}T_{X\_H}}^{\text{Foster}}(s) = \sum \tag{6}$$

$$G_{P_{in}P_X}^{\text{Foster}}(s) = \tag{7}$$

Then the two benchmark indicators Z_{PinTjc} and $G_{PinPout}$ for the given 4 layers Foster thermal network can be solved in (8) and (9):

$$Z_{P_{in}T_{jc}}^{\text{Foster}}(s) = \sum \tag{8}$$

$$G_{P_{in}P_{out}}^{\text{Foster}}(s) = \tag{9}$$

C. Thermal modelling under frequency domain – Equivalent Cauer network [18]

4L Equvilent Cauer model for Module
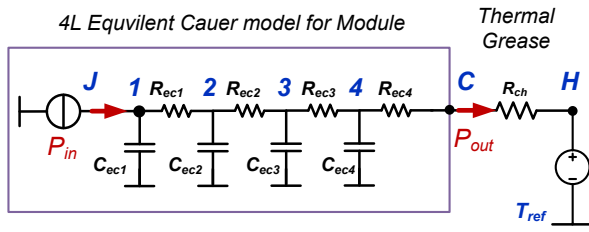
D.

Fig. 5. Equivalent Cauer type thermal network converted from the Foster network shown in Fig.4.

This type of thermal network targets to solve some problems of the Foster type thermal network as mentioned before, and is often used for the electro-thermal simulation of the power device temperature. By applying the mathematical

transformation and boundary conditions shown in [18], the Foster type RC network in Fig. 4 can be converted to an equivalent Cauer type thermal network with the same pair numbers of RC parameters but different values, as shown in Fig. 5 and Table II.

Thereby the frequency domain thermal model for the given 4 layers equivalent Cauer RC network can be established. The gain from input loss P_{in} to the temperature difference between node X and heat sink, as well as the gain from input loss P_{in} to the heat flow/power loss after each node X can be solved in (10) and (11) respectively. The two benchmark indicators Z_{PinTjc} and $G_{PinPout}$ can be solved in (12) and (13):

$$Z_{P_{in}T_{X\_H}}^{\text{eqCauer}}(s) = \tag{10}$$

$$G_{P_{in}P_X}^{\text{eqCauer}}(s) = \tag{11}$$

$$Z_{P_{in}T_{jc}}^{\text{eqCauer}}(s) = \tag{12}$$

$$G_{P_{in}P_{out}}^{\text{eqCauer}}(s) = \tag{13}$$

### E. Limits of existing thermal models based on RC lumps

With the built frequency-domain models of the three types of thermal networks, the bode plots of interesting gains can be compared. One benchmark bode plot is the gain from loss P_{in} to the temperature difference between junction and case, which is normally provided by the manufacturer datasheet or measured by the user as a important thermal characteristic of the power device. As it can be seen in Fig. 6 (a), the gain difference among the three types of thermal model is almost ignorable. However, when comparing the bode plot of the other benchmark gain from P_{in} to the output heat of power device P_{out}, the difference between the three types of thermal models are significant, as shown in Fig. 6 (b): As the correct thermal behaviors assumed in this paper, the reference 7 layers Cauer type thermal network (Cauer_ref) behaves like a second-order low pass filter to the input heat P_{in} with bandwidth around 0.5 Hz; while the curve-fitted 4 layers Foster type thermal network (Foster_4L) behaves transparently to the frequency components of P_{in} whose disturbances will be immediately seen by the thermal grease and heat sink outside the power device (obviously incorrect

in real case). On the contrary the equivalent 4 layers Cauer type thermal network (eqCauer_4L) transformed from

Foster_4L has much lower bandwidth compared to the Cauer_Ref, which means many important disturbances of P_{in} in the real case will be blocked and not seen by the thermal grease and heat sink.
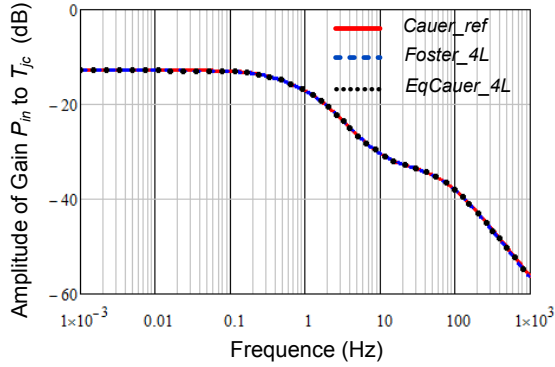
(a) Gains from P_{in} to T_{jc}
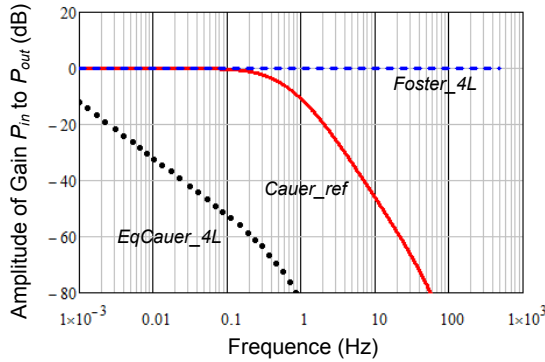
(b) Gains from P_{in} to P_{out}.

Fig. 6. Bode plot of critical gains in various thermal networks under frequency domain. (Cauer_ref: reference 7 layer Cauer thermal network, Foster_4L: 4 layer Foster type fitting network to the temperature response of Cauer_ref, EqCauer_4L: mathematical transformation from Foster_4L to the equivalent Cauer type).

The time domain simulations also agree with the behaviours predicted under the frequency domain, as shown in Fig. 7, where a step power loss P_{in} of 100 W at the time of 1 second is applied to various thermal networks. It can be seen that, compared to the Cauer_Ref model, the Foster network has no filtering effect to the injected power loss/heat, which immediately flows through the thermal grease outside the device and result in large error at the beginning of thermal transient of the junction temperature T_j; but the steady-state T_j is more consistent with the Cauer_Ref. While the equivalent Cauer type network converted from the Foster type has over-filtering effects to the injected power loss/heat, thereby the junction temperature T_j has large error at the steady-state, but it has good agreement at the beginning of the thermal transient with the Cauer_Ref.

As a conclusion, either the Foster or its equivalent Cauer type thermal network has their limits to describe the correct thermal dynamics of power device, the key to achieve more correct thermal modelling, especially when considering the thermal grease and heat sink, is to create a correct filtering to the power loss – or correct heat gain from P_{in} to P_{out} ($G_{PinPout}$) under the frequency-domain.

III. A New Thermal Model for power device under Frequency Domain

A. Characterization of the heat flowing out of device

In the practice, the Cauer type RC parameters based on the structure and material of the power semiconductor devices is difficult to be accurately accessed and the correct heat gain from P_{in} to P_{out} is also hard to be directly solved from the commonly used Foster type thermal network. For
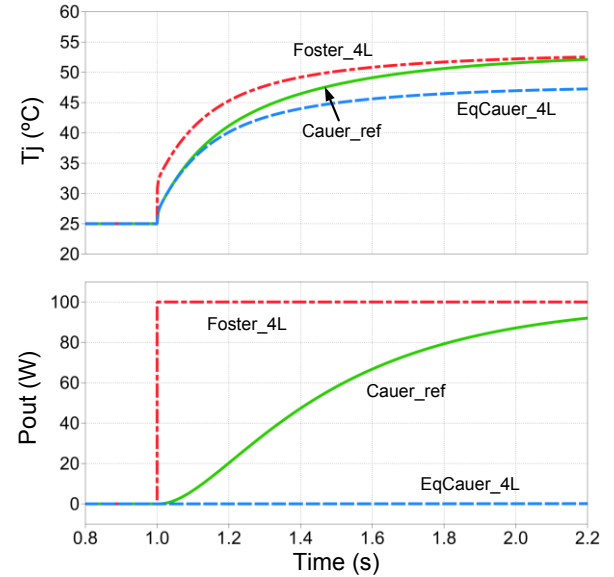

Fig. 7. Time domain simulation of the junction temperature under a step power loss in various thermal networks (100W loss step at 1 second, T_H=25ºC).

this reason new approaches have to be investigated in order to find the correct gain from P_{in} to P_{out}.

By looking at the slopes and corner frequencies of the heat gains G_{PinP1} to G_{PinP7}, the 7 layers of materials in the reference Cauer network can be seen as a series of low pass filters and can be classified into three dominant groups: the first groups consists of layers from chip to the upper copper as shown in Fig. 10, (Node 1 to 4 in Fig. 2), the second group consists of layers from DCB to Base solder (Node 4 to 7), and the third group consists of layer of base plate (Node 7 to C). It is interesting to see that in each group of material layers, the frequency behaviours of heat gains are very similar to each other. And the characteristics (corner frequencies and slope changes) among the three groups of heat gains generally follow the behaviours of three cascaded low-pass filters. As a result, the reference 7 layer Cauer type thermal network for

the device can be degraded to 3 cascaded 1st-order low pass filters, as illustrated in Fig. 8, where C_{jc123}, C_{jc456}, C_{jc7} represent the virtual thermal capacitances for each dominant group of layers, and P_{123}, P_{456}, P_7 represent the virtual heat flowing out of each dominant group of layers.

Because the DC gains of the heat transfer function on each node all equal to 0 dB, the key to establish correct gain from P_{in} to P_{out} ($G_{PinPout}$) is to identify the three dominant corner-frequencies of the cascade low-pass filter.

Based on the simplified thermal network shown in Fig. 8, the benchmark thermal impedance of the power device Z_{PinTjc} can be revised as the sum of three parts:

$$Z_{P_{in}T_{JC}}(s) = \qquad + \qquad +$$

$$= \qquad \cdot \sum \qquad \qquad \sum \qquad \qquad (14)$$

Where

$$G_{P_{in}P_{123}}(s) \approx \qquad \approx \qquad \approx$$
$$G_{P_{in}P_{456}}(s) \approx \qquad \approx \qquad \approx \qquad (15)$$

It can be seen that, the the thermal impedance Z_{PinTjc} is inherently correlated with the heat gains of the three dominant groups of material (14). Therefore it is possible to extract the dominant corner-frequencies of the heat gains from the thermal impedance Z_{PinTjc}, which can be more
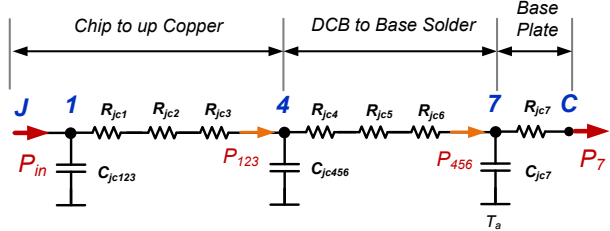
Fig. 8. Transformation of the 7L-Cauer type network to a third order low pass filter according to the frequency behaviours.

accurately and easily acquired with experimental measurement. In Fig. 9, the bode diagram of Z_{PinTjc} and its three components Z_{PinT14}, Z_{PinT47}, and Z_{PinT7C} are plotted with the slope changing information, several corner-frequencies on Z_{PinT14}, Z_{PinT47}, and Z_{PinT7C} can be seen. By deviating the slope of Z_{PinTjc}, the corner frequencies (f_1, f_2 and f_3) in the Z_{PinTjc} can be identified, as shown in Fig. 12, which are closely related to the corner frequencies for the three groups of heat gains as shown in Fig. 9.

However, according (14), the corner-frequencies on Z_{PinTjc} are also influenced by the weighed interaction/summing up among the three groups of heat gains, thereby the corner-frequencies on Z_{PinTjc} are slightly different from the corner-frequencies in the heat gains. One solution is to use a Foster type RC network to re-shape the frequency behaviours of Z_{PinTjc}, by using the boundary conditions for the numbers and range of the critical frequencies identified in Fig. 10. Because

each pair of RC lump in the Foster network can be seen as a first-order lower pass filter, whose corner frequency can be easily calculated based on the RC parameters, and then the interaction among the three dominant heat gains can be decoupled. In the case of the given IGBT module for case study, 3 pairs of RC parameters with corner frequencies f_{c1}= 0.38 Hz, f_{c2}=1.36 Hz,
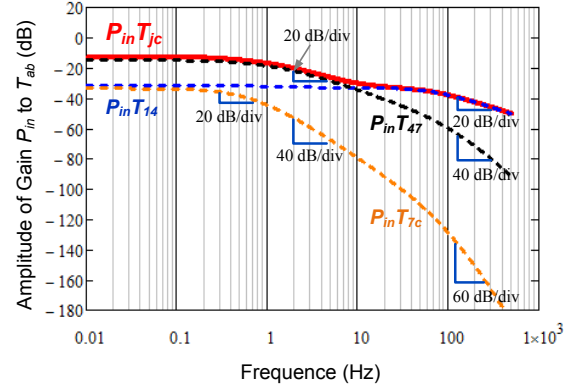
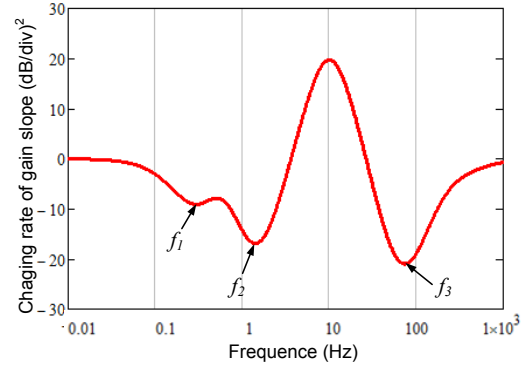Fig. 9. Bode plot and slop of thermal impedance gains for the reference 7L Cauer type network.

Fig. 10. Identified corner-frequencies from bode plot of Z_{PinTjc} in Fig. 9.

and f_{c3}=70.36 Hz, can be extracted. By cascading three 1-order low pass filters with the extracted corner frequencies and unity DC gain, the heat transfer function $G_{PinPout}$ for power device can be recomposed by only the information of the measured Foster type thermal impedance Z_{PinTjc}. So the low-pass filter for the power loss can be calculated as:

$$G_{LPF}(s) = \frac{\qquad}{\qquad + \qquad} + \qquad + \qquad (16)$$

In Fig. 11, the bode plot of the heat gains $G_{PinPout}$ by the new methods are shown, it can be seen that the extracted 3-order Low Pass Filter from the Foster thermal network has almost the same frequency behaviour with the $G_{PinPout}$ in the

reference Cauer thermal network. As a comparison, the $G_{PinPout}$ of the Foster thermal network in Fig. 4 is also shown.

A. A new thermal model under frequency domain

As a result, a new thermal model is proposed based on the extracted $G_{PinPout}$. As shown in Fig. 12, the proposed thermal model contains two paths: The first thermal path is used for the junction temperature estimation inside power device. In this path the datasheet-based or experimentally measured Foster thermal network of power device are used, and only a reference temperature, whose value is determined by the case temperature T_c from the other thermal path, is connected. The second thermal path is used for the temperature estimation outside the device. In this path the extracted low pass filter from the Foster thermal network is used to model the loss behaviours flowing out of device, and the filtered loss can create correct temperature behaviours of thermal grease T_{CH} and heat sink T_{HA} outside the devices.
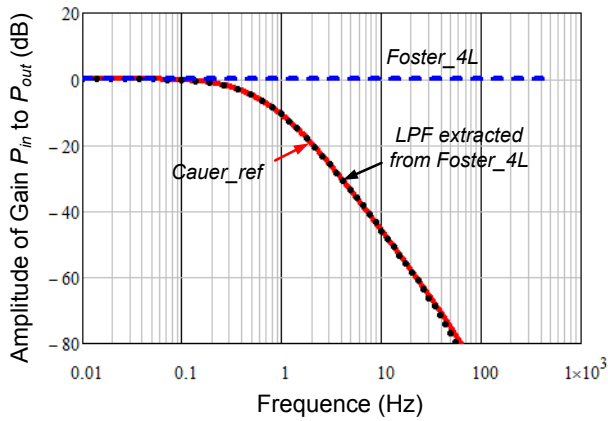

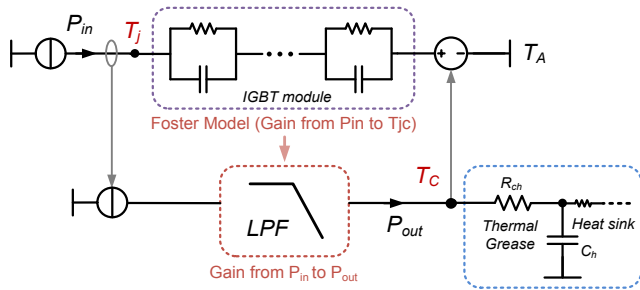Fig. 11. Bode plot of heat gain $G_{PinPout}$ by different thermal networks.

Fig. 12. Proposed thermal model for power device based on frequency domain.

The two benchmark indicators Z_{PinTJC} and $G_{PinPout}$ for the new thermal model can be solved in (17) and (18), and then the gain from P_{in} to junction temperature can be calculated in (19):

$$G_{P_{in}T_{jc}}^{New}(s) = \qquad)$$

(17)

$$G_{P_{in}P_{out}}^{New}(s) =$$

(18)

$$Z_{P_{in}T_j}^{New}(s) = \frac{T}{I_{in}} \qquad = \qquad + \quad .$$

(19)

The bode plot of Z_{PinTj} and time domain simulation on the same conditions of Fig. 8 are implemented on the new thermal model, as shown in Fig. 13, and Fig. 14, respectively. It can be clearly seen that, there are good agreement of the new thermal model with the reference 7 layer Cauer model either in the frequency domain and time domain. It is noted that the new thermal model is only based on the information of Foster type thermal network which is commonly accessed from the datasheet or external measurements of device, and it is independent of the internal materials, structure and heat path information of devices, being a promising advantage.
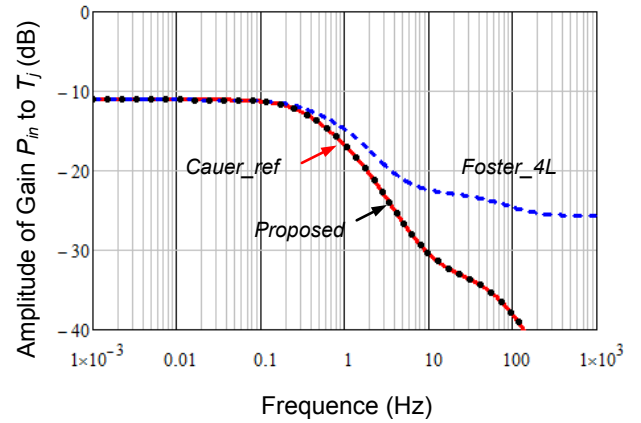

Fig. 13. Bode plot of gains from P_{in} to T_j in various thermal networks. (T_H is used as reference temperature)
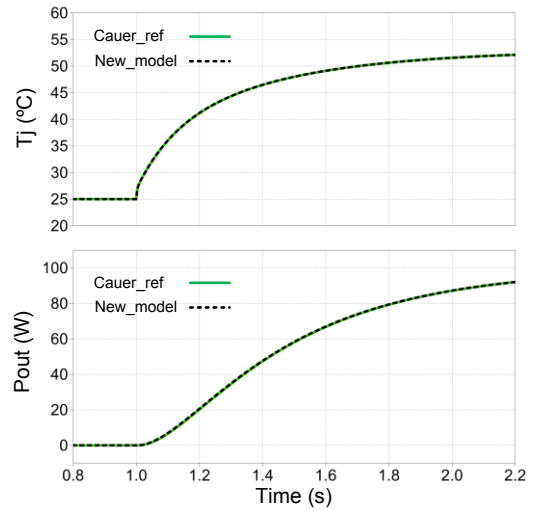
Fig. 16. Time-domain simulation of the thermal dynamics under a step of power loss in the proposed thermal network (same conditions of Fig. 7, 100W loss step at 1 second).

IV. CONCLUSION

The frequency domain modelling is conducted on several typically used thermal networks for power semiconductor devices. It is found that either the widely used Foster type or its equivalent Cauer type thermal networks have their limits to correctly predict the device temperatures, especially when considering the cooling conditions outside device. The main reason is due to the incorrect model of heat behaviours flowing out of device.

A new thermal model is proposed, which puts more efforts to establish correct transfer function for the filtering effects of power loss. It is only based on the information of Foster type thermal network which is easily accessible from the datasheet or external measurements, and it is independent of the internal materials and structure information of power devices. Compared to the existing thermal models, the proposed model can achieve more correctly estimation of device temperature when the attached cooling conditions are considered.

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