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Comparison of Basic Power Cells for Quad-Active-Bridge DC-DC Converter in Smart Transformer

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Keywords

<<Smart Transformer>>, <<DC-DC Converter>>, <<High Voltage>>, <<Multilevel Converter>>, <<Modularity>>

Abstract

Smart Transformer (ST) is a promising technology, which usually requires a high frequency high voltage dc-dc converter. This paper investigates the application of a Quad-Active-Bridges (QAB) converter using multilevel bridges as a solution for the dc-dc stage of Smart Transformer. The focus of this work is to compare in terms of efficiency 2-level and 3-levels bridges in a QAB converter for ST applications. The considered power cell topologies are: H-bridge, Neutral-Point-Clamped (NPC), Flying-Capacitor (FC) and T-type (TT). The NPC and FC show as main advantage reduced voltage over their semiconductors, which allow the utilization of IGBT and diodes with lower forward drop voltage. Meanwhile, the HB topology shows as advantage reduced current through its device. Thus, a comparative study is performed in order to find out the most suitable topology for this application. Two scenarios are defined and the comparison and final results are presented for both scenarios.

Introduction

Smart Transformers (ST) is an essential element to enable the future electric distribution system based on smart grids technologies, due to its capability to provide ancillary services to the grid and its feature of high power density (reduced size and weight) [1] - [4]. In this kind of system, a high frequency isolated dc-dc converter is required to connect the low voltage (LV) dc side to the medium voltage (MV) dc side. This power processing stage is still a challenge to the power electronics, due to the requirements of high current capability in the LV side, high voltage capability in the MV side, besides the high frequency isolation and high efficiency. The requirement of operation with high voltage is the main issue of this converter, because of the technological limitation of the semiconductors available in the market, mainly about its blocking voltage. To overcome this problem, a modular solution based on several LV modules can be used, in order to share the total voltage and power among the modules, enabling the use of standard devices.

In this scenario, this work uses a modular concept to implement the dc-dc stage of the ST, where the basic modules are based on the Quad-Active-Bridge (QAB). The QAB converter, previously proposed in [5]- [6], is composed by four active bridges connected to the same four winding transformer, as shown in Fig. 1 (a). In this application, one active bridge is connected to the LV side (called in this paper as LV cell) and the others three actives bridges are connected to the MV side (called in this as paper MV cell), in order to share the voltage among them. Although the QAB converter has been proposed with H-Bridge (HB) cell in [5]- [6], 3-level topologies (see Fig. 1(b) to (e)) , can also be employed to this converter, presenting the additional advantage of reduced voltage on the semiconductors. Depending on the number of modules and the voltage on the MV side, multilevel cells can be much more advantageous than 2-level cells in terms of efficiency. In this context, this paper investigate the performance of the QAB converter with different power cells in the MV side, when applied as a module of a Smart Transformer. The

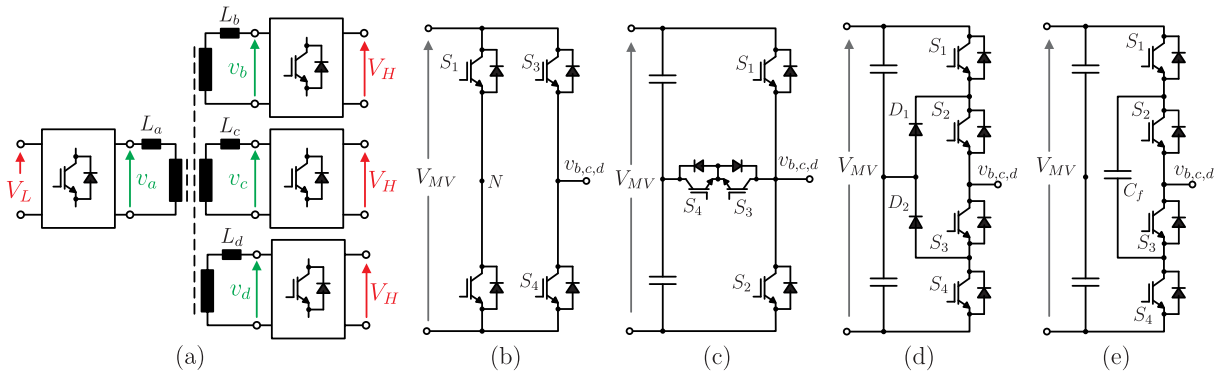


Figure 1: (a) Topology of the Quad-Active-Bridge (QAB) dc-dc converter. (b) to (e) are basic cells used in the Medium-Voltage side of the QAB converter: (b) H-Bridge (HB), (c) T-Type (TT), (d) Neutral-Point-Clamped (NPC), (e) Flying-Capacitor (FC).

topologies studied in this paper are: Neutral-Point-Clamped (NPC), Flying-Capacitor (FC), T-Type (TT) as showed in Fig. 1 (c). Although the T-Type does not present reduced voltage over its semiconductors, in recent years the research has shown high performance of this structure [7], [8]. For that reason, the T-Type converter is also evaluated in this paper. Besides that, the conventional H-bridge topology is also evaluated and a comparison among all the power cells is performed. Independently of the MV cell topology, the LV voltage cell is based on the standard HB topology.

It is important to note that the main objective of this paper is a comparative study in terms of efficiency of multilevel topologies as an active bridge of a QAB converter applied to SST. Details of the ST architecture employing the QAB converter are provide in Section II of this paper. Then, design consideration of the QAB dc-dc converter is presented in Section III, where the modulation strategy, optimum parameters choice and also semiconductor selection and losses calculation are described. Finally, the results of the comparison considering two possible scenarios will be shown and discussed.

Smart Transformer Architectures

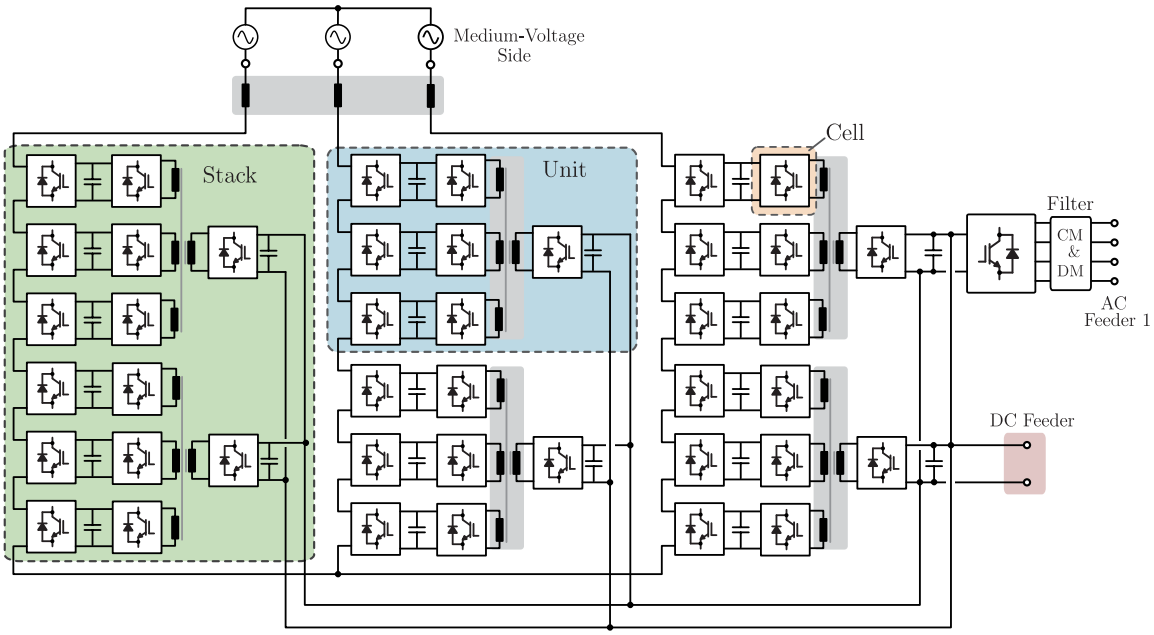
The proposed smart transformer architecture employing the QAB is show in Fig. 2. As can be observed, there are two output available on the LV side, an ac feeder and a dc feeder for direct connection of dc loads. The MV AC to DC conversion is realized by the well-know cascaded H-bridge converter (CHB). To connected the several dc-links on the MV side to the Low-Voltage dc-link (LVDC), the QAB converter is used. A power unit (highlighted in Fig. 2) can be defined as a replaceable part of the system. In this architecture, an unit is composed by an entire QAB converter and some modules of the CHB converter, but only those associated to the QAB converter of the unit, as can be seen in Fig. 2. The power cell is the smallest power block of the unit and it is also highlighted in Fig. 2.

The specification of a typical Smart Transformer for distribution system application is presented in Table I. As can be seen, the total dc-link in the MV side is 10.2 kV. Depending on the number of units, the voltage in each power cell can be still very high. Thus, the comparative study among the different basic power cells (shown in Fig. 1) is carried out for two different scenarios. The first one is a ST architecture with two units per phase, resulting in a total of six units (Fig. 2 (a)). In this scenario, the total voltage dc-link is partitioned among six cells of the QAB converter, resulting in a voltage of 1.7 kV in each dc-link cell. For this condition, the voltage rating of the IGBT must be 3300V for 2-level topologies as MV cell or 1700 V for 3-level cells. The second scenario is a ST based on the same architecture, however with higher number of units per phase. The ST structure is shown in Fig. 2 (b) and it has three units per phase. In this case, the dc-link voltage of each MV cell is 1.14 kV, which allows the use of IGBT with voltage rating of 1700V for 2-level topologies and 1200 V for 3-level topologies. The specification of the QAB converter for both scenarios are shown in Table II.

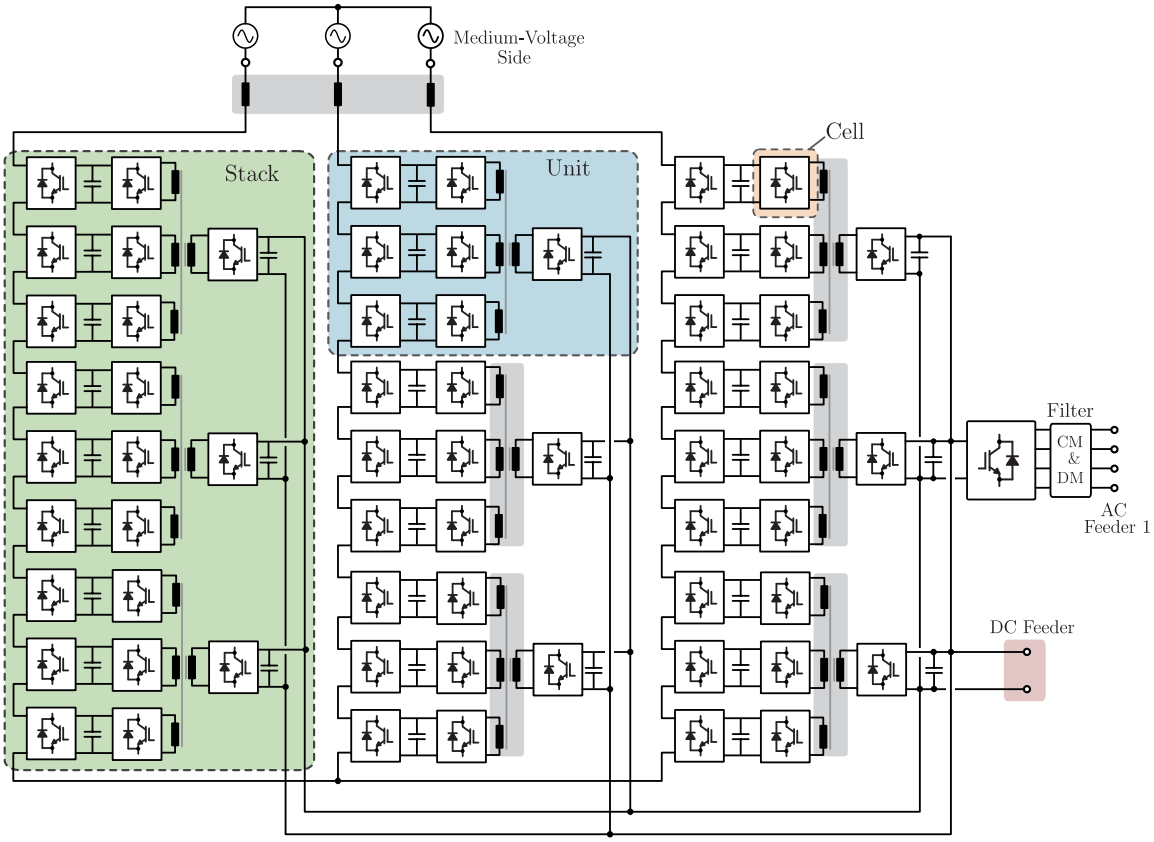
In this paper, the design of the QAB converter parameters, semiconductors selection and losses calculation and the comparative evaluation are carried for both scenarios. It is also important to cite, that the architecture might have additional standby unit to increase the reliability of the system. However, these units are not illustrated in Fig. 2.

Table I: Specification of a Smart Transformer applied to distribution system

	Rated Power	MV level	LV level	MVDC link	LVDC link
ST specification	1 MW	10 kV	700 V	10.2 V	700 V



(a)

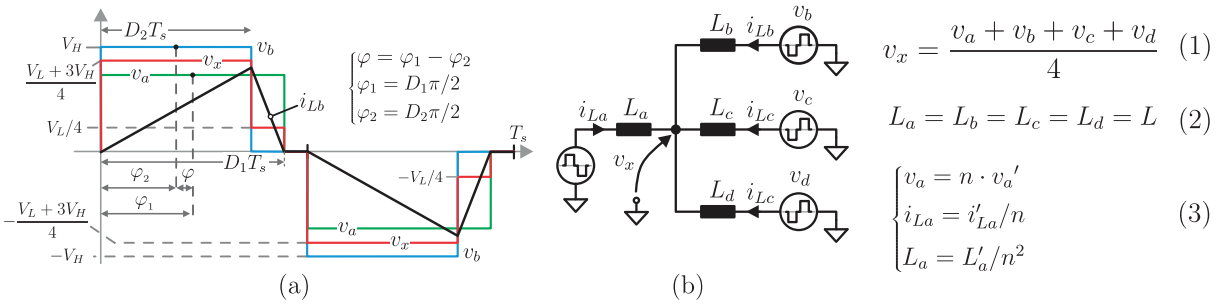


(b)

Figure 2: Proposed architecture of the Smart Transformer using the Quad-Active-Bridge converter: (a) structure with two units per phase and referred as scenario 1 in this comparative work; (b) structure using three units per phase and referred as scenario 2.

Table II: Specification of the QAB converter in both different architecture configuration

	MVDC link	Converters	Power of the Unit	MV cell voltage	LVDC link
Scenario 1	10.3 kV	6	166 kW	1700 V	700 V
Scenario 2	10.3 kV	9	111 kW	1140 V	700 V



$$v_x = \frac{v_a + v_b + v_c + v_d}{4} \quad (1)$$

$$L_a = L_b = L_c = L_d = L \quad (2)$$

$$\begin{cases} v_a = n \cdot v_a{}' \\ i_{La} = i'_{La}/n \\ L_a = L'_a/n^2 \end{cases} \quad (3)$$

Figure 3: (a) Basic waveforms of the QAB converter using triangular modulation strategy (voltage of the port b (v_b) in blue; voltage of the port a (v_a) in green; voltage v_x in red; current through the inductor of the port b (i_{Lb}) in black) and (b) the equivalent Y-model of the QAB used in the analysis.

Design Considerations for the QAB Converter

Fig. 1 (a) shows the topology of a single QAB, while Fig. 1 (b)-(e) shows the 3-level topologies that will be study in this paper as a candidate for the MV side. In a half-bridge configuration the maximum peak to peak voltage amplitude that can be synthesized in the ac side is equal to the dc-link voltage, while in a H-bridge this is equal to two times the dc-link voltage. Therefore, the H-bridge topology requires lower current to process the same amount of power, when compared to the T-type, NPC and FC topologies. On the other hand, the NPC and FC allows the use of IGBT with lower breakdown voltage, which usually presents lower forward drop voltage. Thus, a semiconductor losses calculation, taking into account all this considerations is performed. To analyze, design and compare the topologies the same modulation strategy is used for all bridges. This modulation strategy presents several advantages as soft-switching operation regardless the load and simple power control. A brief description of the modulation strategy and converter design are introduced in this section.

Modulation Strategy

To operate the QAB converter with multilevel bridges, a Triangular Modulation Strategy (TMS), previously proposed in [9] is employed. This strategy imposes a triangular current on the inductors, as shown in Fig. 3 (a). To simplify the analysis, the Y-model of the QAB (shown in Fig. 3 (b)) can be used. Is this model, the bridges are replaced by rectangular voltage source (v_a, v_b, v_c and v_d). The voltage of the central point v_x is given by (1). Considering the same inductance for all inductors, as shown in (2), and referring the variables to the MV side, using the relation shown in (3), the analysis can be performed from the viewpoint of the source v_b. The voltage over the inductor L_j is $v_L = v_j - v_x$, where $j = \{a,b,c,d\}$. The current i_{Lb}, the voltages v_b and v_x are shown in Fig. 3 (a). In this fig. D_1 is the duty-cycle of the LV bridge and D_2 is the duty-cycle of the bridges in the MV side. To achieve zero current switching (ZCS) operation regardless the load and input or output voltages level, the condition $\Delta i_{Lb_{(0<t<D_2T_s)}} = \Delta i_{Lb_{(D_2T_s<t<D_1T_s)}}$ must be satisfied. As a result, the relation between the duty-cycles D_1 and D_2 is found and presented in (4). The relation of the converter duty-cycle and the power processing is given by (5). Hence, D_1 can be used to control the total power transferred from the MV side to the LV side (and also to control the LVDC link), while the duty-cycle D_2 is calculated to ensure ZCS operation. However, ZCS operation is not always possible, since in unbalance condition (i.e. MV cell processing different amount of power) the duty-cycle of the MV cells are slightly changed to control individually the power processed by each MV cell. It is important to note that in this paper, only balanced condition is considered, i.e. the low voltage bridge operates with duty-cycle D1 and all the three MV bridges operate with the same duty-cycle D2.

$$D_2 = \frac{V_L \cdot n}{V_H} D_1 \quad (4)$$

$$P = \frac{3 \cdot {D_1}^2 \cdot (V_L \cdot n)\,(V_H - V_L \cdot n)}{4 \cdot L \cdot f_s} \quad (5)$$

$$I_{pri_{rms}} = \frac{V_L \cdot n}{12 \cdot L \cdot f_s} \cdot \sqrt{\frac{6 \cdot {D_1}^3 \cdot \left({V_H}^3 - 5 \cdot {V_H}^3 \cdot V_L \cdot n + 10 \cdot V_H \cdot (V_L \cdot n)^3 - 6 \cdot (V_L \cdot n)^3\right)}{{V_H}^3}} \quad (6)$$

Converters Design

In order to enable a fair comparison, an optimized design of all the converters must be performed. Some parameters must be carefully chosen, as switching frequency (f_s), inductance (L), transformer ratio ($n = N_{prim}/N_{sec}$), because their values may directly impact the operation and, consequently, the losses of the converter. In addition, the semiconductors must be chosen, as well as the heatsink profile and cooling system, however the design of these elements will be discussed in the next section. For the design, it is considered that the converter is operating with direct power flow (from MV to LV) with maximum power, according to Table II.

The triangular modulation strategy employed imposes two condition that must be satisfied: (1) $D1 < 0.5$ and $D2 < 0.5$; and (2) $V_H \neq n \cdot V_L$. Considering both conditions and the converter specification shown in Table II, the optimum values of all parameter can be easily chosen for each converter. To reduce the losses and increase the efficiency, the parameters are chosen in order to minimize the primary side current, since this current is directly related to the semiconductors (even for LV and MV sides) and transformer losses.

The primary side rms current is described by the equation (6). In this equation, we have the relation between the primary side rms current, transformer ratio, inductance, switching frequency, besides the parameters defined in Table II, V_H, V_L and P. Nevertheless, it is important to keep in mind that the condition $D1 < 0.5$ must be satisfied. Then, equation (5) must be considered and it will limit the range of these parameters. Fig. 4 (a) shows the variation of the duty-cycle D_1 as a function of the transformer turn ratio and inductance(for the given output power and input/output power shown in II) for the QAB with TT/NPC/FC cells operating in scenario 1. As can be observed in the figure, there is a degree of freedom to chose the inductance or turn ratio to allow the converter to operate with $D_1 < 0.5$. However, the graphic of the rms current on the primary side as a function of n and L, depicted in Fig. 4 (b) (for the same condition), shows that the higher inductance and lower turn ratio will reduce the rms current on primary side. Therefore, the inductance is chosen to be the highest possible and the turn ratio is chosen to have $D_1 = 0.45$ for the maximum power processing. Note that higher inductance is more feasible to be built. In both figures, the limits defined by the TMS is very clear and the shaded area is the forbidden operation area.

The same procedure is applied to all cells and the graphics required to determine the parameters of all the converters for both scenarios are shown in Fig. 4. The optimum parameters for all converters are summarized in Table III for both scenarios. In this table, the rms primary current values and the maximum semiconductor voltage is also presented.

Semiconductors Selection and Power Losses Calculation

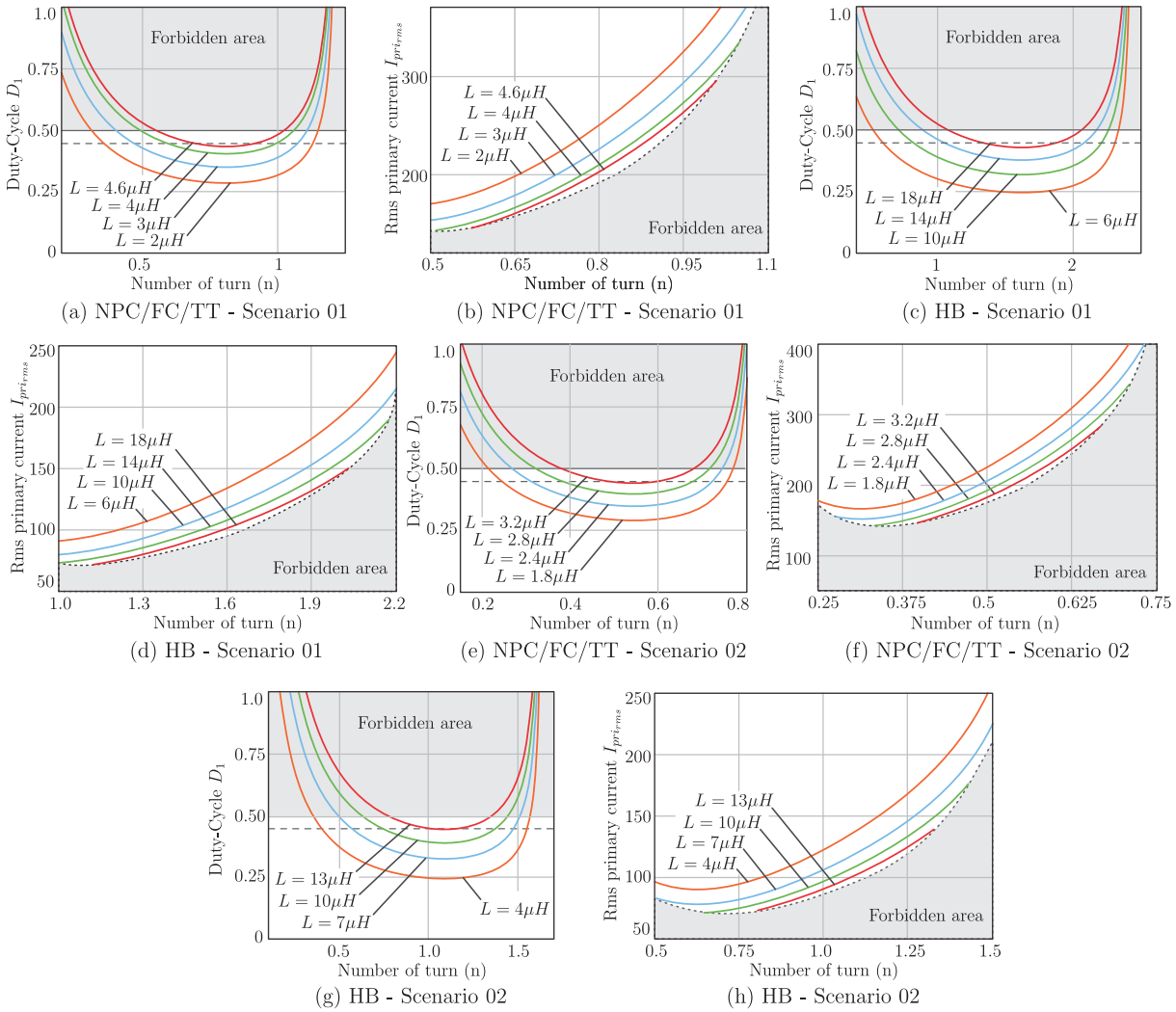
For a fair comparison of all topologies, the current rating and chip size of each semiconductor could be adapted for a given operating point such that the maximum or average IGBT and diode junction temperatures, $T_{J_{IGBT/Ddiode}}$, are equal or less than a predefined maximum value, e.g. $T_{J,max} = 125^{\circ}C$. This strategy not only guarantees optimal semiconductor material usage, but also provides a common basis for comparisons [8], [10]- [11].

The considered power semiconductors are latest generation Trench and Field-Stop 1200 V and 1700 V silicon IGBT4 and 3300 V silicon IGBT2 devices from Infineon that are rated for a maximum junction temperature of $150^{\circ}C$. The devices are presented in Table IV. For the diodes $D_{1,2}$ of the NPC topology, the intrinsic diodes of the IGBT are considered. The device selection is performed using an algorithm, as depicted in Fig. 5, and previously discussed in [12]- [11]. In this algorithm, an initial semiconductor with lower current rating and chip area, is chosen. The losses are computed and the temperature junction is obtained. If $T_j > 125^{\circ}$, a new device with superior current rating and chip area must be selected. The device with temperature junction immediately inferior to $125^{\circ}C$ is chosen to compose the topology. These calculations have been carried out separately for each semiconductor.

The power losses from the semiconductors are determined using the instantaneous current obtained directly by simulation. The instantaneous current, which passes through the semiconductor, is combined with the conduction loss characteristics by a 2nd order equation using fitted coefficients obtained by datasheets, as described in [13]. The switching losses are neglected in this paper, since it is considered

Table III: Optimum parameters of each cell of the QAB converter considering both scenarios.

	Scenario 1				Scenario 2			
	n	L	$i_{pri_{PEAK}}$	V_S	n	L	$i_{pri_{PEAK}}$	V_S
NPC/FC	0.8	4.6μH	205.3 A	850 V	0.54	3.2μH	140.8 A	565 V
T-Type	0.8	4.6μH	205.3 A	1700 V	0.54	3.2μH	140.8 A	1130 V
HB-TMS	1.6	18μH	103.5 A	1700 V	1.1	13μH	104.8 A	1130 V



(a) NPC/FC/TT - Scenario 01 (b) NPC/FC/TT - Scenario 01 (c) HB - Scenario 01

(d) HB - Scenario 01 (e) NPC/FC/TT - Scenario 02 (f) NPC/FC/TT - Scenario 02

(g) HB - Scenario 02 (h) HB - Scenario 02

Figure 4: Curves used to determine the parameters (n=Nprim/Nsec, L) of the converters: (a) Duty-cycle D_1 behavior, according to the parameters n and L variation (considering rated power and voltages) for the NPC/TT/FC converter in scenario 01, while (b) shows the variation of the rms current on the primary side of the transformer for the same parameters (n and L) variation (also for NPC/TT/FC converter in scenario 01). (b) and (c) show similar curves for the HB converter in scenario 01. (d) and (e) NPC/TT/FC converter in scenario 02, finally (f) and (g) NPC/TT/FC converter in scenario 02.

that the converter can work in soft-switching for entire range of load and voltage. Table V shows the selected devices to be used in the comparison.

The thermal performance of all topologies of the MV side is based on a heat sink ($R_{th,ha} = 0.15K/W$), while for the LV side it is based on a heat sink with forced air cooling ($R_{th,ha} = 0.25K/W$). A constant ambient temperature of $50°C$ is assumed in the analysis. Considering the described algorithm and losses computation, the selected IGBT's and Diode are presented in Table V.

Comparative Evaluation

After the selection of proper devices, the converter total losses and efficiency are computed for entire range of load. In this comparison, the transformer losses were not computed, as well as the capacitors losses. Thus, the results presented in this paper take into account only the considered semiconductors losses, which are the major losses of the system. When the converter operates with forward power flow (from MV to LV), the diodes of the LV-bridge will conduct the current, while in the reverse power flow (from LV to MV) the IGBT will conduct the biggest part of the current. Since the the intrinsic diodes of the devices have lower forward drop voltage, when compared to the IGBT channel, thus it is expected lower losses for direct power flow. In this case, different efficiency profiles for direct and reverse power flow are expected. Since, the converter will operate with direct power flow most of the

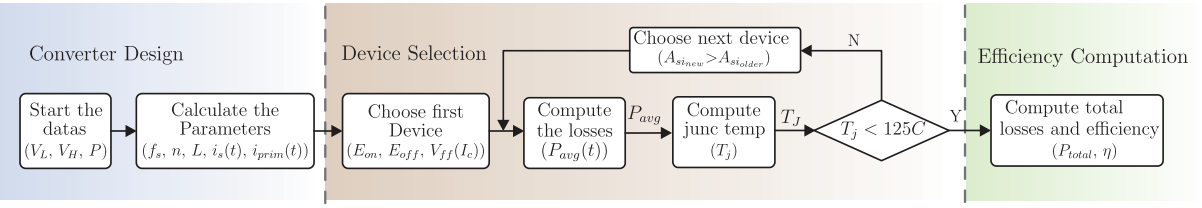


Figure 5: Algorithm flowchart of the IGBT selection considering optimal semiconductor material usage and power losses calculation

Table IV: Optimum parameters of each cell of the QAB converter considering both scenarios

Voltage	Considered devices	Current rating
1200V	FF{50, 75, 100, 200, 300}R12KT4	50, 75, 100, 200, 300
1700V	FF{150, 200}R17RT4	150, 200
3300V	FF200R33KF2C	200

time, this paper presents as result the efficiency profile for the entire range of load, considering direct power flow. Although the converter is also able to operate with reverse power flow, this operation will occurs very rarely and not for the total power. Thus, for reverse operation condition, only the efficiency for one operation point with partial load (around 40% of total load) will be shown. The results of the comparison between all topologies are depicted from Fig. 6 to Fig. 9

Scenario 1

Fig. 6 (a) shows the rms current through the semiconductors of each topology. As can be observed, the the FC and HB converter present balanced losses among their components, however the FC converter present highest current effort in its devices, while HB converter presents lowest effort in its device.

Fig. 6 (b) shows the total losses of the QAB converter, considering each topology in the MV side. As can be seen, the FC and NPC present lower losses and their losses are equal. Although the NPC has two more devices than the FC, their effort and (losses consequently) are lower, as depicted in Fig. 6 (b). The HB bridge presented slightly higher losses than the NPC and FC converter. Although the HB topology is using 3.3 kV, which has higher forward voltage and consequently higher losses, the current though their devices is lower, as can be seen in Fig. 6 (a). Therefore, this converter presented also good performance. The T-type presented the highest losses, because the current efforts in its semiconductors is relatively high (see Fig. 6 (a)) and the employed IGBT in this converter is a 3.3 kV with higher forward drop voltage.

Fig. 6 (c) presents the efficiency curve in function of the total power of the QAB converter, considering the multilevel topologies in MV side. As aforementioned, the FC and NPC presented higher efficiency. On the other hand, the losses across the flying capacitor in the FC topology were not computed, then the NPC topology shows to be more advantageous.

Fig. 7 (a) shows the losses of the total QAB converter, when the converter is processing partial reverse power flow (LV to MV). In this operation point, the converter is processing 35%. In this situation, the HB cell presented lower losses, because of combination of low current on the secondary side with the low voltage drop of the intrinsic diode (since the intrinsic diodes in the secondary bridge are conducting).

Finally, Fig. 7 (b) shows the junction temperature of each device of the evaluated power cells, considering full forward power flow. The NPC and FC converters have lower average junction temperature, considering the same cooling system, due to the lower losses.

Table V: Selected devices for each cell

		HB	TT		FC	NPC		
		S_{1-4}	$S_{1,2}$	$S_{3,4}$	S_{1-4}	$S_{1,4}$	$S_{2,3}$	$D_{1,2}$
Scenario 1	Voltage	3.3 kV	3.3 kV	1.7 kV	1.7 kV	1.7 kV	1.7 kV	1.7 kV
	Selected IGBT	FF200R33KF2C		FF150R17KE4				
Scenario 2	Voltage	1.7 kV	1.7 kV	1.2 kV	1.2 kV	1.2 kV	1.2 kV	1.2 kV
	Selected IGBT	FF150R17KE4		FF100R12RT4				

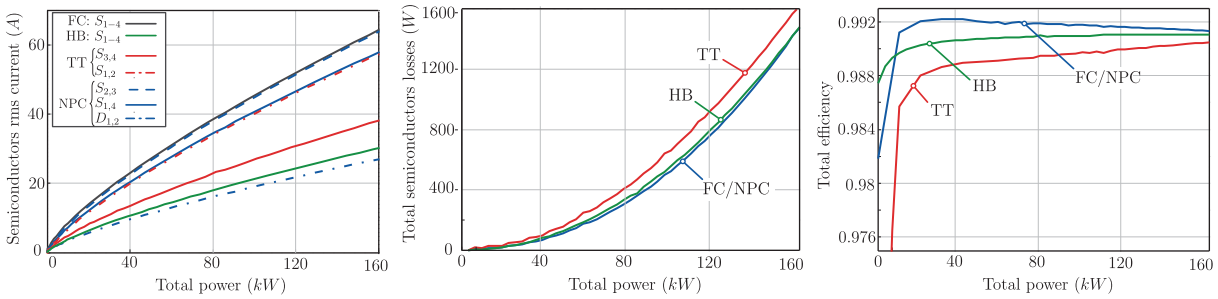


Figure 6: Comparative results for scenario 1: (a) Rms current through the semiconductors of each topology, (b) total QAB converter losses, considering different cells in the MV side, (c) the efficiency of the QAB converter in function of the converter power (considering only the semiconductors losses) for direct power flow.

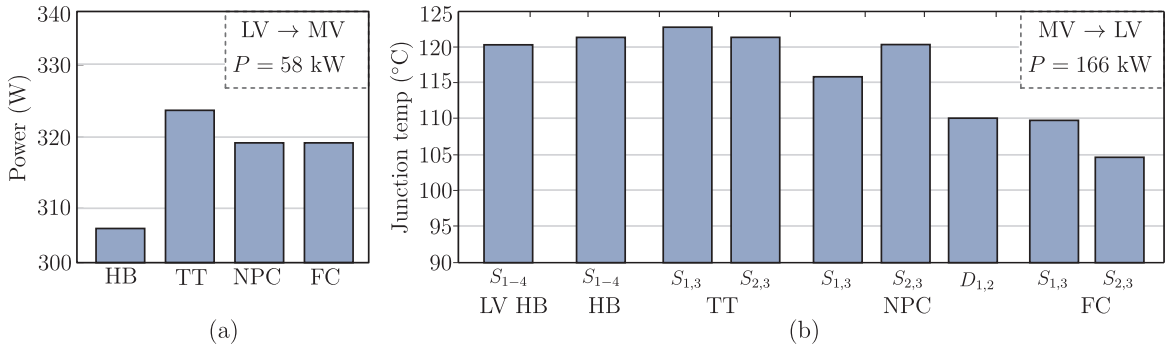


Figure 7: (a) Total losses of the QAB converter considering different cells on the MV side, when the converter is operating with reverse power flow (35% of the total power) in scenario 1. (b) Junction temperature in each semiconductor, considering different MV cells.

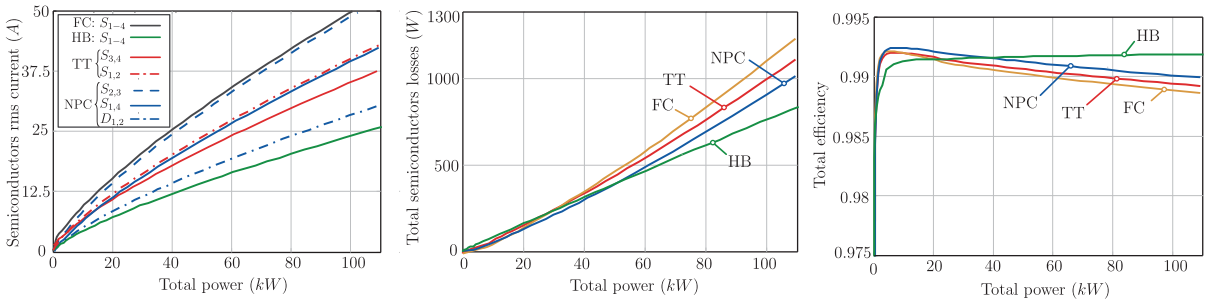


Figure 8: Comparative results for scenario 2: (a) Rms current through the semiconductors of each topology, (b) total QAB converter losses, considering different cells in the MV side, (c) the efficiency of the QAB converter in function of the converter power (considering only the semiconductors losses) for direct power flow.

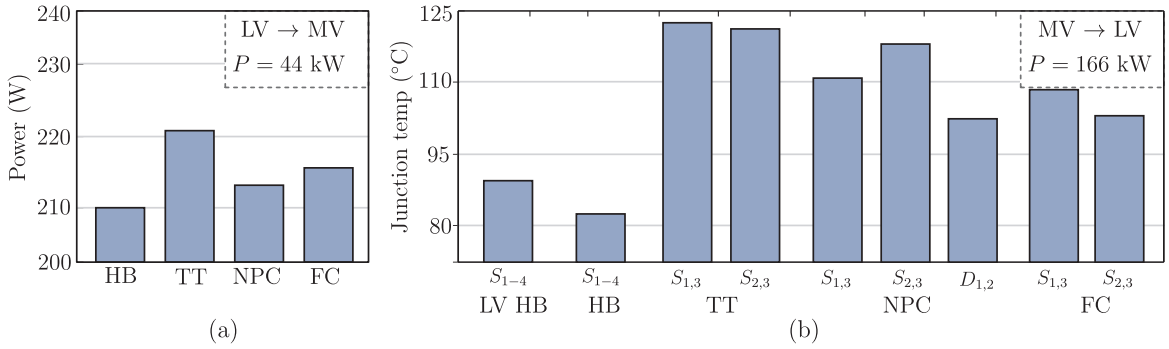


Figure 9: (a) Total losses of the QAB converter considering different cells on the MV side, when the converter is operating with reverse power flow (40% of the total power) in scenario 2. (b) Junction temperature in each semiconductor, considering different MV cells.

Scenario 02

Fig. 8 shows the QAB performance for different power cells, but now for the second scenario. As can be observed in the efficiency curves (shown in Fig. 8 (c)), the HB converter has presented the best performance in this scenario. The main reason for that is use of 1700 V IGBT for HB cell, which has much lower forward drop voltage. Besides that, the current effort on the HB is already lower because of its full-bridge configuration. Thus, these parameters combination has shown the the HB converter is more advantageous.

Comparing the results of Fig. 6 (c) and Fig. 8 (c), it can be concluded that the QAB converter presents slightly better performance in the second scenario. Thus, this study also shown that it is better to use 3 units per cell than only 2 units, in the viewpoint of efficiency. Nevertheless, others parameters (as reliability and cost) might also be considered during the selection of the proper numbers of units.

Fig. 9 (a) shows the losses of the total QAB converter, when the converter is processing partial reverse power flow (LV to MV). In this operation point, the converter is processing 40%. In this situation, the HB cell also presented better performance in terms of efficiency. Finally, Fig. 9 (b) shows the junction temperature of each device of the evaluated power cells, considering full forward power flow. As can be observed, the average junction temperature are lower for all cells.

Conclusion

In this paper an efficiency comparison between the H-bridge topology and multilevel topologies (Flying-capacitor - FC, neutral point clamped - NPC and T-type) as a solution for the MV cell of a QAB converter in Smart Transformer application was presented. The architecture of the ST was presented and two different scenario (considering different number of unit in the ST architecture) was created. The comparison was carried out for both scenarios. The multilevel topology seems to be very advantageous, because the reduced voltage over its semiconductors. However, the current through the semiconductors is higher. Thus, this trade-off is analyzed in this paper. The modulation strategy, design consideration and also an optimized semiconductors selection based on the maximum junction temperature of operation were described in this paper.

For the first scenario, the results have shown that the NPC and FC converters presented higher efficiency than the others studied topologies. The HB presented slightly inferior performance, basically due the utilization high breakdown voltage and, consequently high forward drop voltage IGBT. Nevertheless, the performance of the HB is still high, presenting efficiency over 99%. The T-type converter showed the worst performance when compared to the others topologies and the main reason for that is the requirement of use high voltage IGBT, which presents high forward drop voltage, associate to high current through the semiconductors. On the other hand, for the second scenario, the HB cell has presented better performance than the multilevel cells. The main reason for that is the use of 1700 V IGBT for HB cell associate to its lower current effort, due to its full-bridge configuration.

As an overall overview, the QAB converter has shown high efficiency in both scenarios, when the HB, NPC or FC cell are used. However, the start-up of the Flying-Capacitor is still a issue that must be considered. In addition, higher efficiency is possible to be achieved in the second scenario. Thus, in the efficiency viewpoint, the second scenario presents better performance than the first one. For both scenario, the results has shown that the QAB is suitable for ST application.

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