Digital Object Identifier (DOI): 10.1109/APEC.2017.7931161

Applied Power Electronics Conference and Exposition (APEC), 2017 IEEE

Modulation strategy for highly reliable cascade H-Bridge inverter based on discontinuous PWM

Youngjong Ko
Markus Andresen
Giampaolo Buticchi
June-Seok Lee
Marco Liserre

Suggested Citation

Y. Ko, M. Andresen, G. Buticchi, J. S. Lee and M. Liserre, "Modulation strategy for highly reliable cascade H-Bridge inverter based on discontinuous PWM," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 3241-3246.

Modulation Strategy for Highly Reliable Cascade H-Bridge Inverter Based on Discontinuous PWM

Youngjong Ko[1], Markus Andresen[1], Giampaolo Buticchi[1], June-Seok Lee[2], and Marco Liserre[1]
[1]Chair of Power Electronics, University of Kiel, Kiel, Germany
[2]Korea Railroad Research Institute, Uiwang, South Korea
yoko@tf.uni-kiel.de, ma@tf.uni-kiel.de, gibu@tf.uni-kiel.de, ljs@krri.re.kr, ml@tf.uni-kiel.de

***Abstract*—The Cascaded H-Bridge (CHB) topology is widely employed in high power and high voltage applications due to advantages of the low dv/dt, the low EMI noise, and the low filter inductance. An issue of this modular system is the possible unequal thermal stress of the power semiconductors in the cells, which is affecting the reliability and leads to maintenance costs and down-times. In this paper, the seven-level CHB topology is considered and the modulation strategy based on the Discontinuous PWM (DPWM) is proposed to improve the reliability by reducing the switching losses of a cell experiencing premature wear-out.**

***Index Terms*—Multilevel converter, Cascaded H-bridge, Reliability, Modulation strategy, Discontinuous PWM**

I. Introduction

The two-level Voltage Source Inverter (VSI) has been employed in various applications so far and it is a well-established topology. However, in the high power and high voltage applications [1]–[5], the two-level VSI suffers from the relatively large switching loss and large EMI. As an alternative, the multilevel structure has been extensively studied due to the reduced dv/dt stress and thus smaller filter size in comparison to the two-level structure [6]–[8]. The most popular multilevel converter topologies can be generally categorized into three architectures: the Neutral Point Clamped (NPC) structure, the Flying Capacitor clamped (FC) structure, and the Cascade H-Bridge (CHB) structure [9], [10]. However, in the following work, the CHB converter is considered due to its advantage in comparison with others. One of the advantage is that less components are required for the same output voltage levels, by eliminating the clamping diodes and the flying capacitors.

The reliability has always constituted an important part of the power electronics design. The literature based on the physics of failure approach has claimed that the reliability is closely associated with the thermal stress, consequent with the power profile [11], [12]. According to a commonly applied lifetime model, the failures occur when the accumulated thermal stress exceeds the device's strength [12]. Hence, one of the possibility to prevent failures is to increase the component's strength against the thermal stress, whereas another possibility is to reduce the applied stress. In addition to the latter concept, the thermal stress can be redistributed in such a way, that the components with lower expected lifetimes are unloaded, whereas cells with higher remaining lifetimes are loaded higher [13], [14].

In this paper, the modulation strategy to improve the reliability of the CHB converter is proposed, and it is based on the Discontinuous PWM (DPWM). Assuming that one of the cells is experiencing a premature wear-out, its thermal stress can be reduced by the proposed method without affecting the normal operation. The reliability of the power converter is described to motivate the proposed method in section II. In section III, the principle of the method is introduced and analyzed in terms of the Total Harmonic Distortion (THD). The effect on the loss distribution are simulated as well. In section IV, the feasibility of the proposed method and the reduction of thermal stress are experimentally verified and finally, section V concludes this paper.

II. Reliability of power semiconductor

It has been proved that the reliability of power semiconductors is closely associated to the thermal behavior, and the reliability can be evaluated based on a physics of failure approach [15]. Therefore, the number of cycles to failure N_f can be expressed with regard to the junction temperature fluctuation T_j and the average junction temperature $T_{j,mean}$ as

$$N_f = a_1 \cdot (\Delta T_j)^{-a_2} \cdot e^{\frac{a_3}{T_{j,mean}}} \tag{1}$$

where a_1 and a_2 are parameters determined by experimental data and related with physical characteristics of a power module, a_3 is a constant which can be calculated with the activation energy and the Boltzmann constant. This equation lifetime model does only a single magnitude of a thermal cycles, which is not sufficient to estimate the lifetime based on a real mission profile. In this case, the Miner rule is commonly applied with linear damage accumulation as shown in (2).

$$C = \sum_{i=0}^{\inf} \frac{n_i}{N_i} \leq 1 \tag{2}$$

In this equation, N_i is the number of cycles to failure in the stress range i and n_i the number of detected cycles in the i^{th}stress range. As soon as the accumulated damage $C = 1$, the device is expected to fail.

In stationary conditions, the junction temperature of a power semiconductor T_j can be expressed with

$$T_j = T_C + R_{th,JC} \cdot P_{loss,tot} \tag{3}$$

where T_C represents the case temperature, $R_{th,JC}$ is the thermal resistance between junction and case and $P_{loss,tot}$ is the total

978-1-5090-5366-7/17/$31.00 ©2017 IEEE

loss of the power semiconductors. The overall losses $P_{loss,tot}$ are divided into conduction loss $P_{loss,cond}$ and switching loss $P_{loss,sw}$.

$$P_{loss,tot} = P_{loss,cond} + P_{loss,sw} \tag{4}$$

According to (3), the junction temperature is solely dependent on the power losses, as the thermal resistance is constant and the case temperature settles depending on the junction temperature and the thermal properties of the cooling path. Hence, it is concluded that the losses determine the junction temperature and consequently the lifetime of the system.

A possible method to reduce selectively the losses in a part of the fundamental period is the DPWM since the switching loss can be reduced by clamping the output voltage to either the positive or negative dc-link for a certain time [16], [17]. In addition, considering the modular structure, one of the cells could be required to be repaired due to the premature deterioration. Therefore, it is of interest to reduce the thermal stress of the weak cell in order to prolong the lifetime of the entire converter. The DPWM can allow to reduce such thermal stress by reducing the losses.

III. Proposed Modulation Strategy

A. Principle of the proposed modulation strategy

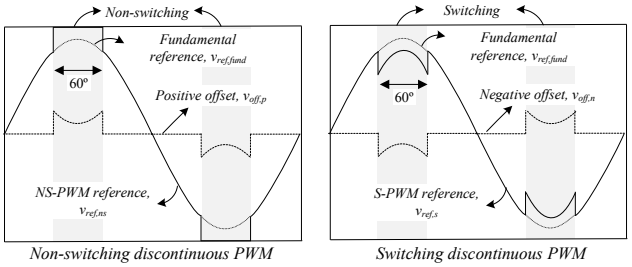
The conventional DPWM methods are generally achieved by adding the offset voltage to the Continuous PWM (CPWM) [18], [19]. The devices are switched in the whole modulating signal of the CPWM, whereas the devices are not switched during the clamping period by the DPWM. Hence, the switching losses can be reduced. Furthermore, since the highest switching losses are generated during the clamping period when the power factor is one, the generated loss can be significantly reduced. Although the 60° DPWM is considered in the following sections, other methods such as 30°, 60° (±30°), and 120° DPWM can be utilized as well [20], [21].

As shown in Fig. 1, the proposed DPWM method has two modulating signals. The two signals are named as NS-DPWM (Fig. 1(a)) and S-DPWM (Fig. 1(b)), where the acronym NS means non-switching and the acronym S represents switching. The NS-DPWM is synthesized by the sum of the fundamental voltage reference $v_{ref,fund}$ and the positive offset voltage $v_{off,p}$, whereas the S-DPWM is generated by the sum of the fundamental voltage reference and the negative offset voltage $v_{off,n}$.

The basic concept of the method and power flows among cells are shown in Fig. 2. For instance, it is assumed that the cell 1 (with diagonal line) is experiencing the premature deterioration. The weak cell is modulated with the NS-DPWM in order to reduce the generated losses while others adopt the S-DPWM so that the offset voltage can be completely compensated as shown in (5). Therefore, the output power has only a fundamental component.

$$v_{off,p1} = v_{off,n2} + v_{off,n3} \tag{5}$$

Here, $v_{off,p1}$ is the positive offset voltage from the cell 1 and $v_{off,n2}$, and $v_{off,n3}$ are the negative offset voltage of cell 2 and cell 3, respectively. Moreover, it should be mentioned that the cells modulated by the S-DPWM are unaffected in terms of the thermal stress, namely, the loss distribution remains identical to the CPWM.



(a) (b)

Fig. 1: Principle of the proposed DPWM method which allows two variants; (a) non-switching and (b) switching.

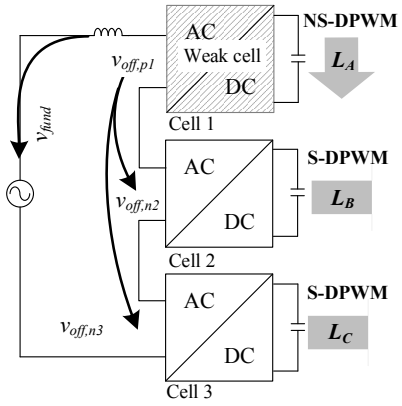


Fig. 2: Power flow when cell 1 is experiencing the premature deterioration.

The positive offset voltage $v_{off,p}$ can be obtained as (6) and this equation is graphically shown in Fig. 3.

$$v_{off,p} = \begin{cases} v_{ref,fund} - mi_{max} & \text{if } v_{ref,fund} > v_{set} \\ v_{ref,fund} - mi_{min} & \text{if } v_{ref,fund} < -v_{set} \\ 0 & \text{if } -v_{set} < v_{ref,fund} < v_{set} \end{cases} \tag{6}$$

In here, mi_{max} and mi_{min} are the available maximum and the minimum modulation index, respectively, and the clamping angle is determined by v_{set} found as

$$v_{set} = mi \cdot cos\left(\frac{60°}{2}\right) \tag{7}$$

where *mi* is the modulation index and the clamping angle is set to 60°. The offset voltage is utilized to obtain the modulation signals in Fig. 1. For the NS-DPWM, the final modulation signal $v_{ref,ns}$ is determined by the sum of the fundamental reference and the positive offset voltage. The S-DPWM signal is obtained by summing up the fundamental reference and the negative offset voltage as shown in (8). It should be pointed out that the negative offset voltage is divided by two, which is the number of the healthy cells in this case.

$$\begin{cases} v_{ref,ns} = v_{ref,fund} + v_{off,p} \\ v_{ref,s} = v_{ref,fund} + \frac{v_{off,n}}{2} = v_{ref,fund} - \frac{v_{off,p}}{2} \end{cases} \tag{8}$$

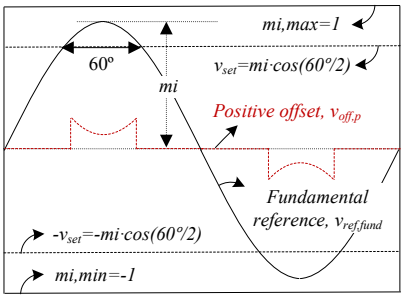
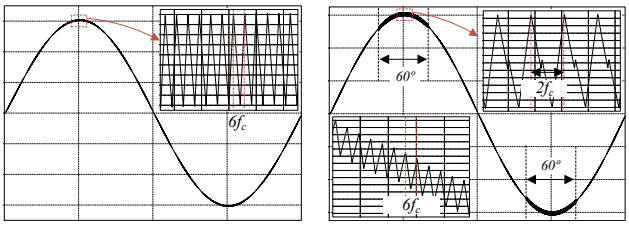


Fig. 3: Fundamental voltage reference and offset voltage.



(a) (b)

Fig. 4: Output current waveform by (a) Continuous PWM and (b) the proposed method.

B. Total harmonic distortion analysis

The phase-shifted carriers are used to implement the proposed method. The major advantage of the phase-shifted carrier modulation is the outstanding performance in terms of the Total Harmonic Distortion (THD) due to a higher equivalent switching frequency. Considering the seven-level CHB converter, the equivalent switching frequency is six times higher. The current waveform of the CPWM with the phase-shifted modulation is shown in Fig. 4(a), when the carrier frequency is f_c. As mentioned above, the switching ripple frequency is $6f_c$. In order to verify the influence of the proposed method, the current waveform is simulated in Fig. 4(b) as well. In contrast with the previous one, the current waveform can be divided into two regions: inside and outside of the clamping region. Outside the clamping region the ripple is at $6f_c$ like in Fig. 4(a), inside the ripple, it is at $2f_c$.

The THD is one of the most important factors to evaluate the power converter's performance. The proposed method is compared to the CPWM in terms of THD as a function of output power as shown in Fig. 5. The normalized values are used and the 60° clamping region is considered in the following analysis. The THD of the current is degraded by 1.4 times at nominal power and by 2.8 times at 10 % of the nominal power. However, this result is expected and the applicability of the method is for power bigger than 25 %.

C. Loss analysis

The losses directly affect the thermal distribution, which is demonstrated by using Matlab/Plecs in Fig. 6(a) and (b) as a function of the carrier frequency and the output power,

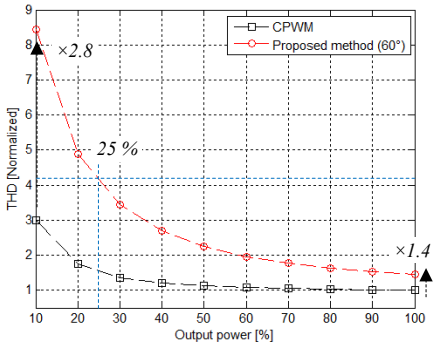


Fig. 5: Performance of THD in accordance with modulation methods (clamping angle=60° and carrier frequency=20 kHz).

respectively. In both cases, the total losses are reduced by the proposed method. Especially, for high output power and high carrier frequency, the method is more effective. The total loss is decreased by 10 % with 30 kHz carrier frequency and 100 % output power, and the total losses are reduced by 7.5 % with 20 kHz and nominal output power.

As it can be seen, the proposed method allows to reduce the losses, consequent the thermal stress of one cell at the expenses of the higher THD of the output current.

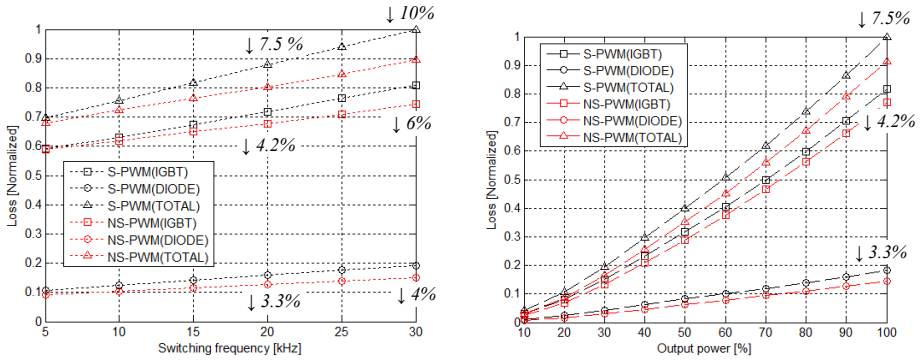
IV. Impact of the Loss Reduction on the Lifetime

As it has been shown in the analytical results of Fig. 6 (b), the losses of the power semiconductors can be decreased by 7.5 %, whereby the losses for the IGBTs were decreased by 5.1 %. If the loss reduction of one power semiconductor is being combined with the lifetime model based on the linear damage accumulation (as expressed in (1)), the thermal cycles will remain constant in the numbers, but will be reduced in their magnitude. This is resulting in the new number of thermal cycles to the failure $N_f^{'}$ (9), because all the thermal cycles, as well as their average temperature, are reduced if the overall maximum losses are reduced:

$$N_f^{'} = a_1 \cdot (\gamma \cdot \Delta T_j)^{-a_2} \cdot e^{\frac{a_3}{T_{j,mean}^{'}}} \tag{9}$$

For a loss reduction, $T_{j,mean}^{'}$ is smaller than the former average junction temperature, which also has a positive effect on the lifetime. By using this model for the linear damage accumulation of (2), the new damage for the system is reduced as well.

For an estimation about how much stress can be reduced with the proposed algorithm, the damage of the two different cases are compared. One case uses the CPWM and the other the proposed DPWM. For this comparison, linear damage accumulation is applied with the coefficients of the LESIT results [22]. To demonstrate the principle, a mission profile with varying output power is generated. This is shown in Fig. 7. For this mission profile, the influence of the CPWM is investigated and compared with the proposed method. As it can be seen in the figure, the loss distribution of each cell is same with the CPWM, whereas the loss of the cell



(a) (b)

Fig. 6: Loss distribution in accordance with (a) carrier frequency (with nominal power) and (b) output power (with 20 kHz carrier frequency).

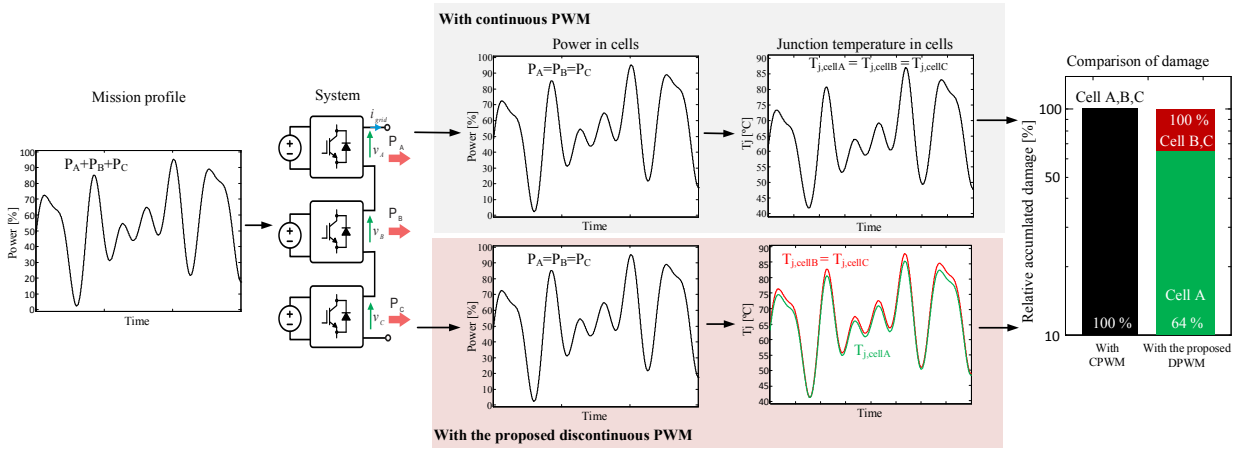


Fig. 7: Demonstration of the impact of the proposed method on the lifetime expectation of the power semiconductors.

A is reduced by the proposed method. As a result, the power distribution among the cells is kept constant for all cells in both cases. However, the loss reduction achieved with the proposed method affects a reduction of the junction temperature of the power semiconductors in the cell A. Even, if this is only achieved by some percentages, the magnitude of all thermal cycles is being reduced. To quantify this by means of a potential increase of the lifetime for these power semiconductors, the Rainflow counting algorithm is applied to extract the thermal cycles. These cycles are used in the lifetime model of (2). As a result, the damage for the cell A with the application of the proposed method, the damage is decreased to 64 % of its prior value with CPWM. Consequently, it has been found that the damage is reduced and the lifetime has been increased by the inverse of this damage, resulting in a lifetime increase of 56 %. As a consequence, after activating the proposed algorithm, the thermal stress of a weak cell can be decreased, leading to this lifetime extension. Instead, the losses in the other cells are not affected and thus the lifetime of their components remains unaffected.

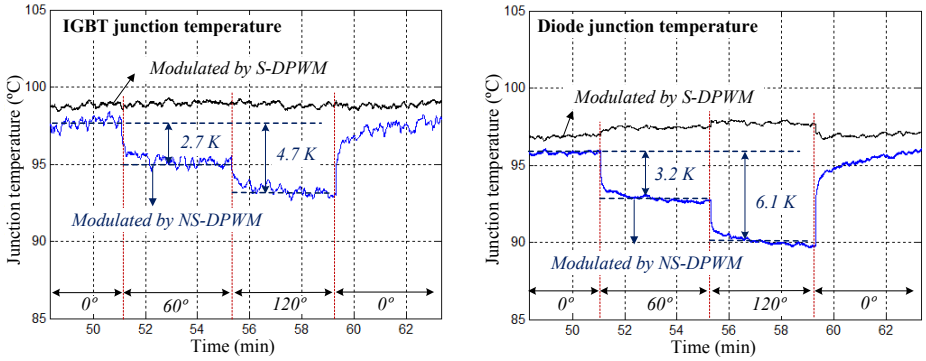
V. Experimental Results

The experimental setup is developed as shown in Fig. 8. It consists of the seven-level CHB converter with three open power modules, a temperature monitoring system, an electrical load, and dc sources. The electrical specification of the power module is 1200 V / 25 A and the total dc-link voltage is 450 V (150 V dc-link voltage of each cell).

The feasibility of the proposed method is verified in experiment. The duty cycles for each cell, the output current, and its FFT analysis are shown in Fig. 9. The output current of both methods is sinusoidal, but as pointed out in previous section, the dominant switching ripple frequency is $6f_c$ with the CPWM while $2f_c$ for the proposed method.

The dynamic response is verified in Fig. 10, when the modulation method is switched from the CPWM to the proposed one. The transfer can be seamlessly conducted without any special technique.

In order to verify the effect of the proposed method, the junction temperature of the power module is measured by fiber optic sensors "OTG-A" and signal conditioner "ProSens", when the carrier frequency is 23 kHz and the output current



(a) (b)

Fig. 11: Junction temperature of power module with 23 kHz carrier frequency and at Vout=230 V / Iout=11.2 Arms. (a) IGBT and (b) freewheeling diode.

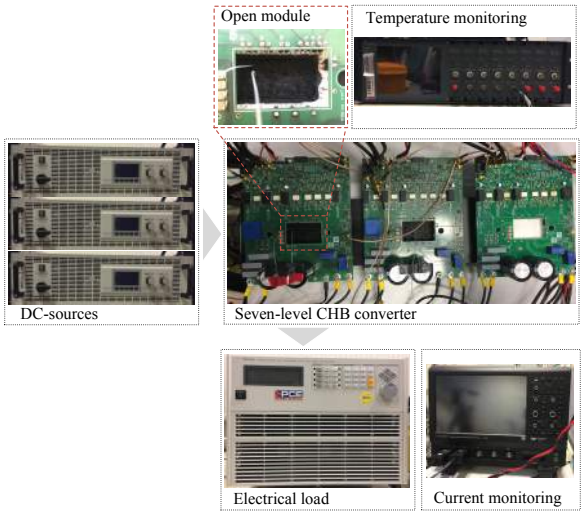


Fig. 8: Experimental setup with open power modules and monitoring system.

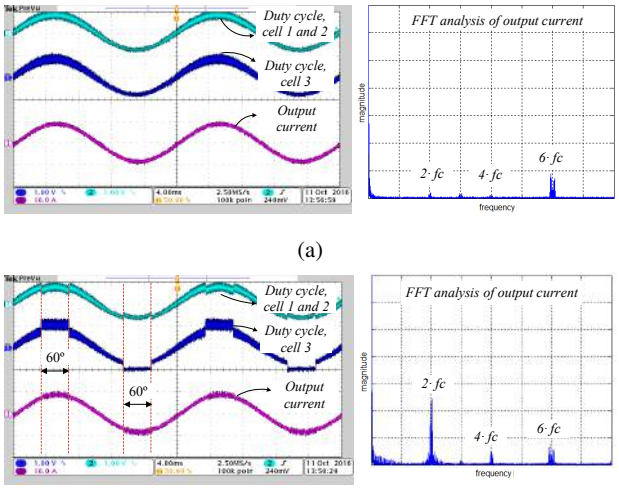


Fig. 9: Duty cycles, output current, and FFT analysis of (a) CPWM and (b) proposed method.

is 11.2 Arms. In Fig. 11(a) and (b), the junction temperature of IGBT and freewheeling diode is shown, respectively. The junction temperature of the module operated with the NS-DPWM is reduced with an increased clamping angle, while the temperature of the module operated with the S-DPWM maintains similar level. As shown in Fig. 11 (a), the IGBT junction temperature is reduced approximately 2.7 K with the 60° clamping angle and 4.7 K with the 120° clamping angle. In case of diode as shown in Fig. 11 (b), the junction temperature decreases approximately 3.2 K and 6.1 K by the 60° and 120° clamping angle, respectively.

VI. Conclusion

In this work, the modulation strategy based on the discontinuous PWM was proposed in order to improve the reliability of the CHB converter. With the proposed method, the thermal stress of a designated cell experiencing premature wear-out can be reduced, possibly extending the lifetime of the system.

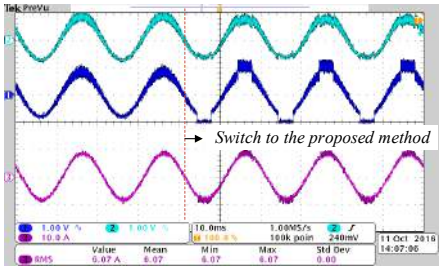


Fig. 10: Dynamic response (switch from CPWM to the proposed method).

It was shown, that the lifetime can be increased by more than 50 %, while the total losses of the cell are reduced by 7.5 %. As an expense for the obtained increase of the lifetime, the THD of the current increases by the factor of 1.4 at nominal output power. The proposed method was experimentally validated by

performing spectral analysis of the output current and junction temperature measurements of the power semiconductors in the CHB converter.

ACKNOWLEDGMENT

The research leading to these results has received funding from the European Union/Interreg V-A - Germany-Denmark, under the PE:Region Project and the European Research Council under the European Union's Seventh Framework Program (FP/2007-2013) / ERC Grant Agreement n. 616344 HEART, the Highly Efficient And reliable smart Transformer.

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[2] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[3] B. K. Bose, "Power electronics and motor drives recent progress and perspective," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 581–588, Feb 2009.

[4] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 708–719, March 2012.

[5] Z. Chen, J. M. Guerrero, and F. Blaabjerg, "A review of the state of the art of power electronics for wind turbines," *IEEE Transactions on Power Electronics*, vol. 24, no. 8, pp. 1859–1875, Aug 2009.

[6] D. Mohan, Z. Xinan, and G. Foo, "Direct torque control of ipmsm driven by a three level npc inverter with torque and capacitor voltage ripple reduction," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 557–564.

[7] Y. Dodo, Y. Sato, T. Ito, and S. Mochidate, "A study for improvement in power density of flying capacitor multilevel inverters for grid-connected applications," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 469–473.

[8] A. Moeini, Z. Hui, and S. Wang, "High efficiency, hybrid selective harmonic elimination phase-shift pwm technique for cascaded h-bridge inverters to improve dynamic response and operate in complete normal modulation indices," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 2019–2026.

[9] C. Wang and Y. Li, "A survey on topologies of multilevel converters and study of two novel topologies," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, May 2009, pp. 860–865.

[10] P. Gaur and P. Singh, "Various control strategies for medium voltage high power multilevel converters: A review," in *Engineering and Computational Sciences (RAECS), 2014 Recent Advances in*, March 2014, pp. 1–6.

[11] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 590–602, Feb 2015.

[12] N. C. Sintamarean, F. Blaabjerg, H. Wang, F. Iannuzzo, and P. de Place Rimmen, "Reliability oriented design tool for the new generation of grid connected pv-inverters," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2635–2644, May 2015.

[13] M. Liserre, M. Andresen, L. Costa, and G. Buticchi, "Power routing in modular smart transformers: Active thermal control through uneven loading of cells," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43–53, Fall 2016.

[14] Y. Ko, M. Andresen, G. Buticchi, M. Liserre, and L. Concari, "Multi-frequency power routing for cascaded h-bridge inverters in smart transformer application," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016.

[15] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, March 2014.

[16] N. V. Nguyen, B. X. Nguyen, and H. H. Lee, "An optimized discontinuous pwm method to minimize switching loss for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 3958–3966, Sept 2011.

[17] Y. Wu, M. A. Shafi, A. M. Knight, and R. A. McMahon, "Comparison of the effects of continuous and discontinuous pwm schemes on power losses of voltage-sourced inverters for induction motor drives," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 182–191, Jan 2011.

[18] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous pwm algorithm," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059–1071, Sep 1998.

[19] J. S. Lee, S. Yoo, and K. B. Lee, "Novel discontinuous pwm method of a three-level inverter for neutral-point voltage ripple reduction," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3344–3354, June 2016.

[20] L. Asiminoaei, P. Rodriguez, and F. Blaabjerg, "A new generalized discontinuous-pwm strategy for active power filters," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2007, pp. 315–321.

[21] J. He, L. Wei, and N. A. O. Demerdash, "Power cycling lifetime improvement of three-level npc inverters with an improved dpwm method," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 2826–2832.

[22] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of igbt modules in traction application," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, vol. 1. IEEE, 1997, pp. 425–430.