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Highly efficient and reliable DC-DC converter for smart transformer

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Highly Efficient and Reliable DC-DC Converter for Smart Transformer

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***Abstract*—The series-resonant converter (SRC) has been used in several application and it recently became popular for Smart Transformers (STs). In this application, the efficiency and reliability are of paramount importance. Although many papers have addressed the design challenges to improve the converter efficiency, discussions about the reliability are still missing in literature. In this context, this paper presents a design procedure focusing on the efficiency and reliability improvement of the SRC for ST application. To improve the efficiency, losses modeling in all components is carefully carried out. Additionally, Silicon-Carbide (SiC) MOSFETs are used to reduce the conduction and switching losses. The reliability is addressed on the converter design by taking the lifetime of the resonant capacitor and the stress on the main components. Experimental results obtained for the optimized 10 kW series resonant converter has shown an efficiency of 98.61%.**

I. Introduction

The series-resonant dc-dc converter (SRC) has been very used in a large range of voltage and power application, such as wireless power transfer for electrical vehicle [1] - [4] (24-600 V / 5-100 kW), battery charger [5] - [6] (24-600 V / 5 100 kW), renewable energy system [7]- [10] (0.1-500 kV / 0.1-100 MW) and high voltage power supply for specific application, such as traveling-wave tube (TWT) for satellite application [11] (1-10 kV / 1-100 kW). Because of its characteristic of output voltage regulation in open loop, associated to its feature of soft-switching, the converter became very popular in Smart Transformer (ST) [12] application. Hence, this converter has been used to implement the dc-dc stage of ST's architectures based on modular [13]–[15] and also non-modular [16] concept.

In this kind of application, high efficiency is extremely desired and many optimization methods focusing on the efficiency improvement have been discussed in the literature [15]. Besides that, the continuity of operation is of paramount importance and then a highly reliable system with a long lifetime is required [17]. Although the reliability is considered even more important than the efficiency in ST application, issues related to the SRC reliability has not been intensively investigated. Currently, very few papers have addressed reliability improvement of dc-dc converters by using fault tolerance approach [18], [19] and the lifetime extension approach for dc-dc converters has not yet been discussed on the literature.

In this context, this paper presents an optimum design of the SRC used as a building block of the dc-dc stage of the ST. The design is focused on the efficiency and reliability optimization. The modular ST architecture using the SRC as a module is presented in Fig. 1, while the topology of the SRC (including the parasitic elements) is shown Fig. 2. The input of the converter is connected on the medium voltage (MV) side of the system and its output is connected to the low voltage (LV) side. To achieve a very high efficiency, the loss modeling in all components is carried out and the characteristic equations are obtained. To further improve the efficiency, SiC MOSFETs with very low on-state resistance are used, reducing drastically the conduction losses. Moreover, the high frequency transformer is carefully designed in order to obtain lowest losses with the smallest size. The reliability is addressed by using the converter lifetime assessment and extension approach. One of the most faulty components of the SRC is the resonant capacitor (C_r). Thus, the influence of the converter parameters selection on the capacitor lifetime is evaluated, with the aim to extend the lifetime of this components and, consequently the converter lifetime.

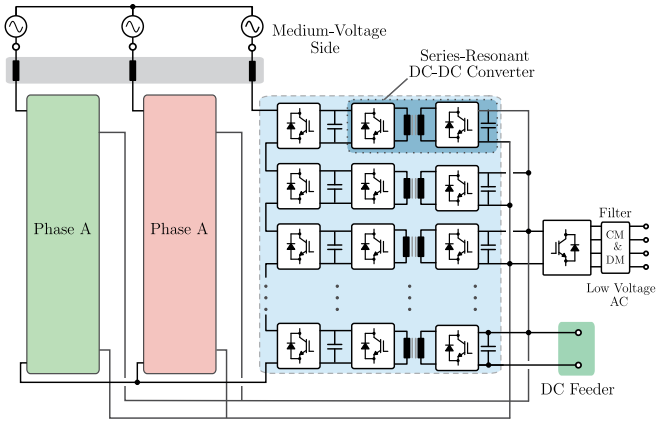

Figure 1. Modular Smart Transformer architecture using the Series-Resonant converter as a building block of the dc-dc stage of the system.

The paper is divided as follows: section II describes the operation principle of the SRC, where the main equations for the design are provided. The losses model in all components of the converter are computed and discussed in section III. In section IV, the capacitors lifetime model is derived and a discussion about the influence of the tank circuit components (resonant inductor L_r and capacitor C_r) selection on the capacitors lifetime is presented. Finally, experimental results

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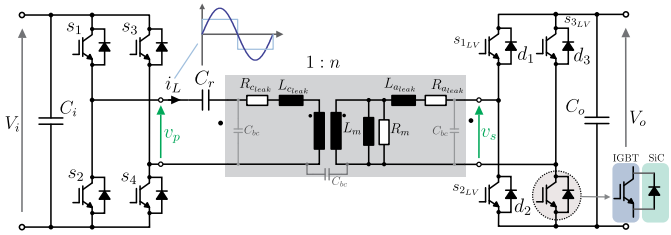


Figure 2. Topology of the Series-Resonant Converter.

Table I
SPECIFICATION OF THE SRC

Input voltage	Output Voltage	Nominal Power	Isolation frequency
600 V	700 V	10 kW	20 kHz

for a 10 kW prototype of the SRC is presented, where an efficiency of 98.61% is demonstrated

II. Operation Principle of the SRC

The topology of the SRC based on full-bridge configuration (FB-SRC) is shown in Fig. 2, while its specification is shown in Table VI. The most efficient operating point of the SRC is when it operates in the discontinuous conduction mode (DCM) with the switching frequency (f_s) equal or slightly below the resonance frequency (f_o). In this operation mode, the primary-side switches achieve zero-voltage-switching (ZVS) and low-current switching, the output diodes achieve zero-current switching (ZCS). As additional advantages, the converter has good transformer utilization and also low EMI emission, due to the smooth current shape (low di/dt). According to [20], the main problem with the SRC is the lack of input voltage regulation. On the other hand, it is an advantage for ST application, once the system has enough degrees of freedom to control the input voltage by using the front-end rectifier (first stage). Consequently, the open-loop operation of the SRC makes the system simpler and inexpensive, since the number of sensors can be reduced.

The main waveforms in this operation mode are shown in Fig 3. To support the analysis, the variables resonant frequency (f_o), resonant angular frequency (ω_0) and characteristic impedance of the resonant network (Z) are defined by (1), in terms of the resonant inductor (L_r) and capacitor (C_r) of the tank circuit.

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}, \quad \omega_0 = 2\pi f_0, \quad Z = \sqrt{\frac{L_r}{C_r}} \tag{1}$$

To operate in dcm, the converter parameters must satisfy the conditions presented in (2) [21], where γ is the angular length of one half switching period and I_o is the load current. From these conditions it is possible to design L_r and C_r, considering the operation range of the converter.

$$\gamma = \frac{\omega_0}{2f_s} > \pi, \quad f_s < f_0, \quad I_o < 8 f_s C_r V_o \tag{2}$$

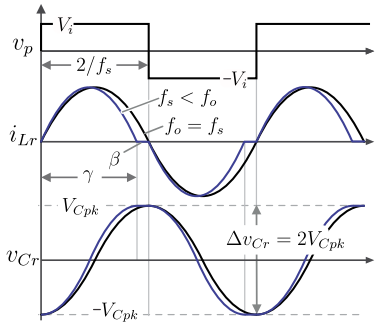


Figure 3. Main waveforms of the SRC.

As the converter with unit gain, the output voltage is defined as (3)

$$V_o = nV_i \tag{3}$$

Generally, the converter is designed to operate at the resonant frequency ($f_s = f_o$) [22], reaching then the maximum efficiency point. To do so, the pair L_r and C_r have to satisfy the condition imposed in (1). Thus, there is one degree of freedom to select one of these parameters, while the other is chosen consequently. Nevertheless, the selection of the pair L_r and C_r has an impact on the current and voltage effort on the resonant capacitor, influencing its lifetime. Therefore, the selection of L_r and C_r plays an important role not only on the converter efficiency, but also on the components lifetime. This aspect will be discussed in the next sections.

III. Losses Analysis of the SRC

As mentioned before, the losses in the main components of the SRC must be carefully computed in function of the main converter parameters, with the aim of properly selecting these parameter, minimizing the losses.

A. Semiconductors

In order to take advantage of the high performance of the new SiC devices, SiC MOSFETs of 1.2 kV voltage rating are considered for the primary side. For the secondary side, active switches need to be used, because of the bidirectional power flow requirement of the converter. However, most of the time, the converter processes direct power flow, while reverse power flow will occurs very rarely. For this reason, on the secondary side of the converter, standard IGBTs in parallel with high performance SiC diodes are used. The list of the considered semiconductors is presented in Table II

The conduction losses of the primary side MOSFETs can be calculated by (4), where the on-resistance ($R_{dc(on)}$) is function of the drain-source current (i_{dc}), junction temperature (T_J) and gate voltage (V_{gs}). Assuming a constant junction temperature of 100°C and a constant gate voltage, the equation is simplified to (5). As can be observed, the conduction losses depends on the inductor peak current (i_{Lpk}) and also γ. Both parameters are highly depends on the tank circuit components (L_r and C_r).

The conduction losses of the secondary side diodes can be calculated in function of the current and devices parameters

Table II
SPECIFICATION OF THE SEMICONDUCTORS CONSIDERED IN THE DESIGN

MOSFET - MV side				
Type	Reference	V	I	$R_{ds(on)}$ (@150 C)
SiC	C2M0040120D	1.2 kV	40 A	$84m\Omega$
SiC	C2M0025120D	1.2 kV	90 A	$43m\Omega$
IGBT - LV side				
Type	Reference	V	I	$V_{CE(on)}$ (@150 C)
Si	IHW40N120R3	1.2 kV	80 A	$2.4V$
Diode - LV side				
Type	Reference	V	I	$R_{ds(on)}$ (@25 C)
SiC	C4D20120D	1.2 kV	16,5 A	$3V$
SiC	C4D40120D	1.2 kV	40 A	$3V$

by (6). Similarly as for the MOSFET, the diodes conduction losses are highly dependent on L_r and C_r. The influence on L_r and C_r is discussed in section V.

As the converter operates under soft-switching condition with ZVS and ZCS on the primary side and ZCS on the secondary, the switching losses can be neglected.

$$P_{prim(cond)} = \frac{1}{T}\int_0^T R_{ds(on)}\left(i_{ds}(t), T_J, V_{gs}\right)\cdot {i_{ds}}^2(t)\,dt \tag{4}$$

$$P_{S_1(cond)} = R_{ds(on)}\cdot I^2_{S_1(rms)} = R_{ds(on)}\cdot\left(i_{Lpk}\cdot\frac{1}{2}\sqrt{\frac{\gamma}{2}}\right)^2 \tag{5}$$

$$P_{\mathrm{sec}(cond)} = \frac{1}{T}\int_0^T V_F\left(i_F(t), T_J, V_{gate}\right)\cdot i_F(t)\,dt \tag{6}$$

$$\begin{aligned} P_{D_1(cond)} &= V_F\cdot I_{D_1(avg)} + R_F\cdot I^2_{D_1(rms)} \\ &= V_F\cdot\left(\frac{i_{Lpk}}{2n\cdot\pi}\right) + R_{ds(on)}\cdot\left(\frac{i_{Lpk}}{2n}\cdot\sqrt{\frac{\gamma}{2}}\right)^2 \end{aligned} \tag{7}$$

B. DC-Link Capacitor

For the dc-link capacitor, the aluminum electrolytic capacitor from EPCOS, with $1000\mu F$ capacitance and voltage rating of 450 V is used. The capacitor has an equivalent-series resistance of $R_{ESR} = 55m\Omega$. Because of the voltage rating of the capacitors, two devices needs to be connected in series. The losses on this component are calculated according to

$$P_{C_o} = 2\cdot R_{ESR}\cdot I^2_{C_o(rms)} = 2\cdot R_{ESR}\cdot\left(\frac{i_{Lpk}}{n}\cdot\sqrt{\frac{\gamma}{2}}\right)^2 \tag{8}$$

C. High Frequency Transformer

In order to optimize the transformer losses, taking into account also the transformer size, a computer-aided design was carried out, and the algorithm flowchart is depicted in Fig. 4. The database based on suitable E-type ferrite cores was created and the list is shown in Table III. Only E-type core were considered, assuming parallel configuration for the implementation and all the considerations are described in Table III. The core-type construction, as shown in Fig. 4 is also assumed. The algorithm starts with the smallest core selection, in this case a single E 55/28/21, and then the basic design is performed. In this point, the number of turn of

Table III
SPECIFICATION OF THE FERRITE CORES CONSIDERED IN THE DESIGN

Core	Ferrite Material	Specification	N° of parallel cores
E 55/28/21	N87/N97	B66335	up to 3
E 65/32/27	N87	B66387	up to 3
E 70/33/32	N87	B66371	up to 2
E 80/38/20	N87	B66375	1

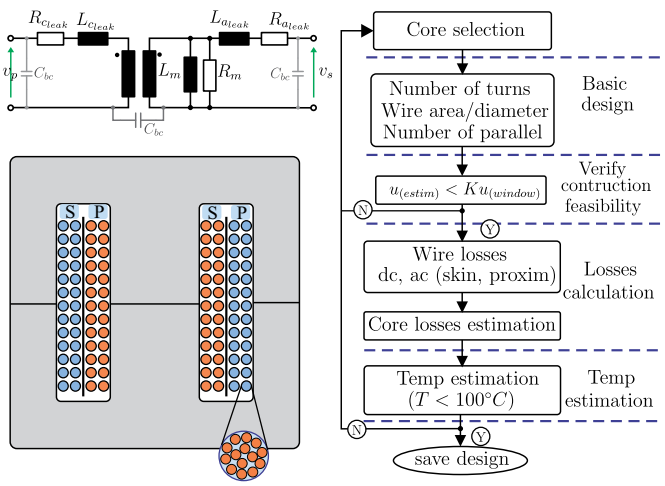


Figure 4. Electric model of the HFT, showing the parasitic elements. Implementation scheme of the HFT, showing the disposition of the primary and secondary windings in the core. The simplified flowchart of the algorithm used to design the optimized HFT.

both windings is calculated and the wires are selected. In the next point, the implementation feasibility is verified by comparing the available window area of the selected core with the area required for the design. If the transformer can not be built, a bigger core is selected and the procedure starts again. Otherwise, the algorithm goes to the next point: losses calculation.

For the wire losses, the skin and proximity effect are considered additionally to the dc losses. To avoid the skin effect, litz wire is used. To losses caused by proximity effect are estimated based on [23]. For the core losses, the Steinmetz equation due to the almost pure sinusoidal current waveforms [24] is used. Finally, the temperature is estimated according to [25] under the assumption of natural convection cooling. The design result is summarized in Table IV. Discussions about the transformer implementation and experimental verification are presented in Section V.

IV. RELIABILITY ASSESSMENT

To achieve high reliability, the most frequent device failures are evaluated and a failure mode and effect analysis (FMEA)

Table IV
TRANSFORMER SPECIFICATION USED FOR ITS IMPLEMENTATION

Core	N of turns	wire	N° of parallel cores
2x E 65/32/27	$n_{pri} = 26$	90 x AWG32	up to 3
	$n_{sec} = 22$	2000 * AWG44	up to 2

for the SRC is carried out, as shown in Table I. According to the industries reports [26], [27], the most susceptible device on the SRC is the the primary side semiconductor, that is usually implemented using MOSFETs [26], [27]. In the second place is the resonant capacitors (C_r).

To improve the robustness of the converter and consequently the smart transformer reliability, the failure causes on these two components are analyzed and a solution to avoid or postpone the fault in each case is proposed.

A. Primary side semiconductor failure

As can be observed in Table V, the faul on the switches reported in [27], regardless the reason, leads to a short-circuit (SC) state of this device. Hence, a solution to avoid this problem, keeping the converter still operational, is to use the fault tolerant SRC topology proposed in [18] (shown in Fig. 5), instead of the classic one shown in 2. Additionally, the topology presented in 5 is also resilient to open-circuit (OC), making it a suitable solution for every kind of semiconductor fault of the primary side.

B. Resonant Capacitor failure

The resonant capacitor is listed as the second most failure device. The reasons for that are the start-up conditions (leading to an overvoltage), and also the current stress caused by the load variation (as short-circuit or overload). Normally, most of the failures lead to an OC condition. In order to postpone as much as possible the capacitor failure, its lifetime model is evaluated, in order to implement a reliability-based design.

The Metalized Polypropylene Film (MPPF) capacitors from WIMA (MKP10 series) are used to implement the tank circuit. The considered capacitors are: $150nF$, $3300nF$, $6800nF$, all rated for 400Vac/650Vac. According to [28], for this kind of capacitor, the lifetime model is given by (9), which depends on the operation temperature (T), operation voltage (V) and characteristic constants (E_a and E_b) [28]. The operation temperature of the capacitor is directly related to the rms current of the tank circuit ($i_{L(rms)}$). The peak voltage on the capacitor is given by (10) [18], which is function of the resonant capacitance and output power (represented by the input current I_i). Then, not only the tank circuit current, but also the capacitor voltage operation and overvoltage during start-up and load variation depend on the L_r and C_r pair selection.

In this context, the influence of the L_r and C_r selection on the capacitor lifetime is evaluated. To do so, the equation

Table V
FAILURE MODE AND EFFECTS ANALYSIS OF THE SRC

Most faulty device	Failure mode	Failure cause	Solution
Semiconductors Devices	Short-circuit	current stress Overvoltage Load SC	Fault tolerance scheme
Resonant capacitor (C_r)	open-circuit	current stress Overvoltage/start-up overload/SC	Optimum parameter selection

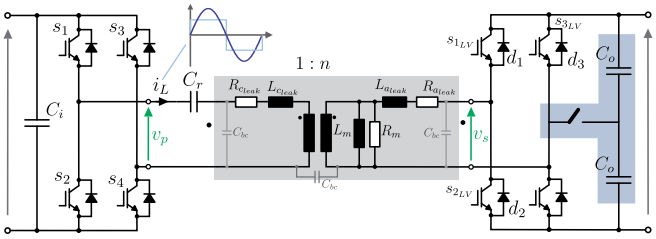


Figure 5. SRC topology with fault tolerance capability used as a basic cell of the dc stage of the ST.

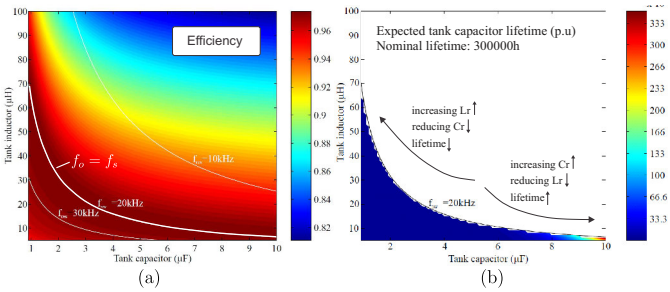


Figure 6. Graphic analysis of the SRC efficiency (a) and reliability (b) in terms of the L_r and C_r.

(9) is expanded and written in function of the $i_{L(rms)}$, tank current overshoot $i_{L(os)}$ (during start-up, load variation of load short-circuit), capacitor voltage (V_{C_r}) and capacitor overvoltage ($V_{C_r(ov)}$) and all these mentioned parameters are written in function of L_r and C_r. Thus, the capacitor lifetime model in function of L_r and C_r is derived and a graphic summarizing the result for the studied case is plotted in 6 (b).

$$L = L_o \cdot \left(\frac{V}{V_o}\right)^{-n} \cdot e^{\left[\left(\frac{E_a}{K_b}\right)\cdot\left(\frac{1}{T}-\frac{1}{T_o}\right)\right]} \tag{9}$$

$$V_{Cpk} = \frac{I_i}{8 f_s C_r} \tag{10}$$

C. Tank Circuit Parameter Selection

Using the previous losses equations, a similar procedure is carried out to obtain the influence of L_r and C_r on the converter losses. Therefore, the estimated efficiency of the converter in function of L_r and C_r is also obtained, as shown in 6 (a). As can be observed, the efficiency reaches its maximum value when $f_o = f_s$, as expected and already discussed. In the graphic 6 (b), the capacitor lifetime is longer for lower value of L_r and higher values of C_r. Therefore, to extended as much as possible the capacitor lifetime, the inductance L_r must be as low as possible, while the capacitance C_r should be as big as possible, keeping f_o constant. The minimum inductance value possible is constrained by the leakage inductance of the transformer. Therefore, only the leakage inductance of the transformer should be used and no external inductance is added.

Table VI
SPECIFICATION OF THE SRC PROTOTYPE

Input voltage	$V_i = 700$ V
Output voltage	$V_o = 600$ V
Nominal output power	$P_o = 10$ kW
Switching frequency	$f_s = 20$ kHz
Transformer turn ratio	$n = 1.45$

Table VII
MEASURED PARAMETERS OF THE HFT

Leakage inductance	$L_{leak} = 13.5\mu H$
Winding resistance (primary and secondary)	$R_{wire} = 86m\Omega$
Magnetizing inductance	$L_m = 7.93mH$
Core Losses	$R_{core} = 309.5k\Omega$
Total Losses	$P_{HFT} = 56.4W$

V. PROTOTYPE IMPLEMENTATION AND EXPERIMENTS RESULTS

In order to evaluate the converter performance experimentally and verify the presented design procedure, a prototype was built and tested. The main specifications are shown in Table VI. The transformer implementation, converter construction and the final results are discussed.

A. High Frequency Transformer Implementation and Tests

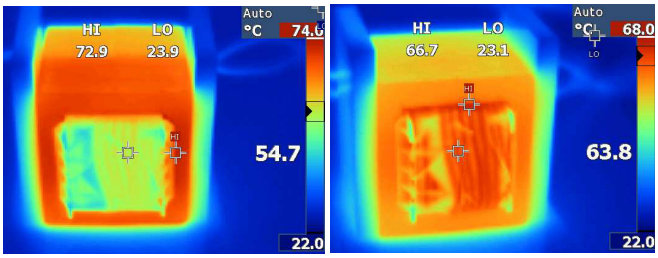
The high frequency transformer (HFT) was implemented according to the design presented in Section III. As a result of the design, 2 cores E65/32/27 from EPCOS/TDK were used in parallel and the physical implementation is described in Table IV. The implemented transformer was experimentally evaluated and its main parameters, as well as the core losses and wire losses were obtained. The intrinsic parameters of the transformer are shown in Table VII.

In order to evaluate more carefully the losses on the transformer, the open-circuit and short-circuit tests were performed according to [29]. With these tests, it is possible to separate the core losses from the wire losses, and to obtain the wire losses decomposition in ac and dc losses. The total losses of the HFT are presented in Table VII, while the losses distribution is depicted in Fig. 12. As can be observed, the wires are responsible for most of the losses (61%), where 22% of this value are the ac losses, due to the proximity effect. The expected ac losses is between 20% and 30% of the total wire losses. Thus, the obtained value is in accordance to the analysis, showing a good implementation of the transformer.

Finally, the temperature were measured in both tests, in order to check the temperature rise due to the core and wire losses individually. The results are presented in Fig. 7 and it is observed that the temperature is well below the maximum of $100°C$.

B. Final Prototype Assembly

Once the resonant frequency and the transformer leakage inductance are chosen, the resonant capacitance (C_r) can be



(a) (b)

Figure 7. Temperature obtained during the open-circuit and short-circuit test on the transformer: (a) core losses (open-circuit test) and (a) wire losses (shot-circuit)

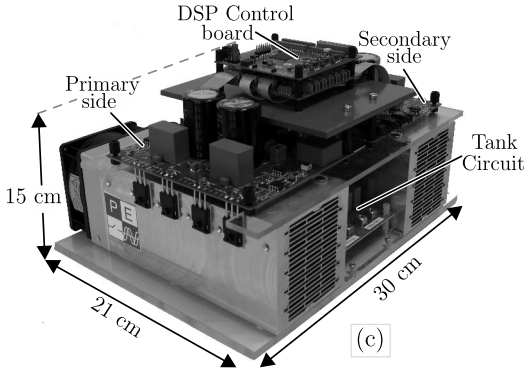


Figure 8. Implemented 10 kW SRC converter hardware prototype (mechanical dimensions: 300 mm x 210 mm x 150 mm).

selected. As discussed in section IV, the resonant inductance should be the transformer leakage inductance, then $L_r = 13.5\mu H$. To select the resonant frequency, the dead-time between the semiconductors of the same leg should be taken into account. Besides that, a resonance frequency slight above the switching should be selected, so that the inductor current can have a small zero-time, allowing the semiconductors to deplete their stored charge. Therefore, assuming a dead-time of $1\mu s$, the resonance frequency of $f_o = 21.7kHz$ is select. To obtain this value, the resonant capacitance should be $C_r = 4.3\mu F$. Thus, the C_r is implemented by using 9 capacitors of $330nF$ and 2 capacitors of $680nF$ connected in parallel.

Fig. 8 shows the photo of the implemented prototype. As aforementioned, the converter operates in open loop and the gate signals are generated by the DSP. Although two different SiC MOSFETs were considered during the design, the results shown is this paper were obtained using the SiC MOSFET C2M0025120D, because of their lower on-resistance. For the secondary side, the silicon IGBT IHW40N120R3 was used in parallel with the SiC diode C4D20120D. The SiC diode was selected because of its very low reverse recovery charge.

C. Experimental Results

The experimental results were obtained for the converter operating in steady-state at nominal load, where the main waveforms were saved and the thermal behavior of the main

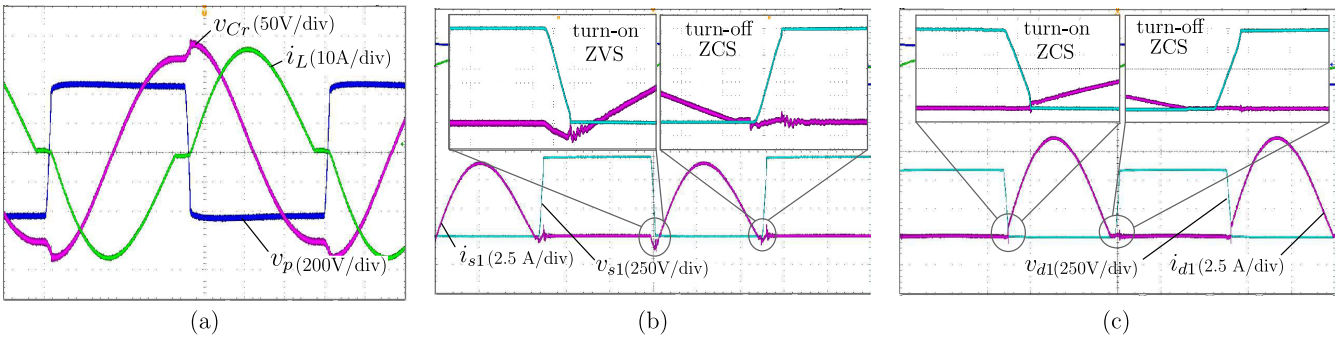


Figure 9. Experimental results obtained in steady-state: (a) primary side voltage (v_p), voltage over the resonant capacitor (v_{Cr}) and tank circuit current (i_{Lr}), (b) current and voltage on the primary side semiconductor (s_1), (c) current and voltage on the secondary side semiconductor (d_1).

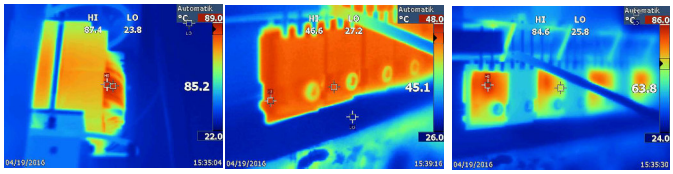


Figure 10. Thermal behavior of the main components of the converter operating under nominal condition: (a) HFT, (b) primary side SiC-MOSFETs, (b) primary side SiC-diodes.

components was evaluated by a temperature measurement system. Additionally, the converter efficiency and the losses distribution on the components are verified and discussed. The results are summarized from Fig. 9 to Fig. 12.

The main waveforms obtained experimentally for the converter operating in steady-state in nominal condition (i.e. 10 kW, 600 V to 700 V) are shown in 9. In Fig. 9 (a), the primary side voltage (v_p), the voltage over the resonant capacitor (v_{Cr}) and the tank circuit current (i_{Lr}) are shown. Fig. 9 (b) shows the current and voltage on the primary side semiconductor (s_1), where soft-switching operation is verified. As expected, the primary side semiconductors turn on in ZVS and turn off in ZCS. The commutation detail is also depicted in Fig. 9 (b). Similarly, the current and voltage on the secondary side diode (d_1) are presented in Fig. 9 (c), where ZCS operation during turn-on and turn-off is observed. Therefore, these results confirmed that the switching losses can be completely neglected during the design of the converter.

The temperatures of the transformer, the primary and secondary side semiconductors for the converter operating at nominal condition are depicted in Fig. 10. As can be noticed, the hotspot on the transformer has an temperature of $89°C$, which is below the maximum of $100°C$ defined by the design. The secondary side semiconductors have higher temperature, because of their higher losses compared to the primary side semiconductors.

Finally, the efficiency curve in function of the output power is shown in Fig. 11, while the losses distribution is presented in Fig. 12. The efficiency curve was obtained experimentally using the high performance power analyzer WT1800 from

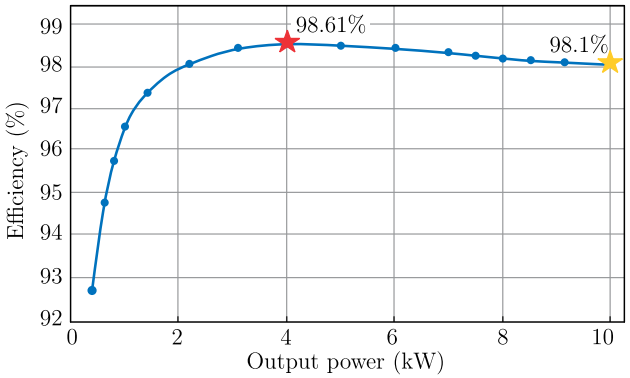


Figure 11. Efficiency curve of the converter as a function of the output power obtained experimentally.

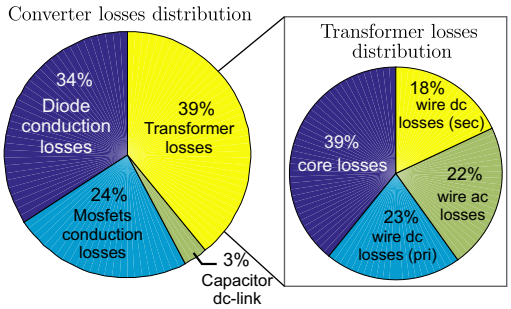


Figure 12. Losses distribution on the main components of the converter and also the losses distribution on the HFT.

Yokogawa (basic power accuracy of 0.02%). As can be seen, the converter has achieved a peak efficiency of 98.61% at a power level of around $4kW$, while at nominal load the converter has achieved around 98.1% of efficiency. This results confirmed the optimum design of the converter, as well as the high potentiality of the SiC technology in this application. Evaluating the losses distribution depicted in Fig. 11, it is noted that the transformer is responsible for most of the losses. It is important to note that the conduction losses of the MOSFETs are lower than the diode conduction losses, even having high rms current, since the MOSFET is connected on

the LV side.

VI. Conclusion

The series resonant converter is a promising topology to be used as building block of the modular dc-dc stage of smart transformer. In this system, high efficiency and reliability are extremely desired. In this paper an optimum design of a series resonant converter to obtain not only high efficiency, but also high reliability was proposed.

To obtain high efficiency, the losses were carefully modeled and a minimization procedure is performed. Additionally, SiC-MOSFETs with very low on-resistance were used on the primary side, while SiC diode associated with IGBT were used on the secondary side of the converter.

To increase the reliability, the two most critical devices are analyzed: the primary side semiconductor and the resonant capacitor. To avoid fault on the switch, a fault-tolerant SRC topology was proposed to be used instead the classic one, avoiding the interruption of the system in faulty case. To extend the reliability of the resonant capacitor, its lifetime model is used and a trade-off between the resonant tank parameters selection is found. As a results, the resonant tank circuit should have a high capacitance value (C_r) and small inductance value (L_r) (for a given resonant frequency). Following this procedure, the capacitor lifetime is extended. In that case, only the leakage inductance of the transformer should be used as the resonant inductor, and no additional components should be included.

Finally, experimental results were provided for a 10 kW prototype. The proposed converter has obtained a peak efficiency of 98.61%, proving the validity of the presented design.

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