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# Analysis and Design of Asymmetric Quad-Active-Bridge Converter

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*Abstract*—**The focus of this paper is on power flow control in the asymmetric quad-active-bridge (QAB) converter and its limitations imposed by uneven values of parasitic elements in the isolation transformer. The QAB converter under study is intended for solid-state transformer applications in asymmetric configuration, where one of the ports is placed at the low voltage side and rated for the threefold power of the medium voltage ports. Significant imbalance between leakage inductance could be observed between them. The steady-state analysis of the asymmetric QAB converter and assessment of power losses using numerical simulation are provided. Experimental waveforms were obtained using a prototype rated for cumulative MV dc link of 2400 V and power of 30 kW.**

*Keywords— bidirectional converters, dc–dc conversion, smart transformer, solid-state transformer, energy efficiency*

## I. INTRODUCTION

The concept of the solid-state transformer (SST) was first introduced in the 1960s and further endorsed for traction applications, where mass and volume reduction justify higher capital costs [1]. Rapid proliferation of the distributed generation paradigm with high impact of renewable energy imposed new challenges of the grid stability, electricity supply security, and power quality. Continuous cost reduction of silicon and wide bandgap power semiconductors encourages research on use of the SST as a smart device that replaces conventional low-frequency transformers to resolve all those issues [2], [3]. The major concerns regarding SST are its cost, reliability, and protection in case of the grid faults.

Usually, an SST interfaces low-voltage (LV) and medium voltage (MV) grids. Three-stage modular SST architecture was widely advertised as a highly reliable approach [2]. It utilizes multilevel converter at the MV side and a high power three-phase inverter(s) at the LV side, which are coupled by a dc-dc stage. Each MV floating dc link is connected to the LV dc link through a dc-dc converter. Numerous topologies were applied to the modular SST architecture, whereas series resonant and dual active bridge (DAB) converters attracted the most attention. The former can be used as a highly efficient dc transformer, while the latter enables flexible control of power flows at the cost of increased switching losses.

Modular approach suffers from uneven aging of switching cells, where semiconductors and dc link capacitors contribute
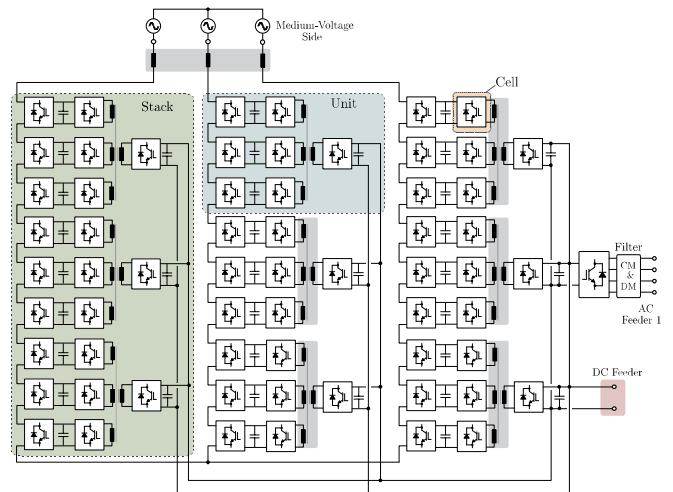


Fig. 1. QAB base semimodular architecture of the solid-state transformer.

the most to the failure rate [4], [5]. The lifetime of capacitors can be prolonged if they operate at voltage and RMS current below rated. Failure of the power semiconductors depends on thermal cycling and correlates with absolute value and swing of the temperature [6]. Time to failure of different cells can vary significantly due to mismatch of parameters, replacement of unit, etc. Junction temperature can be monitored [7], [8] and, therefore, can be restrained by means of the active power flow control to balance aging of modules [9], [10].

To reduce number of units along with the capital costs, the quad-active-bridge (QAB) converter [11], [12] was applied to the SST in asymmetric configuration as shown in Fig. 1 [13]. This solution is capable of the flexible power routing and reduces number of transformers and LV side switching cells. The QAB converter should be designed for asymmetric operation when the LV port processes threefold power of the MV ports. Previous analyses of the QAB converter were considering symmetrical design, while it might not a case in the given application. Power routing should be performed for the composite structure of QAB and cascaded H-bridge (CHB) converters [14]. This study pursues two goals: to analyze operation of the asymmetric QAB converter and to show how the asymmetry influences power flow control and unloading of semiconductors. The next section introduces the asymmetric QAB converter and presents steady state analysis. In the third

section, the influence of asymmetry on power flow control is discussed. Simulation and experimental results are presented in the fourth section. Finally, conclusions are drawn.

## II. OPERATION PRINCIPLE AND ANALYSIS OF THE ASYMMETRIC QAB CONVERTER

The QAB converter topology is shown in Fig. 2a. Inductors in the MV side are considered equal:

$$L_b = L_c = L_d = L. \tag{1}$$

The LV port operates at higher power and could have higher leakage inductance due to larger copper cross section area:

$$L_a = k \cdot L, \, k \geq 1. \tag{2}$$

The inductance values are bounded above to ensure power transfer capability, i.e., balancing of the ratio $k$ with external inductors in the MV ports is limited. It is assumed that the transformer has the unity turns ratio, which allows use of semiconductors rated for the same voltage in all the ports.

### A. Operation of the QAB Converter

The QAB converter contains four full-bridge switching cells, and each of them is denoted by subscript indexes: "$a$" for the LV port, and "$b$", "$c$", and "$d$" for the MV ports. The single phase shift (SPS) modulation shown in Fig. 3 is advantageous for the asymmetric QAB under normal operating conditions [15], and thus it is used in this study. The "Y" ac equivalent circuit of the given QAB converter presented in Fig. 2b explains why energy transfer is possible between all the ports as shown in Fig. 2c. The power semiconductors operate with a duty cycle close to 0.5 and feature zero voltage switching (ZVS). The ZVS can be maintained at any load if $V_a = V_b = V_c = V_d$, otherwise hard switching could occur.

Some of the ports can receive power from one port and transmit it to other port(s). Hereinafter, such port will be designated in the text as the forwarding port. Zero power flow is feasible at the corresponding dc terminals [12]. An unloaded MV port could support surplus power transfer between the LV port and two overloaded MV ports and, at the same time, achieve reduced stress of semiconductors. Fig. 3 explains operation of the QAB with unbalanced power flow. Unloading MV ports could prolong their lifetime together with the corresponding CHB converter cells. Few QAB converters should be used in parallel to unload the LV port [16].

### B. Steady-State Analysis of the Asymmetric QAB Converter

For the further analysis, the "Y" equivalent ac circuit from Fig. 2b was transformed into the corresponding "Δ" equivalent ac circuit shown in Fig. 2d. It introduces two new equivalent inductance values:

$$L_{ML} = (3 \cdot k + 1) \cdot L. \tag{3}$$
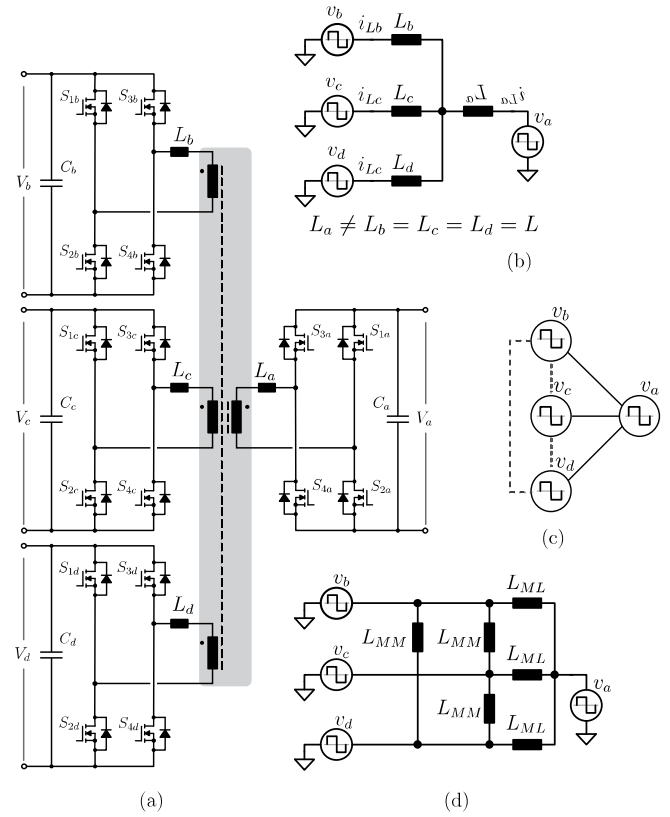
$$L_{MM} = \frac{(3 \cdot k + 1)}{k} \cdot L. \tag{4}$$



Fig. 2. The quad-active-bridge dc-dc converter: (a) topology, (b) "Y" equivalent ac circuit, (c) all possible power path of the converter, and (d) "Δ" equivalent ac circuit.
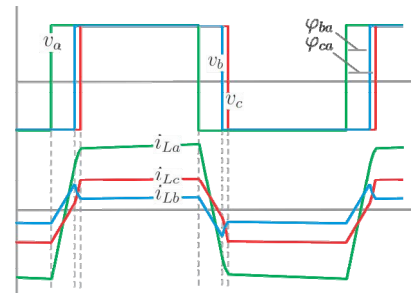


Fig. 3. Idealized transformer current and voltage waveforms of the QAB converter for unbalanced conditions in case of single phase shift control.

The inductances are equal in the symmetrical case when $k = 1$.

Let us assume that the dc link voltage of all the ports equals to nominal voltage $V_{DC}$ in the normal operation conditions with balanced power flows between MV ports and the LV port. Two constants could be defined for normal operation conditions:

$$P_{ML}^{\max} = \frac{V_{DC}^2}{8 \cdot f_s \cdot (3 \cdot k + 1) \cdot L}, \tag{5}$$

$$P_{MM}^{\max} = \frac{V_{DC}^2 \cdot k}{8 \cdot f_s \cdot (3 \cdot k + 1) \cdot L}, \tag{6}$$

where the first is the maximum power that can be transferred between the LV port and any MV port; and the latter is the

maximum power that can be transferred between two MV ports; $f_s$ is the switching frequency. Evidently, the ratio between those powers depends on the parameter $k$:

$$P_{MM}^{max} = k \cdot P_{ML}^{max}, \qquad (7)$$

The power that is transferred from an MV ports $j$ to an MV port $k$, i.e., $j, k \in \{b, c, d\}$, could be defined as a function of the corresponding phase shift angle ($\varphi_{jk}$ in radians):

$$P_{jk}(\varphi_{jk}) = P_{MM}^{max} \cdot \frac{4}{\pi} \cdot \varphi_{jk} \cdot \left(1 - \frac{|\varphi_{jk}|}{\pi}\right), \varphi_{jk} = \varphi_k - \varphi_j, j \neq k . (8)$$

Power transferred between the LV port "$a$" and the $j$-th MV ports can be defined assuming henceforth $\varphi_a = 0$:

$$P_{ja}(\varphi_j) = P_{ML}^{max} \cdot \frac{4}{\pi} \cdot \varphi_j \cdot \left(1 - \frac{|\varphi_j|}{\pi}\right), j \in \{b, c, d\} . \qquad (9)$$

Energy at the dc ports can be calculated as:

$$P_k = \sum_j P_{kj}, \{j, k\} \in \{a, b, c, d\} \Leftrightarrow j \neq k . \qquad (10)$$

In the balanced conditions: $P_b = P_c = P_d = P_{ML}$, $\varphi_{ba} = \varphi_{ca} = \varphi_{da} = \varphi_{ML}$, and $P_a = 3 \cdot P_{ML}$, and there is no power transfer between the MV ports. The best operation conditions at the rated power $P_{QAB}$ are met if the phase shift between the LV port and the MV ports equals 45° [17],[18]:

$$\frac{P_{QAB}}{3} = P_{ML}(\frac{\pi}{4}) = \frac{3}{4} \cdot P_{ML}^{max} . \qquad (11)$$

Hence, the inductances should correspond to the following:

$$3 \cdot L_a + L = (3 \cdot k + 1) \cdot L = \frac{9 \cdot V_{DC}^2}{32 \cdot f_s \cdot P_{QAB}} . \qquad (12)$$

### III. POWER TRANSFER CONTROL IN THE ASYMMETRIC QAB CONVERTER

This section investigates how the control variables change during power transfer control and whether they are influenced by the inductance ratio parameter $k$. The following evaluation is based on the assumption that values of inductors correspond to Eq. (15) for any $k$. Below, all powers are assessed in unit, where a unit corresponds to $P_{QAB}$ defined in Eq. (11).

The power transfer between the LV port and the MV ports depends on the dc link voltage due to gyrator nature of the QAB converter. Each MV port receives one-third of the rated power at the phase shift of 45° in the nominal conditions:

$$p_{ML}^j(\varphi_{ja}) = \frac{16 \cdot m_j}{9 \cdot \pi} \cdot \varphi_{ja} \cdot \left(1 - \frac{\varphi_{ja}}{\pi}\right), j \in \{b, c, d\}, 0 \leq m_j \leq 1, (13)$$

where parameter $m_j = (V_j \cdot V_a)/V_{DC}^2$ defines dc link voltage variations. It is evident from (13) that in case if one of the two dc link voltages drops by 25% ($m_j = 0.75$), the QAB converter still can deliver one-third of the rated power to an MV port at the maximum phase shift of 90°. Further decrease of any of the dc link voltages will lower the power transfer capability below the acceptable level due to the design process optimization for the best performance according to (12). Therefore, converter design should be designed for the worst operating conditions when needed.

The port "$b$" is selected to be the forwarding port with zero average power: $P_{ba} = (P_{cb} + P_{db})$ and $P_b = 0$. Two other ports operate with the same phase shift, i.e., $\varphi_{ca} = \varphi_{da}$ and $P_{ca} = P_{da}$:

$$\varphi_{ba} \cdot \left(1 - \frac{\varphi_{ba}}{\pi}\right) = 2 \cdot k \cdot (\varphi_{ca} - \varphi_{ba}) \cdot \left(1 - \frac{(\varphi_{ca} - \varphi_{ba})}{\pi}\right), \quad (14)$$

where $\varphi_{ca} = \varphi_{ba} + \varphi_{cb}$. Solving (17) with assumptions that $\varphi_{ba} < \varphi_{ca} = \varphi_{da}$ and $\varphi_{ba} < 90°$, function $\varphi_{ba}(\varphi_{ca})$ was obtained:

$$\varphi_{ba}(\varphi_{ca}) = \frac{1}{2(2k-1)} \cdot \left(k(4\varphi_{ca} - 2\pi) - \pi + \right.$$
$$\left. + \sqrt{4\pi^2 k^2 + 4k(2\varphi_{ca}^2 - 4\pi\varphi_{ca} + \pi^2) + \pi^2}\right) . \qquad (15)$$

It is worth mentioning that expression (15) is independent of power level as long as the forwarding port maintains zero average power. Difference between these angles converges to zero when the parameter $k$ rises as shown in Fig. 4:

Cumulative power transfer capability between the LV port and the MV ports of the asymmetric QAB converter with fully unloaded forwarding port "$b$" is plotted in Fig. 5 based on Eqs. (5)-(15). The following assumptions were taken into account: $P_{ba} = P_{cb} + P_{db}$, $P_b = 0$, $P_{ca} = P_{da}$, $\varphi_{ca} = \varphi_{da}$, $P_{cb} = P_{db}$, $\varphi_{cb} = \varphi_{db}$. Cures showed: $P_a$ in case of balanced MV dc links for $k = 5$ – curve (1) and $k = 1$ – curve (2). Curves (3) and (4) show $P_a$ for $k = 5$ and $k = 1$, respectively, when $V_a = V_{DC}$, $V_c = V_d = 1.125 \cdot V_{DC}$ and $V_b = 0.75 \cdot V_{DC}$.
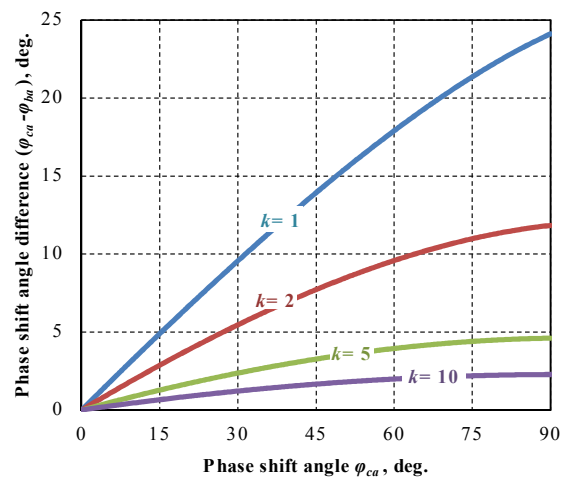


Fig. 4. The phase shift angle difference between the fully unloaded MV forwarding port and the other two overloaded MV ports.
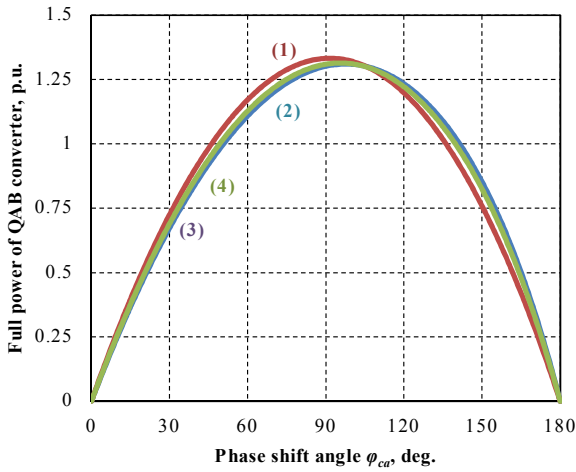
Fig. 5. Power transfer capability of the asymmetric QAB converter.

Controllability of power flows could be compromised at high values of $k$ since regulation of the forwarding port is performed within a narrow range. Also, the capability of the QAB converter to deliver power from the LV port to remaining two MV ports is supported by the fully unloaded forwarding MV port and virtually does not depend on $k$. It is not compromised by uneven MV dc link distribution as long as cumulative MV dc link remain equal to the nominal value: $(V_b + V_c + V_d) = 3 \cdot V_{DC}$. However, the current stress of the semiconductor components in the MV ports would increase at higher values of $k$. Hence, possibility to unload an MV port simultaneously with the MV dc link voltage redistribution is proposed to reduce RMS currents in the overloaded MV ports.

The further analysis evaluates the operation of the asymmetric QAB converter when a forwarding port features reduced voltage at lower average power. The new unloading parameter $\lambda$ was introduced to define this:

$$P_b = \frac{1}{3} \cdot P_{QAB} \cdot (1 - \lambda), 0 \le \lambda \le 1. \quad (16)$$

The following considers the scenario, when the asymmetric QAB converter operates at the $P_a = P_{QAB}$, maintains constant cumulative MV dc link voltage, and control MV dc link voltage distribution proportional to the unloading parameter $\lambda$:

$$P_c = P_d = \frac{1}{3} \cdot P_{QAB} \cdot (1 + \frac{\lambda}{2}), 0 \le \lambda \le 1, \quad (17)$$

$$V_a = V_{DC}, \ V_b = V_{DC} \cdot (1 - \frac{\lambda}{4}), \ V_c = V_d = V_{DC} \cdot (1 + \frac{\lambda}{8}). \quad (18)$$

Based on (16)-(18), a system of equations (19) was derived using (5)-(15). Numerical solutions obtained are plotted in Fig. 6. Expectedly, both angles are equal to 45° at any value of $k$, when the load is balanced ($\lambda = 0$). Considerable inductance asymmetry in the asymmetric QAB converter results in narrow regulation range and, consequently, increased requirements to the control system, especially in dynamic conditions.
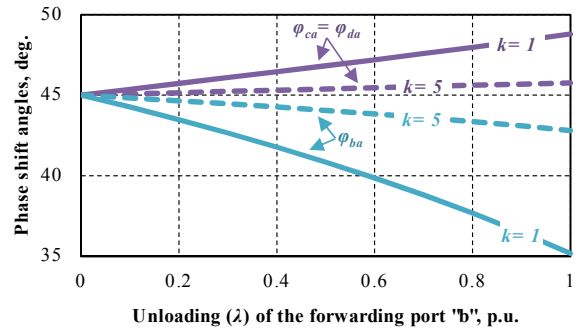


Fig. 6. Numerical solutions of Eq. (19).

$$\begin{cases} \frac{(8+\lambda) \cdot 2}{9 \cdot \pi} \cdot \left[ \varphi_{ca} \cdot \left(1 - \frac{\varphi_{ca}}{\pi}\right) + k \cdot \left(1 - \frac{\lambda}{4}\right) \cdot F \right] = \frac{2+\lambda}{6} \\ \frac{(4-\lambda) \cdot 4}{9 \cdot \pi} \cdot \left[ \varphi_{ba} \cdot \left(1 - \frac{\varphi_{ba}}{\pi}\right) - 2 \cdot k \cdot \left(1 + \frac{\lambda}{8}\right) \cdot F \right] = \frac{1-\lambda}{3} \end{cases}, \quad (19)$$

where $F = (\varphi_{ca} - \varphi_{ba}) \cdot (\pi + \varphi_{ba} - \varphi_{ca})/\pi$.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

Verification of unloading capability of the forwarding MV port "$b$" was performed by means of the numerical simulation in PSIM package. A simulation model was built including model of losses in semiconductor components, parameters of heatsinks and thermal interfaces that are utilized in the existing prototype (Fig. 7). Main simulation parameters are presented in Table I for two possible designs of magnetic components. Conduction losses in passive components were introduced in the model in the form of equivalent series resistance (ESR) on the scale of 20 mΩ each. Power losses in semiconductor power switches were assessed using PSIM add-on "Thermal Module."

Waveforms of the simulated transformer voltages and currents along with the power of each port are presented in Figs. 8 and 9. Cumulative semiconductor power loss, the junction temperature of a switch and RMS current of a series inductor $L_j$, where $j \in \{a, b, c, d\}$, are presented for the each switching cell. Simulation study was performed for two cases: $k = 1$ (symmetric QAB converter) and $k = 5$. The simulation model demonstrates slightly smaller regulation range than that predicted theoretically due to influence of losses and dead-time. Also, symmetric QAB converter features roughly three times wider regulation range when compared to the given asymmetric counterpart.

In the given case, considerable asymmetry of the transformer series inductances results in semiconductor power loss of the forwarding port much higher than that of the other MV ports. Also, absolute values of the semiconductor power loss and junction temperature are much higher in case of the asymmetric QAB when compared to the symmetric counterpart. It can be concluded that the asymmetric QAB converter suffers from higher semiconductor power losses, especially in the unloaded port regardless its zero average power. In the given case, the junction temperature of the switches in the fully unloaded port "$b$" approaches the absolute allowed maximum. This diminishes the main benefit of the

active power flow control – possibility to increase the lifetime of a switching cell through facilitation of its temperature operating conditions. However, the asymmetric QAB is still capable of maintaining power flow constant with one MV port fully unloaded even in case of high asymmetry ($k \gg 1$).

An asymmetric QAB rated for the same power as a symmetric counterpart will have lower efficiency due to higher peak and RMS current stress of semiconductors caused by considerably increased circulation power. Based on the performed analysis, the symmetric design was chosen. The isolation transformer was wound at N87 2×UU93 core with 20 turns per winding. Despite more challenging isolation requirements, design utilizes interleaving when LV winding is split into three parallel sections to minimize leakage inductance. Series inductances were realized as external components based on N87 EE70 core with 9 turns – two core sets for the MV inductors and four core sets for the LV inductor. Tests were performed at the nominal voltage at all ports and power of 10 kW limited by available power supply.

TABLE I.        SIMULATION PARAMETERS

| Parameter | Value | |
|---|---|---|
| $V_{DC}$, $V_a$ [V] | 800 | |
| $f_s$, [kHz] | 20 | |
| Dead-time, [ns] | 250 | |
| $P_{QAB}$, [kW] | 30 | |
| $V_b$, [V] | 600 | |
| $V_c$, $V_d$, [V] | 900 | |
| $P_a$, [kW] | 30 | |
| $P_b$, [kW] | 0 | |
| $P_c$, $P_d$, [kW] | 15 | |
| MV side switches | C2M0040120D: TO-247; $R_{DS(on)}$ = 40 m$\Omega$; $V_{(BR)DSS}$ = 1200 V; $R_{\theta JC}$ = 0.34 K/W | |
| LV side switches | C2M0025120D: TO-247; $R_{DS(on)}$ = 25 m$\Omega$; $V_{(BR)DSS}$ = 1200 V; $R_{\theta JC}$ = 0.24 K/W | |
| $R_{\theta CS}$ (case-to-sink), [K/W] | 0.4 | |
| $R_{\theta SA}$ (sink-to-amb.), [K/W] | MV side: 0.06; LV side: 0.047 | |
| Amb. temperature $T_A$, [°C] | 25 | |
| $k$ | 1 | 5 |
| L, [µH] | 75 | 18.75 |
| $\varphi_{ca}$ simul. (theor.), [deg.] | 48.8 (48.8) | 45.8 (45.8) |
| $\varphi_{ba}$ simul. (theor.) , [deg.] | 34 (35.2) | 40.5 (42.8) |
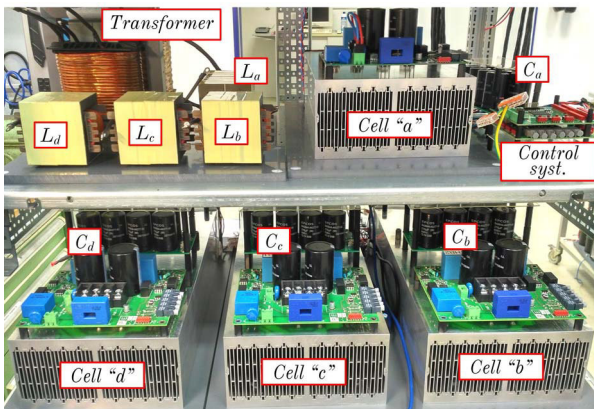


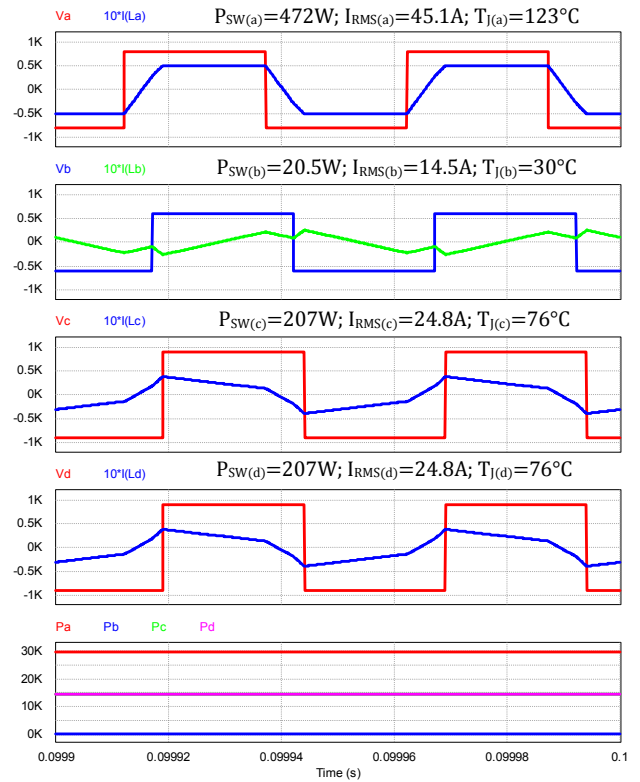Fig. 7.    30 kW experimental prototype under construction.



Fig. 8.    Simulated voltage and current waveforms in the symmetric QAB converter with balanced inductors, i.e. $k$ = 1.


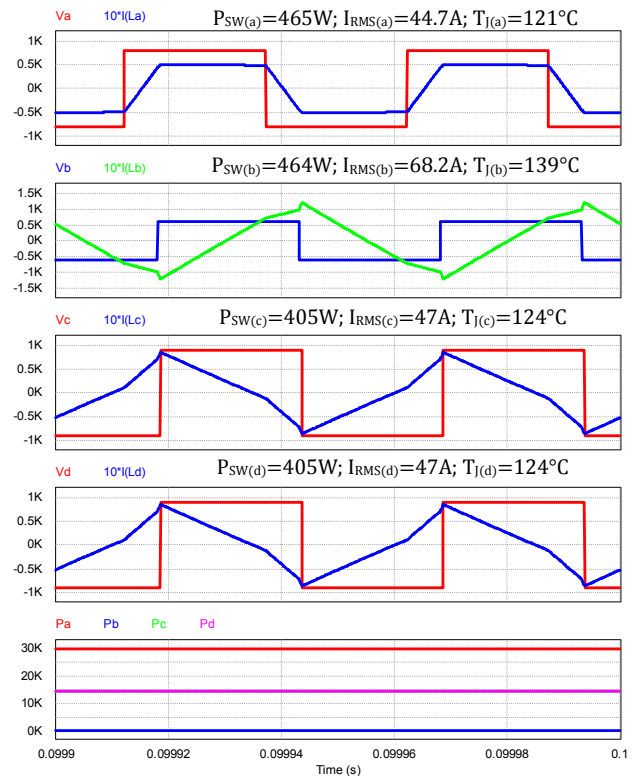
Fig. 9.    Simulated voltage and current waveforms in the asymmetric QAB converter in case of considerably unbalanced inductors: $k$ = 5.
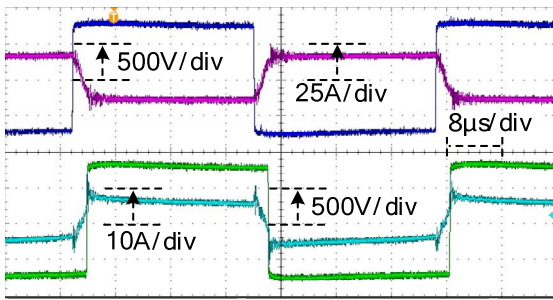
Fig. 10. Experimental voltage and current waveforms of the QAB transformer windings in the LV and MV ports at the power of 10kW.

Epy experimental current and voltage of the transformer windings captured in this operating point are presented in Fig. 10. The simplest SPS control used results in efficiency reaching 96%.

CONCLUSIONS

The proposed steady-state analysis of the asymmetric QAB converter reveals the main challenges that arise from inductance asymmetry. The steady-state analysis was performed taking into account possibility of MV port unloading along with MV dc link redistribution to decrease current stress of the overloaded MV ports. It was demonstrated that MV dc link redistribution does not influence power transfer capabilities of the asymmetric QAB converter as long as the cumulative MV dc link remains constant.

In SST applications, high rated power of the QAB converter results in the need for complicated design of transformer towards minimization of the LV winding inductance. Considerable asymmetry in case of split design of the windings could cause high peak and RMS currents in the semiconductors, i.e., high junction temperature in an unloaded MV port. This eliminates the possibility to increase the lifetime of a corresponding full bridge switching cell. In addition, it should be mentioned, that presented design of the QAB converter inductors aims operation under nominal dc link voltage and rated power. However, design of the series inductors should be changed if the QAB converter should be capable of delivering power under dc link voltage sags. It is not possible to achieve good tradeoff in design of the converter that should withstand large dc link voltage sags.

It was proven that symmetrical design of QAB converter delivers the best performance at the cost of utilization of interleaved windings requiring special measures for robust isolation between ports against partial discharge. Preliminary experimental results presented prove high performance of the symmetric design.

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