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Interleaved Operation of Parallel Neutral-Point Clamped Inverters with Reduced Circulating Current

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Abstract—**Parallel inverters are commonly adopted in high power applications, for instance wind energy system, smart transformer, and power conditioners. Meanwhile, interleaved PWM is usually considered as an optimal approach to reduce the current ripple and harmonics of the parallel inverters. However, in case of a common dc-link, the problem of circulating current emerges and leads to performance degradation. This paper aims at investigating the influence of different modulation techniques on the circulating current of parallel Neutral-Point Clamped (NPC) inverters under interleaved operation. Two modulation techniques: Phase Disposition (PD) and Alternative Phase Opposite Disposition (APOD), have been studied and compared in terms of current ripple, spectrum quality, and circulating current. Though the PD modulation was regarded as the optimum solution in most single NPC cases, it offers worse performance in the parallel NPC application due to higher circulating current. Simulation and experimental validations are provided and show that the APOD leads to much lower circulating current and similar current ripple as well as spectrum quality compared to the PD.**

Index Terms—**NPC inverters, PD, APOD, interleaved operation, circulating current**

I. INTRODUCTION

Parallel inverters are widely utilized in high power applications, including multi-MW wind energy systems [1], smart transformer applications [2], static synchronous compensators (STATCOMs) [3], active power filters (APFs) [4], and electric drives [5]. To improve the current waveform quality, interleaved operation is employed to shift the carrier phases among different modules [6], [7]. In this way, the current ripple of the total current can be reduced and therefore reduces the size of coupled inductors. Nevertheless, in the case of a common dc-link, the circulating current issue raises and would cause critical problems in terms of overcurrent, higher voltage drop, higher thermal stress, and higher stress for dc capacitor. For parallel two-level inverters, it is well known that modulation is one of the key factors that determine the circulating current [6] Optimized modulation techniques have been proposed to minimize the circulating current and largely improve the overall performance [8], [9]. However, for the three-level NPC, this issue and the optimum modulation with reduced circulating current were seldom studied in literature.

Traditionally, two common modulation techniques are employed in a three-level NPC inverter: PD and APOD. The PD

modulation is considered as the best solution in the single NPC inverter, which leads to better waveform and spectrum quality [7], [10]. However, for parallel NPC inverters with common dc-link, the circulating current has to be taken into account during the performance evaluation. With this consideration, it is necessary to reexamine the characteristics of the two well-known modulation in an extensive way.

The main target of this paper is to investigate the impact of different three-level NPC modulation techniques on the circulating current under interleaved operation and find an optimal solution for the Medium Voltage (MV) grid impedance measurement application. In these regards, the common-mode voltage as well as the circulating current of both the PD and the APOD modulation techniques are studied with the consideration of various switching sequences. The performance evaluation in time-domain and phase-domain are carried out by theoretical analysis and simulation/experimental validations The paper structure is organized as follows: the description of a MV grid impedance measurement is given in Section II, with the detailed control and synchronization schemes. In Section III, the problem of circulating current between two parallel NPC inverters under interleaved operation is discussed. Then, the two common multilevel modulation techniques are investigated and evaluated in Section IV in terms of common-mode voltage and circulating current. Simulation and experimental results are provided in Section V to validate the theoretical analyses. Conclusions are drawn in Section VI.

II. MEDIUM-VOLTAGE GRID IMPEDANCE MEASUREMENT SYSTEM

This section describes a MV grid impedance measurement system as an example of parallel inverters in high power applications. In order to guarantee high measurement accuracy over a wide frequency range even in strong grid conditions up to 275 MVA short-circuit (SC) power, the system uses an active, mono-frequency measurement method [11], in which a current at frequencies from 100 Hz to 10 kHz excites the MV grid (at least 1 % grid voltage excitation). Since the high frequency currents require high switching frequencies up to 50 kHz at high power levels, paralleled low-voltage inverters connected to MV transformers for voltage step-up conversion are implemented. In the following, the system configuration
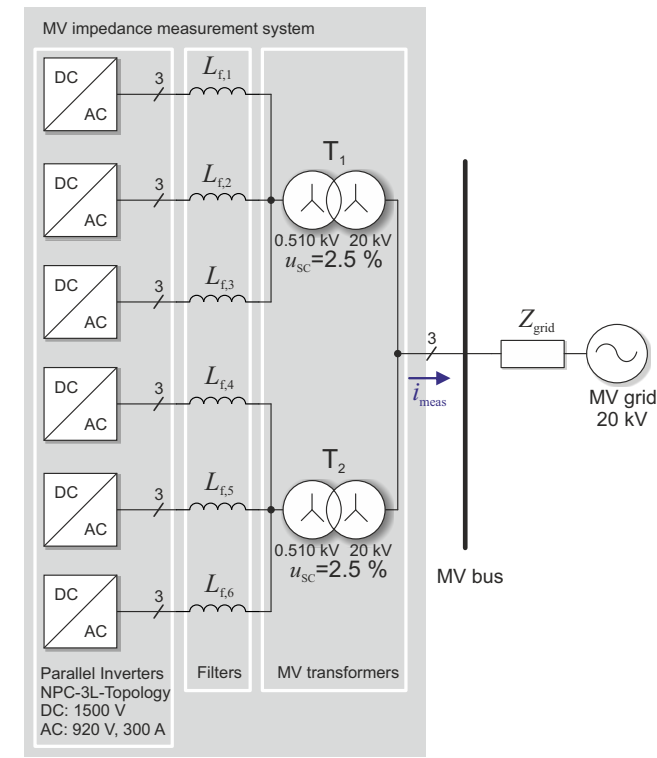
(a)
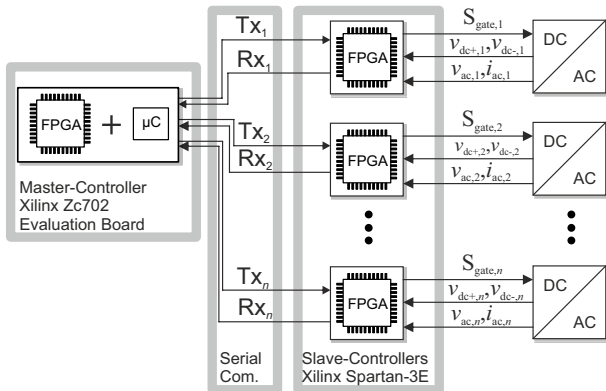
(b)

Fig. 1. MV grid impedance measurement system: (a) System configuration, (b) concept of control and synchronization.

and the control and synchronization of the parallel inverters are explained.

A. System Configuration

An overview of the system configuration is given in Fig. 1a, where the measurement system is connected to a MV bus interfaced with the 20 kV-MV grid. By knowledge of the response of the grid voltage at the MV bus and the injected current i_{meas}, the grid impedance Z_{grid} can be calculated in this specific frequency point. The measurement is repeated from 100 Hz to 10 kHz depending on the chosen frequency resolution. For a total system power of 1.6 MVA, required

to achieve 1 % grid voltage excitation, two MV transformers in star-star configuration (short circuit voltage $u_{\mathrm{SC}} = 2.5\,\%$) are connected in parallel each of which is connected to 3 LV inverters. With the total number of $n = 6$ paralleled LV inverters, the power level of the single LV inverter is chosen to be 480 kVA. Three-level NPC topology is selected due to the additional voltage level, the increased voltage capability and the increased power density in comparison to two-level inverters. Filters such as dv/dt filters, common mode filters or filters for interleaved operation are placed between inverters and transformers. The dc-link of the LV inverters is supplied by the fundamental frequency (50 Hz) of the grid voltage so that power is flowing simultaneously in both directions at different frequencies: The fundamental frequency f_{fund} and the measurement frequency f_{meas}. A common dc-link can be implemented or separate dc-links can be used by which the problem of circulating currents is avoided at the cost of higher control and measurement complexity.

B. Control and Synchronization

The control and synchronization of the parallel inverters is depicted in Fig. 1b with a master controller as supervisory control unit and with slave controllers as local control units at inverter level. The three-phase ac current $i_{\mathrm{ac},m}$ $(m = 1, 2, ...n)$, the three-phase ac voltage $v_{\mathrm{ac},m}$ and the dc link voltages $v_{\mathrm{dc}+,m}$ and $v_{\mathrm{dc}-,m}$ of the single inverters are measured by the slave boards. The measured signals are transmitted to the master via serial communication Tx_m and Rx_m. Note that with common dc-link only one slave board is measuring the dc-link voltages. The main control tasks such as grid synchronization, dc-link voltage and ac current control are executed by the master controller. The three-phase duty cycle d_m, possible carrier offsets for interleaved operation and a signal for switching synchronization of the parallel inverters are fed back to the slave controllers, where the PWM is implemented for calculation of the gate signals $\mathrm{S}_{\mathrm{gate},m}$, which are finally transmitted to the inverters. The maximum measurement frequency f_{meas} of 10 kHz requires high switching frequencies for implementation of PWM. In order to achieve adequate measurements, the sampling frequency is chosen to be at least 5 times higher than the output frequency, resulting in a maximum switching frequency of 50 kHz. It means that less than 20 µs are available for signal conversion, serial communication and calculation of control algorithms. For this reason and due to the parallel computation capability, the control units are based on fast field programmable gate array (FPGA). The slave controller is based on a *Xilinx Spartan-3E* chip up to 125 MHz operation. For serial communication, fiber optic cables are used with 50 MBd transceivers. The master controller is a *Xilinx ZC702 Evaluation Board* based on *Xilinx Zynq-7000* which features a micro-controller (µC) based on *ARM Cortex-A9* up to 1 GHz operation and a FPGA unit up to 200 MHz operation both combined on a single chip.

The control of one inverter m is depicted in Fig. 2. It shows that control algorithms with lower dynamics such as grid synchronization, dc-link voltage control and current reference
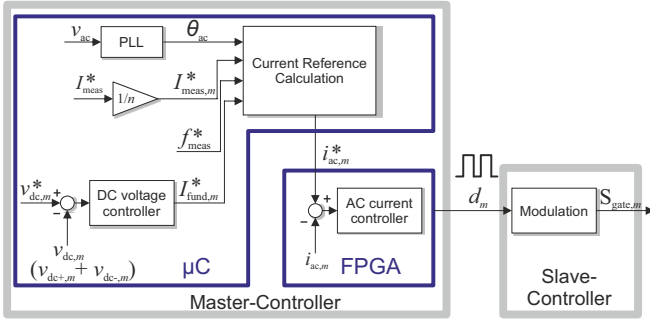
Fig. 2. Block diagram of MV grid impedance measurement system: Single inverter control.

calculation are implemented on the µC, the current control and communication interface, instead, are implemented on the FPGA of the master controller due to the high current dynamics and the simultaneous calculation for n slave controllers as well as due to simultaneous communication with n slave controllers. The inputs of the current reference calculation are the phase angle of the grid, detected by a synchronous reference frame phase-locked loop (PLL), the amplitude and frequency of the measurement current reference $I^*_{\text{meas},m}$ and f^*_{meas} and the amplitude of the fundamental current reference $I^*_{\text{fund},m}$, calculated by the dc-link voltage controller which is based on classical PI control. Note that with a common dc-link only one dc-link voltage controller is needed and in case of separate dc-links n dc-link voltage controllers are required. The current controller is implemented in the dq frame and the classical PI control strategy is employed to achieve good current control capability.

III. CIRCULATING CURRENT

To improve the quality of the total current, the interleaved operation is selected as an optimal solution for the parallel inverters. The interleaved PWM operation requires the carriers for adjacent inverters to be phase shifted by $360°/n$ so that a reduced amplitude of the total current ripple can be achieved [7]. Here, n is the number of the parallel inverters. For instance, in a two-inverter system, a $180°$ phase shift is used. Due to the shared dc-link, the common mode voltage among different inverters would appear which leads to the circulation of the current among the modules. Fig. 3 depicts an example of the cause of the common mode voltage as well as the circulating current. The common mode voltage v_{cm} and the circulating current i_{cir} can be calculated by

$$v_{cm} = v_{cm1} - v_{cm2}$$
$$= \frac{v_{az1} + v_{bz1} + v_{cz1}}{3} - \frac{v_{az2} + v_{bz2} + v_{cz2}}{3}. \quad (1)$$

$$i_{cir} = \frac{3}{2L} \int v_{cm}(t)dt. \quad (2)$$

where v_{cm1} and v_{cm2} are the common mode voltages of the two inverters, v_{kz1} and v_{kz2} ($k = a, b, c$) are the phase-to-
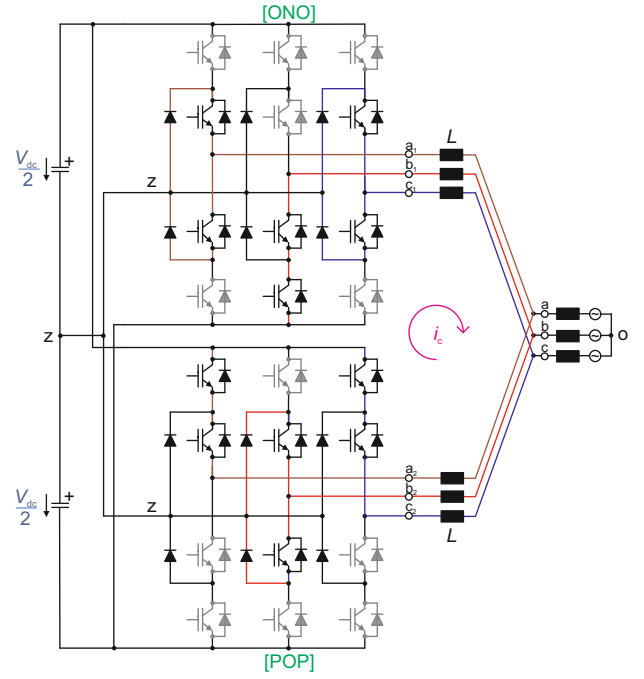

Fig. 3. An example of the common mode voltage and the circulating current in the parallel NPC inverters.

neutral voltages of the Inverter 1 and the Inverter 2, respectively.

In Fig. 3, the worst case considering the possible modulation is demonstrated, where the switching states of the two inverters are [POP] and [ONO], respectively. The common mode voltage between two inverters is half the dc-link voltage which leads to considerable circulating current. Obviously, the magnitude of the common mode voltage depends on the switching states of both inverters. The modulation techniques therefore are one of the most important factors to determine the intensity of the common mode voltage as well as the circulating current. The relationship between the modulation and the circulating current in two-level inverters has been well studied in literature [6], [12]. Several optimized modulation techniques have been proposed to reduce the circulating current while maintaining other grateful features [6], [12]–[14]. However, this topic has seldom been investigated in the three-level NPC applications. To find the best modulation technique for parallel NPC inverters, the analyses and the validations are given in the following sections.

IV. OPTIMIZED MODULATION FOR PARALLELED NPC INVERTERS

In this section, two well-known carrier-based modulation techniques: PD and APOD, are evaluated for parallel NPC inverters application. The common-mode voltage and the circulating current between two parallel inverters are analyzed. The peak-to-peak and root-mean-square (rms) values of the circulating current are calculated for different modulation techniques.
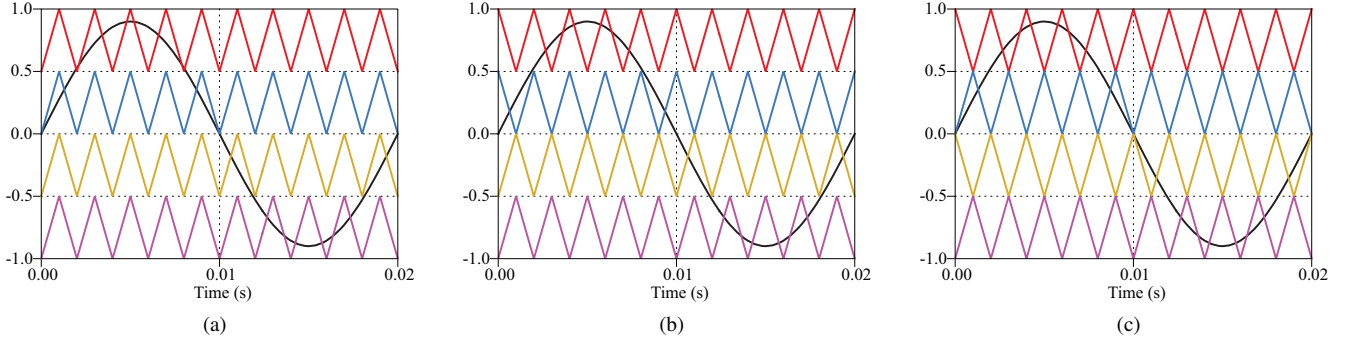
Fig. 4. Modulation techniques for multilevel inverters: (a) PD, (b) POD, and (c) APOD.

A. Modulation for Single NPC Inverter

For the multilevel inverter, three modulation techniques are usually considered: Phase Disposition (PD), Phase Opposite Disposition (POD), and Alternative Phase Opposite Disposition (APOD) [7]. For PD, all carriers are in phase; for POD, carriers above the zero point are out of phase with those below zero by $180°$; for APOD, carriers in adjacent bands are phase shifted by $180°$. An example of three modulation techniques is shown in Fig. 4. Since only two carriers are utilized in the three-level NPC inverter, the POD and the APOD are identical. In literature, it is shown that the PD modulation strategy provides better performance in terms of spectrum profile and current ripple [7], [15]. As a result, for three-level NPC inverter, PD has been employed as common modulation technique and is used in carrier-based space vector PWM [13].

B. PD vs. APOD under Interleaved Operation

For three-phase fundamental modulation signals, six sectors are divided as shown in Fig. 5a according to the relationship between carrier-based PWM and space-vector modulation [13]. To better demonstrate the relationship between the switching states and the corresponding sectors, the division of sectors and regions as well as the switching states is given in Fig. 5b. As can be seen in the figure, each sector can be further divided into four triangular regions (e.g. 1 to 4 in Sector I). The adjoining switching states will be adopted in each region. Since the characteristics (e.g. switching state sequence, switching pattens) of each sector are similar to the others, only Sector I has been taken into account for the sake of simplicity. When the voltage vector $\mathbf{v_{ref}}$ is in region 1 or 2 of Sector I, it can be seen that two of the three switching states are categorized as "small vector" that is able to minimize the neutral-point voltage deviation [7]. Based on the dominate small vector, each of the two regions can be further divided into two subregions as shown in Fig. 5b. For instance, the seven-segment switching sequences in Sector I-2a and Sector I-2b are [ONN], [OON], [PON], [POO], [PON], [OON], [ONN] and [OON], [PON], [POO], [PPO], [POO], [PON], [OON], respectively.

When a common dc-link is implemented, the circulating current must be considered as one of the main indices in par-

alleled NPC inverters under interleaved operation. Regarding (1) and (2), the common-mode voltage as well as the inverter terminal voltages should be obtained for the calculation of circulating current. Firstly, the inverter terminal voltage and the switching states in each region of Sector I using PD and APOD are investigated. An example of the inverter terminal voltage and the switching states of Sector I-1a is given, with two different modulation techniques presented in Fig. 6. In both figures, V_{cp1} and V_{cn1} are the positive and the negative carriers of the first inverter, V_{cp2} and V_{cn2} are the positive and the negative carriers of the second inverter. d_a, d_b, and d_c represent the duty cycles at that sampling interval, while v_{kz1} and v_{kz2} ($k = a, b, c$) are the terminal voltages of first and second inverter, respectively. The time durations of switch-on (T_{kz}) and switch-off ($\bar{T}_{kz}$) in each phase ($k = a, b, c$) of Fig. 6 can be easily obtained and shown in (3) and (4), assuming the modulation index is m_k

$$T_{kz} = |d_k| \cdot T_s \cdot m_k \qquad k = a, b, c. \qquad (3)$$

$$\bar{T}_{kz} = |1 - d_k| \cdot T_s \cdot m_k \qquad k = a, b, c. \qquad (4)$$

Based on the terminal voltages, the common-mode voltage between the parallel NPC inverters can be obtained using (1). Depends on the intensity of common-mode voltage, seven segments are divided with different shades in each half sampling interval. The darker segment represents the higher common mode voltage, for example, in the middlemost area of PD modulation, two switching states: [ONN] and [POO] were applied to the inverters, resulting in the highest common mode voltage between two modules. It is worth noting that the definition of segments (based on common-mode voltage) here is different from the definition of seven-segment switching sequence (based on the switching states) of single inverter modulation. The common-mode-voltage-related segment sequences of both modulation techniques are denoted in the time-axis of Fig. 6.

The detailed common mode voltages (v_{cm}) in that sampling interval using the PD and the APOD are presented in Fig. 7 ($E = V_{dc}/6$). The circulating current between the modules can be calculated using (2) and the waveforms are shown in figures by magenta curves. Compared Fig. 7a to Fig. 7b, it can be seen that the common-mode voltage using the PD is higher
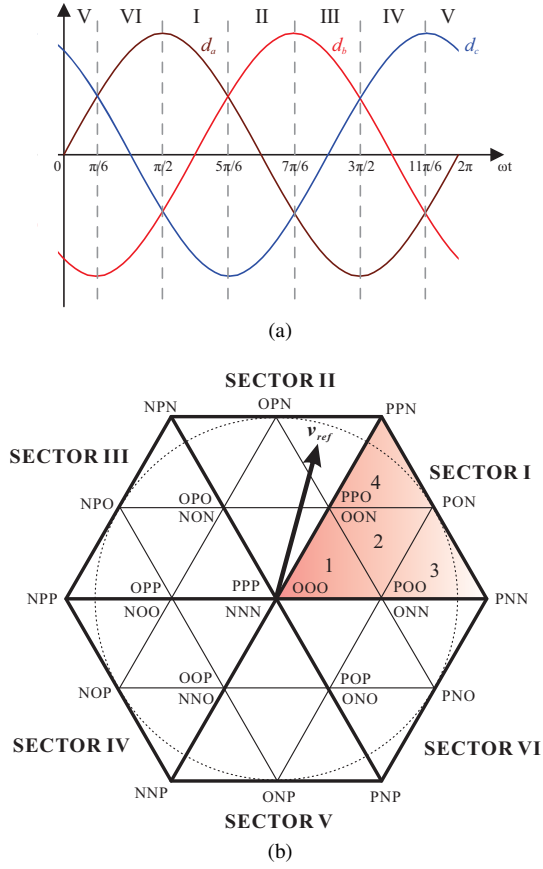
(a)

(b)

(c)

Fig. 5. Fundamental signals and modulation vectors: (a) fundamental modulation signals, (b) division of sectors and regions, and (c) division of six regions of Sector I.
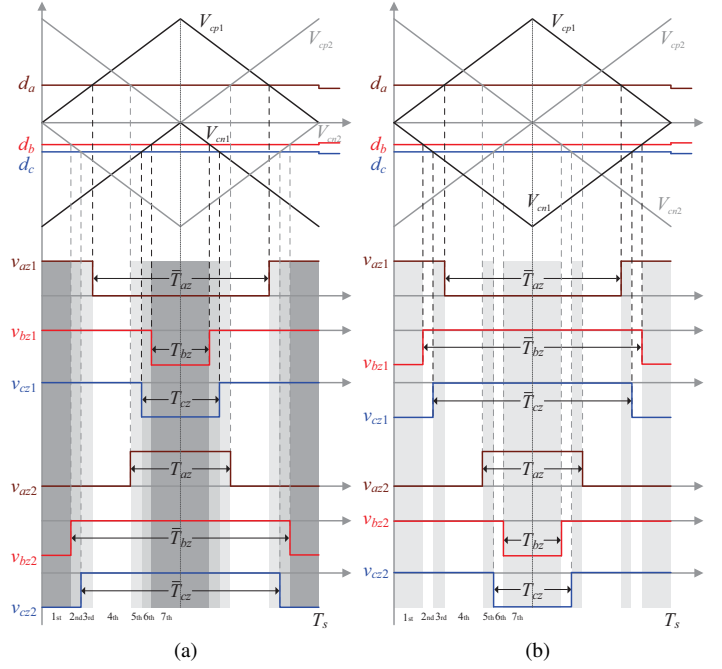

(a)

(b)

Fig. 6. Terminal voltages of parallel NPC inverters in Sector I-1a with different modulation techniques: (a) PD and (b) APOD.

given by (5) and (6).

$$
i_{cir}^{PD} = \begin{cases}
\dfrac{9E}{2L}t & 0 \le t \le T_1 \\[2mm]
\dfrac{3E}{2L}(T_1 + 2t) & T_1 < t \le T_2 \\[2mm]
\dfrac{3E}{2L}\Big(\sum_{k=1}^{2} T_k + t\Big) & T_2 < t \le T_3 \\[2mm]
\dfrac{3E}{2L}\Big(\sum_{k=1}^{3} T_k\Big) & T_3 < t \le T_4 \\[2mm]
\dfrac{3E}{2L}\Big(\sum_{k=1}^{4} T_k - t\Big) & T_4 < t \le T_5 \\[2mm]
\dfrac{3E}{2L}\Big(\sum_{k=1}^{5} T_k - 2t\Big) & T_5 < t \le T_6 \\[2mm]
\dfrac{3E}{2L}\Big(\sum_{k=1}^{6} T_k - 3t\Big) & T_6 < t \le T_7
\end{cases} \tag{5}
$$

$$
i_{cir}^{APOD} = \begin{cases}
-\dfrac{3E}{2L}t & 0 \le t \le T_1 \\[2mm]
-\dfrac{3E}{2L}T_1 & T_1 < t \le T_2 \\[2mm]
\dfrac{3E}{2L}\Big(-\sum_{k=1}^{2} T_k + t\Big) & T_2 < t \le T_3 \\[2mm]
\dfrac{3E}{2L}\Big(-\sum_{k=1}^{2} T_k + T_3\Big) & T_3 < t \le T_4 \\[2mm]
\dfrac{3E}{2L}\Big(-\sum_{k=1}^{2} T_k + \sum_{k=3}^{4} T_k - t\Big) & T_4 < t \le T_5 \\[2mm]
\dfrac{3E}{2L}\Big(-\sum_{k=1}^{2,5} T_k + \sum_{k=3}^{4} T_k\Big) & T_5 < t \le T_6 \\[2mm]
\dfrac{3E}{2L}\Big(-\sum_{k=1}^{2,5,6} T_k + \sum_{k=3}^{4} T_k + t\Big) & T_6 < t \le T_7
\end{cases} \tag{6}
$$

than that using the APOD in every segments entire the whole sampling interval, which leads to a higher circulating current between two inverters.

Secondly, to quantify the circulating currents for different modulation techniques in Sector I-1a, the peak-to-peak value and the rms value in each sampling interval are evaluated. Assuming the initial value of circulating current at the beginning of each interval is zero, the expressions of the circulating currents in Sector I-1a by using the PD and the APOD are

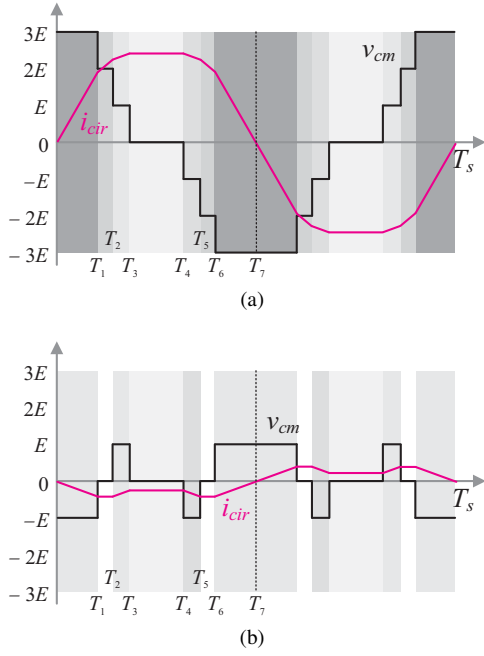where T_1 to T_7 are the time of the seven segments that

Fig. 7. Common-mode voltage and circulating current between parallel NPC inverters in Sector I-1a with different modulation techniques: (a) PD and (b) APOD.

TABLE I
COMPARISONS OF COMMON-MODE VOLTAGE OF SECTOR I

PD Modulation						
Segment	1a	1b	2a	2b	3	4
1st	3E	3E	3E	3E	3E	3E
2nd	2E	2E	2E	2E	2E	2E
3rd	E	E	E	E	E	E
4th	0	0	0	0	0	0
5th	-E	-E	-E	-E	-E	-E
6th	-2E	-2E	-2E	-2E	-2E	-2E
7th	-3E	-3E	-3E	-3E	-3E	-3E
APOD Modulation						
Segment	1a	1b	2a	2b	3	4
1st	-E	E	-E	E	-E	E
2nd	0	0	0	0	-2E	2E
3rd	E	-E	-E	E	-E	E
4th	0	0	0	0	0	0
5th	-E	E	E	-E	E	-E
6th	0	0	0	0	2E	-2E
7th	E	-E	E	-E	E	-E

indicated in Fig. 7, and can be calculated by

$$T_1 = \frac{T_s - \bar{T}_{bz}}{2}, \ T_2 = \frac{T_s - \bar{T}_{cz}}{2}, \ T_3 = \frac{T_s - \bar{T}_{az}}{2},$$
$$T_4 = \frac{T_s - T_{az}}{2}, \ T_5 = \frac{T_s - T_{cz}}{2}, \ T_6 = \frac{T_s - T_{bz}}{2}, \ T_7 = \frac{T_s}{2}. \quad (7)$$

Hereby, the peak-to-peak circulating current by using the PD and the APOD modulation can be written by

$$i^{PD}_{cir,p-2-p} = \frac{3E}{L}(T_1 + T_2 + T_3). \quad (8)$$

$$i^{APOD}_{cir,p-2-p} = \frac{3E}{L}T_1. \quad (9)$$

Compared (8) to (9), it can be seen that the peak-to-peak of the circulating current between modules using the PD technique is much higher than that if the APOD technique is used.

The half cycle rms value of the circulating current by using the PD and the APOD modulation can be written by

$$i^{PD}_{cir,rms} = [-\frac{3E^2}{2L^2T_s}(4T_1^3 + 3T_1T_2^2 + 3T_2^3 + 3T_1T_3^2 + 3T_2T_3^2$$
$$+2T_3^3 + 3T_1T_4^2 + 3T_3T_4^2 + T_4^3 + 3T_1T_5^2 + 3T_2T_5^2 + 3T_3T_5^2$$
$$+3T_4T_5^2 + 3T_1T_6^2 + 3T_2T_6^2 + 3T_3T_6^2 + 3T_4T_6^2 + 3T_5T_6^2$$
$$-T_6^3 - 3(T_1 + T_2 + T_3 + T_4 + T_5 + T_6)^2T_7$$
$$+9(T_1 + T_2 + T_3 + T_4 + T_5 + T_6)T_7^2 - 9T_7^3)]^{1/2}. \quad (10)$$

$$i^{APOD}_{cir,p-2-p} = [\frac{3E^2}{2L^2T_s}(2T_1^3 + 3T_1T_2^2 + T_2^3 - 3T_1T_3^2 - 3T_2T_3^2$$
$$+2T_3^3 - 3T_1T_4^2 - 3T_2T_4^2 + 3T_3T_4^2 + T_4^3 + 3T_1T_5^2 + 3T_2T_5^2$$
$$-3T_3T_5^2 - 3T_4T_5^2 + 2T_5^3 + 3T_1T_6^2 + 3T_2T_6^2 - 3T_3T_6^2$$
$$-3T_4T_6^2 + 3T_5T_6^2 + T_6^3 - 3(T_1 + T_2 - T_3 - T_4 + T_5 + T_6)^2T_7$$
$$+3(T_1 + T_2 - T_3 - T_4 + T_5 + T_6)T_7^2 - 9T_7^3)]^{1/2}. \quad (11)$$

Compared (10) to (11), it can be evaluated that the rms of the circulating current using the PD technique is higher than that if the APOD technique is used. The common-mode voltages of all regions of Sector I using different modulation techniques are listed in Table I. It can be seen that the common-mode voltage using the PD technique is higher than that using the APOD technique of all segments of Sector I, which conjectures that the PD incurs higher circulating current. Therefore, in the paralleled NPC application, the APOD would be superior to the PD in terms of circulating current. Due to the page limit, the rest regions of Sector I are not investigated in details, while the characteristics of circulating current of those regions can be easily obtained by using the same method mentioned in this section.

V. SIMULATION AND EXPERIMENTAL RESULTS

The performance of two parallel NPC inverters with common dc-link under interleaved operation is validated for different modulation by simulation and experiments. The detail results and performance evaluation are presented in the following section.

A. Simulation Results

To validate the analyses, two parallel NPC inverters with common dc-link are simulated in the MATLAB/Simulink envi-
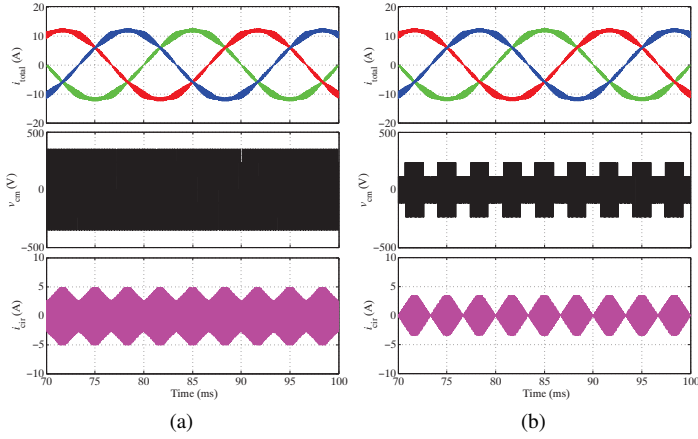
Fig. 8. Performance evaluation of parallel NPCs during interleaved operation using different modulation (modulation index: $m = 0.85$): (a) PD and (b) APOD.
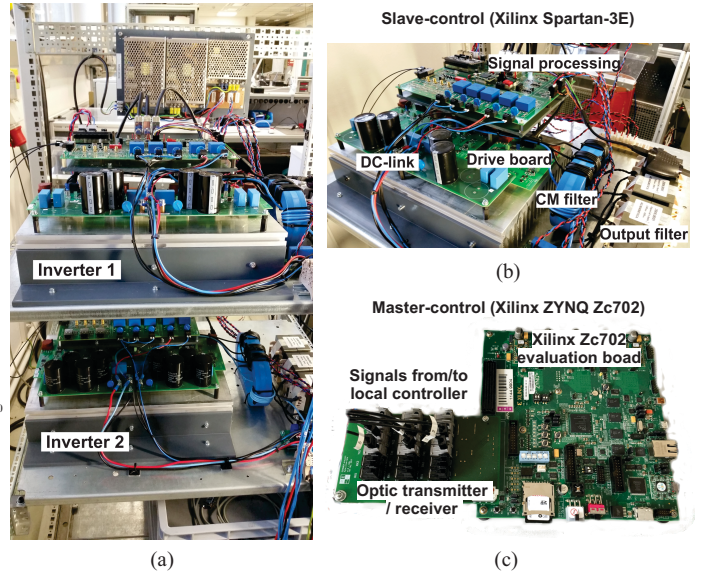

Fig. 9. Experimental Setup: (a) overall prototype, (b) details of inverter 1 as well as the slave control board, and (c) master control board.
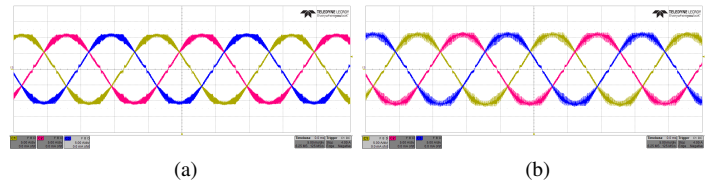

Fig. 10. Three-phase total current of two NPC inverters by using different modulation techniques (modulation index: $m = 0.85$, time: 5 ms/div, current: 5 A/div): (a) PD and (b) APOD.

ronment with the aid of the PLECS toolbox. Both the PD and the APOD techniques are applied to the paralleled modules under interleaved operation. The dc-link voltage is 700 V and the nominal ac voltage is 230 V (rms). The modulation index of $m = 0.85$ is considered in the open-loop control case. The switching frequency is 10 kHz.

Comparisons in terms of total current, common-mode voltage, and circulating current are shown in Fig. 8. It can be seen total currents using two modulation techniques are identical in terms of waveform quality and current ripple. The THDs of both waveforms are evaluated and are 5.47 % for both techniques. Nevertheless, the common-mode voltages and the circulating currents using different modulation techniques are distinct. It is obviously seen that both the common-mode voltage and the circulating current of the PD modulation technique are higher than that uses the APOD modulation. It is worth noting that the voltage vector is sweeping region 2, 3, and 4 of every Sector in every cycle according to the modulation index. As a result, it can be expected that the common-mode voltage of the PD modulation would be 3/2-times to that of the APOD in both region 3 and 4, and 3-times to that of the APOD in region 2, according to Table I, which is validated by the common-mode voltage waveforms in Fig. 8.

B. Experimental Validation

The modulation techniques are also evaluated by the experimental setup which is shown in Fig. 9. For the preliminary test, a 20 KVA prototype with two paralleled NPC inverters are built in the lab, and the dc-link voltage is 700 V. The Infineon three-level phase lag IGBT module ($F3L75R07W2E3\_B11$) has been chosen as the candidate of the NPC inverter setup and can handle current up to 75 A. An inductor of 1.8 mH is used in each phase to limit current ripples and circulating currents. Each module is driven by the dedicated evaluation drive board ($F3L030E07 - F - W2$). A high bandwidth signal processing as well as measurement board is utilized to control each NPC inverter module locally. Meanwhile, the centralized control

scheme shown in Fig. 2 is implemented in a master control board (Xilinx Zc702 evaluation board). The communication between the master control board and the local control board is achieved through the optic fibers.

Firstly, the two parallel NPC inverters are performed under interleaved operation with a switching frequency of 10 kHz. An open-loop control is implemented in the master control board which is able to adjust the modulation index of both inverters online. The three-phase current waveforms by using two different modulation techniques (PD and APOD) are compared as followings. In Fig. 10, the three-phase total currents of both inverters are measured employing the PD and the APOD. It can be seen that the performance of both current waveforms are comparable, in terms of current ripple and power quality. The spectrum analyses of total current of both modulation are presented in Fig. 11. The analyses show that the total current using the PD would establish higher components at switching frequencies (seen from Fig. 11a), while the total current using the APOD is subject to higher low-order harmonics/disturbances (seen from Fig. 11a). In general, the waveform performance of both techniques in frequency-domain are comparable and the THD values of Fig. 10 are 15.95 % (PD) and 16.14 % (APOD).
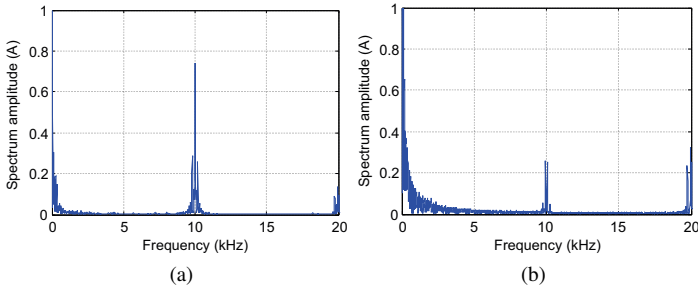
Fig. 11. Amplitude spectrum of total current (Phase A) using different modulation techniques: (a) PD and (b) APOD.
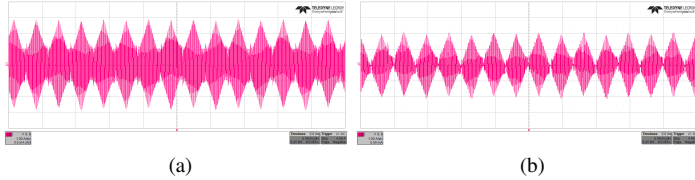

Fig. 12. Circulating current between the parallel NPC inverters using different modulation (modulation index: $m = 0.98$, time: 5 ms/div, current: 1 A/div): (a) PD and (b) APOD.

Secondly, the circulating currents between two NPCs by using two different modulation are measured and shown in Fig. 10. The modulation index of $m = 0.98$ is implemented for both inverters, indicating the region 2, 3, 4 would be swept by the voltage vector. According to the analysis of Section IV and Table I, the common-mode voltage of the PD modulation would be $3/2$-times to that of the APOD most of the cycle (region 3 and 4), and 3-times to that of the APOD in short periods (region 2). From the experimental results, the circulating current of the PD (Fig. 12a) is higher than that of the APOD (Fig. 12b) as expected, especially the adjoining areas between two "rhombus" (that related to region 2 of all Sectors).

To sum up, during interleaved operation, the performance of the total current of parallel inverter using the PD is in the same league as that using the APOD. Nevertheless, the circulating current of the PD modulation is much higher than that of the APOD modulation, especially a small voltage vector is performed (region 1 and 2). As a result, the APOD modulation would be an optimized solution for parallel NPCs applications.

VI. CONCLUSIONS

The interleaved operation of parallel NPC inverters has been used for improving the quality of the current waveform. However, in the case of a common dc-link, the circulating current issue emerges and could lead to critical problems. To minimize the circulating current of parallel NPCs, two common modulation techniques for NPC inverters (PD and APOD) have been investigated and evaluated in an extensive way. Though it is well-known that the PD modulation offers better performance in a single NPC inverter, the APOD modulation has advantages in the parallel NPCs with interleaved operation. The analyses and results in this paper show that the APOD modulation gives remarkably less common-mode voltage/circulating current and similar spectrum quality of total current compared to those using the PD modulation. To conclude, the APOD modulation is an optimum solution for the parallel NPC inverters under interleaved operation.

VII. ACKNOWLEDGEMENT

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